A Low-power CMOS 2-PPM Demodulator for Energy Detection IR-UWB Receivers

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Marco Crepaldi, Mario R. Casu, Mariagrazia Graziano and Maurizio Zamboni

Abstract— **This paper presents an integrated 2-PPM CMOS demodulator for Non-coherent Energy Detection receivers which inherently provides Analog-to-Digital Conversion. The device, called *Bi-phase* integrator, employs an open loop $G_m - C$ integrator loaded with a switched capacitor network. The circuit has been simulated in a mixed-mode UMC 0.18μm technology and its performance figures are obtained through a mixed-signal simulation environment developed with the aid of ADVanceMS (ADMS, Mentor Graphics). Bit-Error-Rate simulations show that the circuit performance is about the same of an ideal Energy Detection receiver employing infinite quantization resolution. In addition, the simulations show that the circuit provides a complete offset rejection. Thanks to its low power consumption (1 mW during demodulation), its application is appealing for portable devices which aim at very low-power consumptions.**

Index Terms— **UWB Communications, VHDL-AMS, Mixed-Signal Integrated Circuits, Pulse Position Modulation, OTA.**

I. Introduction

Impulse-Radio Ultrawideband (IR-UWB) technology is a promising solution for short-range indoor applications. It is particularly suited for applications aimed at connecting portable devices in Wireless-Private-Area-Networks (WPANs). The "carrier-less" transmission relies on short duration pulses which satisfy FCC spectral requirements about both ultra-wide bandwidth occupations and low power spectral densities. Thanks to these features, IR-UWB is particularly suited to ultra low-power applications in which extended battery lives are a fundamental requirement [1]. Generally, transceivers are designed to exploit high bandwidth efficiency, low peak powers at transmitters, low complexities, the flexibility of supporting different data rates and reliable performance.

Two receiver structures are typically employed in these systems, the coherent and the non-coherent ones. Coherent receivers fully exploit multipath richness, gain diversity and timing accuracy according to a waveform template internally generated at the receiver. Typical structures employ high complexity Rake-based schemes which work at very high clock frequencies and are capable of sampling sub-nanosecond time windows.

On the other hand, the main feature of non-coherent receivers is the possibility of acquiring the UWB pulses immersed in a dense multipath environment without requiring any channel estimation. The price to pay for such a complexity decrease is a 3-dB penalty in the BER curve with respect to coherent receivers. The non-coherent approach which requires the lowest complexity is the Energy Detection (ED) one.

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In Energy Detection receivers the UWB signal is simply acquired by evaluating the received pulses energy without any additional information. Due to the nature of ED schemes, receivers are insensitive to BPSK (Bi-Phase Shift Keying) modulations, thus data is transmitted according to Pulse-Position-Modulations (PPM) or On-Off-Keying (OOK).

Thanks to the very low-power dissipation possible, the number of works dealing with the modeling-and-simulation [2], [3] and low-power CMOS front-ends implementation of ED receivers are increasing during years [4]. Typical ED front-ends are Bi-CMOS implementations in which the energy detection of the UWB pulses is performed by Integrate-and-Dump (I&D units): Here, two control signals, *Integrate* and *Dump*, enable respectively the integration and the storage of the UWB pulses. These units are realized with open loop $Gm - C$ integrators for achieving high bandwidths [4].

Aiming at low-power consumption, this work presents an integrated 2-PPM CMOS demodulator which employs an open-loop $G_m - C$ structure, called *Bi-phase* integrator. It consumes low power (1 mW), provides inherently Analog-to-Digital Conversion with significative offset rejection and exhibits nearly the same error-rate performance of an ideal Energy Detection receiver. Thanks to a VHDL-AMS mixed-signal simulation environment developed with the aid of ADVanceMS (ADMS, Mentor Graphics) the circuit has been tested with a reliable UWB pulses waveform database and BER performance figures have been obtained [5]. The circuit has been designed in a mixed-mode UMC CMOS 0.18 μm technology and simulated with SPICE BSIM3 transistor models.

The rest of this paper is organised as follows: Section II introduces the principle of operation of the receiver and discusses how the structure reduces the effects of parasitics on performance. Section III explains the typical design issues and clarifies the trade-off between performance and low-power consumptions. Section IV shows a BER comparison among an ideal Energy Detection receiver and the Bi-phase demodulator; furthermore it presents results in which the offset rejection capability is proven. Finally, conclusions are drawn in section V.

II. Demodulator concept and circuit analysis

A. Principle of operation

Typical ED receivers front-ends include a Low-Noise-Amplifier (LNA), a Squaring Unit ($()^2$), an analog integrator and finally an A/D converter. Thus, after amplification, the signal is squared, integrated and the resulting energy is A/D

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converted to a digital format. A typical modulation scheme is the 2–PPM (Bi–phase Pulse–Position–Modulation) in which the transmitted pulse is modulated according to its position in time. Whether a '0' is sent, the pulse is placed in the first half of the Pulse–Repetition–Interval (PRI) while, in case of a '1', the pulse is placed in the second one. The ED receiver thus demodulates data by comparing the energies of the two PPM phases numerically.

The aim of this work is to allow the replacement of the front–end A/D with a simple zero–threshold comparator by giving the analog integrator the capability to provide a voltage whose sign determines the information bit. With respect to the typical Energy Detection receivers, here the front–end includes the Bi–phase integrator and the comparator as the final blocks rather than any ADC (figure 1). In order to show the functionalities of the block, figure 2 provides a principle scheme of the sole Bi–phase unit.

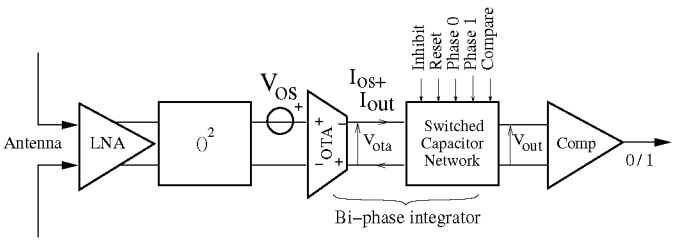

Fig. 1. Energy Detection receiver with Bi–phase demodulator

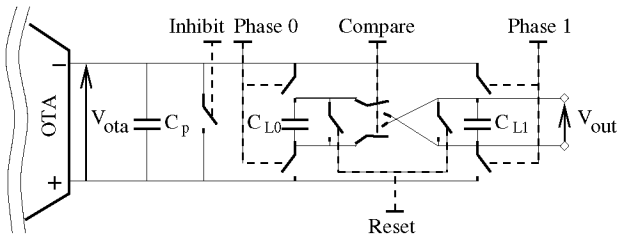

Fig. 2. Principle of the Bi–phase integrator

The demodulator includes two parts, the Operational Transconductance Amplifier (OTA) [6] and the integration network. The former transforms the input voltage variations V_{in} into current I_{out}, while the latter, a switched capacitor network [7], controls current and performs inherently Analog–to–Digital Conversion. Two equal integration capacitors C_{L0} and C_{L1} are responsible for the integration of each of the two PPM phases. The overall parasitic capacitance due to the integration network and the OTA output stage is modeled as C_p. The Bi–phase demodulator operates with five control signals, *Phase 0*, *Phase 1*, *Compare*, *Reset* and *Inhibit*. The first three control the integration of the incoming UWB pulses, the fourth one resets the state of the integrating capacitors and finally the fifth one inhibits the output terminals of the transconductance amplifier and makes the circuit insensitive to parasitics contributions. As explained later, the whole demodulation behaviour is based on the charge redistribution principle.

When the device is idle, signal *Inhibit* forces the differential output terminals of the OTA to be at the same potential. In practice it allows the voltage across integration capacitor C_p to be zero before starting the integration of the first PPM phase. When the first integration starts, *Inhibit* is deactivated and signal *Phase 0* is asserted forcing current I_{out} in the equivalent capacitor $C_{L0} + C_p$. When the first integration phase finishes, signal *Phase 0* is deactivated and *Inhibit* is asserted again. When the second integration starts, signal *Inhibit* is deactivated and *Phase 1* is asserted therefore forcing current in $C_{L1} + C_p$. In the end, the charge in C_{L0} and C_{L1} is proportional to the input signal: After the assertion of signal *Inhibit*, the final demodulation is possible by activating signal *Compare*. Charge redistribution principle is responsible for setting the sign of output voltage V_{out} according to the information bit. The comparator gives the information bit by comparing such voltage to zero. Finally, signal *Reset* zeroes the charge in C_{L0} and C_{L1} and another demodulation cycle is possible.

It is easy to understand that the device inherently provides offset rejection thanks to its fully balanced structure. In fact, if the sole offset voltage V_{OS} is present at the OTA input, the resulting offset current I_{OS} is fed alternatively in C_{L0} and C_{L1}: After the final charge redistribution the resulting output voltage is ideally zero.

B. Parasitic effects reduction

The calculations shown in the following clarify the use of the *Inhibit* signal. In the first part of the discussion no resets switches across C_p are considered. In the second part, it is shown by means of analytical models how the *Inhibit* switch can eliminate demodulation errors caused by parasitics. In this discussion the OTA and the integration network are assumed to be ideal.

When the receiver acquires modulated data, the device operates in a "steady state" mode thus integration control signals are asserted periodically. On top of figure 3 the control phases signals are schematized. In such conditions, the delays between activation of *Phase 0* and *Phase 1* remain the same for each demodulation period. The figure shows different states (from A to F) according to the current operation phase and allows to follow voltage variations across C_p and integration capacitors C_{L0} and C_{L1}. With this scheme it is possible to focus on the initial and final conditions across C_p and C_{L0}, C_{L1} and to understand how to combine them together according to the full device operation, (i.e. from the beginning of Phase 0 to the end of Phase 1) to obtain the mathematical expression representing the influence of parasitics on V_{out}. State G is related to the final charge redistribution after having completed the two demodulation phases.

We define the quantity T_i as the idle time between the deactivation of *Phase 0* and the activation of *Phase 1* and vice–versa. To understand how the device works it is necessary to state how the initial and final conditions on voltage across C_p impact on C_{L0} and C_{L1} at the beginning and at the end of each demodulation phase. For doing this we define the quantities $V_{i_{ph0}}^{p,(n)}$, $V_{f_{ph0}}^{p,(n)}$, $V_{i_{ph1}}^{p,(n)}$, $V_{f_{ph0}}^{p,(n)}$, where n indicates the number of demodulated periods since when the device has been synchronized. Subscripts i and f indicate the initial and final conditions across C_p during the idle period, for

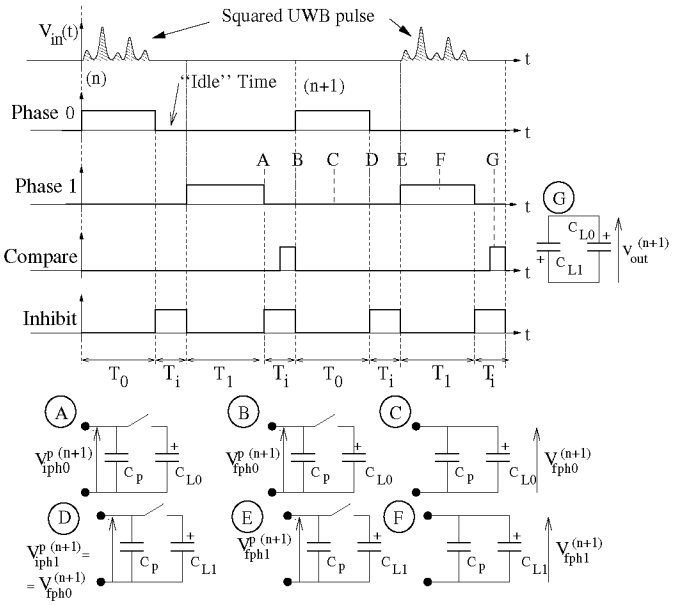

Fig. 3. Circuit operation scheme during demodulation

Phase 0 and *Phase 1* operation states, respectively. Superscript p indicates that the quantity is related to C_p. At deactivation of *Phase 0* and *Phase 1*, voltage across C_{L0} is maintained constant until state G is reached.

At the successive integration $(n+1)$ the charge stored in C_p is transferred to the load capacitors. To take into consideration the charge transfer it is also necessary to define the quantities $V_{i_{ph0}}^{(n)}$, $V_{f_{ph0}}^{(n)}$, $V_{i_{ph1}}^{(n)}$ and $V_{f_{ph0}}^{(n)}$ using the same convention as above. When signals *Phase 0* and *Phase 1* are asserted, the OTA performs integration of the UWB signal. During these phases, its output represents the information required for demodulation. We thus define the quantities $V_O^{(n)} = \frac{1}{C_p+C_{L0}} \int_{T_0^{(n)}} G_m V_{in}(t)$ and $V_1^{(n)} = \frac{1}{C_p+C_{L1}} \int_{T_1^{(n)}} G_m V_{in}(t)$ as the voltages obtained across the two C_L's after having integrated the input signal, where T_0 and T_1 indicate the domains of integrations of equal duration for Phase 0 and Phase 1, respectively. With these hypotheses it is possible to obtain equations 1–4 which model the operation of the device for the first PPM integration.

$$V_{f_{ph0}}^{p,(n)} = \frac{I_{OS}T_i}{C_p} + V_{i_{ph0}}^{p,(n)} + N_{f_{ph0}}^{p,(n)} \quad (1)$$

$$V_{i_{ph0}}^{(n)} = \frac{C_p}{C_p + C_{L0}} V_{f_{ph0}}^{p,(n)} \quad (2)$$

$$V_{f_{ph0}}^{(n)} = V_{i_{ph0}}^{(n)} + V_0^{(n)} \quad (3)$$

$$V_{i_{ph1}}^{p,(n)} = V_{f_{ph0}}^{(n)} \quad (4)$$

This first equation set is equivalent to states A–D of the graphical representation given in figure 3. **State A - equation 1**: It is assumed that the $(n-1)-th$ modulation has already completed thus the remaining voltage across C_p is $V_{i_{ph0}}^{p,(n)}$. After an an idle time T_i which separates the end of the $(n-1)-th$ Phase 1 and the beginning of the $n-th$ Phase 0, it is possible to calculate the expression of $V_{f_{ph0}}^{p,(n)}$. The formula includes also the offset contribution due to V_{OS} and the unexpected integration through C_p of the input signal immersed in additive gaussian noise $N_{f_{ph0}}^{p,(n)}$ when device is in idle state. This quantity is defined as $N_{f_{ph0}}^{p,(n)} = \frac{G_m}{C_p} \int_{T_i^{(n)}} Vin(t)dt$. **State B - equation 2**: when signal *Phase 0* is activated, a first charge redistribution is performed between C_p and C_{L0}, leading to an initial integration voltage $V_{i_{ph0}}^{(n)}$ across $C_p + C_{L0}$. **State C - equation 3**: At the end of the integration of the UWB pulses, the final voltage across $C_p + C_{L0}$, $V_{f_{ph0}}^{(n)}$ is obtained. The information about the integration of the first PPM phase is included in V_0. **State D - equation 4**: When signal *Phase 0* is deactivated, the remaining voltage across C_p is also the final voltage obtained during this last phase.

For the second PPM phase, it is possible to obtain a similar set of equations using the same hypotheses of above (equations 5–7, states E, F and G).

$$V_{f_{ph1}}^{p,(n)} = \frac{I_{OS}T_i}{C_p} + V_{i_{ph1}}^{p,(n)} + N_{f_{ph1}}^{p,(n)} \quad (5)$$

$$V_{i_{ph1}}^{(n)} = \frac{C_p}{C_p + C_{L1}} V_{f_{ph1}}^{p,(n)} \quad (6)$$

$$V_{f_{ph1}}^{(n)} = V_{i_{ph1}}^{(n)} + V_1^{(n)} \quad (7)$$

$$V_{f_{ph1}}^{(n)} = V_{i_{ph0}}^{p,(n+1)} \quad (8)$$

In this case, the quantity which accounts for the integration of UWB signal through C_p is $N_{f_{ph1}}^{p,(n)} = \frac{G_m}{C_p} \int_{T_i^{(n)}} Vin(t)dt$. The last condition of (8) relates the n-th demodulation cycle to the successive one. At activation of signal *Compare*, considering that the integration capacitors are equal ($C_{L0} = C_{L1} = C_L$), the final output voltage after the final charge redistribution (**state G**) is given by $V_{out}^{(n)} = \frac{1}{2}\{V_{f_{ph1}}^{(n)} - V_{f_{ph0}}^{(n)}\}$.

If we combine these equations, we can express $V_{out}^{(n)}$ as a function of $V_{out}^{(n-1)}$ (equation 9).

$$\begin{aligned} V_{out}^{(n)} = \frac{1}{2}\{V_1^{(n)} - \frac{C_L}{C_p + C_L} V_0^{(n)} + \\ + \frac{C_p}{C_p + C_L}\{N_{f_{ph1}}^{p,(n)} - N_{f_{ph0}}^{p,(n)} - V_1^{(n-1)}\} + \\ + \frac{C_p^2}{(C_p + C_L)^2}\{V_{out}^{(n-1)} - N_{f_{ph1}}^{p,(n-1)} + \\ + N_{f_{ph0}}^{p,(n-1)}\}\} \end{aligned} \quad (9)$$

In the case in which no reset switches across C_p are employed, the differential output voltage for the n-th integration $V_{out}^{(n)}$ depends on the stochastic processes $N_{f_{ph0}}^{p}$ and $N_{f_{ph1}}^{p}$ both for the n-th and the $(n-1)$-th demodulation phase. If C_p is zero, it is easy to demonstrate that demodulation voltage is ideal, that is $V_{out}^{(n)} = \frac{1}{2}\{V_1^{(n)} - V_0^{(n)}\}$. To obtain a similar effect in presence of parasitics, it is sufficient to reset the charge accumulated in C_p before a new phase starts with signal *Inhibit*. In this case, $V_{i_{ph0}}^{p,(n)} = V_{f_{ph1}}^{p,(n)} = 0$: That is, using the reset switches across C_p, the obtained output voltage is ideal. However, in both cases, the equations presented show how the symmetric structure of the circuit completely eliminates the effect of offset contribution V_{OS}. In fact, the final output voltage does not depend on current I_{OS}. In summary, the possibility of resetting charge in C_p before starting a new

demodulation allows to obtain almost ideal demodulation performance.

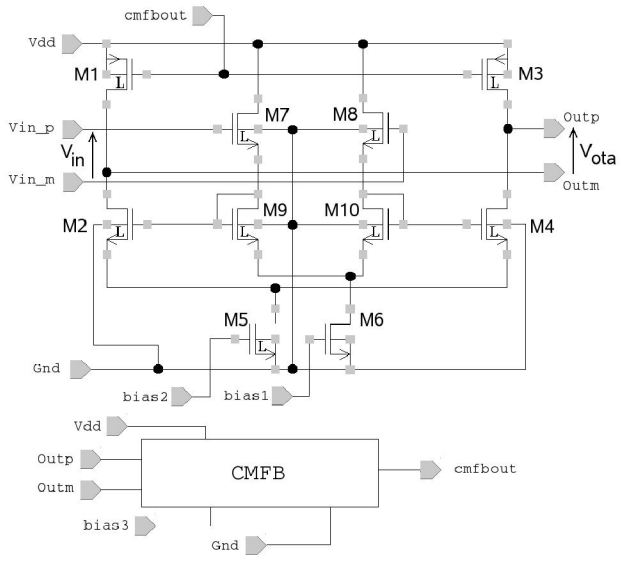

Fig. 4. Schematic of the Transconductance Amplifier

III. Design

The overall schematic of the Bi-phase integrator is presented in figures 4 and 5. The first shows the internal Operational Transconductance Amplifier structure, while the second shows the integration switches network. The aim of the design is to obtain a very high gain-bandwidth product to allow the integration of the UWB pulses (about 3.1–5 GHz for the first sub-band). The technology employed here is a mixed-mode CMOS 0.18 μm process. The circuit is fully differential and the OTA input stage consists of a source-follower differential stage. Current variations at the input are mirrored in the output stage through a MOSFET configuration similar to a current mirror. For enhancing overdrives some of the employed transistors have Low-threshold Voltages (L).

The amplifier includes auto-biasing circuits and also a simple Common Mode Feedback Network (CMFB) employing a differential stage only (not shown here for sake of brevity). On the one hand, as clarified in [8], the use of a common mode stabilization network is mandatory for integrators employing open-loop transconductors, thus an increase in the overall device power consumption is unavoidable. On the other hand no precise control of output voltages is necessary because demodulation is based upon a relative voltage comparison. In addition, temperature drifts, aging and voltage supply variations are reflected in the two integrated voltages V_0 and V_1 in the same way: As a result, the OTA does not require any transconductance tuning [9].

The supply voltage is 1.8 V and the common mode input bias is 0.9 V. The dynamic input and output ranges are limited to 160 mV and 600 mV respectively as the work aims at low-power consumptions [8]. The integrator has been simulated at different temperatures (up to 90° C) showing gain decrease of approximately 5 dB with respect to the nominal value (about 20 dB at 30° C, typical process) and greater self discharge in the load capacitors. Notwithstanding this, demodulation performance is only marginally affected by these effects because the integration time is limited and also because of the relative nature of the energy comparison. The integration capacitors are about 1 pF each.

In the schematic, the transistors aspect ratios are such that $M2 = M4$, $M3 = M1$, $M7 = M8$ and $M9 = M10$. If we analyze the small-signal equivalent model, neglecting drain–source resistances it is possible to reach a closed form of the equivalent OTA transconductance G_m,

$$G_m = \frac{g_{m2}}{2(1 + \frac{g_{m7}}{g_{m9}} + \frac{g_{mb7}}{g_{m7}})} \tag{10}$$

where g_{m2}, g_{m7}, g_{m9} are the equivalent transconductances of M2, M7 and M9, respectively. The quantity g_{mb7} is the body effect transconductance of M7. The gain can be increased by rising the M2 aspect ratio and by reducing the M7 W/L with respect to M9. As shown in the formula, gain is only affected by the M7 body-effect transconductance. This is not surprising because the source terminals of the other transistors (i.e. M2, M4, M9 and M10) are not connected in a differential stage fashion. Even though the input and output stages cannot be formally considered in a differential fashion, voltages V_A and V_B shown in figure 4 do not vary with the differential input signal. This results in a "balanced" simplification of such effect on both left and right branches of the circuit. In this work G_m is 167 μS at 30 ° C.

Neglecting parasitic MOSFET capacitances and taking into account the drain-source resistances of the output stage, it is also possible to calculate (equation 11) the overall transfer function of the OTA, $\frac{I_{out}}{V_{in}}$, which depends on a generic load impedance Z_L,

$$\frac{I_{out}}{V_{in}} = -\frac{g_{m2}}{(1 + \frac{g_{m7}}{g_{m9}} + \frac{g_{mb7}}{g_{m7}})(2 + \frac{Z_L}{r_{ds2}} + \frac{Z_L}{r_{ds1}})} \tag{11}$$

where r_{ds2} and r_{ds1} are the drain-source resistances of M2 and M1, respectively. The load impedance Z_L models the integration capacitances inclusive of parasitics and in the case of $Z_L = \frac{1}{s(C_L+C_p)}$, the output function $V_{out} = Z_L I_{out}$ presents a pole at low-frequency. It is easy to note that the equivalent output impedance of the OTA, which depends on the above drain-source resistances, influences the cut-off frequency of the resulting first order pole.

The pole in the OTA transfer function (at about 30 MHz), limits the maximum integration time to 30 ns. The integration of longer pulses would cause unacceptable losses in the computed energies because the pole time constant would be comparable to the integration time. The aspect ratios of MOSFET at the OTA output stage affect gain and bandwidth of the transconductance amplifier. Incrementing W/L has the effect of increasing the OTA gain and thus compensates the various drops in the output switching network. On the other hand rising W/L expands the frequency of the above mentioned pole: This leads to the reduction of the maximum integration time and shifts down high order poles (not shown in the above formula), reducing the overall system bandwidth.

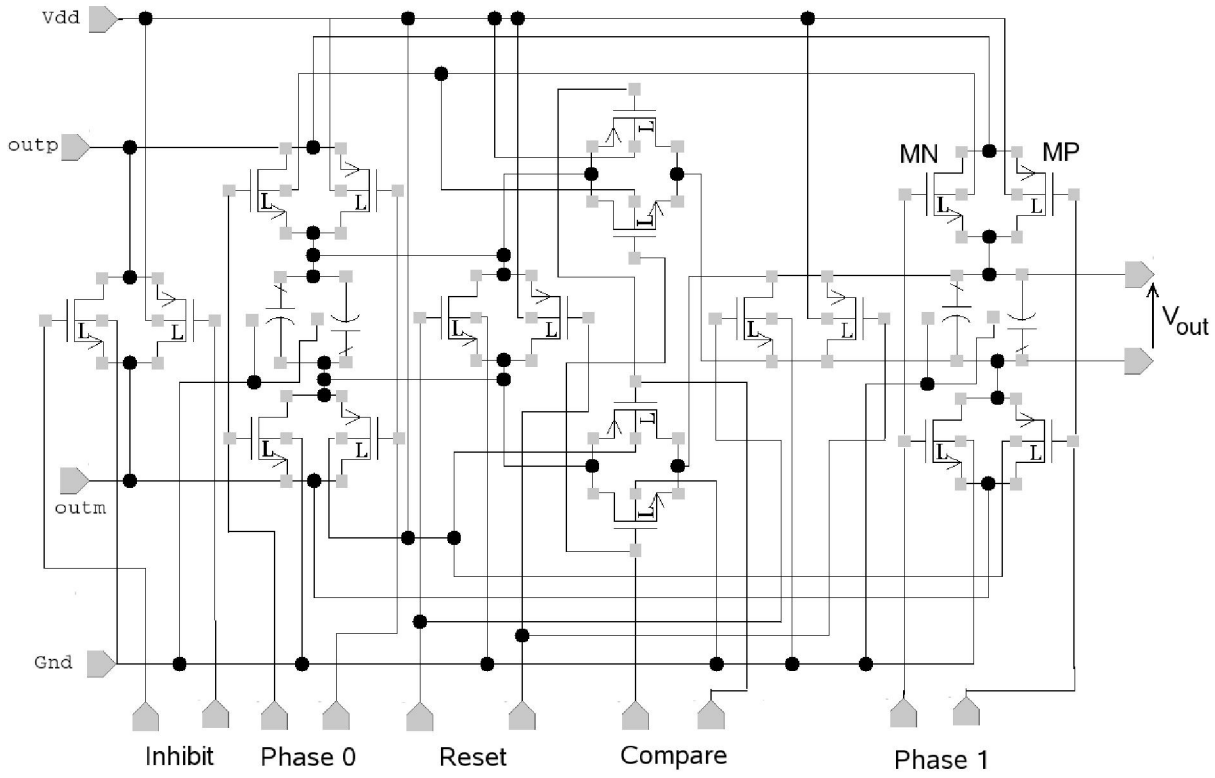

Fig. 5. Schematic of the Switched Capacitor Network

Moreover, the selection of transistor aspect ratios significantly influences other device characteristics: An increase of W/L mitigates distortions and increases gain but leads to higher power dissipations. Thanks to the non-coherent Energy Detection approach receivers do not require extremely precise pulse elaboration, thus it is possible to keep low W/L and take into consideration low-power aspects only.

The demodulation performances are influenced by the symmetrization of output-to-ground parasitic contributions in the two switching branches and thus by the symmetry of the fully differential architecture. The structure automatically avoids this problem as the integration network intrinsically provides the symmetry required to keep these contributions balanced. Moreover, each of the two integration capacitors C_{L0} and C_{L1} are implemented as a pair of anti-parallel MIM capacitors. The integration switches, as shown in figure 5 consist of transmission gates to ensure very low dropouts during activation. A compromised value for the aspect ratio (in this work on the order of 20) must be chosen to minimize the effects on integration gain: As the aspect ratio increases, drain-source resistances decrease but the higher to-ground parasitics reduce the integrator gain considerably.

Table I shows a summary of the transistors aspect ratios for the proposed solution. To minimise sub-micron effects, except for L transistors, channel lengths have been kept higher than the minimum values. MP and MN aspect ratios refer to p-MOS and n-MOS of the transmission gates.

IV. Simulations

In order to test the circuit in a realistic environment, an ad-hoc mixed VHDL-AMS/SPICE testbed has been created. It includes all the receiver blocks shown in figure 1, such as LNA, squaring unit, comparator, as well as the Spice model of the Bi-phase demodulator that includes the BSIM3 MOSFET models. An UWB 802.15.4a waveform database of measured channel responses for an indoor multipath environment (CM1) has been also included in the testbed: The possibility of including such pulses allows extensive BER simulations with the possibility of varying the noise level. Here, the modulation takes place every 200 ns of Pulse Repetition Interval (PRI) and an integration time of 30 ns, as previously mentioned, is used for both the 2-PPM phases.

Thanks to the flexibility of the mixed-signal simulation environment and particularly the possibility of performing transient simulations with reliable UWB pulses, it is possible to estimate both the quiescent and the average device power consumption. When the device is idle and no signal is present at the input, the power consumption, inclusive of biasing circuit, is 400μW. During normal operation, the power averaged on 4 ms of demodulation activity, is 1 mW. Even though the comparator is still an ideal block in the simulations, its power contribution does not appreciably modify the overall power figure. For instance, a typical comparator used in CMOS applications aimed at very high sampling rates (2GS/s) consumes just 360 μW [10], and rates lower of orders of magnitude are expected here.

It is possible to compare the circuit performance with an ideal Energy Detection receiver employing an integration

TABLE I

SOME OF THE ASPECT RATIOS OF THE MOSFET EMPLOYED IN THE BI–PHASE DEMODULATOR.

MOSFET	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	MP, MN
$W/L\,(\mu\text{m})$	11.2/0.24	2.4/0.24	11.2/0.24	2.4/0.24	10/10	45/5	7.2/0.24	7.2/0.24	2.4/0.24	2.4/0.24	4.8/0.24

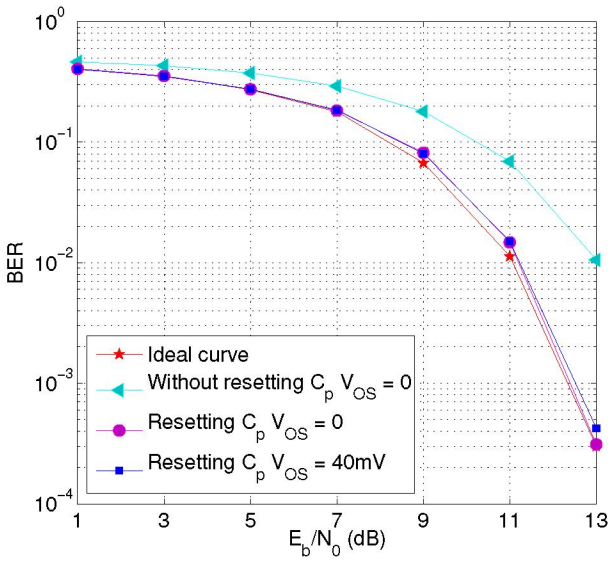

Fig. 6. BER curves comparison (ideal Energy Detection Receiver *vs* Bi–phase demodulator)

window of 30 ns using BER simulations. Figure 6 shows the comparison of error–rate performance between an ideal Energy Detection receiver and the Bi–phase demodulator. For the circuit three cases have been considered: In the first one the Bi–phase demodulator includes the *Inhibit* switches across C_p, in the second one the circuit does not employ any reset control on C_p. In the third one the offset rejection is proven: The simulation includes 40 mV of constant input offset V_{OS}, input range 80 mV, and the circuit includes the *Inhibit* switches across C_p. The large difference between the first two curves is thus due to the *Inhibit* switch: As previously shown in (9), the demodulation is affected by the voltage across C_p stored in each operation phase and by the output voltage of the previous demodulation cycle. While in the former case the effect of $N_{f_{ph0}}^{p,(n)}$ and $N_{f_{ph1}}^{p,(n)}$ is completely cancelled out, in the second case it remains. Thanks to the *Inhibit* switches, the Bi–phase integrator can reach about the same performance of an ideal Energy Detection receiver with infinite quantization resolution.

In the third case, it is possible to note how the circuit provides very high offset rejection as the curve perfectly overlaps the ideal trend. Thanks to the perfectly balanced integration switches network, the circuit allows to obtain the same performances of an ideal energy detection receiver, even if a significative offset contribution is present at input. These important results permit to verify the correctness of the hypotheses used in the design.

Considering the results obtained in this work, final design steps such as silicon fabrication are worthy of consideration. On the one hand, to ensure the symmetry of the circuit, careful layout placement is mandatory to minimise capacitive couplings among transistors. On the other hand, mixed–signal insulation techniques are essential to prevent that substrate couplings compromise OTA operation and inject charge in the load capacitors.

V. CONCLUSIONS

This paper presented a new CMOS 0.18 μm 2–PPM demodulator architecture based on a switched capacitor network and a $G_m - C$ open loop integrator. Through analytical models it has been shown how the device manages parasitics for obtaining very high performance. The circuit has been tested with a mixed–signal simulation environment employing the realistic TG4a channel model and the BSIM3 MOSFET models. BER simulations have shown that the device has about the same performance of an ideal Energy Detection receiver employing infinite A/D resolution. The performance figures show that circuit provides a total offset–rejection thanks to its perfectly balanced output switching network. Its low power consumption, 1 mW during demodulation, makes the device appealing for low–power portable devices based on the non–coherent Energy Detection paradigm. This work justifies further design steps such as silicon fabrication aiming at comparing simulations and measured results.

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