RF Immunity of Digital Integrated Circuits: Measurements, Modeling and Validation

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USTL LILLE 1

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Friday June 15 **10:45 am – 12:30 am**

POSTER SESSION II, Room: Cloister

WIRELESS SYSTEMS

1) *On the use of wireless communication systems on ships*, C. Klunder, A. Schoof and J. L. Ter Haseborg
2) *Conditions of EMC of narrowband and ultrawideband radio equipment: a method of calculation*, N. I. Azamatov, Y. Mosienko, V. Voloshin and S. Kuntsevich
3) *Propagation in noisy multipath environment: extraction of paths characteristics*, A. Nasr, M. Lienard and P. Degauque
4) *Mask based mobility model: A 2D-outdoor 3D-indoor mobility model*, C. Joumaa, A. Caminada and S. Lamrous
5) *On the use of EMC compliance test results to demonstrate EMF compliance*, D. W. Harberts

CIRCUIT LEVEL

1) *Effect of DQ/GIO data pattern and power delivery design on EMI in DRAM*, J. Lee, D. K. Yoon, K. Park, H. Lee, J. Chang and J. Kih
2) *An enhanced interconnect model for SI analysis*, G. Antonini, A. Di Pasquale, F. Ferranti, M. Italiani, A. Orlandi, R. Rizzi
3) *RF immunity of digital integrated circuits: measurements, modeling and validation*, I. S. Stievano, E. Vialardi and F. Canavero
4) *A near field injection model including power losses for susceptibility prediction in IC*, A. Alaeldine, A. Boyer, R. Perdriau, M. Ramdani, E. Sicard and M. Drissi
5) *Modelling of components and circuits up to 3 GHz*, H. Maghdad, L. Nuno, J. J. Jerez and J. V. Balbastre
6) *Power converters conducted emissions and EMC filtering*, Y. Poiré, O. Maurice, M. Ramdani, M. Drissi and A. Sauvage
7) *Coupling MoM and PEEC methods with Kron's transformation for EMC study of embedded systems*, J. Ben Hadj Slama, O. Maurice, R. Titreville, A. Louis and B. Mazari
8) *Analysis of Package Inductance and DQ driver strength dependency on DRAM EMI*, D. Yoon, J. Lee, K. Park, H. Lee, S. Lim and J. Kih
9) *Engineer tool for analysis of EMC systems: power of SPICE modelling*, A. Alcaras, N. Gouedard, C. Girard and R. Chatraoui
10) *Magnetic cartography and susceptibility of logic circuits*, S. Jarrix, A. Penarier, P. Nouvel, T. Dubois, D. Gasquet and B. Azaïzs
11) *EMC studies of switching noise and near-field couplings in electrical transport architectures*, E. Batista and J. M. Dienot

RF IMMUNITY OF DIGITAL INTEGRATED CIRCUITS: MEASUREMENTS, MODELING AND VALIDATION

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Abstract: This paper demonstrates that the Mπlog technique, already proposed in the literature for the generation of accurate and efficient IC macromodels, can be extended to the prediction of device immunity effects. The proposed models account for both the functional and the out-of-band behaviour of devices. The IC models are generated from port device responses only and can be implemented in any commercial tool based on SPICE or VHDL-AMS solvers. The approach is demonstrated on a real test board by injecting a RF noise disturbance into a digital IC: a systematic study comparing actual measurements and simulation predictions is carried out.

I. INTRODUCTION

Nowadays, the complexity of modern high-end electronic equipments as well as the time-to-market constraints require the assessment of system performance in the very preliminary stage of their design. Many ICT systems like mobile phones or safety equipments mounted on vehicles, airplanes and trains are immersed in a noisy EM environment and must satisfy severe reliability constraints in terms of signal integrity and electromagnetic compatibility. In the above electronic systems, the most critical elements are the digital devices that may poorly operate in the presence of EM disturbances.

In this paper, we propose a systematic study of the effects of RF noise directly or indirectly coupled to digital systems. This study will lead to the generation of accurate and efficient macromodels of digital devices, accounting not only for their functional behaviour, but also providing insights on their RF immunity. Predictions obtained by means of the proposed IC macromodels and SPICE simulations are compared to actual measurements carried out on a real test board.

II. TEST BOARD

For the sake of simplicity, the study is conducted on a data communication link composed by two digital devices interconnected by a PCB trace. In order to inject the RF noise into the system, the test board shown in Fig. 1 has been designed as suggested by [1]. The board implements the idea of injecting a disturbance through a long coupled interconnected structure. The two devices, i.e., a driver on the right side in Fig. 1 and a receiver on the left, are connected to terminals 4 and 2 of the coupled structure, respectively. A RF generator is connected to the terminal 3 and a 50 Ω matching resistor to terminal 1. The interconnection, that has a length of 25 cm, is designed to maximize the coupling between the signal communication line and the aggressor trace carrying the RF disturbance. In this study, the two digital ICs in Fig. 1 are simple inverter gates (TI SN74AUC1G04DBVR), optimized for 1.8-V operation. This simplified structure and the two inverters are considered to avoid the complexity of real ICs mounted on an application board and thus allowing to completely understand and model the RF immunity of a digital circuit.

In this work, all the parts composing the complete system in Fig. 1, i.e., the coupled interconnect and the two devices, are modeled by means of suitable modeling methodologies, as suggested in [2]. All the models are then implemented in SPICE in order to simulate the complete interconnected structure.

In particular, the macromodels for the two digital devices are obtained by means of the state-of-the-art Mπlog (Macromodeling via Parametric Identification of Logic Gates) methodology [3]. A brief review of the Mπlog technique is provided in Section III.

The coupled line structure on the board was characterized by means of a two-port network analyzer that has provided a complete set of S parameters up to 2 GHz. These measurements were used to generate a model of the linear interconnect, by means of the IdEM (Identification of Electrical Macromodels) methodology [4]. IdEM is a modeling technique based on the estimation of a reduced order rational

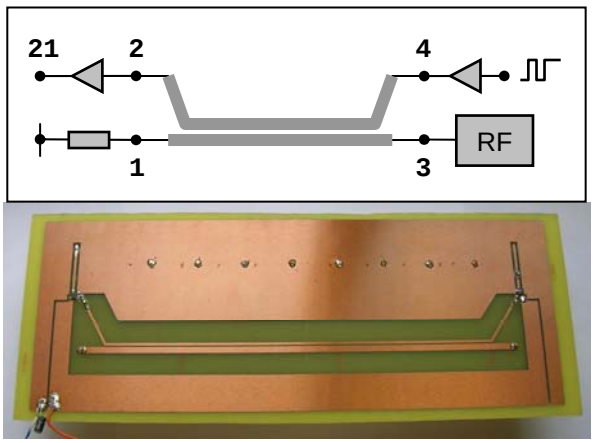

Fig. 1. Ideal setup designed to inject the RF noise into a digital IC (top panel). Test board (bottom panel).

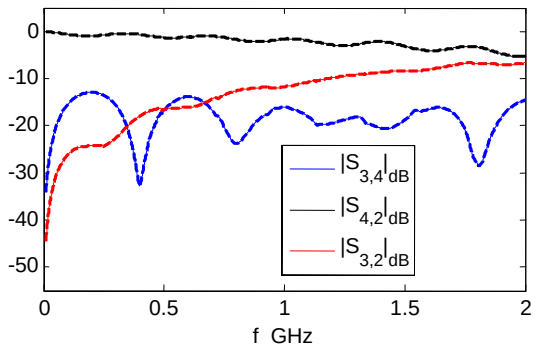

Fig. 2. Selection of S parameters of the test board in Fig 1. Solid lines: measured parameters; dashed lines: model responses.

approximation reproducing the port behaviour of a complex linear structure from their port responses. The approximation is performed via the powerful and well-known Vector Fitting (VF) algorithm [5], with an a-posteriori correction to assure the passivity of the obtained rational model [6]. Fig. 2 shows a selection of port frequency responses; the comparison of measurements and fitting highlights the accuracy of the obtained model to reproduce the real measurements.

III. IC MACROMODELS

In this Section, we briefly review the Mπlog approach [2-3], providing an effective methodology for the construction of accurate and efficient behavioral models of logic devices. This approach amounts to the estimation of parametric relations from suitable device port transient responses. The device stimuli are voltage sources devised to excite every possible dynamic behaviour of the port within a predefined bandwidth, thus allowing the obtained models to account for both the functional and the out-of-band behaviour of devices.

As an example, output buffer constitutive relations are sought as dynamic nonlinear parametric two-piece models of the form

$$i(t) = w_H(t)\, i_H(v(t),d/dt) + w_L(t)\, i_L(v(t),d/dt) \qquad (1)$$

relating the port voltage v and current i variables, where i_H and i_L are parametric submodels describing the port behaviour in the HIGH and LOW logic states, respectively, and $w_H(t)$ and $w_L(t)$ are weighting coefficients describing state transitions. Parametric nonlinear relations and system identification methods like those involving the identification of mechanical systems, economic trends, etc. allow us to obtain improved nonlinear dynamic models for submodels $i_{H,L}$ in the above representation. Parametric models are usually expressed as sums of basis (e.g., sigmoidal) functions of the involved variables and their parameters are estimated by fitting the model responses to suitable transient responses of the input and output variables related by the model. In this case, the related variables are the voltage and current of the output port in fixed logic state and the model parameters are computed by minimizing a suitable error function between voltage and current waveforms of the model and real device. Specific algorithms are available to solve this problem, depending on the choice of the family of basis functions used to define the parametric models [3].

Parametric models offer rigorous mathematical foundations, identifiability from external observations, good performances for the problem at hand as well as preserving the ability to hide the internal structure of the modeled devices. Finally, parametric models can be readily implemented according to standard industrial simulation tools like SPICE and VHDL-AMS. In addition, such already-mentioned SPICE and VHDL-AMS implementations are completely compatible with the multilingual extension of IBIS (Input/output Buffer Information Specification), which is the most established standard for the behavioral description of IC ports. In fact, ver. 4.1 of IBIS specification [7] is an extension, recently devised to overcome some limitations of the original standard, allowing for more general models not necessarily based on simplified circuit interpretations.

Details on parametric modeling of single-ended CMOS devices, possibly accounting for the device temperature, the power supply voltage, and the power supply current drawn by buffers, can be found in [3], where the parametric approach is applied to the modeling of input and output ports of commercial devices by means of the transient responses of their transistor-level models. The estimation of parametric models from measured transient responses is demonstrated in [8]. Recent advances on the modeling of receiver circuits, including the logic detection mechanism and the effects of power supply voltage fluctuations are reported in [9]. Finally, results on the modeling of differential Low Voltage Differential Signaling (LVDS) devices are described in [10].

The Mπlog modeling procedure discussed in this Section is applied to build the macromodels for the two ICs mounted on the test board of Fig. 1. For this study, the models are obtained from the responses of detailed transistor-level descriptions of the devices that are freely available from the official website of the vendor. These macromodels are computed for a power supply voltage of 1 V, which will be hereinafter used for carrying out our study. This supply level, which is close to the lower limit indicated by the manufacturer, was adopted since it is representative of the most critical bias conditions of the device for its noise immunity.

The obtained Mπlog models are implemented as SPICE subcircuits and then validated by comparing measurements and simulation results of the complete interconnected structure of Fig. 1 in the absence of any RF noise (i.e., the RF source is not connected and is replaced by a matching resistor of 50 Ω). The model results are in excellent agreement with measurements, as already documented in the literature [3,8] (detailed results are not reported here for lack of space).

IV. DEVICE IMMUNITY

In this Section, the test board shown in Fig. 1 is used to perform a systematic set of measurements aimed at the assessment of the immunity of the receiver circuit mounted on the left side of the board. As already outlined in the introduction, a RF generator with 50 Ω internal impedance and a variable frequency and power is used to inject a disturbance into the communication system. The RF noise, which couples with the functional signals transmitted on the communication line, is increased to verify the receiver immunity thresholds. For this reason, the voltage signal at input terminal 2 of the receiver and the transmitted voltage at terminal 21, i.e., the data processed by the receiver circuit, are monitored to verify possible communication errors. It is worth to remark that the noise immunity of the driver is not considered since, for technological reasons, the internal circuitry of a driver is much more immune to a disturbance injected into its output port. In this experiment, the RF generator produces a 267 MHz sinusoidal waveform and its power is varied between 10 and 23 dBm. The input terminal 41 of the driver circuit is instead connected to a waveform generator producing a square wave signal, i.e. a 010 cyclic bit stream, with a period of 100 ns. A digital scope (Lecroy WavePro 7000A Series) and passive voltage probes (Tektronix P6114B) with a bandwidth of 3 GHz are used to record the voltage signals along the propagation path.

In order to verify the feasibility of the proposed modeling approach to predict the immunity effects of devices, the agreement between real measurements and simulations is assessed. The macromodels obtained for both the devices and the coupled line are used together in a SPICE environment to simulate the complete interconnected structure of Fig. 1. It is worth adding that the lumped equivalents of the voltage probes, as provided by the supplier, are included in the simulation setup to reproduce the real measurements.

Fig. 3 shows an example of a comparison between measured and predicted responses for the voltage signal at the input (terminal 2) and at the output (terminal 21) ports of the receiver when the power of the RF generator is 10 dBm. The plots are obtained by wrapping in time twenty different periods of the receiver port voltage responses. This comparison highlights that the accuracy of signals predicted by the macromodels are in very good agreement with actual measurements. Besides, the differences between measurements and simulations are mainly due to the model that has been generated from the transistor-level description of devices. Better results could be obtained for models generated from measured data as suggested in [8]. It is also worth to notice that, in this case, the power of the injected disturbance is not sufficient to generate errors in the transmission of the functional signal, even if the input voltage of the receiver has a quite large amount of noise superimposed to the functional part of the signal.

Table I.
RF Immunity of the Receiver at High and Low States

RF power level (dBm)	errors @ receiver output - V21 (measurements / simulations)	
	HIGH state	LOW state
10	no / no	no / no
13	no / no	possible / possible
16	no / no	yes / possible
20	possible / possible	yes / yes
23	yes / yes	yes / yes

The power of the injected RF signal is then increased to verify potential errors of the received bit at terminal 21. Table I collects the main results of the study and provides in a compact form the information for both the received data 0 (output of the receiver at low state) or 1 (output of the receiver at high state). Each cell compares the possibility of receiver errors estimated from measurement or simulation. Apart from the classical indications (*yes* and *no*), a third keyword (*possible*) is used in this table: it means that some glitches in the corresponding H or L states exist and, consequently, error detections at the output of the receiver are possible, depending upon the sampling time. An example of this behaviour is the simulation curves reported in the bottom panel of Fig. 4, where results of the RF injection of 16 dBm are shown. In this case, the low state is perturbed just after the

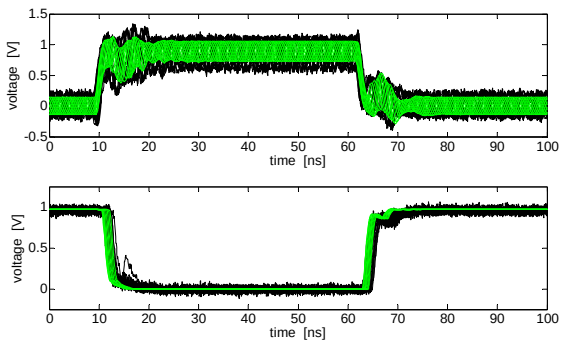

Fig. 3. Voltage signals at input port (top panel) and output port (bottom panel) of the receiver for an injected RF noise level of 10 dBm. Black lines: measurements; green lines: simulations.

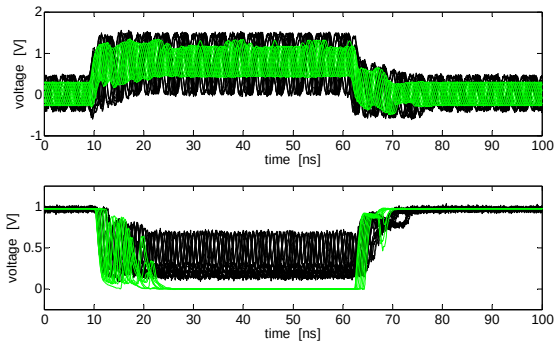

Fig. 4. Voltage signals at input port (top panel) and output port (bottom panel) of the receiver for an injected RF noise level of 16 dBm. Black lines: measurements; green lines: simulations.

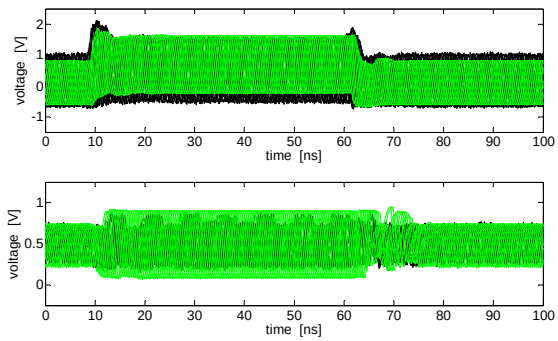

Fig. 5. Voltage signals at input port (top panel) and output port (bottom panel) of the receiver for an injected RF noise level of 23 dBm. Black lines: measurements; green lines: simulations.

switching by some spurious transitions which can generate faults in the data communication link.

Moreover, the 16 dBm test case shows an asymmetric behaviour of the device immunity for the two logic states: the H state is more robust than the L one. In fact (see Table I), a RF level of 23 dBm must be injected in the system for inducing regular faults in the high state, whereas a noise power of 13 dBm may already provoke errors in the low state.

Even in such a critical situation of asymmetry, the Mπlog approach proves its capabilities, thanks to the two-piece structure (see Eq. 1). Only in the L logic state of the test employing a power of 16 dBm, a discrepancy between the model and the measurements can be noticed in the bottom panel of Fig. 4: the output of the real receiver is perturbed by spurious transitions whatever the sampling time is, while the Mπlog predicts them only just after the switching. This discrepancy can be explained by analyzing the top panel of the same Fig. 4 reporting the voltage at the input port of the receiver (terminal 2): it highlights differences between measurement and simulation results on the amplitude of the oscillations, especially for the H input state. This leads to suspect a non-optimal transistor-level description of the device input port and confirms the need of an Mπlog macromodel extraction from ad-hoc measured data.

Finally, when the injected power reaches 23 dBm (Fig. 5), the receiver is no longer able to reproduce at its output port the functional signal, both for the L and the H state, but such signal is so distorted that it appears to be almost a replica of the injected noise disturbance. Also in this case, the Mπlog models (even if extracted from transistor-level descriptions) ensure good quality predictions of the out-of-band and out-range behaviour of the devices, both in terms of amplitude level and of waveform shape.

V. CONCLUSION

This paper describes a preliminary application of the systematic Mπlog methodology for the modeling of the noise immunity of inverter gates representing the input ports of digital ICs. Obtained results highlight the capability of the proposed approach to model both the functional and the out-of-band behaviour of such devices. Next steps towards the generation of a complete IC macromodel will have to focus on the injection of RF noise into the power supply net of the device and on the modeling of these effects.

VI. AKNOWLEDGEMENT

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