Linear and Nonlinear Macromodels for Power/Signal Integrity

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***Abstract*— In this paper, a systematic methodology for the assessment of Power/Signal Integrity effects in high-speed communication and information systems is presented. The proposed methodology leads to accurate and efficient macromodels for logic devices, transmission-line interconnects and discontinuities that can be easily implemented in any commercial tool and can be combined for the simulation of the whole system. The SPICE implementation of macromodels is used for the prediction of power/ground noise and signals propagating on interconnects. An assessment of the impact that possible simplifications in the macromodel generation phase have on the simulation of a realistic application example, is discussed.**

I. Introduction

In today's digital and mixed-signal circuit design, a serious concern is represented by interference noise, caused by crosstalk on signal busses and by current transients due to the synchronized switching of a huge number of digital gates. To assess and circumvent such problems prior to fabrication, a reliable analysis needs to be conducted during the design and verification process.

Such an assessment amounts to predicting the power and ground noise fluctuations and the signals propagating on the interconnects via numerical simulation. The combination of propagation effects with possibly very complex geometry and with nonlinear/dynamic behavior of logic devices makes a direct full-wave approach not feasible. Therefore, the feasible strategy that we present here amounts to subdividing the propagation path into separate and well-defined sub-structures, each of which is separately characterized by a macromodel, *i.e.,* a set of equations that are able to reproduce with sufficient accuracy the port behavior. Different macromodeling strategies are needed for the different structures: the nonlinear drivers and receivers terminating the interconnects, the interconnection elements characterized by a complex geometry, *i.e.,* discontinuities such as packages or via holes, and segments of uniform transmission-line structures at chip, module or board level. The proposed macromodels offer good accuracy and improved efficiency and can be easily implemented in any commercial tool as SPICE subcircuits and be used in any conventional circuit solver for the simulation of the whole system.

The following Sections provide short descriptions of the separate modeling methodologies adopted for the three classes of devices that we use to build the entire communication system. The paper is then concluded by a discussion of the impact that different simplifications in the generation of macromodels can produce on predicted signals.

II. Discontinuities

Discontinuities in the transmission paths represent a critical bottleneck for the integrity of high-speed signals in electronic systems, since their presence typically imposes serious bandwidth limitations. Such discontinuities can be vias and via arrays, bends, junctions, connectors, etc. A careful assessment of their effects requires a proper modeling of such structures, whose geometry and material properties must be taken into account, thus requiring a complex full-wave electromagnetic analysis.

The modeling approach is based on the characterization of discontinuities via full-wave analysis and/or by direct measurement. As a result of the characterization, a set of port responses in time or frequency domain are available, and constitute a large amount of data to be processed to obtain a global macromodel. For this reason, a partial macromodeling of several disjoint subsets of P_k port responses each is done first; the partial macromodels, which are processed independently, are then easily assembled into a global macromodel for the entire structure.

The Vector Fitting algorithm, either in its conventional frequency-domain formulation [1] or in its more recent time-domain extension [2] is the main macromodeling engine providing a rational approximation for each subset in the following form

$$\boldsymbol{H}_k(s) \simeq \boldsymbol{H}_{k,\infty} + \sum_{n=1}^{N_k} \frac{\boldsymbol{R}_{k,n}}{s - p_{k,n}} \,, \tag{1}$$

with diagonal $\boldsymbol{H}_{k,\infty}$ and $\boldsymbol{R}_{k,n}$. The global macromodel for the entire structure is recovered by tiling the partial macromodels according to

$$\boldsymbol{H}(s) = \sum_{k=1}^{K} \boldsymbol{Q}_k^T \boldsymbol{H}_k(s) \boldsymbol{P}_k \,, \tag{2}$$

where matrices $\boldsymbol{P}_k$ and $\boldsymbol{Q}_k$ are $P_k \times P$ selectors having a single unitary entry in each row with all the other entries vanishing. As a final step, the poles/residues representation (1) is translated by standard techniques into an equivalent state-space representation, which is suitable for implementation into

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standard industrial simulation tools like SPICE and VHDL-AMS.

The resulting macromodel is usually characterized by excellent accuracy, and it is stable by construction. However, it might not be passive since it was identified by a sequence of least squares solutions that do not guarantee passivity a priori. Since a non-passive macromodel can lead to unstable solutions when its terminations are changed, passivity is checked and enforced using spectral perturbation of an associated Hamiltonian matrix [3].

III. Transmission-Line Interconnects

At each scale (chip, board or system level), the information is exchanged via busses, that often can be represented as transmission lines. Their main effects on the conducted signals are delays due to their physical length, shape distortion due to losses in the conductors and substrate, and crosstalk among adjacent traces. An accurate and efficient transient analysis of the information propagation on busses is still a challenging task, due to the intrinsic difficulties in the design of stable algorithms for the time-domain analysis of structures with frequency-dependent parameters.

As a simulation strategy, we employ a generalized version of the well-known Method of Characteristics, that allows to deal with multiconductor lines whose per-unit-length parameter matrices have a possibly complex dependence on frequency. In such case, both the characteristic admittance and the propagation operators of the line are frequency-dependent. In our approach [4], the line equations are projected onto their high-frequency asymptotic modes. This leads to a particular form of the propagation operator that allows an easy extraction of the asymptotic line modal delays, as follows:

$$\mathbf{P}(s) = \mathrm{diag}\{e^{sT_k}\}\,\mathbf{M}_\infty^{-1}\,e^{-\mathcal{L}\boldsymbol{\Gamma}(s)}\,\mathbf{M}_\infty, \tag{3}$$

where $\boldsymbol{\Gamma}^2(s) = \mathbf{Y}(s)\mathbf{Z}(s)$, and $\mathbf{Z}(s)$, $\mathbf{Y}(s)$ are the per-unit-length matrix impedance and admittance of the line, respectively; T_k represent the line modal delays and $\mathbf{M}_\infty$ is a matrix of their corresponding eigenvectors.

A second step is the generation of a rational approximation of the above-defined delayless propagation operator,

$$\mathbf{P}(s) \simeq \sum_n \frac{\mathbf{R}_n^P}{s - q_n} + \mathbf{P}_\infty$$

and of the characteristic admittance

$$\mathbf{Y}_c(s) = \boldsymbol{\Gamma}^{-1}(s)\mathbf{Y}(s) \simeq \sum_n \frac{\mathbf{R}_n^Y}{s - p_n} + \mathbf{Y}_\infty \tag{4}$$

The final step of the macromodeling procedure is the generation of a lumped equivalent that can be used in a system-level simulation environment. The synthesis of lumped equivalents corresponding to rational expansions of characteristic admittance and delayless propagation operators is a standard task: SPICE-like implementation uses the basic elements, combined with dependent sources and ideal lossless lines, while the VHDL-AMS model implements the corresponding delayed differential equations.

IV. Logic Devices

In the distribution networks of digital signals, the terminations represented by the IC drivers and receivers are critical elements, since their intrinsic nonlinear and dynamic behavior can significantly affect the capacity of the propagation paths. Therefore, accurate and efficient macromodels are required.

In this Section, we briefly review the Mπ*log* approach [5], providing an effective methodology for the construction of accurate and efficient behavioral models of logic devices. In this approach, output buffer constitutive relations are sought as dynamic nonlinear parametric two-piece models of the form

$$i(t) = w_1(t)i_1(v(t)) + w_2(t)i_2(v(t)) \tag{5}$$

where $i_n(t)$, $n = 1, 2$ are submodels describing the port behavior in the HIGH and LOW logic states, respectively, and $w_n(t)$, $n = 1, 2$ are weighting coefficients describing state transitions.

Parametric nonlinear relations and system identification methods like those involving the identification of mechanical systems, economic trends, etc. allow us to obtain improved nonlinear dynamic models for submodels $i_{1,2}$ in (5), see [7]. Parametric models are usually expressed as sums of sigmoidal functions of the involved variables and their parameters are estimated by fitting the model responses to suitable transient responses of the input and output variables related by the model. In this case, the related variables are the voltage and current of the output port in fixed logic state and the model parameters are computed by minimizing a suitable error function between voltage and current waveforms of the model and real device. Specific algorithms are available to solve this problem, that depend on the choice of the family of basis functions used to define the parametric models. Parametric models offer rigorous mathematical foundations, identifiability from external observations, good performances for the problem at hand as well as preserving the ability to hide the internal structure of the modeled devices. Finally, parametric models can be readily implemented according to standard industrial simulation tools like SPICE and VHDL-AMS. In addition, such already-mentioned SPICE and VHDL-AMS implementations are completely compatible with the multilingual extension of IBIS (Input/output Buffer Information Specification), which is the most established standard for the behavioral description of IC ports. In fact, ver. 4.1 of IBIS specification [6] is an extension, recently devised to overcome some limitations of the original standard, allowing for more general models not necessarily based on simplified circuit interpretations.

Details on parametric modeling of single-ended CMOS devices can be found in [7], where the parametric approach is applied to the modeling of input and output ports of commercial devices by means of the transient responses of their transistor level models. The estimation of parametric models from measured transient responses is demonstrated in [8]. The extension of the methodology in order to take into account the device temperature, the power supply voltage, the

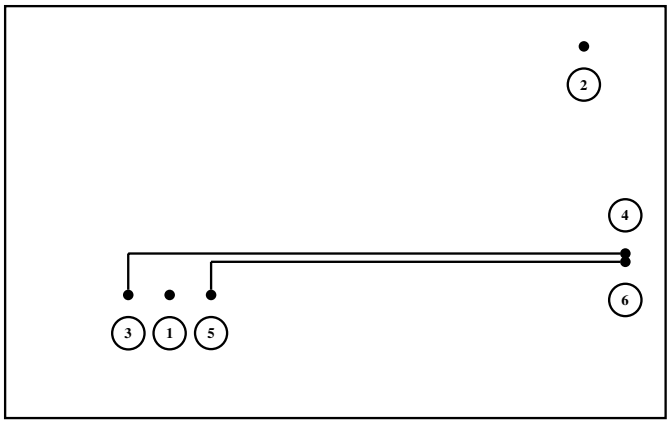

Fig. 1. PCB structure used for illustration of the proposed methodology. The board size is 16×10 cm, with a power-signal-ground configuration ($\sigma = 5.9 \times 10^7$ S/m for all conductors). Each layer ($\varepsilon_r = 4.2$, $\tan\delta = 0.001$) is 0.7 mm high. The stripline conductors are 0.2 mm wide with a separation in the coupled segment of 0.5 mm. Port locations are, in mm units from the bottom-left corner, 1:(40,30), 2:(140,90), 3:(29,31), 4:(150,41.1), 5:(49,31), and 6:(150,40.6).

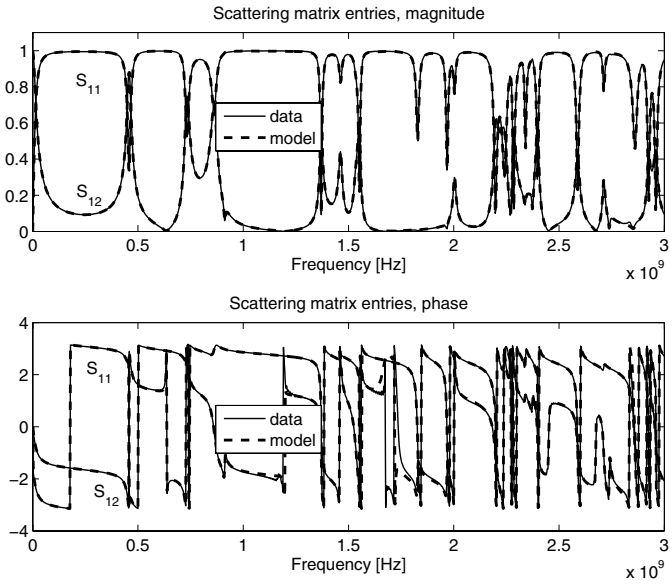

Fig. 2. Macromodel generation for the power/ground structure depicted in Fig. 1.

power supply current drawn by buffers as well as to model tri-state devices is addressed in [5]. Finally, some preliminary results on the modeling of differential Low Voltage Differential Signaling (LVDS) devices has appeared in [9].

V. Examples

In this section, we apply the proposed methodology to a simple PCB test case, depicted in Fig. 1. Ports 1 and 2 are located between the power and ground conductors, while ports 3–6 provide the termination to a coupled stripline structure. A full-wave transient solver based on the Finite Integration technique [10] was used to generate the frequency-dependent scattering responses of the structure up to a maximum frequency of 3 GHz. Two different simulations were performed. The first simulation included both power/ground planes and stripline conductors, and resulted in a 6-port scattering matrix. In the second simulation, we removed the signal conductors and we obtained a simplified unpopulated power/ground structure with only ports 1 and 2 left. This second run is aimed at the assessment of the power-ground model variations due to the presence of additional signal conductors in the structure.

Passive macromodels were generated for both populated and unpopulated structures. First, a rational fit based on the Vector Fitting algorithm was generated. Then, the correction scheme of Section II was used to enforce the macromodel passivity. As an example, we compare in Fig. 2 some macromodel responses to the original scattering responses for the populated board case. The plots show that the accuracy that can be achieved with the proposed technique is excellent, throughout the entire modeling bandwidth.

The above macromodels were synthesized into equivalent circuits in SPICE form, and three different SPICE decks were run. In all cases, the two stripline conductors were connected at port 3 and 5 to the output ports of two identical switching drivers forcing a bit pattern of 01001 and 00100, respectively. The driver is a Philips LVC244 3.3 V CMOS device, whose reference transistor-level description is available from the official site www.semiconductors.philips.com. A macromodel of the driver has been generated from the responses of the reference model by means of the Mπ*log* procedure of Sec. IV and the SPICE implementation of the macromodel is used for the simulation experiment. Also, the striplines were terminated by 50Ω loads at ports 4 and 6. Port 2 was connected by a 3.3 V battery in series with a 1Ω resistance, while port 1 was directly connected to the power supply ports of the two switching drivers.

The difference in the three SPICE runs is only on the models that were used for the power, ground, and signal conductors, as itemized below.

- (i) The first setup used a fully rational macromodel for the complete 6-port structure representing power, ground, and signal conductors.
- (ii) The second setup used a rational macromodel only for the 2-port power/ground structure obtained for the populated board case. The stripline conductors were modeled as lossy transmission lines using the procedure outlined in Section III. The two lines were considered coupled only in the parallel segment (see Fig. 1).
- (iii) The third setup used the simplest rational macromodel of the unpopulated 2-port power/ground structure. The stripline conductors were modeled as lossy transmission lines as for the second setup.

Note that, in order to produce a fair comparison between the three cases, a correction for the DC resistance of the stripline conductors of case (i) was necessary. In fact, the employed full-wave solver allowed only a $\sqrt{f}$ type of conductor loss,

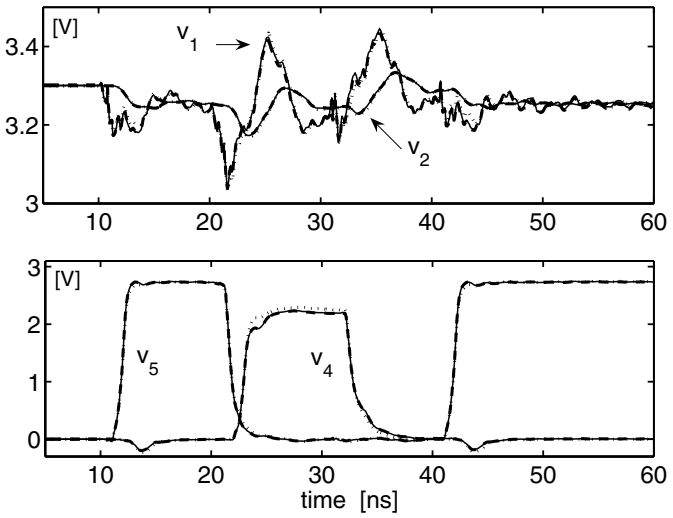

Fig. 3. Set of port voltage responses for the three SPICE runs of the example test case of Sec. V: (i) full macromodel for the structure of Fig. 1 (dotted lines); (ii) two-port macromodel for the populated power net and the line macromodel (dashed lines); (iii) simplified two-port macromodel for the power net and the line macromodel (solid lines).

resulting in no DC losses for all conductors. Consequently, no DC loss was present in the corresponding 6-port rational macromodel. On the other hand, an accurate set of frequency-dependent per-unit-length line parameters was generated for cases (ii) and (iii) via 2D transverse electromagnetic simulation, including the DC resistance. This resistance (about 5Ω) was therefore inserted as a lumped component in series to each stripline port in the SPICE deck of case (i).

Figure 3 shows the transient responses of voltages $v_1(t)$, $v_2(t)$, $v_4(t)$ and $v_5(t)$ for the above SPICE simulations. For the example board of Fig. 1, the above curves highlight a very good agreement between the three different predictions of transmitted signals on conductors, on power/ground noise and on sensitive effects like crosstalk. Even if simplified (uncoupled) macromodels for the power/ground part are used and combined to conventional transmission line macromodels for the signals conductors, only negligible differences can be registered for the steady state values of voltage responses v_4 and v_5 due to the correction of DC resistance, as already mentioned above.

As an additional index of performance, Table I summarizes the results on the efficiency of macromodels for the computation of the curves of Fig. 3, thus highlighting the speed-up improvement introduced by the simplified macromodels used in the SPICE runs (ii) and (iii).

TABLE I

CPU TIME COMPARISON FOR THE PREDICTION OF THE CURVES OF FIG. 3.

SPICE run	Sim. time
(i) fully rational macromodel	426 s
(ii) 2-port macromodel	129 s
(iii) simplified 2-port macrom.	119 s

VI. CONCLUSIONS

This paper presents different macromodeling strategies devised for the various structures that can be found along high-speed propagation paths. Macromodels of logic devices, that are nonlinear dynamic circuits, are expressed in terms of parametric equations reproducing the device behavior; signal busses, that can be represented as transmission lines with significant propagation delays together with dispersion and losses, are macromodeled as lumped equivalents combined with the line modal delays; finally, macromodels of discontinuities are linear, lumped equivalents fitting the port characteristics of the structure. All macromodels can be cast in terms of equivalent circuits, ready for system-level analyses using SPICE-like circuit solvers. The application example developed in this work shows the efficiency of using the advocated decomposition approach for the power and signal integrity characterization of high-performance digital systems. The considerable simulation speed-up and the readiness for trying several different configurations by simply linking macromodels is appealing for a designer who must perform what-if analyses during each new product development. Also, the excellent accuracy achieved in this paper, although for a simplified study case, is very promising and makes more complex structures of common use in real systems worth of further investigations.

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