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Abstract: The use of simulation and macromodels to assess the performance of a typical interconnecting system is addressed. A receiver macromodel including threshold decision of received signals is proposed, and an efficiency analysis demontrates that the use of well-designed macromodels for all parts of the transmission chain dramatically speeds up the simulation. Also, a careful discussion of simulated eye diagrams shows that macromodels guarantee timing accuracy even in very long bit sequences.

1 Introduction

Data transmission in modern ICT devices requires higher and higher bit rates, and the analog nature of transmitting digital data on interconnects becomes increasingly important. This trend involves interconnects and links at any scale, from chip to system level, and reproduces also at smaller scales the transmission problems that are typical of traditional data link. Thus, the designers need to worry more and more of the analog signals reaching the receiver input and the corresponding eye diagrams, from which information on the data link reliability and bit error rate can be extrapolated.

In the design phase, the prediction of received signals and the generation of eye diagrams is currently done by means of analog simulation. In order to highlight those critical effects like jitter, intersymbol interference, crosstalk, etc., simulations must be able to handle very long bit streams on transmission structures that are realistically modeled. This requirement inevitably calls for a simulation power that might exceed the capacity of available computers. Efficient models are therefore imperative, and a combination of driver and receiver macromodels with a clever solution method of long interconnects, and a reduced-order representation of connectors and junctions has been demonstrated to potentially enable the simulation of data link operation during the transmission of long bit sequences [1]. Of course, questions may arise about the accuracy of data link performances assessed by using device macromodels, that are approximations of reality. In particular, the accumulation of errors during the simulation of a very long bit-stream transmission might raise concerns about the validity of simulation results.

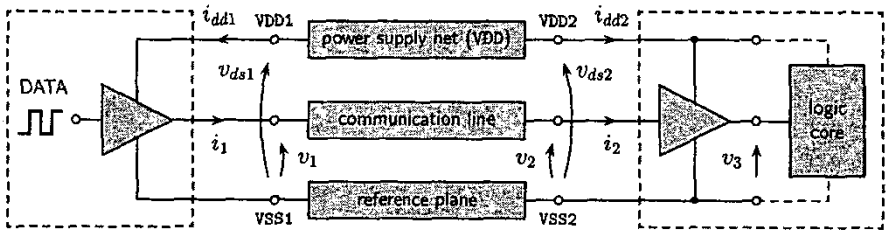

Figure 1: Structure of a generic high-speed data communication link with the relevant blocks and electrical and logical variables of interest.

The aim of this paper is to discuss the impact of device macromodels on the accuracy of signal integrity and performance predictions for critical data link of ICT devices. Figure 1 shows the structure of a typical data link, that is composed of a driver (left side) and a receiver (right side) communicating via an interconnect, and energized by a common power supply network. For this structure, the performance assessment requires the simulation of $v_2(t)$ (for checking timing and distortion effects), as well as of the eye diagram at the receiver level, essential for the prediction of the bit error rate of the link.

The scheme of Fig 1 defines also $v_3(t)$, that is the analog output of the first receiver stage, where $v_2(t)$ is compared with a threshold value. This signal v_3 is presently not considered by the designers, since it is not readily accessible, if one-port models of the receivers are used. However, it has two great advantages, *i.e.*, it includes the threshold detection carried out by the receiver, and it carries additional information on the effects of the power supply noise and of electromagnetic interferences as they reach the logic core of the receivers. Later in this paper, we discuss the value

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of including v_3 in the receiver model and using it for the performance estimation of an entire data link.

2 Device macromodels

This Section shortly reviews the basic macromodels of CMOS drivers and receivers. For drivers, we use the state-of-the-art Mπ*log* approach [2], briefly outlined below. For receivers, we propose an extension of conventional one-port models, as elaborated in Sect. 2.2.

2.1 Drivers

Macromodeling of single-ended CMOS drivers is a well-established process, providing a mathematical relationship between the analog port voltage and current variables (v_1 ands i_1 in Fig. 1), controlled by the DATA stream of Fig. 1.

Since the input signal, even if accessible from measurements or simulation, can be hardly included directly in the macromodel definition, the best way to create a driver macromodel is by means of a two-piece model representation, where the input signal acts as a logic input forcing the state transition only, and the output buffer behavior turns out to be almost uncorrelated to the small amplitude variations of such an input signal. As an example, for the driver of Fig. 1 this writes

$$i_1(t) = w_H(t) i_H(v_1, d/dt) + w_L(t) i_L(v_1, d/dt) \tag{1}$$

where i_H and i_L are dynamic submodels accounting for the port behavior at fixed logic High or Low state, respectively, and w_H and w_L are weighting coefficients playing the role of the input signal and accounting for logic state transitions.

A detailed discussion of possible representations of (1) can be found in [3], and a model extension, that includes the variation of power supply terminals `VDD1` and `VSS1` as well the inclusion of temperature parameter and the tri-state operation is discussed in [2].

2.2 Receivers

The conventional model representation for the receiver input port is obtained as a sum of a static and a dynamic part, as follows

$$i_2(t) = f_s(v_2, v_{ds2}) + f_d(v_2, v_{ds2}, d/dt) \tag{2}$$

where submodel f_s is the 2-dimensional static characteristic of the input port of the receiver and submodel f_d is a general nonlinear dynamic model. A similar representation holds for current i_{dd2}. In this work, the static surface f_s is approximated via a linear interpolation of the static characteristics (i_2, v_2) computed for two different values of the power supply, and the dynamic submodel f_d is a linear parametric model as described in [4]. It is worth mentioning that a simple linear dynamic model for f_d can hardly reproduce the dynamic behavior of the receiver when the effects of the power and ground clamps are dominant. However, the accuracy of the macromodel can be improved by using finer approximations for the static submodel f_s and nonlinear parametric models for f_d, as already proposed for drivers [2].

In order to model the transmission between the receiver input and output ports, the analog output feeding the logic core v_3 is represented as a controlled voltage source, since the logic core behaves as a fixed load for the receiver output port:

$$v_3(t) = \hat{v}_3(t)\left(\frac{v_{ds2}(t)}{V_{\mathrm{DD}}}\right) \tag{3}$$

where $\hat{v}_3$ accounts for the ideal transmission behavior, and is obtained by juxtaposing in time the basic up and down state transitions of voltage v_3, consequent to up (or down) state transitions of the receiver input voltage v_2. The state transitions of $v_3(t)$ are triggered when v_2 crosses a suitable threshold value (or more than one for a receiver with hysteresis) and the shape of the $v_3(t)$ edges is indipendent of the shape of $v_2(t)$. Finally, the elementary transitions composed into $\hat{v}_3$ are recorded while the power supply terminals `VDD2` and `VSS2` are set to their nominal values, and the effect of the power supply voltage variation is included in the model by a linear correction $v_{ds2}(t)/V_{\mathrm{DD}}$, since we assume that $v_3(t)$ is roughly proportional to the power supply voltage $v_{ds2}(t)$.

3 Discussion of test cases

In order to study the influence of device macromodels on data links performance assessment, we simulate the operation of the typical data link shown in Fig. 1 by using different combinations of driver and receiver models. The interconnect between driver and receiver is an 8 cm-long MCM land, that is modeled as a lossy dispersive transmission line. The power supply network is considered either ideal or modeled by a lumped equivalent (see below), and no transitions or junctions are included in the transmission path, for the sake of simplicity. A high-speed IBM CMOS transceiver ($V_{\mathrm{DD}} = 1.8$ V) is used in place of the driver and of the receiver. A transistor-level model of this device is

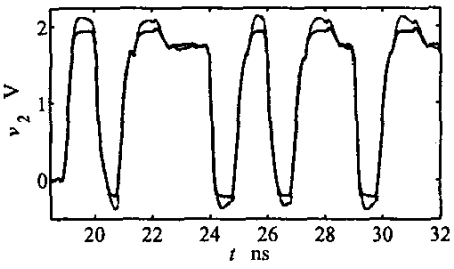

Figure 2: Voltage waveform $v_2(t)$ for the test case #1. Solid thin line: reference; dashed thick line: approximate **MR** set; solid thick line: approximate **MM** set.

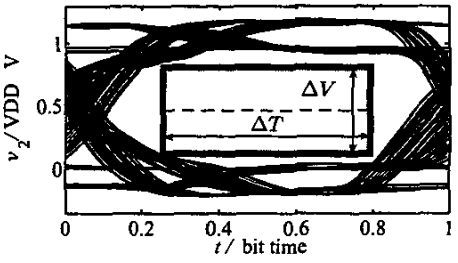

Figure 3: Eye diagram arising from the reference waveform $v_2(t)$ of test case #1 and the definition of the eye opening parameters ΔV and ΔT.

used as a reference, and specialized macromodels for the driver and the receiver are derived from the responses of such a transistor-level model, and are implemented as SPICE-like subcircuits. The structure of the receiver macromodel is the one proposed in Sec. 2.2 with a linear dynamic part. Additional details of the transceiver utilized in this study and on the generation of its macromodels can be found in [2, 4]. The data pattern used for this study is a 256 bit-long sequence with 1 ns bit time and jitter error uniformly distributed in the range $[-50, 50]$ ps. All simulations are carried out by means of PowerSPICE and two test cases are considered, including or not noise effects on the power supply network.

The following simulation strategy has been adopted: a set of reference waveforms is computed by using transistor level models for both the driver and the receiver devices; then, two sets of approximate waveforms are generated by using: (1) a macromodel for the driver and the reference transistor level model for the receiver (hereafter, labelled with **MR**); (2) macromodels for both devices (labelled with **MM**). The goal is to provide comparisons between the reference and approximate waveforms, and their corresponding eye diagrams, to estimate the impact of possible errors introduced by macromodels.

Test case 1. The first case is defined by the data link described above with a power supply network modeled by a V_{DD} battery and a perfectly conducting reference plane, in order to exclude all possible power supply disturbances.

Table 1: Efficiency comparison (PowerSPICE simulation of a 256 bit pattern on the structure of Fig. 1)

Device models	CPU time
reference transistor-level	143 min
macromodels (**MM** set)	4.3 min

Figure 2 shows the reference and approximate waveforms of the voltage $v_2(t)$, for a duration of 14 ns, picked at random along the simulation of the entire bit pattern. A very good correlation among the different curves, especially during the transitions, indicates that the simplified macromodels are capable of providing accurate timing information. In fact, the timing error on $v_2(t)$, computed as the maximum delay between the reference and the approximate waveforms at 0.9 V level, turns out to be always less than 2% of the bit time over the entire bit sequence for both set of approximate waveforms. The sole deviation of the **MM** curve from the reference is in the overshoots and undershoots regions, where the v_2 shape is mainly decided by the receiver clamps, and the corresponding macromodels implementing a simple linear dynamic part demonstrate (as expected) their inadequacy in clamp regions.

Figure 3 shows the eye diagram derived from the reference waveform of $v_2(t)$. As one can anticipate from the analysis of Fig. 2, the waveforms obtained by the simulations of macromodels are not adding significant information, as all diagrams look very similar. However, the receiver analog output $v_3(t)$ is expected to be more informative, since it already includes the effects of the threshold detection carried out by the receiver on the $v_2(t)$ waveform. In order to estimate the differences between the eye diagrams of $v_3(t)$ arising from reference and approximate waveforms, we compute the eye apertures ΔT and ΔV defined in Fig. 3 and plot ΔT vs. ΔV in Fig. 4. In this plot, for every value of ΔV, the difference of the corresponding ΔT's quantifies the error in the eye opening caused by the use of approximate waveforms, and Fig. 4 shows that the openings of eye diagrams obtained from simulations with macromodels are within 2% of openings from reference simulations.

Test case 2. In this second case, both the power supply network and the reference plane are modeled by realistic lumped equivalent circuits, in order to account for the switching noise.

Figure 5 shows the reference and approximate waveforms for $v_2(t)$ and $v_{ds2}(t)$. As for the first test case, the accuracy of the approximate models is confirmed, and the timing error on v_2 turns out to be less than 3% of the bit time

over the entire bit sequence for both the **MR** and **MM** waveforms.

Figure 6 shows the reference and approximate $v_3(t)$ signals, the latter obtained by inputting to equation (3) two different $v_2(t)$ waveforms, that is, the reference one and the result of the **MM** simulation. From Fig. 6, the accuracy of the receiver macromodel in reproducing the power supply fluctuations on v_3 can be clearly appreciated. Figure 7 shows the reference and approximate ΔT vs. ΔV curves, computed from the eye diagrams of $v_3(t)$ (not shown), thus confirming, for a realistic test case, errors less than 4% in the eye opening diagrams caused by the use of macromodels.

Finally, Table 1 shows a comparison of the CPU time required by the PowerSPICE simulation of the reference 256 bit-long transmission of test case #2 and the corresponding time of the simulation using macromodels; the speed-up factor is on the order of 33.

From the previous analysis, we can conclude that the small eye opening errors evidenced by Fig.s 4 and 7 are a clear demonstration that timing errors unavoidably introduced by macromodels do not accumulate in very long bit sequences. This first conclusion, coupled with the superior computational efficiency of macromodels, leads us to remark that the macromodel simulation can be exploited for the reliable and accurate prediction of eye openings and data link performance.

Acknowledgements

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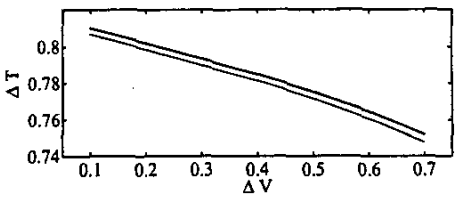

Figure 4: Eye opening parameter values (defined in Fig. 3) for the eye diagrams of waveforms v_3 computed in test case #1. Solid thin line: reference; solid thick line: approximate **MM** set.

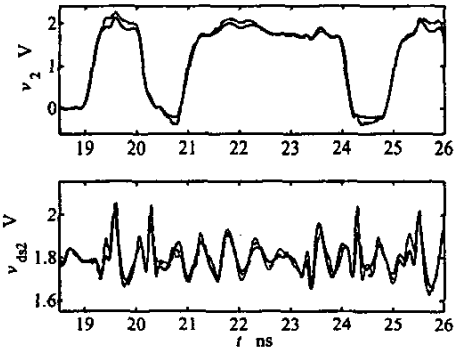

Figure 5: Voltage waveforms $v_2(t)$ and $v_{ds2}(t)$ for the test case #2. Solid thin line: reference; dashed thick line: approximate **MR** set; solid thick line: approximate **MM** set.

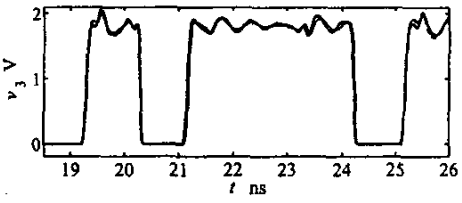

Figure 6: Voltage waveforms $v_3(t)$ at the output of the receiver for the test case 2. Solid thin line: reference; dashed thick line: prediction from v_2 of set **MR**; solid thick line: prediction from v_2 of set **MM**.

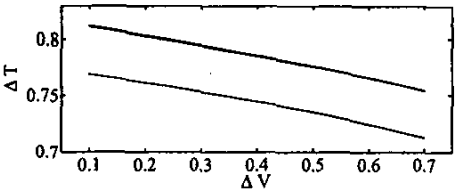

Figure 7: Eye opening parameter values (defined in Fig. 3) for the eye diagrams of waveforms v_3 computed in test case #2. Solid thin line: reference; solid thick line: approximate **MM** set.

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