UWB Receiver Design and Two-Way-Ranging Simulation using VHDL-AMS

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***Abstract*— Ultra-Wide Band (UWB) impulse radio systems are appealing in location aware applications because of the high resolution of the measurement of pulses Time-Of-Flight (TOF). This paper describes a complete UWB receiver for indoor localization based on the non-coherent Energy Detection approach, and the simulation of a Two-Way-Ranging (TWR) Time-Of-Arrival (TOA) scheme between two transceivers. This is done with the aid of the design flow provided by the ADVanceMS simulator and the VHDL-AMS modeling language. The tool is suitable for every application aimed at the integration of mixed-signal Systems on Chips (SoC) allowing successive refinement steps starting from the VHDL-AMS models of the analog front-end and going down to their equivalent Spice/Spice-RF models. The complete VHDL/VHDL-AMS receiver model is described and, in order to validate the simulation tool, preliminary results obtained with the Alt. PHY UWB 802.15.3 indoor channel model are presented.**

I. Introduction

The UWB impulse radio is an interesting solution for short-range low-data rate mobile communications [1]. It allows localization capabilities thanks to its extremely short pulse duration (on the order of one nanosecond) and seems to promise significant savings in terms of power consumption. Nowadays the UWB transmission for commercial use is allowed by the Federal Communication Commission (FCC) in a 7 GHz band of unlicensed spectrum and, both in indoor and outdoor environments, the peak transmission power is bounded to lower levels with respect to other narrowband systems.

The UWB state-of-the-art receivers can be classified as coherent and non-coherent. The formers base the communication on the correlation of the incoming waveform to an internally generated template ideally matched to the channel response; typical solutions employ complex Rake receivers and high-speed ADC which are not compatible to low power requirements. On the other hand, non-coherent receivers have low complexity and low-power consumption at the cost of reduced performances. The ADC sampling rate is thousands of times lower than in coherent receivers, being matched to the pulse repetition rate rather than the Nyquist frequency, with the advantage of limited power consumption. These advantages are to be weighted with drawbacks like a worse BER performance ($\simeq$ 3dB) and a lower immunity to interference compared to coherent receivers. Among the non-coherent approaches, the Energy Detection is particularly suited to the hardware-implementation in a single mixed-signal IC. A few works document the use of this approach both in low cost UWB sensor TAG systems [7] and in frequency domain UWB receivers with pulse sense capabilities and multitiming recovery [5].

Although a few UWB TAG transceivers CMOS implementations are available in literature (as referred in [3]), at the simulation level the ranging capability has not been tested yet. This paper deals with a low-cost Energy Detection UWB receiver architecture for indoor localization. Even though the architecture has not been validated by silicon implementations, the localization capability is checked through a Two-Way-Ranging (TWR) simulation using parametric VHDL/VHDL-AMS models. In section II we report a brief introduction on the design entry point and the design flow used. Section III deals with a brief description of each receiver function. In section IV the Time-Of-Flight (TOF) simulation results and an example of functional simulation are presented. Conclusions are drawn in section V.

II. Entry point: The Energy Detection concept and VHDL-AMS as a flexible design procedure

The modulation scheme proposed for the Energy Detection receiver is the Binary Pulse Position Modulation (2-PPM): The received signal is expressed by

$$r(t) = \sum_{j=-\infty}^{+\infty} s\left(t - jT_s - \alpha_j T_s/2 - \tau\right) + n(t) \qquad (1)$$

where $s(t)$ is the channel response to an isolated UWB pulse emitted from the transmitter, T_s is the symbol time, α_j is the transmitted bit, τ is the timing difference between transmitter and receiver clocks and $n(t)$ is AWGN with two sided noise spectral density $N_0/2$. In each symbol period, jT_s, the modulation is given by translating the time reference of the pulse of a quantity $T_s/2$ for the case $\alpha_j = 1$ and 0 for $\alpha_j = 0$. The decision rule consists of comparing the energies of the first and second halves of the received pulse (equations 2 and 3): The received bit is "zero" if $z_k^{(0)} > z_k^{(1)}$, "one" otherwise. The integration window Δ is on the order of the channel spread.

$$z_k^{(0)} = \int_{kT_s+\tau}^{kT_s+\tau+\Delta} r^2(t)dt \qquad (2)$$

$$z_k^{(1)} = \int_{(k+1/2)T_s+\tau}^{(k+1/2)T_s+\tau+\Delta} r^2(t)dt \qquad (3)$$

The limited complexity of this Energy Detection scheme is such that only few blocks are necessary for performing

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each function required for receiving the signal, acquiring the synchronization and demodulating it.

In mixed-signal systems both the analog, RF and digital parts are typically designed and analyzed separately through the use of different simulators. The new extension of VHDL modeling language (VHDL-AMS) and the ADVanceMS^{TM} simulation tool [8] allow the modeling and the co-simulation of the entire receiver with significant advantages in terms of flexibility. The tool supports VHDL, VHDL-AMS, Spice languages (Eldo, Eldo-RF) and provides a multi-resolution capability with the advantage of making evident the trade-off between accuracy and CPU time. The possibility of having both very accurate (e.g. transistor level) and differential equations based models (e.g. behavioural VHDL-AMS) is interesting, especially in top-down flows where successive refinement steps are mandatory for giving the building blocks the necessary details without losing the whole-system view. A few works document the use of VHDL-AMS for efficiently design complex telecommunication systems using a top-down methodology (see [3] and references therein).

Our claim is supported by the coherence between standard simulators, like Matlab and ADMS, obtained after exaustive simulations. Figure 1 reports the results of Bit-Error-Rate (BER) varying the E_b/N_0 at the receiver input. In this case, the tool coherence for the highest level simulation is proved using a Matlab model of the receiver. This simulation is done using the 802.15.3a UWB channel model adding AWGN and supposing the timing perfectly acquired (as in equation 1). The Matlab code has been translated into a VHDL-AMS description, employing a simple model of the receiver blocks. The simulation of the VHDL-AMS receiver has been then conducted in two different ways, in the following referred to as "VHDL-AMS 1" and "VHDL-AMS 2" (performed in a "continuous time differential equation" fashion, and in a "sampled discrete time" integration, respectively). The results show the complete matching between the three curves although the simulation time was very different (870 SNR point per hour for VHDL-AMS 1, 9200 for VHDL-2 and 14100 for Matlab). The conclusions are that the countinuous time model is unsuited for fast performance evaluation while the discrete time model CPU time is comparable, though higher, to Matlab. Thus, VHDL-AMS2 can be a valid substitute to Matlab with the advantage of using a single simulation environment. VHDL-AMS1 "continuous time" simulation, is unsuited for system level analyses but can be used for detailed design.

III. Receiver architecture

The receiver architecture is shown in figure 2. In order to limit the power consumption, the receiver is designed implementing as many blocks as possible in digital, thus limiting the front-end complexity. The main analogue and RF blocks are developed using a parametric VHDL-AMS model with a significant number of non-idealities (transfer function, offset, saturation, non-linearities,...) while the other parts which compose the digital backend are developed in VHDL. The received signal is amplified by the Low-Noise-Amplifier

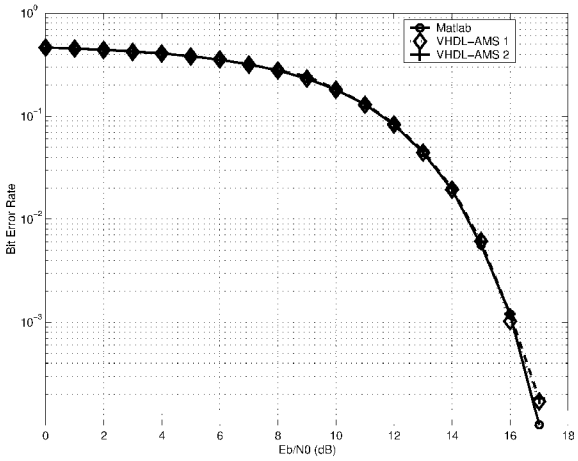

Fig. 1. BER curves: Matlab vs. VHDL-AMS 1 and VHDL-AMS 2.

(LNA) and the Variable-Gain-amplifier (VGA), squared and then integrated by the Integrate-and-Dump block (I & D). With respect to [7], in which eight Analog-To-Digital Converters (ADC) are used (each one with a resolution of 4 bits), the receiver employs only one I & D block and one 5 bits ADC for digital energy conversion and digital data elaboration.

The digital PHY architecture contains a demodulation block, some arithmetic units for pulse energy elaboration, a correlator, a counter and other logic for formatting the demodulated bit-stream for MAC processing; no forward error correction coding techniques are considered. The simple 2-PPM demodulator contains only a comparator and, thanks to the simplicity of the algorithms implemented in the receiver, the pulse energy elaboration is obtained with adders, comparators and maximum extractors only. The Start-Of-Frame-Delimiter (SFD) detection is performed by the correlation block which searches for the maximum correlation with the expected SFD. The overall system operation is coordinated by a digital controller (DC/PMU) which includes a power management unit that shuts down the unused receiver blocks during the operation phases.

The receiver runs through several phases while receiving a packet (for the packet structure, we refer the reader to [2], revisited by the TG4a in the context of WPAN applications [1]): After the *Noise Estimation* phase in which noise energy is estimated, the *Clear Channel Assessment* (CCA) detects whether the wireless medium is busy, sampling the channel energy for the entire symbol duration and for a certain number of times. The presence of the preamble sequence is checked by comparing the noise energy with the energy sensed through the CCA phase counting if it exceedes the noise level a sufficient number of times. A *Gain Adjustment* (AGC) phase is fundamental to adapt the maximum signal energy in the ADC input range; this is achieved by a Look-Up Table (LUT) whose entry is the difference between the energy captured during the CCA and the NE phase; output data is the digital gain converted by a DA Converter. The mixed signal AGC block contains both the LUT and the DAC. The

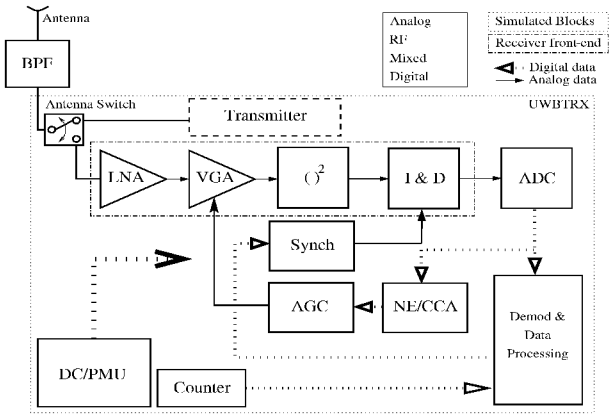

Fig. 2. Receiver structure.

phase which aims at recovering the timing reference of the non-modulated preamble sequence to a sufficient accuracy for the following demodulation is called *Coarse Synchronization*. As referred in [3], it consists of a linear search in time of the maximum energy position in the preamble sequence. Basically, the symbol period T_s is divided in time slices and the N_c-th slice is selected. Once coarse timing is acquired, the receiver seeks for the preamble delimiter called SFD and then starts demodulating data contained in the payload. At the same time, *Fine Synchronization* which guarantees the accuracy necessary for localization is performed; it consists of a finer linear search around the coarse lock point. The difference with respect to the coarse acquisition presented in [3] resides in the integration of both 2-PPM positions and in data insensitivity as a consequence. The output of the fine synchronization is index N_f which varies in $[-N_{Tf}/2, N_{Tf}/2]$ around the previous lock point, as shown in figure 3. As a result, the overall synchronization time within a symbol period is given by

$$t_c = N_c T_{cs} + (N_f - N_{Tf}/2)T_{fs} \quad (4)$$

where T_{cs} and T_{fs} are the coarse and fine synchronization steps, respectively. The two synchronizers are depicted as a single unit (*Synch*) in the architecture of figure 2.

The TWR simulation between two UWB TAG transceivers requires also a behavioural parametric model of the transmitter and a Path-Loss (PL) model; in this case an $1/r^2$ PL model is chosen and an ideal parametric transmitter description is developed. The TWR-TOA data exchange between two TAG UWB systems (**A** and **B**) whose mutual distance is d works as follows (refer to figure 3 and equations 4 and 5):

- **Start** - Transceiver **A** sends the request packet to Transceiver **B** and starts running its internal counter.
- **Phase 1** - Transceiver **B** receives the packet and performs coarse and fine synchronization (that is calculates the coarse synchronization index $N_c|B$ and the fine synchronization index $N_f|B$).
- **Phase 2** - Transceiver **B** sends the acknowledge packet whose payload contains $N_c|B$ and $N_f|B$.
- **End** - Transceiver **A** receives the acknowledge, performs coarse and fine synchronization (that is calculates $N_c|A$ and $N_f|A$), extracts data from payload, determines the synchronization times $t_c|A$ and $t_c|B$ according to (4) and stops the counter whose output is N symbols. It then calculates the Time-Of-Flight [6]:

$$T_{of} = \frac{(N - N_{offset})T_s - (T_s - t_c|A - t_c|B)}{2} \quad (5)$$

N_{offset} is the clock cycles count for a complete packet exchange if TOF were 0. The distance estimation is given

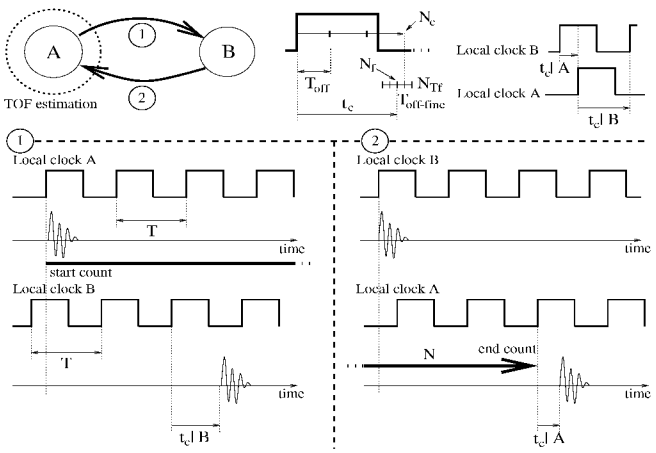

Fig. 3. Two-Way-Ranging scheme.

by $d \simeq cT_{of}$ where c is the speed of light.

IV. Functional Simulations

The core of the receiver is the synchronizer, which as described before is able to recover the timing for demodulation and ranging. An example of the simulation results of the coarse synchronizer is reported in figure 4. The quantity *Noisy input* is first squared (quantity *Input square*) and then integrated delaying the integration window of a fixed quantity at each step (signal *Increasing delay*). The quantity *Integration* shows the captured energies while shifting the integration window in time. The system determines the maximum energy and the clock for demodulation is generated (*Locked clock*) while the *Lock* signal is asserted. The decision on synchronization is taken in digital domain using the ADC output as depicted in figure (signal *ADC output*). In these conditions the integration window is 30 ns and the synchronization step is 10 ns.

The TWR ranging results for a single packet exchange are reported in figure 5. Here, the simulation includes the operation of all parts of the receiver and the ADMS simulator has been set to a 500 ps fixed integration step to improve simulation speed and accuracy. Indeed, both for greater integration steps and for the default adaptative integration methods, simulation results are quite different. The simulation is performed once for each distance reported in figure by simply changing a parameter in the description. A Line of Sight (LOS) 802.15.3a channel model is used and the Signal-to-Noise Ratio is fixed for a given distance, bounding the minimum E_b/N_0 at 16 dB, which according to figure 1 guarantees a BER of 10^{-3}, at a distance of 28 m; the symbol timing is 200 ns. The link

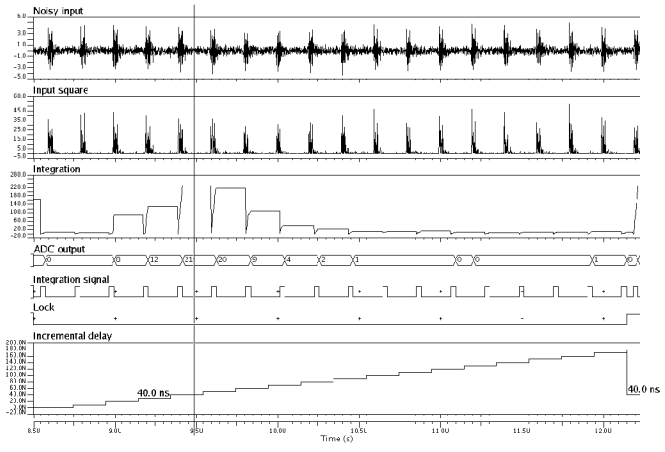

Fig. 4. Operation of the Coarse Synchronization

margin accounts for both thermal noise and noise figure of the analog front-end of the receiver. To allow a ranging accuracy of ideally 2 ns, the steps of coarse synchronization and fine synchronization have been set to 10 ns and 1 ns respectively, while the integration window duration is approximately as long as the channel spread, that is 30 ns. Even though results seem to be good at short distances, the simulations show low accuracy on TOF estimation for distances greater than 14 meters caused by the adopted ranging algorithm. The average distance measurement corresponds to the expected one but the maximum error varies: For distances greater than 15 m and shorter than 3 m the maximum error is greater than 1 m, while at short distances (3-10 m) is about 60 cm.

The Gain Adjustment is fundamental because the correct operation of the coarse and fine synchronizers is strongly influenced by ADC saturation and finite resolution. For short distances the AGC is incapable of setting the gain because the ADC is already saturated during the CCA phase. As a consequence, the AGC cannot set a smaller gain than the output data of the LUT which corresponds to the maximum entry. This causes the impossibility of identifying the different energy levels for each integration window position. On the other hand, the low sensivity at high distances leads to a loss in the precision of the TOF measurement. The integration window influences the distance measurement as well: The more it is different from the channel spread, the lower the performance is.

In order to increase the ranging accuracy a different preamble with a specific structure for the ranging operation is mandatory, as envisioned by the TG4a [1]. One of the properties of such preamble is its length, larger than the one used here, which allows performing both coarse and fine synchronization during its reception. Furthermore, the gain control phase has to be enhanced to avoid saturation at short distances.

At this stage of the work, the non-ideal effects of the blocks are not accounted for, or, if so, they are coarsely modeled. The future works will deal with the accurate modeling of each part of the analog front-end, going down to the transistor level, the refinement in the description of the parameters and the use of the TG4a channel model.

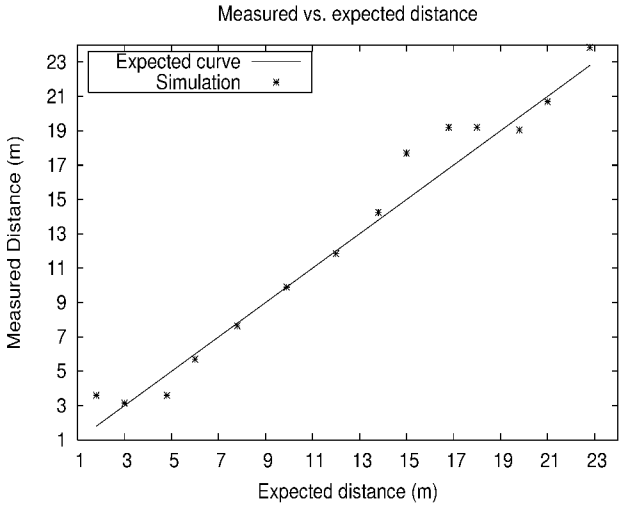

Fig. 5. Single TWR packet exchange simulation results

V. Conclusion

We have shown in this paper that a complete UWB receiver development and simulation is possible thanks to the innovative design flow provided by ADVanceMS and VHDL-AMS modeling language. The results obtained through the behavioural simulation of a TWR scheme are interesting for the detailed study of the device. They show that the system is not capable of localization accuracies < 1 m at long distances, but on the other hand its low complexity is promising in terms of low power performance. The future works will deal with the detailed modeling of each part of the analog front-end going down to transistor level, the refinement in the description parameters for realism enhancement and the use of the TG4a draft and channel model specifications. This will give the necessary simulation details for justifying the feasibility for a full custom CMOS-IC.

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