A Unique March Test Algorithm for the Wide Spread of Realistic Memory Faults in SRAMs

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A. Benso, A. Bosio, S. Di Carlo, G. Di Natale, P. Prinetto
Politecnico di Torino
Dipartimento di Automatica e Informatica
Torino, Italy
E-mail {benso, bosio, dicarlo, dinatale, prinetto}@polito.it
http://www.testgroup.polito.it

***Abstract*-Among the different types of algorithms proposed to test Static Random Access Memories (SRAMs), March Tests have proven to be faster, simpler and regularly structured. A large number of March Tests with different fault coverage have been published. Usually different march tests detect only a specific set of memory faults.**

The always growing memory production technology introduces new classes of fault, making a key hurdle the generation of new march tests. The aim of this paper is to target the whole set of realistic fault model and to provide a unique march test able to reduce the test complexity of 15.4% than state-of-the-art march algorithm.

1. INTRODUCTION

Memories are one of the most important components in digital systems, and semiconductor memories are nowadays one of the fastest growing technologies. *System-On-a-Chip* (SOC) technologies allow to embed in a single chip all the components and functions that historically were placed on a hardware board. Within SOCs, embedded memories are the densest components, accounting for up to 90% of chips area [1]. It is thus common finding, on a single chip, tens of memories of different types, sizes, access protocols and timing. Moreover they can recursively be embedded in embedded cores.

In the latest decade published researches mainly focused on the definition of new fault models [2] [3] [4]. The high number of fault models can be reduced considering so called *Realistic Faults* only. Those faults have been proved to be realistic by performing fault injection and circuit simulation experiments [4][8][9].

The realistic fault models can be clustered in three main fault sets: (i) static un-linked (ii) dynamic un-linked and (iii) static linked faults. [8].

Up to now, researchers mainly focused on the minimization of existing memory tests for a single target fault set [5] [6] [7]. In case of complex fault lists, the typical test strategy is to apply several march tests customized for the different fault sets. As an example to detect both static un-linked and static linked faults a typical approach is to apply a march test for static un-linked faults followed by a test algorithm for static linked fault. The main lack of this solution is the time effort. It is the sum of the complexity of the two march tests. Moreover, since some fault models are usually detected by both the algorithms the resulting strategy is redundant.

The aim of this work is to propose a unique non redundant march test able to detect the whole set of realistic fault models (static un-linked, dynamic un-linked and, static linked faults). The proposed solution reduces the test effort of about 15.4% w.r.t state of the art algorithms by applying just a single march test having a complexity of 22n.

The paper is structured as follows: Section 2 introduces the fault taxonomy; Section 3 and Section 4 introduce the proposed solution. Section 5 summarizes the main contributions and outlines future research activities.

2. FAULT MODEL TAXONOMY

For test purposes, faults in memories are usually modeled as Functional Faults. A *Functional Fault Model* (FFM) is a deviation of the memory behavior from the expected one under a set of performed operations.

Each FFM can be described by a set of Fault Primitives (FPs) [9].

In this paper we focus on the following sets of realistic fault models:

- **Static un-linked faults** (TABLE **1** and **TABLE 4**)
- **Dynamic un-linked faults** : (**TABLE 2** and **TABLE 5**)
- **Static linked faults**: described in **TABLE 3** and TABLE 6. They are composed by a combination of static un-linked faults as described in definition 1.

Definition 1 : two FPs, FP1 = <S1/F1/R1> and FP2 = <S2/F2/R2>, are said to be *Linked,* and denoted by

"FP1 → FP2", if both of the following conditions are satisfied:

- FP2 masks FP1, i.e., F2 = not (F1);
- Read operations of FP1 and FP2 don't detect a fault.
- The Sensitizing operation (S_2) of FP2 of is applied after S1, on either the *a*-cell or *v*-cell of FP1.

TABLE 1 Single Cell Static Un-linked Faults

FFM	***FPs***
SF	<x / y>
WDF	<yw_y / x / ->
TF	<xw_x / x / ->
RDF	<xr_x / y / y>
DRDF	<yr_y / x / y>
IRF	<yr_y / x / y>

TABLE 2 Single Cell Dynamic Un-linked Faults

FFM	***FPs***
dRDF	<z$w_x r_x$ / y / y>
dDRDF	<z$w_x r_x$ / y / x>
dIRF	<z$w_x r_x$ / x / y>

TABLE 3 Single Cell Static Linked Faults

Linked Fault	***FPs***	***FP1***
FP1→WDF	FP1 → <xw_x / y / ->	TF, WDF, DRDF
FP1→ RDF	FP1 → <xr_x / y / y>	TF, WDF, DRDF

TABLE 4 Two Cell Static Un-linked Faults, z, k, x, y ∈ {0,1}, x = not(y), z = not(k)

FFM	***FPs***
CFst	<z ; x / y /->
CFds	<zr_z ; x / y / ->, <zw_z ; x / y / ->, <zw_k ; x / y / ->
CFtr	<z ; xw_y / x / ->
CFwd	<z ; xw_x / y / ->
CFrd	<z ; xr_x / y / y>
CFdr	<z ; xr_x / y / x>
CFir	<z ; xr_x / x / y>

TABLE 5 Two Cell Dynamic Un-linked Faults, , z, k, x, y ∈ {0,1}, x = not(y), z = not(k)

FFM	***FPs***
dCFds	<z$w_k r_k$; x / y / ->
dCFrd	<z ; k$w_x r_x$ / y / y>
dCFdrd	<z ; k$w_x r_x$ / y / x>
dCFir	<z ; k$w_x r_x$ / x / y>

TABLE 6 Two Cell Static Linked Faults

Type	***Linked Fault***	***FP1***
LF2aa	FP1 →CFds	CFds, CFtr, CFwd, CFdr
	FP1→CFwd	CFds, CFtr, CFwd, CFdr
	FP1→CFrd	CFds, CFtr, CFwd, CFdr
LF2av	FP1→WDF	CFds, CFtr, CFwd, CFdr
	FP1→RDF	CFds, CFtr, CFwd, CFdr
LF2va	FP1 →CFds	WDF, TF, DRDF
	FP1→CFwd	WDF, TF, DRDF
	FP1→CFrd	WDF, TF, DRDF

3. FAULT DETECTION

Single cell faults can be detected by two Fault Coverage Conditions:

- **FCC1** = $\Updownarrow(r_y,w_x,r_x,w_x,r_x)\ \Updownarrow(r_x\ldots)$
- **FCC2** = $\Updownarrow(r_x,w_y,r_y,w_y,r_y)\ \Updownarrow(r_y\ldots)$

Two cell faults can be detected by the following FCC:

- **FCC3** : $\Downarrow(r_x,w_y,r_y,w_y,r_y)\Downarrow(r_y,w_x,r_x,w_x,r_x)$ $\Uparrow(r_x,w_y,r_y,w_y,r_y)\Uparrow(r_y,w_x,r_x,w_x,r_x)\ \Updownarrow(r_{x,\ldots})$

4. MARCH SOLUTION

March AB [10] shown in **Fig. 1**, contains all the FCCs required to cover the full set of realistic memory faults.

$\{\Updownarrow(w_0)\ \Downarrow(r_0,w_1,r_1,w_1,r_1)\ \Downarrow(r_1,w_0,r_0,w_0,r_0)\ \Uparrow(r_0,w_1,r_1,w_1,r_1)$
M0 *M1* *M2* *M3*
$\Uparrow(r_1,w_0,r_0,w_0,r_0)\ \Updownarrow(r_0)\}$
M4 *M5*

Fig. 1 : March AB.

5. CONCLUSIONS

This paper proposed a new March Test targeting the entire set of realistic memory faults. Our test provides the same coverage of the state-of-the-art test algorithms but reducing test complexity of 15.4% and therefore the test time. It makes possible resort to a single march test able to detect the bigger set of realistic memory fault, therefore March AB becomes a natural candidate for memory BIST architectures, building our test solution very attractive for the industry.

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