Test engineering education in Europe: the EuNICE-Test project

Original

Availability:
This version is available at: 11583/1499946 since:

Publisher:
IEEE

Published
DOI: 10.1109/MSE.2003.1205266

Terms of use:
openAccess
This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

Publisher copyright

(Article begins on next page)
Test engineering education in Europe: the EuNICE-Test project


Published in the Proceedings of the IEEE International Conference on Microelectronic Systems Education (ICMSE), 1-2 Jun. 2003, Anaheim (CA), USA.

N.B. This is a copy of the ACCEPTED version of the manuscript. The final PUBLISHED manuscript is available on IEEE Xplore®:

URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=1205266

DOI: 10.1109/MSE.2003.1205266

© 2000 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.
Test Engineering Education in Europe: the EuNICE-Test Project

Y. Bertrand, M-L. Flottes
Centre de Ressources de Test du CNFM (CRTC), and Laboratoire d’Informatique, de Robotique et de Microélectronique de Montpellier (LIRMM), University of Montpellier, France

L. Balado, J. Figueras
Universitat Politècnica de Catalunya, Barcelona, Spain

A. Biasizzo, F. Novak
Jozef Stefan Institute, Ljubljana, Slovenia

S. Di Carlo, P. Prinetto
Politecnico di Torino, Torino, Italy

N. Pricopi, H-J. Wunderlich
Institute of Computer Science, Computer Architecture, Universität Stuttgart, Stuttgart, Germany

J-P. Van der Heyden
Agilent Technologies France

Abstract

The paper deals with a European experience of education in industrial test of ICs and SoCs using remote testing facilities. The project addresses the problem of the shortage in microelectronics engineers aware with the new challenge of testing mixed-signal SoCs for multimedia/telecom market. It aims at providing test training facilities at a European scale on both initial and continuing education contexts. This is done by allowing the academic and industrial partners of the consortium to train engineers using the common test resources center (CRTC) hosted by LIRMM (Laboratoire d’Informatique, de Robotique et de Microélectronique de Montpellier, France). CRTC test tools include up-to-date/high-tech testers that are fully representative of real industrial testers as used on production testfloors. At the end of the project, it is aimed at reaching a cruising speed of about 16 trainees per year per center. Each trainee will have attend at least one one-week training using the remote test facilities of CRTC.

1. EuNICE-Test Genesis

This European network for test education is mainly based on the French CRTC experience [1-3]. A mixed approach is chosen, that combines both distributed and centralized test resources. Indeed, considering the huge cost of high-tech IC testers, the idea is to develop a one and only one test center for all the European academic partners. To avoid any expensive traveling of students from their university to CRTC in Montpellier, the implementation has been thought to make the CRTC tester reachable by net from any remote center.

CRTC is mainly equipped with high performing ATEs such as Agilent 83000-F330t VLSI tester. In each of the European centers, a server with test software facilities is implemented to allow the local development of test programs (Figure 1).

![Network implementation for remote test](image)

Figure 1. Network implementation for remote test

At the very last moment of the physical test, trainees connect on CRTC tester through the net and execute the test of the Device-Under-Test (DUT). Such an original remote testing implementation permits to save money first by equipping only one test center with performing resources and second by avoiding expensive costs induced by trainees traveling and accommodations.
2. EuNICE-Test Activity

The training courses we propose is opened for pre- and post-doctoral students from universities or engineering schools [4]. These training courses contribute to address the shortage of skills in circuit testing for microelectronics industry. In particular, it is aimed to allow the trainee to acquire a solid knowledge in the strategic domain of mixed-signal and SOC testing.

The two main training courses we propose to initiate students and engineers to digital IC test are issued from those developed by Agilent for the 83000 tester. After completing level 1 training, each trainee will be able to make competent use of any digital ATE to test a device for its performance parameters and specifications, build up a test flow to automate the test execution and create a test program to be executed on the production test floor. After completing level 2 training, he will have gained the knowledge on test complex devices, convert simulation data and make optimum use of tester resources. Both training courses use a standard digital circuit as DUT (Device Under Test) to simply illustrate all the test functions. Each training is built up on lessons and related lab exercises. The network configuration of CRTC allows any trainee in any distant center to prepare lab exercises using the local resources. Also the correctness of both input, signal shapes and output strobe locations may be locally verified. Only the test execution itself necessitates a remote connection on the CRTC tester in Montpellier.

![Figure 2. EuNICE-Test Project activities](image)

3. Acknowledgements

The European Network for Test Education presented here is partly funded by European Community, through IST-2000-30163 Project: EuNICE-Test "European Network for Initial and Continuing Education in VLSI/SOC Testing using Remote ATE facilities" [5].

Authors wish to thank R. Lorival for his support and involvement in efficiently using Agilent testers.

4. References