DC-AC Conversion Strategy optimized for Battery or Fuel-Cell-Supplied AC Motor Drives

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A. Fratta (member), P. Guglielmi, G.M. Pellegrino and F. Villata (member)
Dept. of Electrical Engineering, Politecnico di Torino, C.so Duca degli Abruzzi, 24, 10129 Torino ITALY

Abstract - . **A novel DC-AC conversion strategy is presented, which is proposing outstanding performances in DC-supplied AC motor drives. Theoretical power system design analyses and wide experimental verifications suggested the adoption of regulated H-Bridge boost DC-DC converter stage improving overall cost and efficiency with respect to direct PWM VSI connection to variable voltage battery supply. In this work, the modulation and control strategies are investigated, suitable for the best exploitation of the power system capabilities. Through a controlled coordination between H-Bridge and VSI modulation patterns and control tasks, minimum PWM ripple contents and linear voltage transfer up to six-step operation are the targets. The resulting strategy, called Cross-over Voltage Modulation, is reported for the first time together with the requested 3-ΦPWM enhancement called Balanced Envelopes Modulation. CVM strategy is realized and experimental tests are reported showing very satisfactory results, achieving new automotive AC motor drive quality.**

I. Introduction

The DC/AC conversion structure depicted in Fig.1b is the result of accurate power system analysis, PSpice simulations and prototypes experimental verifications, providing results as successful as expected [1-4].

Whenever the DC-source voltage may span around the range 1÷2, as in the case of battery or fuel cell supplies [4, 5÷7, 9÷12], the proposed power system takes to a list of benefits, with reference to the simplest 3Φ-VSI connection to the DC-source (Fig.1a):

- power semiconductors size and overall cost reduction, with related conduction and switching loss improvement;
- capability of large reduction of PWM ripple content on the AC motor voltages and related additive losses;
- reduction of filter capacitor size requested for low-ripple current supply from the sensitive DC-source.

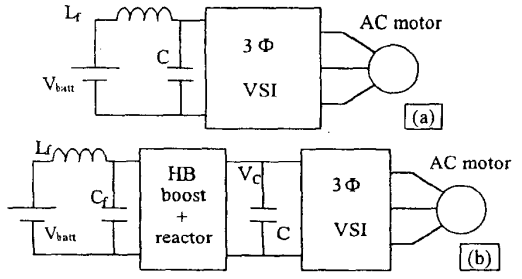

Figure 1: Converter's configuration: (a) Conventional; (b) Adopted

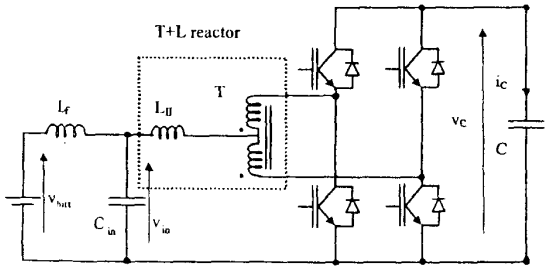

Figure 2: Adopted HBridge Boost Converter

The main drawback appears related to the need of the coupling power inductor. However, the peculiar H-Bridge structure in Fig.2, adopting a "T+L" reactor (inductive transformer), has proven compact and efficient, with the aid of suitable modulation technique (half modulation period displacement) and high performance current control loops. This allows also for large reduction on input-output current ripple and for increased DC-link voltage control loop bandwidth, strongly reducing DC capacitance size down to PCB soldered film capacitors.

Control complexity might be considered a drawback, nowadays avoided by available integration technologies.

In any case, the possible AC drive system performances are here investigated, in the power system shown in Fig.1b and adopting the DC-DC converter scheme in Fig.2.

Few basic targets are implied: PWM ripple content and related losses minimization by regulated DC-link voltage; linearity between reference and realized fundamental AC voltage from zero up to Six-Step mode, at the maximum allowable voltage for the chosen IGBTs (400V).

II. Balanced Envelopes Modulation (BEM)

A. Modulation target and concept.

The basic target of the BEM technique is to obtain the maximum possible linear PWM range in 3Φ-VSI by means of a real-time algorithm. This is achieved by real-time addition of a particular common-mode (null-sequence) quantity to the 3Φ-references (symmetrical components of the reference vector) to balance their positive and negative envelopes, implicitly maximizes the linear PWM range, that is the 3Φ-VSI voltage exploitation.

B. Analysis of BEM technique.

With reference to Fig.3, the symmetrical components of the reference voltage vector are defined by (1):

$$\vec{V}_N^* = \hat{V}\left[\cos(\vartheta) \quad \cos\left(\vartheta - \tfrac{2}{3}\pi\right) \quad \cos\left(\vartheta - \tfrac{4}{3}\pi\right)\right]^T \qquad (1)$$

The 3Φ-components envelope "E_{pos}" = $max(V_{iN})$ and the negative one "E_{neg}" = $min(V_{iN})$ have main impact in BEM concept. Note the third component of (1), not generating neither E_{pos} nor E_{neg} , is called "E_{tr}" representing the

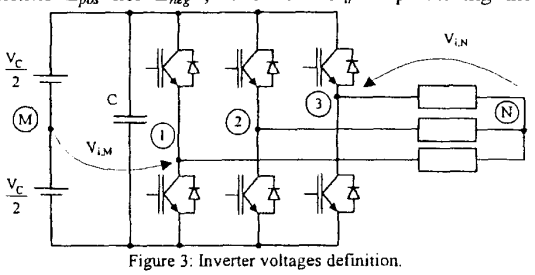

Figure 3: Inverter voltages definition.

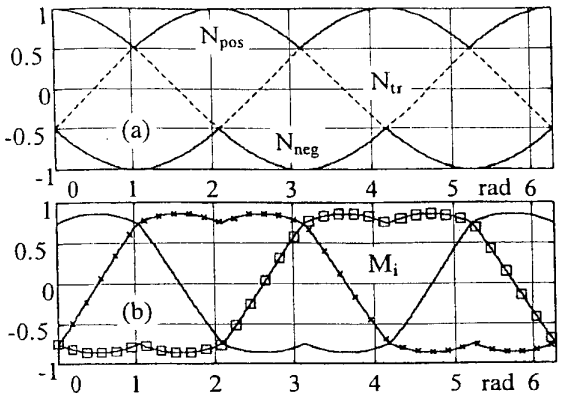

Figure 4: Modulation indexes vs phase angle in BEM technique.

component in "transition" from one envelope to the other, having also a triangular-like shape (see Fig.4a).

Two modulation indexes are defined, namely "*N*" (2) according to phase-to-neutral voltage components:

$$\vec{N} = \vec{V}_N^* \frac{1}{V_C/2} \tag{2}$$

and "*M*" (3) for phase-to mid-point VSI voltages:

$$\vec{M} = \vec{N} + [I] \cdot M_{NM} \tag{3}$$

whose components are actually compared to the PWM triangular carrier having unity envelopes (±1 ≡ triangular carrier peak); "M_{NM}" represents the common-mode quantity added to reference symmetrical components N_i.

The realized voltages to mid-point can be expressed as:

$$V_{i,M} \equiv \frac{V_C}{2} M_i; \quad \text{being always} |M_i| \le 1; \tag{4}$$

In the BEM technique M_{NM} is set and defined in order to balance the envelopes of the vector components M_i (and equivalently the requested voltages to mid-point V_{iM}). The related common-mode voltage "V^*_{NM}" results as follows:

$$V^*_{NM} = -\left(E_{pos} + E_{neg}\right)/2 = E_{tr}/2 \tag{5}$$

and the related common-mode index value is:

$$M_{NM} = N_{tr}/2 = -\left(N_{pos} + N_{neg}\right)/2 \tag{6}$$

Figure 4b shows the components M_i resulting from sinusoidal references N_i and application of (6) to (3), implicitly defining the transformed indexes N_{tr} N_{neg} N_{pos}.

The common-mode rejection is a property of three phase loads without neutral connection, as known, so that the load voltage components V_{iN} reappear equal to reference ones provided that M_i* modules are lower than unity:

$$V_{iN} = V_C/2\left(M_i - M_{NM}\right) \tag{7}$$

This technique allows for easy linearity extension up to physical real-time limits. In steady-state sine operation BEM performs as other method does (SVM or added 3rd harmonics), achieving 15% more linear range with respect to holding $M_{NM}=0$, as deduced from Fig.4 graphs.

III. Crossover Voltage Modulation (CVM)

The BEM technique is adopted all over the AC voltage range, from zero up to six-step mode, as the fundamental building block of CVM. The real-time DC-link voltage regulation allows for sinusoidal or high-quality AC outputs by switching only one 3ΦVSI-leg per 3Φ–sector.

A. Basics of single-leg PWM by balanced envelopes.

The BEM technique can be used to reproduce a linear three phase modulation strategy by switching only one 3ΦVSI-leg in each sector, thus largely reducing switching losses and PWM ripple content.

The statement for first sector ($0 \le \vartheta \le \pi/6$) is reported:

$$\vec{M}^* = \left[1 \quad f(\vartheta) \quad -1\right]^T ; \; M_{NM} = f(\vartheta)/3 \tag{8}$$

Two M_i components set the envelopes to unity and the third component is in "transition" between the envelopes according to the generic function "$f(\vartheta)$", which implicitly defines the common mode index M_{NM} shape (8).

The effects of such modulation approach are:

- the vector argument is set by the transition component, that is the function $f(\vartheta)$;
- the voltage vector amplitude is set by actual dc-link voltage value and it is affected by argument function.

Since the PWM allows for straightforward realization of every $f(\vartheta)$ value within unity, the main control task is represented by real-time control the DC-link voltage.

1. Sinusoidal output by Quasi-Trapezoidal Modulation.

The real-time DC-link voltage regulation in the electrical period can hold single-leg PWM benefits with linear voltages transfer function.

Equating (1) and (7) with the constraint (8) yields:

$$E6 = E_{pos} - E_{neg} \tag{9}$$

$$V_C = E6 = V^*_{1N} - V^*_{3N} = \hat{V}\sqrt{3}\cos\left(\vartheta - \tfrac{1}{6}\pi\right) \tag{10}$$

$$f(\vartheta) = \frac{\frac{3}{2}E_{tr}}{\frac{1}{2}V_C} = \frac{\frac{3}{2}V^*_{2N}}{\frac{1}{2}V_C} = \sqrt{3}\tan\left(\vartheta - \tfrac{1}{6}\pi\right) \tag{11}$$

The same calculation can be done for all sectors showing that first part of eqs. (9-11) are valid by properly defining E_{pos}, E_{neg} and E_{tr} according to section II.

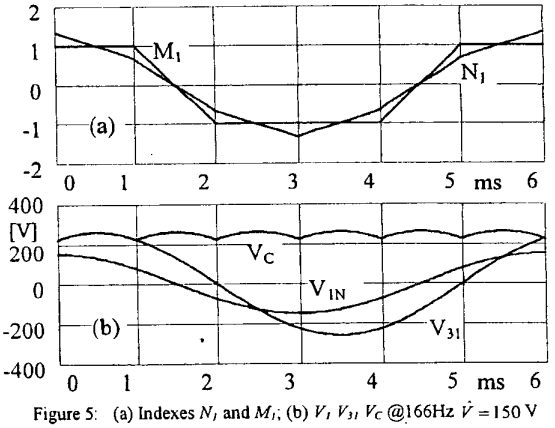

Figure 5: (a) Indexes N_1 and M_1; (b) V_1 V_{31} V_C @166Hz $\hat{V}$ = 150 V

Figure 5 shows coherent waveforms of homologous modulation indexes N_1, M_1, output voltage V_1 together with the DC-link voltage V_C. The line-to-line voltage V_{31} gives evidence to relationship with the DC-link voltage.

Being ±1 the modulation limits, each inverter leg is not in PWM mode when the homologous index module is equal or greater than unity.

2. QTM with double-clamped DC-voltage.

The drawback of DC-link voltage profile is the related rms current in the DC-link capacitors (dotted line Fig.6b).

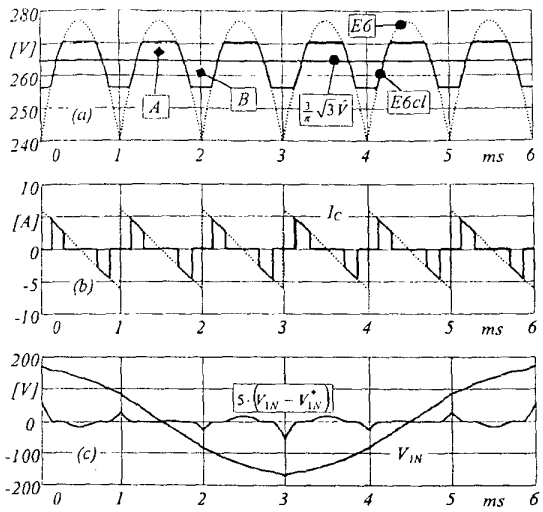

Figure 6: DC-link voltage clamp effect @166Hz $\hat{V}=150$ V

Minimum DC-link capacitor value has been suitably realized, together with PWM phase and frequency relationship between DC and AC converter sides in order to contain the produced rms current value. Anyway the DC-link voltage should be limited with increasing AC voltage amplitude and motor electrical frequency.

The adopted control solution, reported in Fig.7, clamps the DC voltage reference $V_{C,ref}$ (otherwise equal to *E6*) at proper max-min values $a\sqrt{3}\hat{V}$ and $b\sqrt{3}\hat{V}$, respectively, obtaining the current ripple reduction reported in Fig.6.

Signals "a" and "b" span over the ranges.

$$\frac{3}{\pi} \le a \le 1; \qquad \frac{\sqrt{3}}{2} \le b \le \frac{3}{\pi} \tag{12}$$

Their instantaneous values are related to each other in order to hold the mean value of the *E6cl* signal equal to that of the input signal *E6*. This means that the areas of the two part "A" and "B" in Fig.6a have to be equal in order to maintain the fundamental component of realized AC voltages equal to the reference one. This has been proved numerically obtaining an error of less than 0.2%.

In the overall control scheme in Fig.7, the value of the clamping signal a is imposed by a pure integral regulation of the dc-link capacitor rms current to less than a maximum reference value; suitable function $b(a)$ is then realized. The $I_{C,rms}$ current in the DC-link capacitor bank is derived from the DC-link voltage V_C signal.

The effects on voltages of this limitation is easily explained when $a=b=3/\pi$. In this condition the realized voltages to mid-point are trapezoidal-like as modulation indexes M_i are. If $a \neq b$ the shape of the AC voltages is sharing trapezoidal and sinusoidal segments as it can be seen in Fig.6c on phase-to-neutral voltage, where the zoomed transfer error points out the double clamp effect.

This clamping technique holds the first harmonic linearity also when the upper clamp is provided by $V_{C,ref}$ limitation to maximum DC-voltage $V_{C,MAX}$.

B. CVM operation vs. AC voltage amplitude.

Due to the adopted DC-DC-AC structure and to physical limitations, there are four different operating ranges depending on reference voltage amplitude. Fig.7 block scheme is valid for all of these ones.

1. Conventional 3Φ–PWM mode: constant $V_C \equiv V_{batt}$

The first range represents the usual PWM operation at constant DC voltage, since the DC link voltage V_C cannot be controlled down to zero due to the DC-DC boost configuration.

If $V_{batt} \ge \sqrt{3}\hat{V}$, V_C must be equal to battery voltage and the 3Φ-VSI is equivalently connected to the battery by the free-wheeling diodes of the DC-DC converter (motoring).

The variable gain represented by V_{drv} in Fig.7 is coherently fixed to $V_{batt}/2$ by a saturation block simulating the DC-DC behavior.

As a result, the 3Φ-VSI operates the PWM control of both phase and amplitude of the realized voltage vector (as a common SVM, here substituted by the defined BEM).

The modulation frequency for this range can be set by tradeoff between current ripple and switching losses. In our prototype it is fixed at 5kHz thanks to reduced DC voltage.

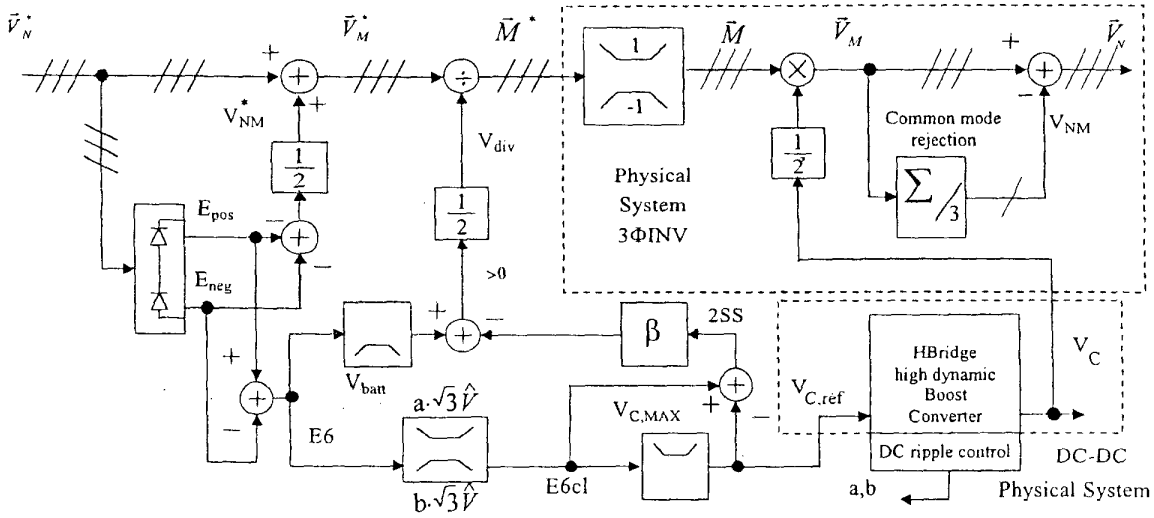

Figure 7: CVM technique block scheme

2. Transition to QTM: $V_{batt} \le V_C \le 2/\sqrt{3}\, V_{batt}$

Equation (10) shows that the QTM can be adopted with two limitations to be verified at the same time:

$$min\left(V_{C,ref}\right) = \frac{3}{2}\hat{V} \quad and \quad max\left(V_{C,ref}\right) = \sqrt{3}\,\hat{V} \qquad (13)$$

When battery voltage is within the two limits in (13) the system follows two different modulation strategies (3Φ-BEM and single-leg QTM) depending on the continuously variable instantaneous ratio between $V_{C,ref}$ and V_{batt}.

Fig.8a shows the angular modulation segments ofthe modulation index vector locus (bolded line), while Fig.8b shows the related V_C waveform evidencing the inherent lower clamp function of the boost converter.

The two modulation zones adopt different modulation carriers (5kHz for 3Φ-BEM and 20kHz for single-leg QTM) holding low switching losses. A simple Gate Array logic operates the change between the PWM carriers at lowest frequency (5kHz). This carrier changes allows for phase and frequency coordination between DC-DC and DC-AC power stages, thus minimizing DC capacitor ripple and rms current value.

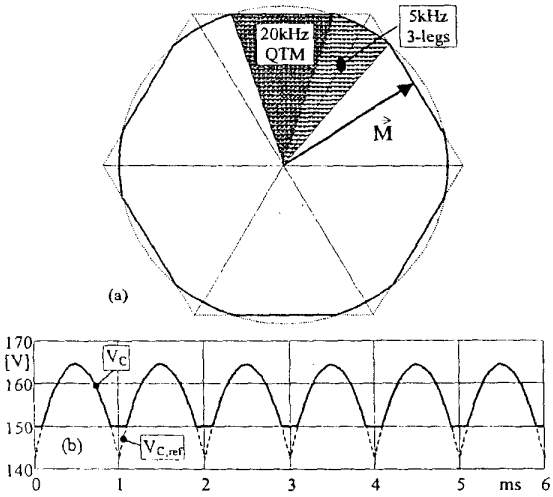

Figure 8: (a) Modulation index locus on the limit hexagon; (b) V_C in the transition to QTM zone @ V_{batt}=150V, $\hat{V}$ = 95 V

3. QTM: $2/\sqrt{3}\, V_{batt} < V_C < V_{C,MAX}$

In this third range the DC-link voltage could be completely controlled and the modulation of the 3Φ-VSI can be realized by switching only one leg per sector.

This range can be further divided in three zones depending on clamps action as described in section III.A.2.

- 3.1 Sinusoidal output: no clamps act in this zone; outputs are sinusoidal (instantaneous linearity)
- 3.2 Double-clamped V_C: current limitation arise and odd harmonics are added to the fundamental output;
- 3.3 Constant V_C: when the two clamps are equal to each other $\left(a = b = 3/\pi\right)$ the DC-voltage is set to the mean value of *E6* $\left(V_C = \sqrt{3}\,\hat{V}\,3/\pi\right)$; outputs derive from trapezoidal-like QTM indexes shape.

It can be supposed that these three zones are sequentially performed with the reference vector amplitude, since voltage and frequency are generally proportional to each other, thus making grow of the $I_{C,rms}$ component with fundamental amplitude.

4. From QTM to Six-Step mode: $V_C = V_{C,MAX}$

When $\vec{V}_N^*$ is generating an *E6* signal with a mean value greater than $V_{C,MAX}$, $V_{C,ref}$ is fixed to $V_{C,MAX}$ (switches maximum voltage rating protection).

By constant and constrained V_C value, the first harmonic content of AC voltages can grow a few percent up to six-step operation, however the modulation indexes have to grow up faster than the reference voltage does (pure Six-Step mode obtainable by infinite modulation indexes).

Holding the triangular carrier PWM, the adopted scheme in Fig.7 increases the gain on modulation indexes by reducing the divider V_{div} , proportionally to the difference between the mean value of *E6* and $V_{C,MAX}$. β could represent a suitable function, while in the proposed scheme it is simply a proportional gain; the maximum linearity error is less than 1.2% on the realized fundamental component of AC voltages.

In Fig.9 a simulation of quasi-six-step operation is presented; only part of each sector is modulated by a single phase. This allows for monotonous rise to maximum realizable fundamental component, reported by (14):

$$\hat{V}_{MAX,SS} = 2/\pi\; V_{C,MAX} \approx 255V \qquad (14)$$

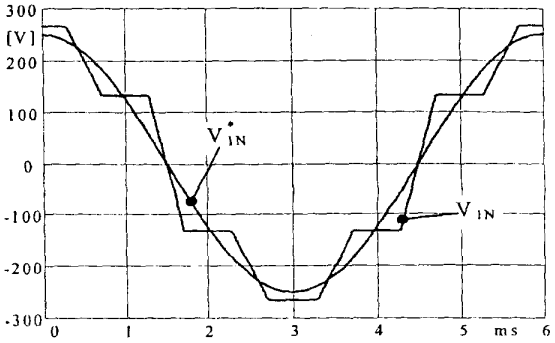

Figure 9 : Quasi Six Step mode,@ V=250V, V_C=400V, f_{ac}=166Hz

5. Full-range voltage transfer

The graphs in Fig.10 reports the calculated main harmonics (fundamental, 5th and 7th) all over the different modulation ranges, versus the reference line-to-line voltage amplitude and at V_{batt}=150V.

PWM, QTM and related transition perform "perfect" transfer without main harmonics.

The upper *a* dc-link clamp action is started at 250V and it is linearly enhanced (zone 3.2) to reach QTM constant-V_C operation at 350V. As shown, the unity transfer function of fundamental component (line-to-line amplitude) is maintained till the maximum realizable amplitude, while harmonics appear in zone 3.2, monotonously increasing with the clamp action.

These harmonics hold the QTM spectrum in zone 3.3, their absolute value varying only with the DC voltage.

In the last range, the harmonics grows up to six-step spectrum content. Note the small fundamental transfer error, related to simple linear reduction of the divider V_{div} (constant gain β) with reference amplitude.

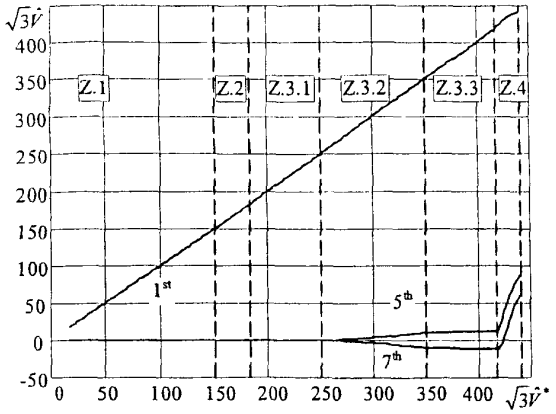

Figure 10 Working zones; fundamental, 5th and 7th harmonics of line-to-line voltage vs. reference one, V_{batt}=150V, $V_{C,MAX}$=400V

IV. Experimental Results

The power system is composed by two equal 3Φ power PCBs, connected each other by the DC-link side and differently disposed to realize the DC-DC (one leg unused) and the DC-AC stages.

Each PCB adopts high-rms-current small film capacitors (Unlytic) and one 3Φ-IPM (Mitsubishi PM200CVA060) with dedicated driver opto-insulated buffers, supply and auxiliary protection circuits, as shown in Fig.11.

The principal characteristics of the power system are:

- 30kW peak power, limited by 150Vx200A DC input;
- Extremely low DC-link capacitance (C=42μF film);
- Small input capacitance filter (3.3mF electrolytic);
- Modulation frequencies: 10kHz for the DC-DC side; 5-20kHz for the inverter side depending on operating point (see section III.b.2).

Such a low capacitance value has been purposely tested for overall integration and cost, improving the dynamic performance of the DC-DC converter and reducing the $I_{C,rms}$ value needed to follow the reference voltage profile. The DC-DC converter is closed-loop controlled by a dedicated non linear strategy already reported [3].

The battery has been simulated by rectifying a variable AC source with large DC capacitor bank (60mF).

A small induction motor at no load is used as open-loop electrical AC load, regulating independently amplitude and frequency to verify all operating voltage ranges.

The experimental results are reported in Figs.12-17 by equal scaling factors: in the upper part the line-to-midpoint voltage V_{1M} and the modulation index M_1 (bolded); in the lower part the line-to-neutral voltage V_{1N} and its mean value. This one is realized by oscilloscope digital filter and suffers of critical compromise between sampling and filtering rates.

All operating ranges are reported, showing very good experimental performances, matching numerical results.

Figure 13 reports zoomed sixth of electrical period, pointing out the modulation frequency change from 5 to 20 kHz without modulation error.

What clearly appears on motor voltages is the strong reduction of PWM content, related to minimum DC-voltage in Fig.11 and disposed by QTM technique for increasing AC voltage values. Sinusoidal output is held until Fig.15 zone, while progressively increased harmonic distortion is introduced up to quasi six-step zone in Fig.17.

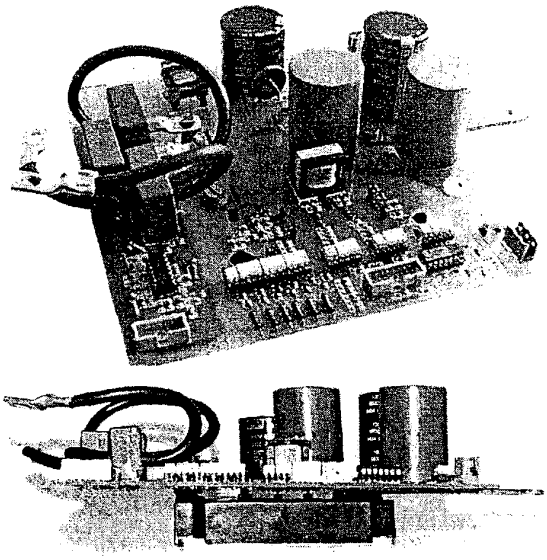

Figure 11 Power PCB arranged for HB DC-DC converter

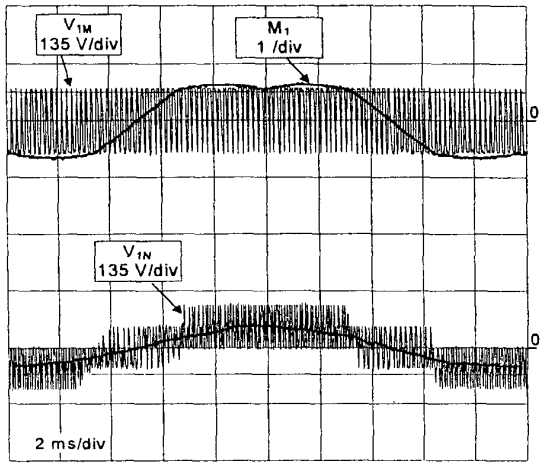

Figure 12 Zone 1: $\hat{V} = 100/\sqrt{3}$ V; fac=50Hz; f_{sw}=5kHz;

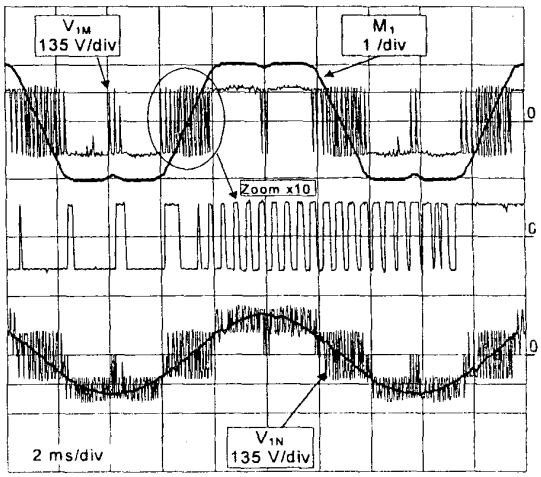

Figure 13 Zone2: $\hat{V} = 164/\sqrt{3}$ V; fac=82Hz; f_{sw}=5-20kHz;

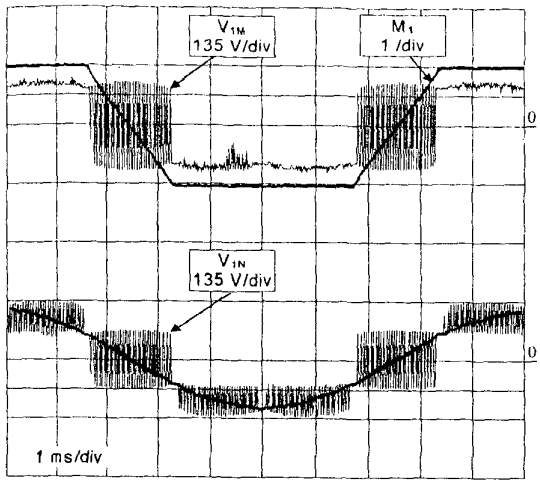

Figure 14 Zone 3.1: $\hat{V} = 200/\sqrt{3}$ V; fac=100Hz; f_{sw}=20kHz;

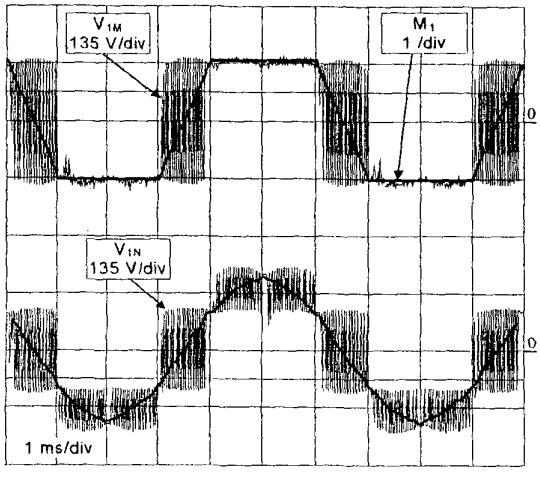

Figure 15 Zone 3.2: $\hat{V} = 300/\sqrt{3}$ V; fac=166Hz; f_{sw}=20kHz, a=0.97.

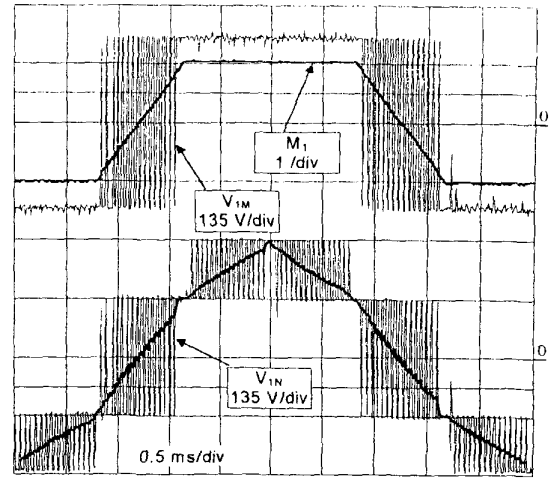

Figure 16 Zone 3.3: $\hat{V} = 400\pi/(3\sqrt{3})$V (~242V); fac=200Hz; f_{sw}=20kHz,

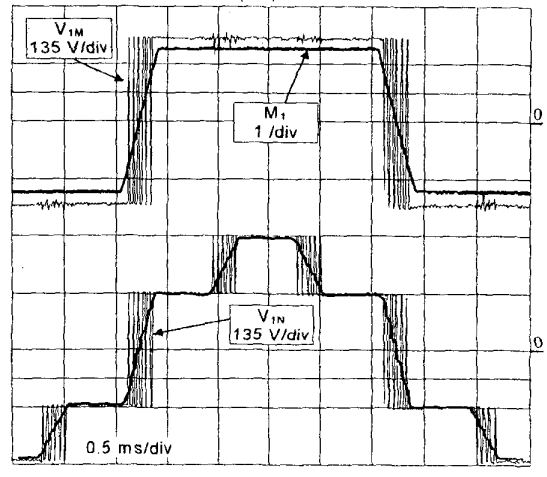

Figure 17 Zone 4 $\hat{V}$ = 250 V; fac=200Hz; f_{sw}=20kHz;

V. Conclusions

A novel DC-DC-AC power conversion system has been presented for automotive DC-supplied AC motor drives.

New BEM technique and CVM concept have been investigated in order to fulfill the improvements achievable by the cascaded DC-DC-AC power stages, defining the different voltage ranges and modulation properties.

The experimental results are very satisfactory, showing outstanding AC motor voltage quality, obtained together with improved overall DC-AC conversion efficiency.

Further investigations are planned for the evaluation of the expected reduction on AC motor eddy PWM losses, achieved by the new CVM strategy.

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