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# Behavioral Macromodels of Differential Drivers

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**Abstract**

This paper addresses the development of behavioral macromodels of differential drivers for the assessment of signal integrity and electromagnetic compatibility effects in high-speed digital systems. The obtained macromodels are readily implemented as SPICE-like subcircuts to be included in any circuit simulation environment. Accuracy and efficiency of macromodels are assessed by applying the proposed methodology to actual differential devices.

## 1 INTRODUCTION

Low Voltage Differential Signaling (LVDS) is going to establish as the dominant standard for on-board and off-board high-performance data links [1, 2, 3]. It allows extremely high data rates, on the order of one Gbps, along with reduced EMI effects and reduced power absorption.

In order to simulate the operation of LVDS link for the assessment of Signal Integrity (SI) and ElectroMagnetic Compatibility (EMC) problems, suitable behavioral models (or macromodels) of differential drivers and receivers are needed. To this aim, in this paper, we address the behavioral modeling of LVDS differential driver output buffers. The proposed modeling procedure exploits piecewise models and parametric relations introduced in [4] for single-ended devices, and is demonstrated by two modeling examples.

## 2 DEVICE AND MODEL STRUCTURE

The output buffers of LVDS drivers operate via current steering techniques, as shown in Fig. 1. Two voltage controlled current source devices are used to provide the current sent to and drawn from resistor $R_r$ at receiver input terminals. When switches $A$ are closed, $i_r$ is positive, whereas when switches $B$ are closed $i_r$ is negative and the voltage across receiver input terminals changes polarity. In actual applications, output buffers may contain matching resistors across the output terminals and control subcircuits to ensure proper output current and voltage values over possible process, supply voltage and temperature variations (*e.g.*, see [9, 10, 11] for possible implementations of control circuits).

In fixed logic state, the ideal LVDS output buffer of Fig. 1 can be considered as a three-terminal circuit element characterized by constitutive relations of the form (which we call submodels)

$$\begin{cases} i_1 = i_{1H}(v_1, v_2) \\ i_2 = i_{2H}(v_1, v_2) \end{cases} \quad \begin{cases} i_1 = i_{1L}(v_1, v_2) \\ i_2 = i_{2L}(v_1, v_2) \end{cases} \tag{1}$$

where $H$ and $L$ denote the HIGH and LOW logic state, respectively, and the output currents are allowed to be functions of both voltages to take into account variants of the buffer basic scheme with internal resistor and control circuits. If useful, the above constitutive relations can be expressed in terms of different variables obtained as linear combinations of port voltages $v_1$ and $v_2$. A typical set of alternative variables are the

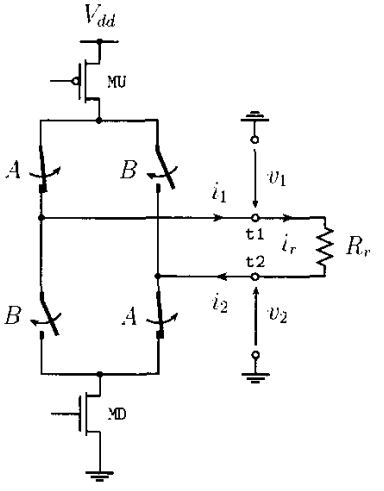


Figure 1: Generic structure of a LVDS driver and its relevant electric variables.

common mode voltage $v_c = \frac{(v_1+v_2)}{2}$ and the differential voltage $v_d = (v_1 - v_2)$. A complete macromodel describing state switching from steady state operation can be obtained by combining in a two-piece model the constitutive relations (1) by means of time-varying weighting coefficients

$$\begin{cases} i_1 = w_{1H}(t) i_{1H}(v_1, v_2) + w_{1L}(t) i_{1L}(v_1, v_2) \\ i_2 = w_{2H}(t) i_{2H}(v_1, v_2) + w_{2L}(t) i_{2L}(v_1, v_2) \end{cases} \tag{2}$$

where $w_{nH}$ and $w_{nL}$, $n = 1, 2$ are the weighting coefficients accounting for logic state transitions. Representation (2) approximates the external device behavior including the information on state transitions without assumptions on the device internal structure. The problem is then to devise suitable relations for the submodels of (1), to estimate their parameters and estimate the weigthing coefficients of (2).

A straightforward approach is to represent $i_{nH}$ and $i_{nL}$ by a sum of a static mapping and a (possibly nonlinear) relation taking into account dynamic effects, as discussed in [4] for the case of single-ended devices. As an example, for $i_{nH}(v_1, v_2)$ such a representation is

$$\begin{cases} i_{1H}(v_1, v_2) = \hat{i}_{1H}(v_1, v_2) + \bar{i}_{1H}(v_1, v_2, t) \\ i_{2H}(v_1, v_2) = \hat{i}_{2H}(v_1, v_2) + \bar{i}_{2H}(v_1, v_2, t) \end{cases} \tag{3}$$

where $\hat{i}_{1H}$ and $\hat{i}_{2H}$ are the static characteristics of currents $i_1$ and $i_2$ for the driver forced in the fixed HIGH logic state and $\bar{i}_{1H}$ and $\bar{i}_{2H}$ are the dynamic submodels. Similar equations occur for $i_{nL}(v_1, v_2)$ of (2).

Owing to the well established theory of system identification for approximating the nonlinear dynamic behavior of *almost any* nonlinear dynamical system and the large availability

of methods for estimating model parameters, model representations defined by nonlinear parametric relations can be effectively used for the dynamic terms in (3). A complete review of possible representation can be found in [6].

For those devices with dynamic behavior dominated by linear capacitive effects, as in the example devices considered in the paper, the dynamic terms in (3) can be replaced by linear parametric models involving the derivative of port voltages only, and further simplified as follows.

$$\begin{cases} \bar{i}_{1H} = -C_{1H}\frac{dv_1}{dt} - C_{12H}\frac{d(v_1-v_2)}{dt} \\ \bar{i}_{2H} = +C_{2H}\frac{dv_2}{dt} + C_{12H}\frac{d(v_2-v_1)}{dt} \end{cases} \quad (4)$$

It is worth noting that the model representation defined by equations (2-4) is reminiscent of models based on simplified equivalent circuits (*e.g.*, see [12] and [5]). Such a representation, however, is more general and does not significantly affect the complexity of the resulting macromodel. It approximates a port constitutive relation and includes both static and dynamic coupling effects between the terminal variables without any specific assumption on the internal structure of device. Equation 4, has been written in terms of the equivalent capacitors $C_{1H}$, $C_{2H}$ and $C_{12H}$ as unknown variables of a parametric linear capacitive relation since this is the most common way for representing such a kind of behavior and can be replaced by an arbitrary nonlinear parametric model when this simplified assumption is not met.

Both the static mapping and the dynamic part can be estimated from currents caused by suitable test sources connected to driver output terminals, like in Fig. 2. The static mappings easily arise from steady state current values, whereas the dynamic parts can be estimated from suitable transient responses (*e.g.*, those caused by large fast variations of sources of the estimation setup of Fig. 2). Of course, the terminal voltage variations applied by test sources should correspond to differential and common mode voltage variations within limits specified by the LVDS standard. Once suitable submodels are available for terminal currents in fixed logic states, the weighting coefficients of single up (`01`) and down (`10`) state transitions (basic weighting coefficients) can be obtained via linear inversion of (2) from voltage and current waveforms recorded during such transition events. Finally, for a specific logic activity of the device (*e.g.*, a bit stream `01001101011...`), the weighting coefficients are obtained by generating a sequence in time by juxtaposition of the basic weighting coefficients of up and down transitions.

## 3 APPLICATION EXAMPLES

In this Section, the proposed modeling approach is demonstrated on two different devices defined by detailed transistor-level models, which are assumed as the *reference* models hereafter. All simulations are carried out by HSPICE and the reference models are used to compute the responses needed for the estimation of macromodel parameters and for model validations. Both examples are addressed by the model representation of (4) and the obtained models are implemented as a SPICE-like subcircuits by means of standard components.

**Example 1** The first modeled device is the Fairchild FIN1001 ($V_{dd} = 3.3$. V) LVDS High Speed Differential Driver, whose

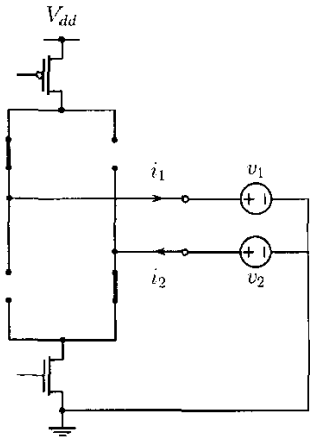


Figure 2: Common setup for both the estimation of the static characteristics and the dynamic behavior of the LVDS device of Fig. 1 in the HIGH logic state.

HSPICE encrypted transistor-level model is available from the official website `www.fairchildsemi.com`. This device bahaves like a plain differential driver (see Fig. 1) without internal matching resistors or control mechanisms.

For the macromodel estimation, both the static and the dynamic parts of (4) are computed through the procedure discussed in the previous Section. As an example, Fig. 3 shows the static characteristic $\bar{i}_{1H}(v_1, v_2)$. In order to facilitate the model implementation, the static characteristics $\bar{i}_{1H}$ and $\bar{i}_{2H}$, that are known as sets of sampled DC curves, are approximated by suitable analytical expressions (*i.e.*, sigmoidal expansions in this case [6, 7, 8]).

The estimation of the dynamic contribution is carried out by recasting 4 as a linear least square problem for $\{C_{1H}, C_{2H}, C_{12H}\}$ and $\{C_{1L}, C_{2L}, C_{12L}\}$. This is achieved by recording the device responses $i_1(t)$ and $i_2(t)$ while the driver is forced in the HIGH or LOW logic state and the terminals are connected to noise voltage sources as in Fig. 2. In this example, independent gaussian noise sources with mean value equal to the nominal common mode voltage (*e.g.*, 1.25 V) and small/amplitude standard deviation (*e.g.*, 10 mV) are used. In addition, the linearity of the dynamic contribution has been verified by applying noisy signals with amplitude on the order of the full voltage swing of 350 mV specified by the LVDS standard. The values estimated for the coefficients of the dynamic part are $\{C_{1H}, C_{2H}, C_{12H}\} = \{1.65, 1.66, 0.125\}$ pF and $\{C_{1L}, C_{2L}, C_{12L}\} = \{1.66, 1.62, 0.109\}$ pF. The weighting coefficients are computed as described in the previous Section, by means of switching experiments while the device is connected to a 100 Ω differential load resistor.

In order to validate the macromodel, two different simulation test cases are considered. The first test circuit is composed of the modeled device driving a 50 Ω differential resistor with a logic HIGH pulse. For this test case, Fig. 4 shows the reference and macromodel responses of the output terminal voltages $v_1(t)$, $v_2(t)$ and of the differential voltage $v_d(t)$.

The second test circuit is composed of the modeled de-

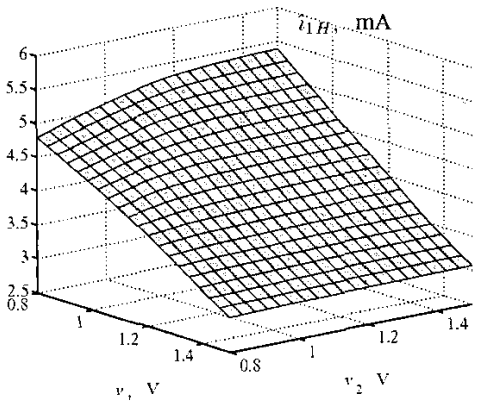


Figure 3: Static characteristic $i_{1H}(v_1, v_2)$ for the Example 1 driver forced in the HIGH logic state.

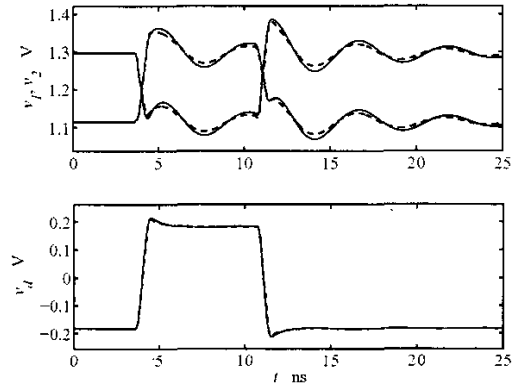


Figure 4: Output port voltages $v_1(t)$, $v_2(t)$ (top panel) and differential voltage $v_d(t)$ (bottom panel) computed for the first test circuit of Example 1 (see text). Solid line: reference, dashed line: macromodel.

vice driving a coupled transmission line (differential mode impedance $Z_o = 50\,\Omega$, common mode impedance $Z_e = 100\,\Omega$, line length 0.15 m) loaded by a $100\,\Omega$ differential resistor with a logic HIGH pulse. For this test case, Fig. 5 shows the reference and macromodel responses of the output terminal voltages $v_1(t)$, $v_2(t)$ and of the differential voltage $v_d(t)$.

The accuracy of the proposed macromodel has been quantified by computing the timing error and the maximum relative voltage error. The timing error is defined as the maximum delay between the reference and the macromodel differential voltage responses measured for the zero voltage crossing. For the two test cases illustrated in Figs. 4 and 5, the maximum timing error is 15 ps. The maximum relative voltage error is computed as the maximum error between the reference and macromodel voltage responses divided by the nominal voltage swing of 350 mV. For the previous validation cases, the maximum relative error turns out to be 5.4%.

Finally, macromodel efficiency is assessed by the CPU-time

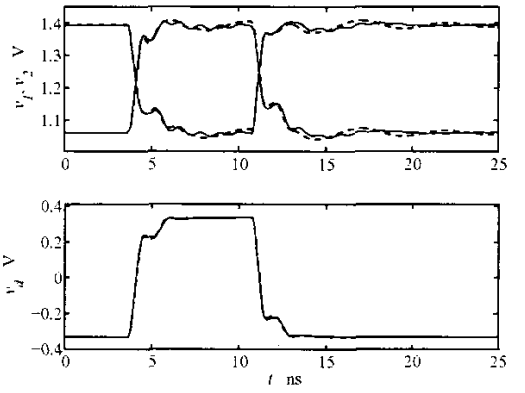


Figure 5: Output port voltages $v_1(t)$, $v_2(t)$ (top panel) and differential voltage $v_d(t)$ (bottom panel) computed for the second test circuit of Example 1 (see text). Solid line: reference, dashed line: macromodel.

Table 1: CPU time and memory usage for the computation of the curves of Fig. 4 by means of HSPICE.

| Model | CPU time | Memory |
|---|---|---|
| reference | 10.70 sec | 1430 Kb |
| macromodel | 2.35 sec | 490 kb |

and memory usage required for circuit simulations. For the example device of this Section, Tab. 1 collects the figures of the efficiency comparison between the reference transistor-level model and the macromodel for the computation of the curves of Fig. 4.

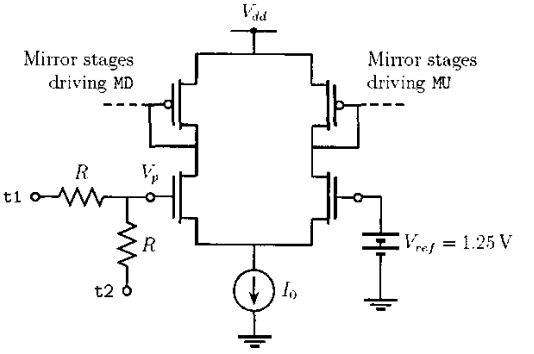


Figure 6: Control circuit for the example driver 2.

**Example 2** The second modeled device is an idealized implementation of the differential driver proposed in [9], that exploits a control mechanism to reduce the fluctuations of the common mode voltage $v_c$ around a reference voltage (*e.g.*, 1.25 V). Here, the mechanism is implemented by the differential amplifier and current mirrors of Fig. 6, regulating the drain currents of MU and MD of Fig. 1. The probe voltage $V_p$ is obtained by a high resistance ($R = 100\,\text{k}\Omega$) voltage divider connected to the output

terminals of Fig. 1. In this paper, Both the output stage of Fig. 1 and the control circuit of Fig. 6 are implemented in HSPICE and used as the reference model for Example 2.

Figure 7 shows the static characteristic $i_{1H}(v_1, v_2)$ (versus voltages $v_c$ and $v_d$) for this device. According to the purpose of the control circuit, the variations of this characteristic versus $v_c$ is dominant, and, since $v_c = (v_1 + v_2)/2$, the usual simplification $i_{1H}(v_1, v_2) \approx i_{1H}(v_1)$ does not hold. The coefficients of the linear part are estimated as in Example 1 and their values are $\{C_{1H}, C_{2H}, C_{12H}\} = \{0.563, 0.563, 0.063\}$ pF.

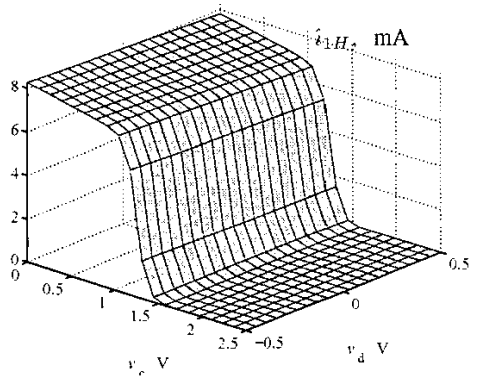


Figure 7: Static characteristic $i_{1H}(v_1, v_2)$ for the Example 2 driver forced in the HIGH logic state.

The validation test for this example is devised to highlight the differences introduced by the control mechanism and to assess the accuracy of the proposed model even for devices with enhanced features. The test circuit consists of the example driver forced in HIGH state and connected to a differential load composed of a 100 Ω resistor in series with an independent voltage source. The voltage source produces a pulse with 0.5 V amplitude and 100 ps transitions. The common mode voltage $v_c$ and load current waveforms predicted by using the reference and the estimated models in such a test circuit are shown in Fig. 8. The good agreement of the curves confirms the ability of model (4) to describe differential drivers with control mechanism and highlights the importance of taking into account the dependence of the modeled currents on both output voltages.


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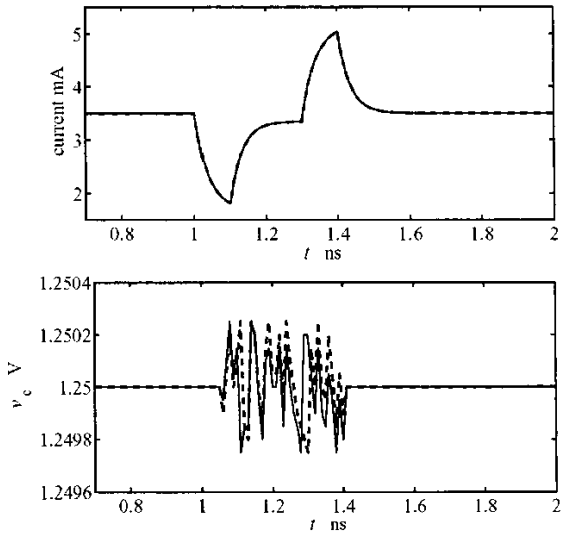


Figure 8: Load current (top panel) and common mode voltage $v_c(t)$ (bottom panel) computed for the test circuit of Example 2 (see text). Solid line: reference, dashed line: macromodel.


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