An approach to harmonic load- and source-pull measurements for high-efficiency PA design

An Approach to Harmonic Load– and Source–Pull Measurements for High-Efficiency PA Design

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***Abstract*—High-efficiency power-amplifier design requires numerous efforts to investigate both input and output harmonic terminations effects. A simplified theoretical approach to clarify the relevance of such terminations is presented here, and design criteria to improve efficiency for high-frequency applications are briefly discussed. An advanced active load/source–pull test-bench has been used to validate theoretical harmonic tuning techniques, characterizing an active device. The adopted optimization strategy is presented, together with measured results obtained with a medium-power 1-mm MESFET at 1 GHz. Input second harmonic impedances effects are stressed, showing a drain efficiency spread between 37%–49% for a fixed input power level, corresponding to 1-dB compression. Finally, as predicted by the presented theory, after input second harmonic tuning, further improvements are obtained, increasing fundamental output load resistive part, demonstrating an additional drain efficiency enhancement, which reaches a level of 55% at 1-dB compression.**

***Index Terms*—Harmonic tuning, high efficiency, load–pull, power amplifiers (PAs).**

I. Introduction

WIRELESS network operators main requests are operational costs reduction and, at the same time, system capabilities increase. In particular, deployment of smaller base stations, featured by higher flexibility, efficiency and lower cost, becomes one of the system suppliers main goals.

In this scenario, power amplifiers (PAs) play a key role, becoming crucial elements of transmitter units in many microwave systems, including handy phone applications, satellite payloads, microwave transponders, and many others.

Usual PA design approaches seek high power efficiency coupled with suitable gain and output power levels. The former is required to improve battery lifetime and to ease thermal management, thus reducing operating cost, while the latter specifications are needed to reduce the number of amplifier stages together with unit size and weight, thus decreasing manufacturing costs. Such requirements are contrasting ones, therefore, demanding a design compromise on achievable performances.

Several design strategies have been proposed up to now. In particular, for narrow-band applications, harmonic tuning strategies have been addressed and successfully applied at microwave frequencies [1]–[5], resulting in significant improvement in both output power and conversion efficiency.

For PA design, nonlinear techniques are required, due to the intrinsic active device nonlinear behavior; two different approaches are available: one is based on large-signal simulations, the other on measurements and experimental results. In the former case, a full nonlinear model for the active device is needed, joined with nonlinear analysis algorithms. The major drawback of this design approach is related to the use of an appropriate and accurate nonlinear model [6], [7].

The experimental approach is mainly based on load/source–pull techniques, in which the actual active device is fully characterized in terms of output power, matching impedances, efficiency, and any other required performance, by means of exhaustive and intensive measurement activity [8]–[11]. As a matter of fact, the experimental approach represents a direct solution since the actual device is characterized in real time (no models are required) and design quantities are readily available. Obvious disadvantages of this approach are related to test-bench equipment cost and to actual device availability in the appropriate testing form.

In both cases, however, if harmonic tuning approaches need to be exploited, some considerations must be applied to reduce design efforts and to avoid misleading results, with the help of some theoretical guidelines proposed in the past, by means of a simplified analysis [12].

The goal of this paper is to present the combination of an advanced harmonic load–pull test bench with harmonic tuning guidelines, thus forming an accurate and effective tool for PA design. Moreover, although the design procedure that will be presented is focused on an experimental approach, it also provides useful indications for approaches based on nonlinear simulation, avoiding time-consuming nonlinear optimization algorithms, which may lead to local minima and whose goals could be difficult to identify and define.

In Section II, the measurement setup and calibration are described, while in Section III, the theory of harmonic tuned PA design is focused. Section IV presents the experimental validation and, finally, in Section V, some conclusions are drawn.

II. Nonlinear Test Bench

The measurement test set, already proposed in [11], combines S-parameter capability, real-time load- and source–pull (single tone or harmonic) with time-domain waveform measurements [13]–[15] and has been extended to intermodulation (IM) measurements.

Any linear vector network analyzer (VNA) with at least two samplers (or mixers) can be used as linear receiver, while a mi-

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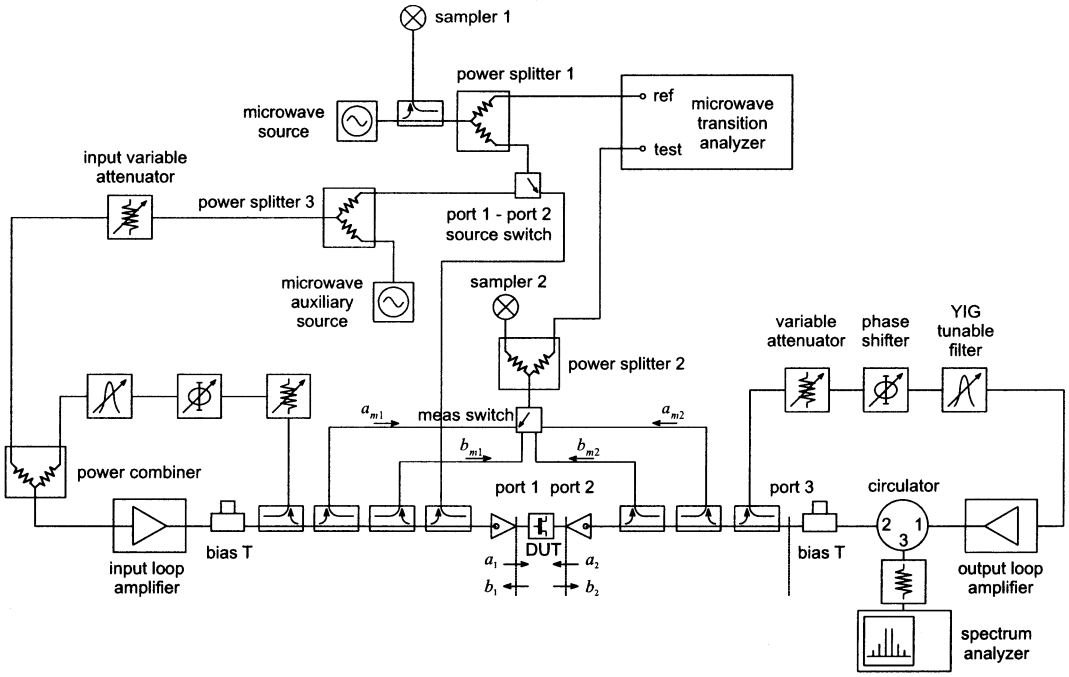

Fig. 1. Simplified scheme of the load/source–pull and IM setup, with waveform measurement capabilities.

crowave transition analyzer (MTA) is used as a nonlinear receiver, measuring the phase relationships between harmonics of the signals at the device-under-test (DUT) ports. The setup is completed with two independently controlled active loops (more loops could be added). The loops can be set at the input or output of the device, and tuned both for single tone and harmonic measurements. A simplified scheme of the test bench is shown in Fig. 1.

The linear and nonlinear receivers are simply combined by means of two power splitters. In other words, the two receivers work in parallel on the same DUT. The information achievable with this system are, therefore: 1) input and output reflection coefficients, at fundamental and harmonics; 2) source reflection coefficient ("port 1–port 2 source switch" allows an RF switching technique [8]), at fundamental and harmonics; 3) input and output power, at fundamental and harmonics; 4) input and output time-domain waveforms; 5) power-added efficiency; and 6) IM products.

This is a more effective (but also more expensive) technique if compared to other similar systems [10], where only an MTA is used as a receiver: the flexibility, accuracy, and speed of a real-time load–pull and S-parameter test set is combined with the additional waveform information provided by the MTA. Indeed, after the calibration phase, the slower MTA measurements are performed only if and when needed. The quantities of interest and performances are measured with higher speed and accuracy with the VNA. Moreover, the simultaneous presence of the two receivers allows simple verification capabilities of both time/frequency-domain measurements.

The general calibration procedure, not described in detail before, is an extension of the on-wafer techniques described in [16] and [17] and improved for the coaxial MTA-based system in [10]. During calibration, the "port1–port2 source switch" is connected, as in Fig. 1, in cascade to "power splitter 1," but its ways are connected at the input and output of the DUT, excluding the two bias Ts. Thus, S-parameter calibration of the system is performed by inserting the proper standards at "port 1" and "port 2" [with any two-port technique, e.g., thru-relect line (TRL), line-reflect match (LRM)].

Let us call [18] $a_{m1}^{(i)V}, b_{m1}^{(i)V}, a_{m2}^{(i)V}, b_{m2}^{(i)V}$ and $a_{m1}^{(i)M}, b_{m1}^{(i)M}, a_{m2}^{(i)M}, b_{m2}^{(i)M}$ the raw measurements at the ith frequency (f_i) obtained, respectively, with the VNA and MTA. We write the error boxes for VNA and MTA measurements

$$\begin{pmatrix} a_{1/2}^{(i)} \\ b_{1/2}^{(i)} \end{pmatrix} = \boldsymbol{X}_{\mathbf{1/2}}^{(i)V/M} \begin{pmatrix} a_{m1/2}^{(i)V/M} \\ b_{m1/2}^{(i)V/M} \end{pmatrix} \tag{1}$$

$$\begin{pmatrix} a_{3}^{(i)} \\ b_{3}^{(i)} \end{pmatrix} = \boldsymbol{X}_{\mathbf{3}}^{(i)V/M} \begin{pmatrix} a_{m2}^{(i)V/M} \\ b_{m2}^{(i)V/M} \end{pmatrix} \tag{2}$$

$$\begin{aligned} \boldsymbol{X}_{\boldsymbol{j}}^{(i)V/M} &= K_{jj}^{(i)V/M} \boldsymbol{Y}_{\boldsymbol{j}}^{(i)V/M} \\ &= K_{jj}^{(i)V/M} \begin{pmatrix} -\mathcal{H}_{jj}^{(i)V/M} & \mathcal{L}_{jj}^{(i)V/M} \\ -\mathcal{M}_{jj}^{(i)V/M} & 1 \end{pmatrix} \end{aligned} \tag{3}$$

where $j = 1, 2,$ and 3.

After the two calibration procedures with the VNA and MTA, the coefficients of $\boldsymbol{Y}_{\boldsymbol{j}}^{(i)V/M}$ and the quantities

$$\alpha^{(i)V/M} = K_{11}^{(i)V/M} \cdot K_{22}^{(i)V/M} \tag{4}$$

are known.

In order to compute power waves at the DUT reference plane, the magnitudes and phases of each $K_{jj}^{(i)V/M}$ must be calculated.

To obtain the magnitudes, we follow the procedure for on-wafer power level calibration described in [16], exploiting coaxial port ("port 3"). This auxiliary port is connected to a power meter and to three coaxial standards.

The phases of $K_{jj}^{(i)V/M}$ now need to be determined.

Let us define the scattering matrix of the network linking ports 2 and 3 as

$$\begin{pmatrix} a_2^{(i)} \\ b_3^{(i)} \end{pmatrix} = \begin{pmatrix} S_{11}^{(i)} & S_{12}^{(i)} \\ S_{21}^{(i)} & S_{22}^{(i)} \end{pmatrix} \begin{pmatrix} b_2^{(i)} \\ a_3^{(i)} \end{pmatrix}. \tag{5}$$

After one-port and power calibration at port 3 (with a VNA), performed with a generic device (e.g., a thru) connected between ports 1 and 2, the quantities $S_{11}^{(i)}, S_{22}^{(i)}$ and $S_{12}^{(i)} \cdot S_{21}^{(i)}$ are known.

Since the connection between ports 2 and 3 is realized with directional couplers and cables, we can write $S_{12}^{(i)} = S_{21}^{(i)}$. The phase indetermination is solved on the basis of a linear group-delay approximation $S_{12}^{(i)} = \tau f_i$. Now the matrix of the network connecting ports 2 and 3 is completely characterized.

The phase information at the MTA "test" port must be transferred to the VNA and MTA error boxes. This is achieved performing an additional direct connection of the MTA "test" port to port 3, while a thru device is connected between ports 1 and 2, and measuring with both the MTA and VNA. In this situation,

$$b_2^{(i)}\Big|_{\mathrm{MTA}\,p3} = a_t^{(i)M}\Big|_{\mathrm{MTA}\,p3} \frac{1 - S_{22}^{(i)}\Gamma_{\mathrm{MTA}}^{(i)}}{S_{21}^{(i)}} \tag{6}$$

where $\Gamma_{\mathrm{MTA}}^{(i)}$ is the reflection coefficient of the MTA "test" port and $a_t^{(i)M}|_{\mathrm{MTA}\,p3}$ is the MTA measurement.

The reflection coefficient $\Gamma_{\mathrm{MTA}}^{(i)}$ is computed from the corrected VNA measurement when the MTA is connected at port 3 from the following:

$$\frac{a_2^{(i)}}{b_2^{(i)}} = S_{11}^{(i)} + \frac{S_{12}^{(i)} S_{21}^{(i)}}{1 - S_{22}^{(i)}\Gamma_{\mathrm{MTA}}^{(i)}}. \tag{7}$$

Now, from the VNA raw measurements performed when the MTA is connected at port 3,

$$b_2^{(i)}\Big|_{\mathrm{MTA}\,p3} = K_{22}^{(i)V}\left(-\mathcal{M}_{22}^{(i)V}\, a_{m2}^{(i)V}\Big|_{\mathrm{MTA}\,p3} + b_{m2}^{(i)V}\Big|_{\mathrm{MTA}\,p3}\right). \tag{8}$$

Combining (6) and (8), we obtain an expression for $K_{22}^{(i)V}$.

The MTA error coefficients phases $K_{22}^{(i)M}$ are then computed by calculating the quantity $b_2^{(i)}$ in the following two ways:

- with the new VNA error coefficients;
- with the MTA error coefficients

when a 50-Ω load is connected at port 3.

To translate this to formulas, we combine the following two equations, coming from the measurements with the MTA and VNA with $k = M$ and $k = V$, respectively:

$$b_2^{(i)}\Big|_{50\ \Omega p3} = K_{22}^{(i)k}\left(-\mathcal{M}_{22}^{(i)k}\, a_{m2}^{(i)k}\Big|_{50\ \Omega p3} + b_{m2}^{(i)k}\Big|_{50\ \Omega p3}\right), \quad k = M, V. \tag{9}$$

Finally, since $\alpha^{(i)V/M} = K_{11}^{(i)V/M} \cdot K_{22}^{(i)V/M}$ is known, $K_{11}^{(i)V/M}$ are now also fully known.

In conclusion, let us resume the absolute phase and power calibration of the proposed VNA–MTA setup. The calibration algorithm goes through the following steps.

Step 1) Two-port calibration (e.g., LRM, TRL, etc.) at ports 1 and 2 with the VNA ("sampler 1–2").

Step 2) Two-port calibration at ports 1 and 2 with the MTA.

Step 3) Power calibration exploiting port 3 (three standards plus power meter) for the MTA and VNA.

Step 4) Phase calibration exploiting port 3 (direct connection to the MTA) computing the following:

- $\angle S_{12}^{(i)}$;
- $\Gamma_{\mathrm{MTA}}^{(i)}$;
- $b_2^{(i)}$ when the MTA is connected at port 3;
- phase-corrected VNA error coefficients;
- $b_2^{(i)}$ from the new VNA coefficients when 50 Ω is connected at port 3;
- $b_2^{(i)}$ from MTA coefficients when 50 Ω is connected at port 3;
- phase-corrected MTA error coefficients.

The operating procedure, i.e., standard connection sequence, corresponding to this algorithm is anyway rather simple and fast as follows:

- standard connections (any two-port calibration can be applied) at ports 1 and 2, if possible ending the sequence with a thru device;
- thru between ports 1 and 2, with port 3 connected to: 1) three coaxial standards; 2) a power meter; and 3) the MTA.

III. Harmonic Tuning Approach

Starting from simple power balance considerations, the drain efficiency η of a PA can be expressed as [12]

$$\eta = \frac{P_{\mathrm{out},f}}{P_{\mathrm{diss}} + P_{\mathrm{out},f} + \sum_{n>1}^{\infty} P_{\mathrm{out},nf}} \tag{10}$$

where

$$P_{\mathrm{diss}} = \frac{1}{T}\int_0^T v_{\mathrm{ds}}(t) \cdot i_d(t)\,\mathrm{d}t \tag{11}$$

is the dissipated power on the active device, with $v_{\mathrm{ds}}(t)$ and $i_d(t)$ being the drain voltage and current waveforms, and

$$P_{\mathrm{out},nf} = \frac{1}{2} V_n I_n \cos(\phi_n), \qquad n = 1, 2, \ldots \tag{12}$$

the active power delivered from the device to the output matching network at fundamental f ($P_{\mathrm{out},f}$) and harmonic frequencies nf ($P_{\mathrm{out},nf}, n > 1$). V_n and I_n are the voltage and current amplitude harmonic components and ϕ_n are their phase shift, i.e., the phase of the output harmonic terminations

$$Z_{L,n} = \frac{V_n}{I_n} e^{j\phi_n}. \tag{13}$$

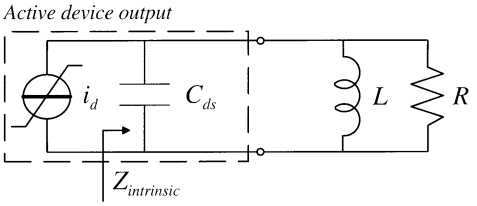

Fig. 2. Simplified active device output model.

TABLE I
HARMONIC TUNED PA DESIGN PARAMETERS FOR (16)

Controlled frequencies	k_2	k_3	δ
f (Tuned Load)	0	0	1
f, $3f$ (Class F)	0	−0.17	1.15
f, $2f$	−0.35	0	1.41
f, $2f$, $3f$	−0.55	0.17	1.62

From (10), it follows that maximum drain efficiency η is achieved if one of the following conditions is fulfilled:

$$c_1 \rightarrow \text{fundamental output power } P_{\text{out},f} \text{ is maximized or} \tag{14a}$$

$$c_2 \rightarrow \text{the sum of } P_{\text{diss}} \text{ and } P_{\text{out},nf} \text{ for } n > 1 \text{ (i.e., } P_{\text{loss}}\text{) is minimized.} \tag{14b}$$

All the harmonic tuning PA design approaches are recognized to follow one of the above conditions. Moreover, the relevance of both the input and output harmonic impedances has been evidenced. In particular, for the output intrinsic harmonic impedances, closed-form expressions are inferred under particular operating conditions, i.e., ideal cases (class F [19], [20] and class E [21], [22]) or assuming short-circuit impedances at highest harmonic frequencies [12].

In the last cases, assuming a MESFET device with a simplified output model, as depicted in Fig. 2, the voltage-controlled current source i_d is described by

$$i_d(t) = I_0 + \sum_{n=1}^{\infty} I_n \cdot \cos(n \cdot 2\pi f \cdot t) \tag{15}$$

and the intrinsic drain impedances $Z_{\text{intrinsic}}$ must be purely resistive (R_{HM}), and their values are expressed by

$$R_{\text{HM},f} = \delta \cdot R_{\text{TL}}$$
$$R_{\text{HM},nf} = \delta \cdot k_n \frac{I_1}{I_n} \cdot R_{\text{TL}}, \qquad n = 2, 3, \ldots \tag{16}$$

where R_{TL} is the optimum fundamental load resistor for a tuned load (TL) approach [23], and δ and k_n $(n = 2, 3)$ are optimum design values, which are summarized in Table I.

From (16), harmonic tuning approaches can be exploited only if positive values for $R_{\text{HM},nf}$ are obtained. This implies that current harmonic components I_2 and I_3 have to be in a proper phase relationships with respect to I_1.

Such phase relationships can be controlled in two ways: choosing a proper input driving waveform or exploiting input nonlinearity phenomena. Usually the former solution is less practical than the latter. Unfortunately, no closed-form expressions can be easily derived for input harmonic impedances, thus only qualitative considerations can be theoretically performed [12].

In more general cases, however, useful statements can be inferred from (14) and results arising from (16); in particular, if a harmonic tuning strategy is adopted, then the fundamental output load resistive part has to be increased with respect to the value obtained without harmonic manipulation.

In Section IV, an experimental validation of theoretical considerations on harmonic manipulation PA design criteria will be provided, stressing both the input impedance at $2f$ relevance and the further benefit arising from the output fundamental load resistive part increase after the input tuning.

IV. EXPERIMENTAL VALIDATION

The device used is a medium-power MESFET ($10 \times 100\ \mu$m) by Alenia Marconi Systems (AMS), Rome, Italy, which has been separately modeled by a full nonlinear model employing neural-network concepts [24]. The device knee voltage is $V_k = 0.9$ V and its maximum intrinsic drain current is $I_{\max} = 220$ mA. A drain-bias voltage of 5 V has been selected, while the gate-bias voltage has been chosen at -2 V, corresponding to an intrinsic dc drain current $I_{\text{DC}} \simeq 40$ mA. In the experiment, $f = 1$ GHz has been chosen as the fundamental frequency.

To perform a multiharmonic load–pull, the test set depicted in Fig. 1 has been adopted, in which one active loop should be added to control each harmonic termination.

To reduce test-bench cost and complexity, only two active loops (AL_{IN} and AL_{OUT}) have been adopted, respectively, for the input and output loads, thus controlling a single harmonic impedance at a time. In particular, AL_{OUT} has been used to control the fundamental output impedance, thus performing traditional load–pull; conversely, AL_{IN} has been used to perform source–pull at the second harmonic.

The remaining harmonic impedances were not tuned, but have been measured up to 5 GHz, resulting in almost matched terminations (i.e., 50 Ω). The actual input (Z_S) and output (Z_L) active device terminations are then

$$Z_{S,nf} = \begin{cases} \text{tuned } (Z_{S,2f}), & \text{for } n = 2 \\ \simeq 50\,\Omega, & n \in N, n \neq 2 \end{cases} \tag{17}$$

$$Z_{L,nf} = \begin{cases} \text{tuned } (Z_{L,f}), & \text{for } n = 1 \\ \simeq 50\,\Omega, & n > 1. \end{cases} \tag{18}$$

The proposed measurement procedure can be summarized in the following steps.

Step 1) Perform a load–pull on Z_{Lf} to find the optimum load at the output port.

Step 2) Perform a source–pull on $Z_{S,2f}$ to analyze the effects of the load at the input port at the second harmonic.

Step 3) Perform a load–pull on $Z_{L,f}$ again to demonstrate that further increases on device performances can be obtained.

If the load–pull test set has harmonic tuning capabilities, only the first two steps are usually performed, thus neglecting the

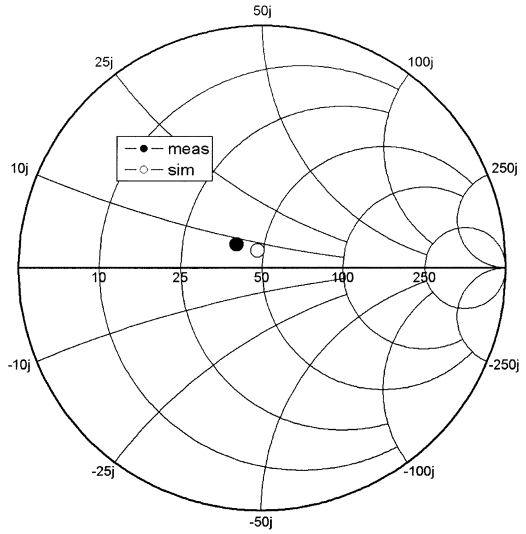

Fig. 3. Measured (filled) and simulated (unfilled) fundamental output load.

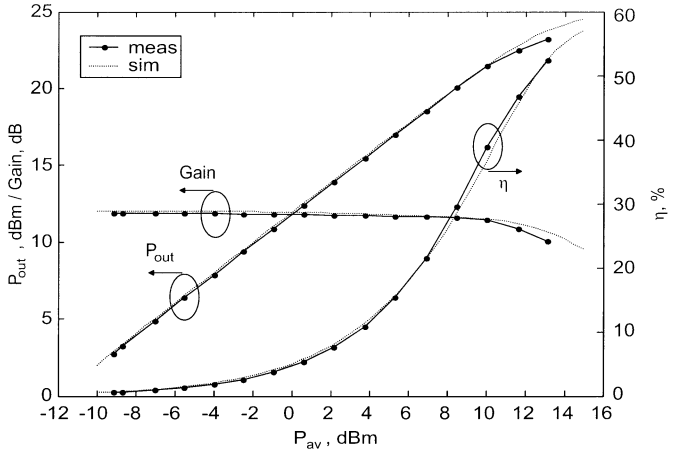

Fig. 4. Single-tone measured performances (dotted lines) compared with simulation results (solid lines) at 1 GHz.

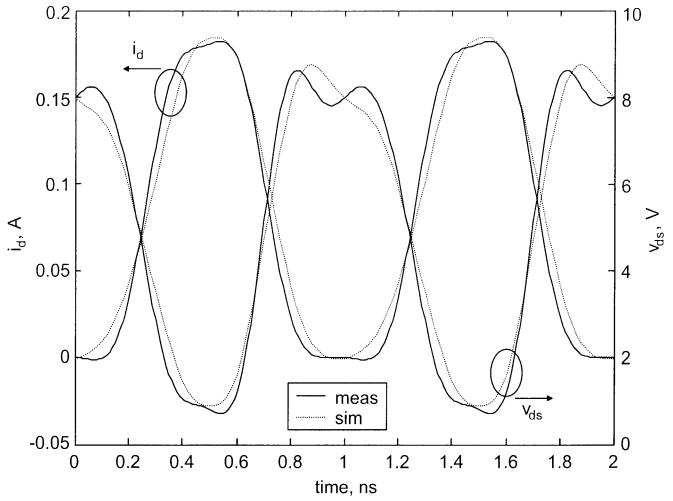

Fig. 5. Measured (solid lines) versus simulated (dotted lines) time-domain waveforms for voltage and current at 1-dB compression.

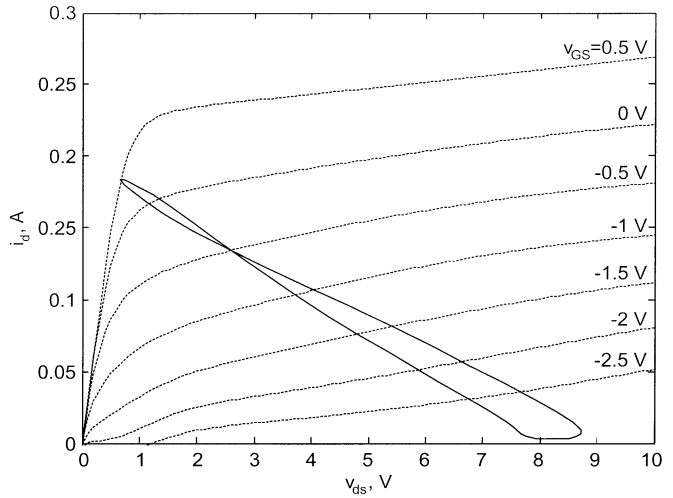

Fig. 6. Simulated intrinsic load curve.

benefits arising from the third one, as will be shown in the following.

A. Load–Pull on $Z_{L,f}$

The first step is a traditional load–pull on output termination at fundamental frequency to obtain the optimum load $Z_{L,f}$. To further reduce time effort, a starting point for $Z_{L,f}$ is estimated by means of simplified considerations inferred through a linearized active device model [23], [25]. After that, on the test bench, $Z_{L,f}$ values are tuned, changing the attenuation and phase shift of the fundamental output active loop $\mathrm{AL_{OUT}}$, thus mapping the Smith chart around the starting point until an optimum is obtained. In this experiment, the optimum output load value $Z_{L,f} = 40.0 + 6.3j$ has been determined and a comparison between simulated and measured optimum fundamental output load is reported in Fig. 3.

Output power at fundamental frequency, drain efficiency, and gain measurements and simulations are depicted in Fig. 4 versus available input power (P_{av}), while drain current and voltage waveforms (at 1-dB compression) measurements and simulations are plotted in Fig. 5. The nonlinear simulation, both for time-domain and single-tone measurements, were achieved with a commercial computer-aided design (CAD) tool, using a homemade nonlinear model, and they are in good agreement with measurements.

Moreover, from simulation results, it is possible to note (Fig. 6) that the load curve at the intrinsic device terminals is very narrow, showing that the output intrinsic value must be purely resistive [23].

B. Source–Pull on $Z_{S,2f}$

The second step of the procedure is a source–pull, in order to investigate the effects of the input second harmonic termination $Z_{S,2f}$ [12]. For this purpose, a fixed input drive level has been assumed, corresponding to 1-dB output compression ($P_{\mathrm{av}} \simeq 11.5$ dBm in the experiment), and all the possible (passive) values for $Z_{S,2f}$ have been investigated, leaving fundamental termination at the value of the prior step.

Measured contour plot of drain efficiency as a function of $Z_{S,2f}$ is shown in Fig. 7.

The efficiency clearly exhibits maximum and minimum points, in the following, referred to as case 1 and case 2. Output

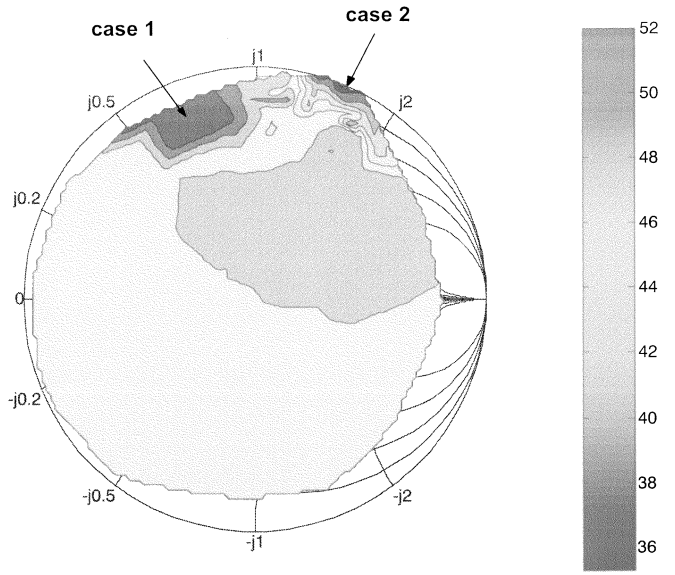

Fig. 7. Measured contour plot of drain efficiency versus $Z_{S,2f}$.

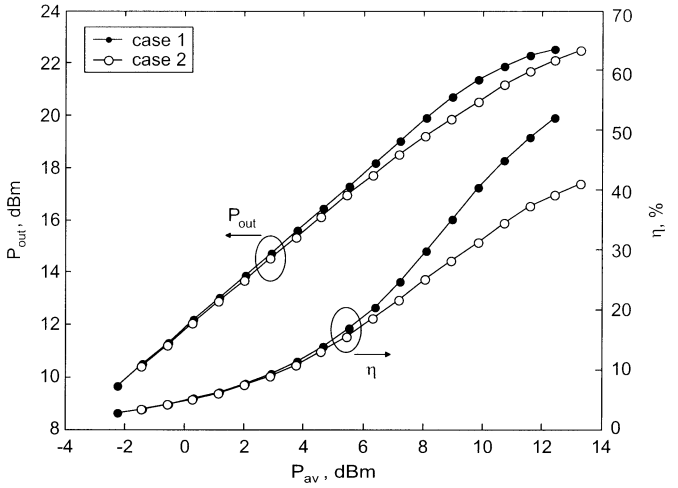

Fig. 8. Measured output power and efficiency for case 1 and case 2.

power and efficiency measurements obtained in both cases are shown in Fig. 8 as a function of available input power, while the corresponding measured output voltage and current waveforms (at 1-dB compression) are reported in Fig. 9.

From this figure, different second harmonic components, due to different input harmonic generation, can be noted. In particular, in case 1, voltage and current waveforms are flattened, resulting in lower dissipation on the device, even if the power delivered at the second harmonic is higher than in case 2.

Simulated values of $P_{\rm diss}$ (11) and $\sum_{n>1}^{\infty} P_{{\rm out},nf}$ (12) are reported in Fig. 10. The active power delivered to the output load at harmonic frequencies is higher in case 1 compared to case 2. However, the power dissipated in the active device is lower and the total

$$P_{\rm loss} = P_{\rm diss} + \sum_{n>1}^{\infty} P_{{\rm out},nf} \tag{19}$$

is minimized according to (14b).

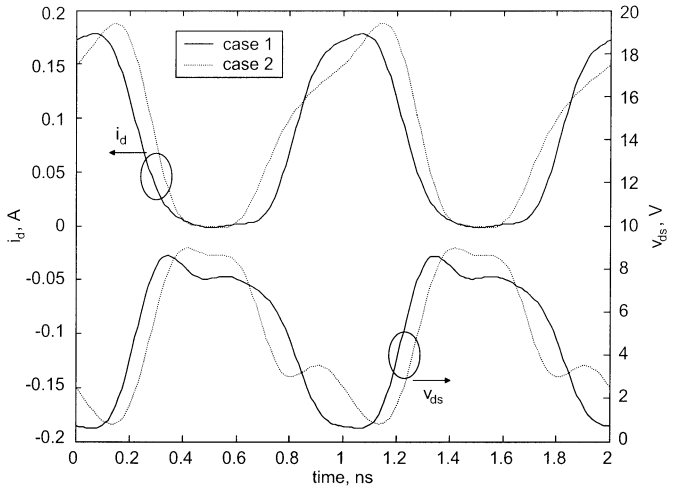

Fig. 9. Output voltage and current waveforms corresponding to case 1 and case 2.

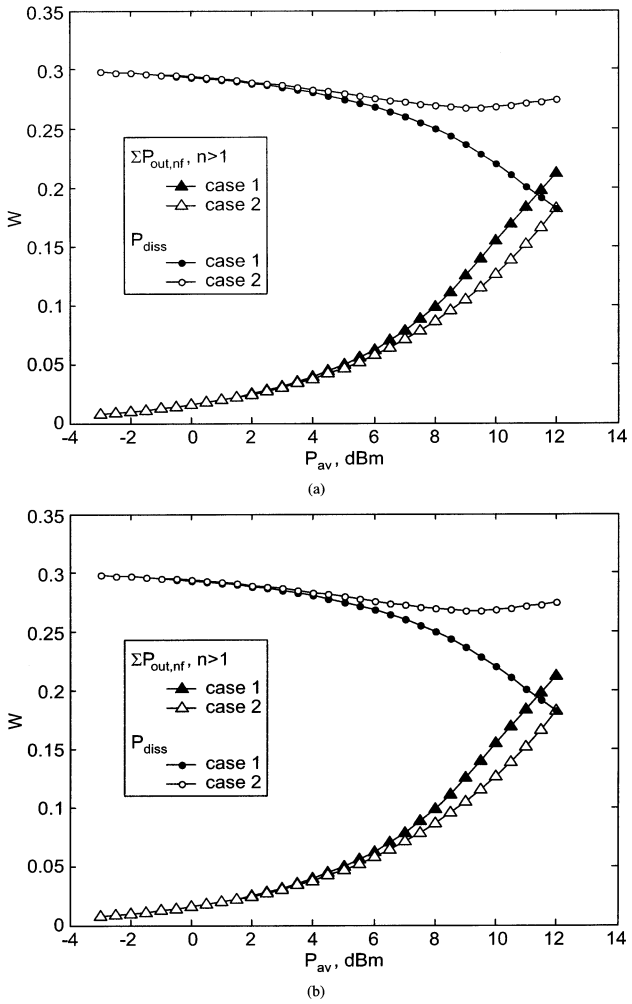

Fig. 10. (a) Dissipated power and power delivered at harmonic frequencies. (b) Total power loss (19) simulated as a function of available input power.

C. Load–Pull on $Z_{L,f}$ Again

To show that further improvements can be obtained increasing the fundamental output load resistive part, according to (16) [12], a load–pull has been again performed, leaving

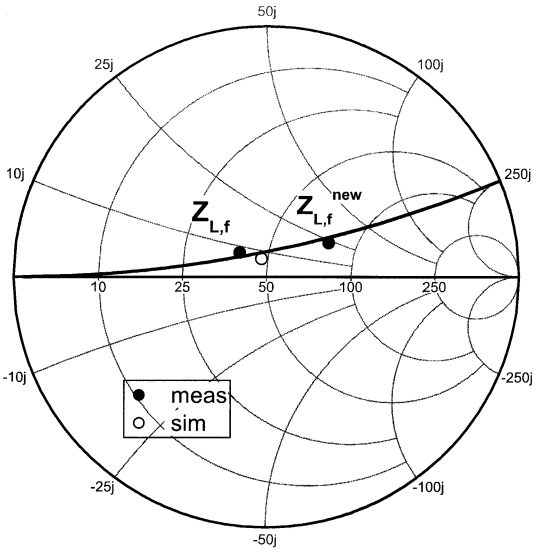

Fig. 11. Initial ($Z_{L,f}$) and final ($Z_{L,f}^{\rm new}$) optimum output load at fundamental.

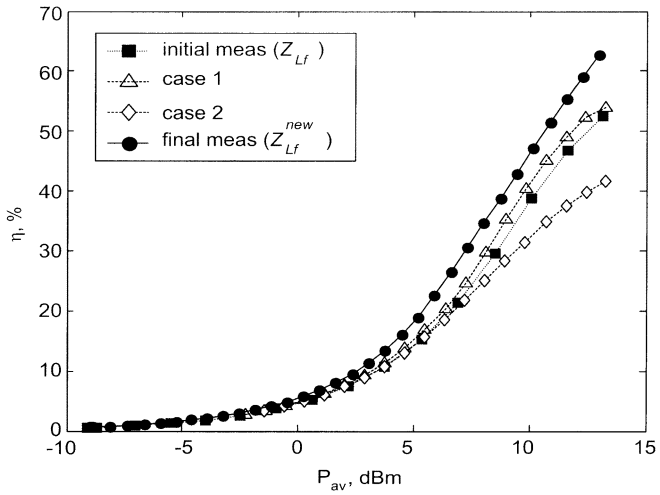

Fig. 12. Efficiency performances measured during the three-step experiment.

second harmonic source termination unchanged from the previous case. The final optimum output load (namely, $Z_{L,f}^{\rm new}$) is shown in Fig. 11. The new output fundamental load has moved on a constant susceptance ($Y_S \simeq -0.004j$) curve, while its resistance value is increased. This is in agreement with the assumption that the active device output behavior can be modeled with a current source i_d with a parallel capacitor ($C_{\rm ds}$), as depicted in Fig. 2.

The obtained drain efficiency, compared with the previous cases, is shown in Fig. 12, while the drain efficiencies measured at a fixed input available power $P_{\rm av} \simeq 11.5$ dBm are summarized in Table II.

The efficiency level at 1-dB compression exhibits an increase from 49% (obtained at step 2) to 55%, i.e., a relative increase with respect to the initial efficiency value (46%) of approximately 13%.

Finally, the $\rm IM_3$ (tone spacing $\Delta f = 100$ kHz) performances obtained during the three steps of the experiment are reported and compared in Fig. 13. From the obtained results, it can be noted that $Z_{S,2f}$ also affects the device IM distortion. This result

TABLE II
DRAIN EFFICIENCY MEASURED FOR A FIXED INPUT AVAILABLE POWER $P_{\rm av} \simeq 11.5$ dBm

$P_{av} \simeq 11.5$ dBm	η	$\Delta\eta/\eta_{initial}$
Initial	46%	/
Case 1	49%	+6.5%
Case 2	37%	-19.5%
Final	55%	+19.5%

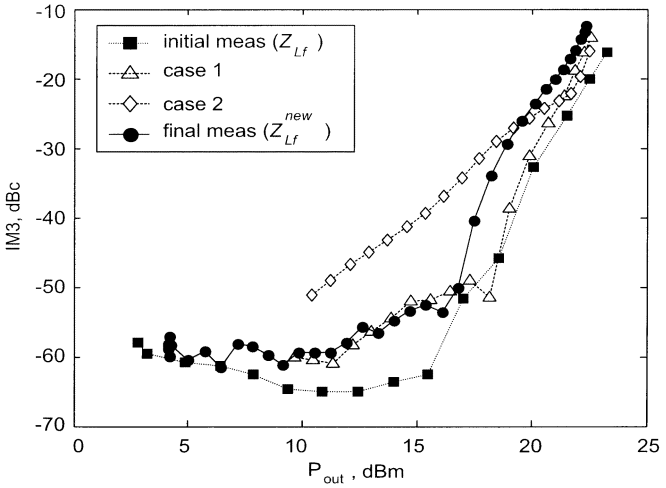

Fig. 13. Intermodulation performances measured during the three-step experiment.

was already demonstrated to be a typical effect of the harmonic manipulation procedure [3]. Moreover, the improvement on the $\rm IM_3$, related to second harmonic input termination, was stressed in [26]. Under small-signal excitation, case 2 is the worst condition, due to the highest $\rm IM_3$ levels. On the other hand, under large-signal excitation, the final case exhibits a higher $\rm IM_3$ value due to the highest output resistive load. In fact, in this case, device physical limitations and, in particular, ohmic region, are reached for lower output power levels.

V. CONCLUSION

A simplified theoretical approach to clarify the relevance of active device harmonic terminations, both at the input and output ports, has been presented, suggesting design criteria to improve efficiency for high-frequency PAs. To validate theoretical considerations and to provide a suitable measurement optimization procedure, an advanced harmonic load/source–pull bench and its calibration procedure have been presented. The proposed measurement bench has been used to investigate the effects of second harmonic (2 GHz) input and fundamental (1 GHz) output terminations on a 1-mm power MESFET device. In particular, a drain efficiency spread between 37%–49% for a fixed input power level, corresponding to a 1-dB compression point, has been experimentally observed, varying second harmonic input termination. Further improvements have been obtained by increasing the fundamental output load resistive part after input second harmonic tuning, thus reaching a drain efficiency value of 55% at 1-dB compression.

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