Parametric Macromodels of Differential Drivers and Receivers

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Igor S. Stievano, *Member, IEEE*, Ivan A. Maio, *Member, IEEE*, Flavio G. Canavero, *Senior Member, IEEE*, and Claudio Siviero

***Abstract*—This paper addresses the modeling of differential drivers and receivers for the analog simulation of high-speed interconnection systems. The proposed models are based on mathematical expressions, whose parameters can be estimated from the transient responses of the modeled devices. The advantages of this macromodeling approach are: improved accuracy with respect to models based on simplified equivalent circuits of devices; improved numerical efficiency with respect to detailed transistor-level models of devices; hiding of the internal structure of devices; straightforward circuit interpretation; or implementations in analog mixed-signal simulators. The proposed methodology is demonstrated on example devices and is applied to the prediction of transient waveforms and eye diagrams of a typical low-voltage differential signaling (LVDS) data link.**

***Index Terms*—Circuit modeling, digital integrated circuits, electromagnetic compatibility, low-voltage differential signaling (LVDS), macromodeling, signal integrity, system identification.**

I. Introduction

THE demand coming from telecommunication and information technology applications for moving more data, faster, and with less power, has been the driving force for the development of the low-voltage differential signaling (LVDS) standard [1]–[3]. LVDS uses high-speed analog circuit techniques to provide multigigabit data transfers on copper interconnects and has proven advantages of cost, low power consumption, and noise control. In order to simulate the operation of LVDS links for the assessment of signal integrity (SI) and electromagnetic compatibility (EMC) problems, suitable behavioral models (or macromodels) of differential drivers and receivers are needed. The macromodels must be efficient and accurate enough to handle the complexity of actual simulation problems and to yield reliable predictions of reflections and sensitive effects like crosstalk or radiation.

A common approach to the modeling of devices is via simplified equivalent circuit representations, in which the information on the internal structure of the device is used to derive a simplified equivalent circuit. The equivalent circuit is composed of various blocks, accounting for a specific static or dynamic effect. A well-known example of this structure is provided by the input/output buffer information specification (IBIS) [4], that has been established as a standard for the ports description of a digital integrated circuit (IC), leading to a large availability of device descriptions and commercial tools handling models based on IBIS. Recent advances on the IBIS modeling of differential drivers can be found in [5]–[7].

The growing complexity of recent devices and their enhanced features like pre-emphasis and specific control circuitry, however, demands for refinements of the basic equivalent circuits. In order to facilitate the modeling of these features, this paper proposes a modeling alternative based on equations and circuit theory, aimed at reproducing the electrical behavior of device ports, without any use of physical insights and of equivalent circuit representations. The advantage of this approach relies in the flexibility of the mathematical description with respect to the circuit representation. In particular, the parasitic effects and some of the exotic effects inherent to the nonlinearity of devices are difficult to capture if we have at our disposal only capacitors, inductors, and resistors (even if nonlinear). On the contrary, equations allow us to better fit the complex behavior of components. Besides, the proposed equation-based macromodels can be easily converted into circuit equivalents and implemented as SPICE-like subcircuits to be used in any SPICE-type simulator or can be directly plugged into commercial simulators accepting direct equation descriptions of macromodels like Verilog-AMS or VHDL-AMS.

The paper is organized as follows. Section II introduces the proposed macromodels for differential drivers and receivers and provides the details of the procedure for their estimation. Section III discusses possible implementations of macromodels. Section IV shows modeling examples for two different drivers and a receiver of interest. Finally, Section V discusses the application of the proposed modeling procedure to the prediction of transient waveforms and eye diagrams on a complete high-speed differential link.

II. LVDS Device Macromodels

This section describes the macromodels proposed for differential drivers and receivers, and discusses the estimation of their parameters. This paper is a better systematic presentation and an extension of the macromodeling technique via parametric identification, originally presented in [8].

A. Drivers

The output buffers of LVDS drivers operate via current-steering techniques, as shown in Fig. 1. Two voltage-controlled current sources are used to provide the current sent to and drawn from resistor R_r at receiver input terminals. When the

Manuscript received August 23, 2004; revised November 29, 2004. This work was supported in part by the Italian Ministry of University (MIUR) under a Program for the Development of Research of National Interest (PRIN Grant #2002093437) and by CERCOM, Center for Multimedia Radio Communications of the Electronics Department, Politecnico di Torino.

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Digital Object Identifier 10.1109/TADVP.2005.846931

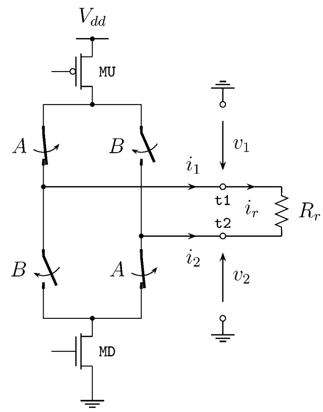

Fig. 1. Generic structure of a LVDS driver and its relevant electric variables.

switches denoted by A are closed, the current i_r is positive; on the contrary, when switches A are open and B closed, current i_r is negative and the voltage across receiver input terminals changes polarity. In actual applications, output buffers may contain matching resistors across the output terminals and control circuits to ensure proper output current and voltage values over possible variations of the technological process, supply voltage, and temperature (e.g., see [9]–[11] for possible implementations of control circuits).

In a fixed logic state, the ideal LVDS output buffer of Fig. 1 can be considered as a circuit element of terminals t1, t2, and ground and characterized by constitutive relations of the form

$$\begin{cases} i_1 = i_{1H}(v_1, v_2) \\ i_2 = i_{2H}(v_1, v_2) \end{cases} \begin{cases} i_1 = i_{1L}(v_1, v_2) \\ i_2 = i_{2L}(v_1, v_2) \end{cases} \tag{1}$$

where subscripts H and L denote the HIGH and LOW logic state, respectively, and the output currents are allowed to be functions of both terminal voltages, in order to take into account variants of the buffer basic scheme with internal resistor and control circuits. As an alternative, the above relations can be expressed in terms of different variables obtained as linear combinations of port voltages v_1 and v_2. A typical set of alternative variables are the common mode voltage $v_c = ((v_1 + v_2)/2)$ and the differential voltage $v_d = (v_1 - v_2)$.

A complete macromodel describing state switching from steady state operation can be obtained by considering relations (1) as partial models (hereafter submodels) holding in the two logic states, and by combining them by means of time-varying weighting coefficients, as already proposed in [8], [12]. The resulting two-piece model writes

$$\begin{cases} i_1 = w_{1H}(t) i_{1H}(v_1, v_2) + w_{1L}(t) i_{1L}(v_1, v_2) \\ i_2 = w_{2H}(t) i_{2H}(v_1, v_2) + w_{2L}(t) i_{2L}(v_1, v_2) \end{cases} \tag{2}$$

where w_{nH} and w_{nL}, $n = 1, 2$ are the weighting coefficients accounting for the switching of submodels, i.e., for logic state transitions. Model representation (2) approximates the external device behavior including the information on state transitions without any assumptions on the device internal structure. The generation of model (2) for a given device amounts to devising suitable parametric relations for submodels i_{nH} and i_{nL}, to estimating their parameters and finally to determining the weighting coefficients w_{nH} and w_{nL}. These steps are discussed below.

Simple parametric relations for submodels i_{nH} and i_{nL} can be obtained by summing a static mapping and a (possibly nonlinear) relation taking into account dynamic effects, as discussed in [13]. As an example, for $i_{nH}(v_1, v_2)$ we adopt the following representation:

$$\begin{cases} i_{1H}(v_1, v_2) = \hat{\imath}_{1H}(v_1, v_2) + \bar{\imath}_{1H}\left(v_1, v_2, \frac{d}{dt}\right) \\ i_{2H}(v_1, v_2) = \hat{\imath}_{2H}(v_1, v_2) + \bar{\imath}_{2H}\left(v_1, v_2, \frac{d}{dt}\right) \end{cases} \tag{3}$$

where $\hat{\imath}_{1H}$ and $\hat{\imath}_{2H}$ are the static characteristics of currents i_1 and i_2 for the driver forced in the fixed HIGH logic state, and $\bar{\imath}_{1H}$ and $\bar{\imath}_{2H}$ are the dynamic parts of submodels. Similar equations hold for $i_{nL}(v_1, v_2)$ of (2). Equation (3), and their corresponding form for the LOW state, approximate the port constitutive relation in fixed logic state, including both static and dynamic coupling effects between the terminal variables. The dynamic parts of submodels, accounted for by $\bar{\imath}_{nH}$ and $\bar{\imath}_{nL}$ terms, can be effectively represented by nonlinear parametric relations, assuming the form of discrete-time models involving the present and past samples of input and output variables. As an example, submodel $\bar{\imath}_{1H}(v_1, v_2, d/dt)$ in (3) becomes

$$\bar{\imath}_{1H}(k) = f(\bar{\imath}_{1H}(k-1), \ldots, v_1(k), v_1(k-1), \ldots, v_2(k), \ldots) \tag{4}$$

where k is discrete-time and f is a parametrized nonlinear mapping. A complete review of possible relations as well as of the methods for estimating their parameters can be found in [14]. Finally, for devices having a dynamic behavior dominated by linear effects, (4) can be replaced by

$$\begin{aligned} \bar{\imath}_{1H}(k) = & \alpha_{01}\bar{\imath}_{1H}(k-1) + \cdots \\ & + \alpha_{10} v_1(k) + \alpha_{11} v_1(k-1) \\ & + \cdots + \alpha_{20} v_2(k) + \cdots \end{aligned} \tag{5}$$

where α_{ij} are the parameters of the equation [15]. In some cases, even simpler linear capacitive models, as discussed in [8], may be used.

The parameters of submodels (3) can be obtained by fitting their responses to so-called estimation signals, that are the responses of the device to be modeled. The estimation signals of a differential driver can be obtained by exciting its output terminals with suitable voltage waveforms, as illustrated by the conceptual setup of Fig. 2. The static parts of the submodels are simply represented by the output terminal currents arising from dc analyses at fixed logic state. Of course, the terminal voltage swings applied by test sources should correspond to differential and common mode voltage variations within the limits specified by the LVDS standard. Estimation signals for dynamic parts, instead, are obtained by recording $i_1(t)$ and $i_2(t)$ when the driver is in fixed logic state and the voltage sources of Fig. 2 apply staircase waveforms with wide random steps for the case of nonlinear parametric models or white noisy signals or pseudorandom bit sequences for the case of linear parametric models. The parameter values are derived by fitting (4) and (5) to the sampled estimation signals (e.g., $i_1(k) = i_1(kT)$, T being the sampling period) collected from the devices to be modeled. Algorithms and tools for this fitting are available from the *System Identification* literature (e.g., see [16] for the estimation of linear

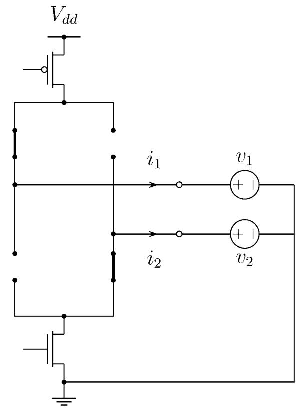

Fig. 2. Common setup for the estimation of the static characteristics and of the dynamic behavior of the LVDS device (see Fig. 1) in the HIGH logic state.

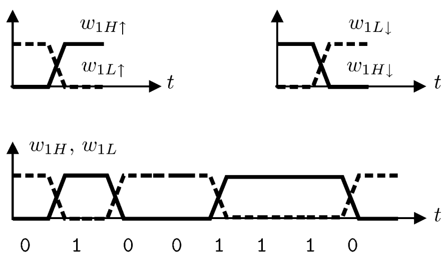

Fig. 3. Example of elementary weighting coefficient $w_{1H\uparrow}$ and $w_{1L\uparrow}$ for the up state transition and $w_{1H\downarrow}$ and $w_{1L\downarrow}$ for the down state transition (top panel). Weighting coefficients w_{1H} and w_{1L} corresponding to the bit pattern "01001110" are obtained as juxtaposition of the elementary weighting coefficients in the bottom panel.

dynamic models and [19], [20] for the estimation of nonlinear dynamic models).

The estimation of the weighting coefficients w_{nH} and w_{nL} starts once submodels i_{nH} and i_{nL} are completely defined. The weighting coefficients of single up (01) and down (10) state transitions are computed first, via linear inversion of (2), from voltage and current waveforms recorded during such state transitions. Then, for a specific logic activity of the device (e.g., a bit stream "01001110..."), the weighting coefficients are obtained by juxtaposition of the proper weighting coefficients of single up and down transitions, as illustrated in Fig. 3. Details on the concatenation of weighting coefficients as well as on their estimation can be found in [12], where a similar two-piece model representation is exploited for the case of single-ended CMOS devices.

B. Receivers

The basic structure of the input stage of a differential receiver is shown in Fig. 4. In principle, it consists of a purely differential circuit converting the received port voltage (i.e., the differential voltage between input terminals t1 and t2) into the single-ended signal v_r via suitable mirroring stages, thus, rejecting the information on common mode voltage carried by the input terminals. The extracted signal v_r is then forwarded to the internal logic circuitry (labeled as Logic core in Fig. 4) for detection and further processing. In actual applications, receiver circuits may contain internal matching resistors across the input terminals and hysteresis detection circuitry or possible enhanced control features for improving the noise rejection and the quality of detected signal v_r. For additional details on LVDS receivers, the reader may refer to [9].

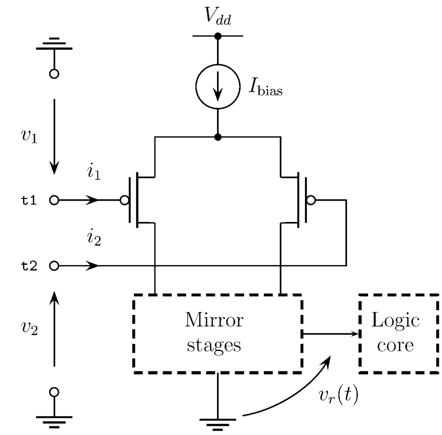

Fig. 4. Generic structure of a LVDS receiver and its relevant electric variables.

The general structure of receivers is such that the loading of the logic core on the electrical inputs is negligible (see Fig. 4). Thus, receivers, from an analog point of view, can be considered as nonlinear dynamic time-invariant three-terminal elements $(\mathtt{t1}, \mathtt{t2}, \text{ground})$ and, similarly to drivers, the following model representation can be used for their electrical ports

$$\begin{cases} i_1(v_1, v_2) = \hat{\imath}_1(v_1, v_2) + \bar{\imath}_1\left(v_1, v_2, \frac{d}{dt}\right) \\ i_2(v_1, v_2) = \hat{\imath}_2(v_1, v_2) + \bar{\imath}_2\left(v_1, v_2, \frac{d}{dt}\right) \end{cases} \quad (6)$$

where i_1 and i_2 are the currents flowing into the input terminals of the receiver, and v_1 and v_2 are the associate voltages. In the above equation, $\hat{\imath}_1$ and $\hat{\imath}_2$ are the static characteristics of the modeled receiver, whereas $\bar{\imath}_1$ and $\bar{\imath}_2$ are the dynamic parts of the model. In general, differential receivers have a nearly linear dynamic behavior; thus, linear parametric relations can be used for the dynamic parts of the model.

The estimation of model parameters proceeds as for to the driver case. Estimation signals are applied by means of voltage sources to terminals t1 and t2 of Fig. 4 and the model parameters are computed by means of the *System Identification* techniques already mentioned in Section II-A. It is worth noting that, in general, the modeling process of differential receivers is relatively easier, and their models are simpler than for drivers. In fact, the receivers static characteristics are significant only in the clamp regions (if any), and their dynamic behavior is very close to a purely linear capacitive one.

III. MACROMODEL IMPLEMENTATIONS

In order to address the implementation of models (2), (3), and (6), it is expedient to focus on their functional forms. For the sake of conciseness, and without loss of generality, we concentrate on submodel i_{1H} (i.e., the submodel for terminal t1 of a driver in HIGH logic state), as expressed by (3). An effective representation of the static part is based on a sigmoidal basis functions expansion of the dc characteristic, i.e.

$$\hat{\imath}_{1H}(v_1, v_2) = \sum_n a_n \tanh(b_{0n} + b_{1n}v_1 + b_{2n}v_2) \quad (7)$$

where $a_n, b_{0n}, b_{1n}, b_{2n}$ are the approximation parameters. The dynamic part is a special form of (5)

$$\begin{aligned}\bar{\imath}_{1H}(k) = {} & \alpha_{01}\bar{\imath}_{1H}(k-1) + \alpha_{02}\bar{\imath}_{1H}(k-2) \\ & + \alpha_{10}v_1(k) + \alpha_{11}v_1(k-1) \\ & + \alpha_{12}v_1(k-2) + \alpha_{21}v_2(k-1) \\ & + \alpha_{22}v_2(k-2) \end{aligned} \tag{8}$$

where the dynamic order (i.e., the number of past time samples included) is assumed to be 2.

For the implementation of these dynamic relations as macromodels, it is useful to convert them into the continuous-time domain. This can be done by substituting back in the difference operator, the time derivative, i.e., $(d/dt)z(t) \approx (1/T)(z(k) - z(k-1))$ (see [12] for more details). After this conversion, the complete equation for terminal `t1` writes

$$\begin{cases} \frac{d}{dt}\begin{bmatrix} x_{01}(t) \\ x_{02}(t) \\ x_{11}(t) \\ \cdots \end{bmatrix} = \frac{1}{T}\begin{bmatrix} \bar{\imath}_{1H}(t) - x_{01}(t) \\ x_{01}(t) - x_{02}(t) \\ v_1(t) - x_{11}(t) \\ \cdots \end{bmatrix} \\ \bar{\imath}_{1H}(t) = \alpha_{01}x_{01} + \alpha_{02}x_{02} + \alpha_{10}v_1 + \alpha_{11}x_{11} + \cdots \\ i_{1H}(t) = \sum_n a_n \tanh(b_{0n} + b_{1n}v_1(t) + b_{2n}v_2(t)) + \bar{\imath}_{1H}(t). \end{cases} \tag{9}$$

In order to use models expressed by differential-algebraic equations in the form of (9) for the numerical simulations of signal integrity problems, two practical choices are available: 1) convert the equations into circuit equivalents and exploit a SPICE circuit simulator; 2) implement them as they are in analog mixed-signal (AMS) simulation environments, like Verilog-AMS and VHDL-AMS, that accept and solve differential-algebraic equations.

The conversion of differential-algebraic equations into circuit equivalents and their implementation as SPICE subcircuits is a standard procedure that is based on controlled-current sources for the static submodels, and resistors, capacitors, and controlled source elements for the dynamic parts. As an example, the SPICE-like implementation of a generic nonlinear dynamic parametric model is discussed in [12]. It is worth noting that standard SPICE commands do not allow an easy evaluation of the driver weighting coefficients by means of the juxtaposition procedure shown in Fig. 3. Therefore, w_{nH} and w_{nL} functions and their circuit counterparts in the SPICE script are usually computed offline for a predetermined bit pattern.

The implementation of the model in AMS metalanguages is much easier, since no conversion is required. AMS tools can handle the interaction between the internal functional part of the IC and the analog output ports of buffers driving the external interconnects, thus, allowing the mixed simulation of the analog signals propagating paths between drivers and receivers and their digital processing taking place inside the devices. Besides, they allow an effective evaluation of the weighting coefficients that can be generated on the fly from the digital signal controlling the output state on the driver. Details on VHDL-AMS can be found in [17], [18].

Both previous model implementations are also compatible with IBIS version 4.1 [4] that allows the coexistence of traditional IBIS models and external models defined by SPICE or VHDL-AMS code. This is particularly important, because nowadays most SI/EMC simulations are carried out by specialized commercial tools, where large component libraries and powerful utilities are available. Since these tools are IBIS compliant, the *IBIS multilingual extension* of IBIS version 4.1 offers a strightforward way to implement the proposed parametric models in these simulation tools. A simple IBIS script allows to interface models defined by external code with the IBIS world, thereby enabling the simulation environment of choice to run parametric models. Fig. 5 shows parts of an IBIS script of this kind, which declares a differential output buffer connected to pins 1 and 2; the section of the external call to the VHDL-AMS code defining the buffer model is framed. A very similar call is possible for models defined by SPICE scripts.

```
[IBIS Ver] 4.1
[File name] driverX.ibs
[File Rev] 1.0
[Date] 30/03/2004
|********************
[Component] DRIVER
[Manufacturer] Polito
[Package]
...
[Pin] signal_name model_name R_pin L_pin C_pin
1    TXP    MACROMODEL
2    TXN    MACROMODEL
[Diff_Pin] inv_pin vdiff tdelay_typ tdelay_min tdelay_max
1   2   0.1V   0.0s   NA   NA
|********************
|
[Model] MACROMODEL
Model_type Output_diff
Polarity Non-Inverting
  [External Model]
  Language VHDL-AMS
  |
  | corner_name file_name circuit_name
  Corner   Typ   driverX.vhd   driverX(bufferbehav)
  |
  Ports   D_control   A_signal_pos   A_signal_neg
  |
  [End External Model]
...
[end]
```

Fig. 5. Example IBIS description of a digital IC consisting of a differential driver whose model is externally specified. The framed area highlights where the external VHDL-AMS model is called. Bold text indicates the information the user must fill in the IBIS structure.

IV. Modeling Examples

In this section, the proposed modeling approach is demonstrated on different example devices defined by detailed transistor-level models, which are assumed as the *reference* models hereafter. Reference models are used to compute the responses needed for the estimation of macromodel parameters and for model validations. All the required responses are computed by means of HSPICE. The examples are addressed by the model representations (2), (3), and (6) and the obtained models are implemented as SPICE-like subcircuits. According to Section II, the static parts are represented by sigmoidal-based expansions (7) and the dynamic parts by linear parametric models (8).

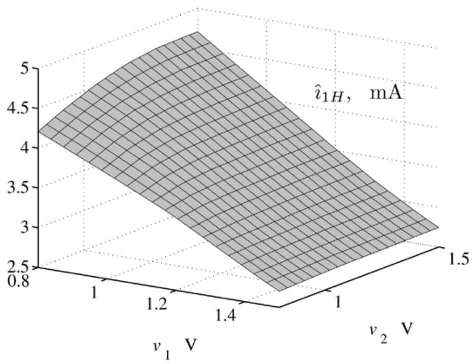

Fig. 6. Static characteristic $\hat{\imath}_{1H}(v_1, v_2)$ for the Example 1 driver forced in the HIGH logic state.

Example 1: The first modeled device is the Fairchild FIN1019 ($V_{dd} = 3.3.$ V) LVDS High-Speed Differential Transceiver used as a driver, whose HSPICE-encrypted transistor-level model is available from the website www.fairchildsemi.com. This device behaves like a plain differential driver (see Fig. 1) without internal matching resistors or control mechanisms.

For the macromodel estimation, both the static and the dynamic parts of (3) are computed through the procedure discussed in Section II-A. As an example, Fig. 6 shows the static characteristic $\hat{\imath}_{1H}(v_1, v_2)$. The dynamic parts are obtained from the port current responses i_1 and i_2 to independent gaussian noise sources v_1 and v_2 (cfr. Fig. 2), whose mean value equals the nominal common mode voltage (1.25 V), and whose amplitude standard deviation is 10 mV. In addition, the linearity of the dynamic part has been verified by applying noisy signals, having an amplitude on the order of the full voltage swing of 700 mV specified by the LVDS standard. The weighting coefficients are computed as described in Section II-A, by means of switching experiments while the device is connected to a 100-Ω differential load resistor.

In order to validate the macromodel, two different HSPICE simulation test cases are considered. The first test circuit is composed of the modeled device driving a 50-Ω differential resistor with a logic HIGH pulse. For this test case, Fig. 7 shows the reference and macromodel responses of the output terminal voltages $v_1(t), v_2(t)$ and of the differential voltage $v_d(t)$. The second test circuit is composed of the modeled device driving with a logic HIGH pulse a coupled and lossless transmission line (differential mode impedance $Z_o = 50\ \Omega$, common mode impedance $Z_e = 90\ \Omega$, line length 0.15 m) loaded by a 100-Ω differential resistor. For this test case, Fig. 8 shows the reference and the macromodel responses of the output terminal voltages $v_1(t)$, $v_2(t)$ and of the differential voltage $v_d(t)$.

The accuracy of the proposed macromodel has been quantified by computing the timing error and the maximum relative voltage error. The timing error is defined as the maximum delay between the reference and the macromodel differential voltage responses measured for the zero voltage crossing. For the two test cases illustrated in Figs. 7 and 8, the maximum timing error is 15 ps. The maximum relative voltage error is computed as the maximum error between the reference and macromodel voltage responses divided by the nominal voltage swing of 700 mV.

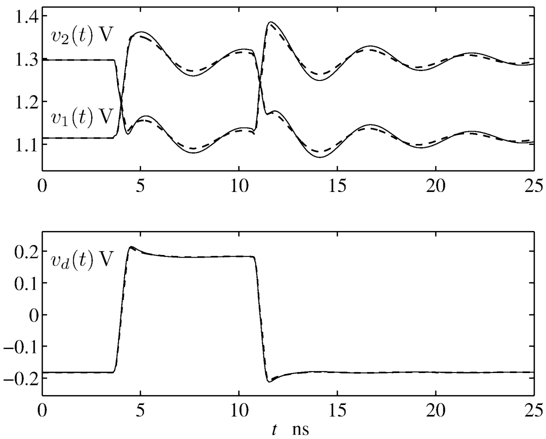

Fig. 7. Output port voltages $v_1(t)$, $v_2(t)$ (top panel) and differential voltage $v_d(t)$ (bottom panel) computed for the Example 1 driver connected to a 50-Ω differential resistor and producing the bit pattern "010." Solid line: reference, dashed line: macromodel.

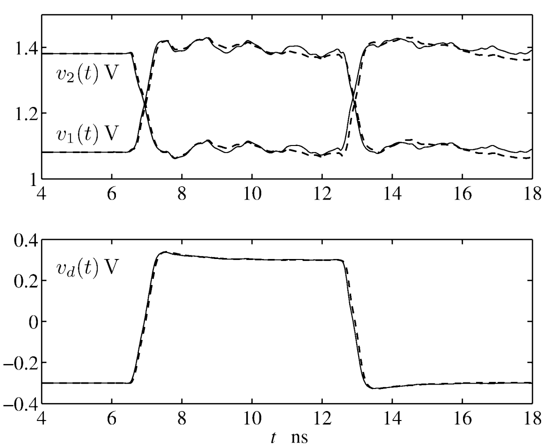

Fig. 8. Output port voltages $v_1(t)$, $v_2(t)$ (top panel) and differential voltage $v_d(t)$ (bottom panel) computed for the Example 1 driver producing the bit pattern "010." The driver is loaded by a coupled interconnect, whose termination is a resistor (see text for details). Solid line: reference, dashed line: macromodel.

TABLE I
CPU TIME AND MEMORY USAGE FOR THE HSPICE COMPUTATION OF THE CURVES OF FIG. 7

Model	CPU time	Memory
reference	41 sec	2736 kB
macromodel	6 sec	600 kB

For the previous validation cases, the maximum relative errors turn out to be 4.2% for port voltages v_1 and v_2 and 1.4% for the differential voltage v_d. Macromodel efficiency is assessed by the CPU-time and memory usage required for circuit simulations. For the example device at hand, Table I compares the efficiency between the reference transistor-level model and the macromodel for the computation of the curves of Fig. 7: a factor of seven speedup, and almost a factor of five in memory saving are evidenced in Table I.

Example 2: The second modeled device is an idealized version of the differential driver proposed in [9] that exploits a control mechanism to reduce the fluctuations of the common-mode voltage v_c around the reference voltage of 1.25 V. Here, the

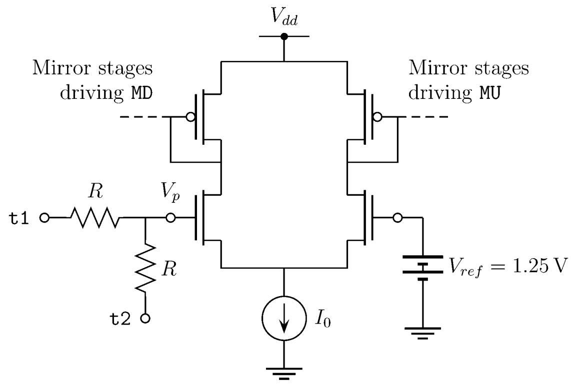

Fig. 9. Control circuit for the Example driver 2.

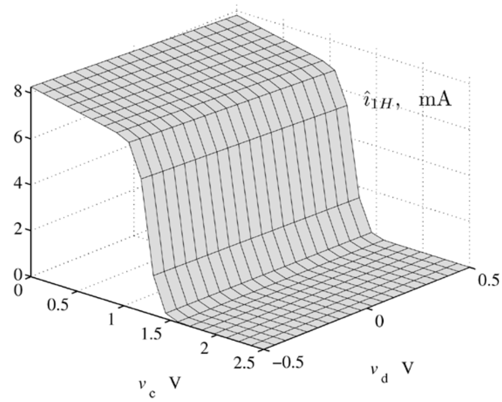

Fig. 10. Static characteristic $\hat{\imath}_{1H}(v_d, v_c)$ for the Example 2 driver forced in the HIGH logic state.

mechanism is implemented by the differential amplifier and current mirrors of Fig. 9, regulating the drain currents of MU and MD of Fig. 1. The probe voltage V_p is obtained by a high resistance $(R = 100\text{- k}\Omega)$ voltage divider connected to the output terminals of Fig. 1.

Fig. 10 shows the static characteristic $\hat{\imath}_{1H}(v_d, v_c)$ for this device. According to the purpose of the control circuit, the variations of this characteristic versus v_c is dominant, and, since $v_c = (v_1 + v_2)/2$, the usual simplification $\hat{\imath}_{1H}(v_1, v_2) \approx \hat{\imath}_{1H}(v_1)$ does not hold.

The validation test circuit devised for this example consists of the driver forced in HIGH state and connected to a differential load composed of a 100-Ω resistor in series with an independent voltage source. The voltage source produces a pulse with 0.5-V amplitude and 100-ps transitions. The load current waveforms predicted by using the reference and the estimated models in such a test circuit by means of HSPICE are shown in Fig. 11. The good agreement of the curves confirms the ability of model (3) to describe differential drivers with control mechanism and highlights the importance of taking into account the dependence of the modeled currents on both output voltages.

Example 3: The third modeled device is the same Fairchild FIN1019 LVDS High Speed Differential Transceiver of Example 1 used as a receiver. This device behaves like a plain differential receiver with high input impedance, leading to a macromodel representation defined by (6) where the static

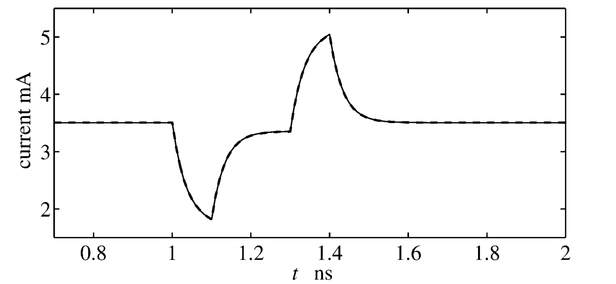

Fig. 11. Load current computed for the test circuit of Example 2 (see text). Solid line: reference, dashed line: macromodel.

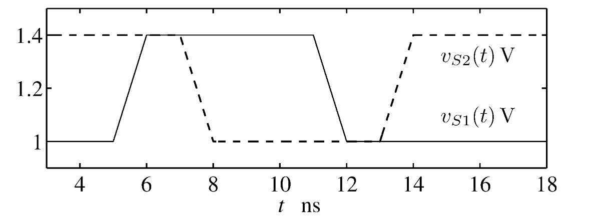

Fig. 12. Voltage waveforms $v_{S1}(t)$, $v_{S2}(t)$ of the Thevenin sources for the validation test case of the Example 3 receiver.

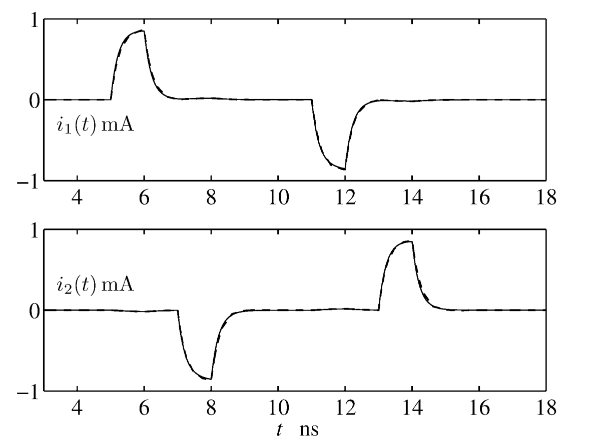

Fig. 13. Port currents i_1 and i_2 flowing into the input terminals of the Example 3 receiver. The device input terminals are excited by means of Thevenin sources composed of 100 Ω resistors connected to the voltage sources v_{S1} and v_{S2} of Fig. 12. Solid line: reference, dashed line: macromodel.

characteristic terms $\hat{\imath}_1$ and $\hat{\imath}_2$ are neglected. The dynamic parts are computed through the procedure discussed in Section II-B.

As a validation, a test setup consisting of two Thevenin sources connected to the input terminals of the example receiver is considered. Each Thevenin source consists of the series connection of a $R_S = 100\text{-}\ \Omega$ resistor and an independent voltage source. Fig. 12 shows the waveforms of the two voltage sources (labeled as $v_{S1}(t)$ and $v_{S2}(t)$). It is worth noting that the above sources sweep the range of the possible operating voltages of the receiver and have nonsynchronous transitions in order to excite both the differential and the common mode operation of the device. Fig. 13 shows the reference and macromodel responses of port currents i_1 and i_2 flowing into the input terminals of the receiver. The reference and predicted curves turn out to be almost indistinguishable, leading to negligible errors, thus, confirming the good accuracy of the proposed receiver macromodel.

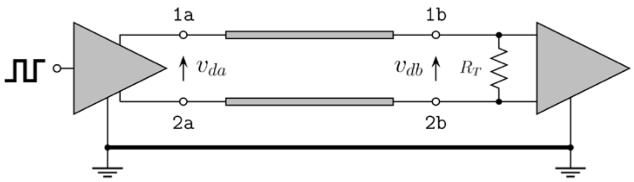

Fig. 14. Application test case: a high-speed data communication link with the relevant electrical variables (see text for details); Fairchild 1019 transceiver model is used at both terminations.

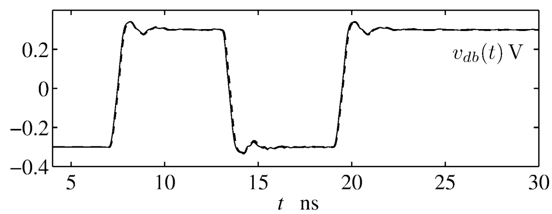

Fig. 15. Far-end differential voltage $v_{db}(t)$ computed for the application test of Fig. 14 consisting of a realistic propagation path between the Example 1 driver and the Example 3 receiver (see text). The driver produces a "01011" bit stream with a bit time of 6 ns. Solid line: reference, dashed line: macromodel.

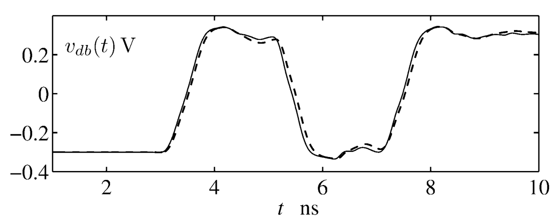

Fig. 16. Far-end differential voltage $v_{db}(t)$ computed for the application test of Fig. 14 consisting of a realistic propagation path between the Example 1 driver and the Example 3 receiver (see text). The driver produces a "01011" bit stream with a bit time of 2 ns. Solid line: reference, dashed line: macromodel.

V. Application Test Case

As a realistic application, the test setup of Fig. 14, consisting of a complete propagation path between a driver and a receiver, is considered. The Fairchild transceiver of Example 1 and Example 3 is used at both terminations of the transmission channel. The propagation path is composed of a coupled and lossless transmission line (differential mode impedance $Z_o = 50\ \Omega$, common mode impedance $Z_e = 90\ \Omega$, line length 0.15 m) with a resistor $R_T = 100\ \Omega$ at the far-end.

As a first test, the example driver is set to produce the bit stream "01011" with a 6-ns bit time. In this test, the bit time is chosen long enough to allow all waveforms to reach their steady state values before any state transition begins. Fig. 15 shows the comparison between the reference and predicted differential voltage $v_{db}(t)$ at the receiver side. As a second test, the example driver is set to produce the same bit stream with a more realistic bit time of 2 ns (0.5 Gbps). For this case, Fig. 16 shows the comparison between the reference and predicted differential voltage $v_{db}(t)$ at the receiver side.

As a final test, the driver produces a 128 pseudorandom binary signal with 2-ns bit time and a 100-ps uniformly distributed jitter. Waveforms computed for voltage v_{db} are used to build the eye diagram of the link. Fig. 17 shows the comparison between diagrams arising from the reference and predicted waveforms.

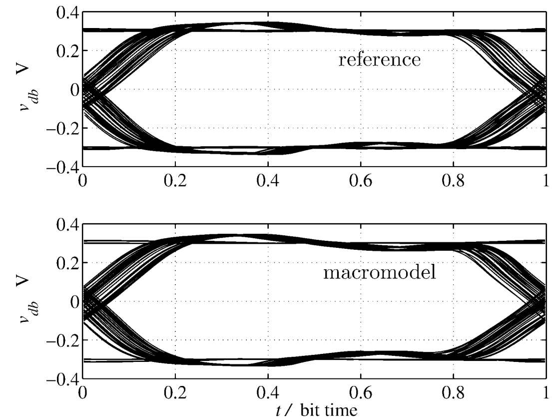

Fig. 17. Eye diagram computed from the voltage waveform $v_{db}(t)$ obtained by means of HSPICE simulation of the test circuit of Fig. 14 with transistor-level (top panel) and macromodels (bottom panel) descriptions of the driver and receiver blocks.

From the previous curves, it is worth noting that the good accuracy of predicted curves is confirmed for a realistic application involving a complete propagation path: timing errors of 1–2% of the bit time and maximum relative voltage errors on the same order of those found in the validation of Example 1 driver are obtained.

VI. Conclusion

This paper proposes a systematic procedure for the behavioral modeling of differential devices for the analog simulation of high-speed digital interconnection systems. The procedure is based on the use of parametric relations that allow accurate and efficient reproduction of device terminal behaviors without requiring any circuit interpretation of the operation of the modeled devices. The obtained models are defined by differential-algebraic equations that hide the internal structure of the device and protect the intellectual properties of IC vendors. These models can be easily implemented in any circuit simulation environment as SPICE-like subcircuits and in mixed-signal simulators via direct metalanguage code descriptions like VHDL-AMS. Besides, they can be added to any commercial SI simulator supporting IBIS version 4.1 by means of the IBIS multilingual extension that allows for models defined by external code. The modeling procedure is demonstrated on example devices and applied to the simulation of a realistic interconnection system involving a complete propagation path between a driver and a receiver. The proposed models turn out to be structurally simple, efficient, and very accurate. They are not limited by the need for circuit interpretations and can easily handle device-enhanced features like driver control circuits.

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