Linear and Nonlinear Macromodels for System-Level Signal Integrity and EMC Assessment

IEICE TRANSACTIONS

on Communications

VOL.E88-B
NO.8
AUGUST 2005

A PUBLICATION OF THE COMMUNICATIONS SOCIETY

The Institute of Electronics, Information and Communication Engineers
Kikai-Shinko-Kaikan Bldg., 5-8, Shibakoen 3chome, Minato-ku, TOKYO, 105-0011 JAPAN

IEICE TRANS. COMMUN., VOL. E88-B, No. 8 AUGUST 2005, pp. 1121-1126

INVITED PAPER *Special Section of 2004 International Symposium on Electromagnetic Compatibility*

Linear and Nonlinear Macromodels for System-Level Signal Integrity and EMC Assessment

Flavio CANAVERO †, Stefano GRIVET-TALOCIA †, Ivano A. MAIO † and Igor S. STIEVANO †, *Nonmembers*

Summary
This paper presents a systematic methodology for the system-level assessment of signal integrity and electromagnetic compatibility effects in high-speed communication and information systems. The proposed modeling strategy is illustrated via a case study consisting of a critical coupled net of a complex system. Three main methodologies are employed for the construction of accurate and efficient macromodels for each of the sub-structures typically found along the signal propagation paths, i.e. drivers/receivers, transmission-line interconnects, and interconnects with a complex 3D geometry such as vias and connectors. The resulting macromodels are cast in a common form, enabling the use of either SPICE-like circuit solvers or VHDL-AMS equation-based solvers for system-level EMC predictions.

Key words:
Signal Integrity, Electromagnetic Compatibility, Macromodeling, Digital Integrated Circuits, Transmission Lines, 3D Interconnects, Passivity

1. Introduction

This paper presents a systematic methodology for the Signal Integrity and EMC simulation of distribution networks of digital signals in high-speed communication and information systems. It is well known that such analysis is very challenging, since a broadband characterization of all the geometrical/electrical features that have some influence on the signals must be taken into account. The main strategy that we present here addresses the problem at two different levels, of which the first one concerns the physical description and the second one the appropriate simulation tools.

The combination of propagation effects with possibly very complex geometry and with nonlinear/dynamic behavior of drivers and receivers makes a direct full-wave approach not feasible. Therefore, a feasible strategy must subdivide the propagation path into separate and well-defined sub-structures, each of which is separately characterized by a macromodel, i.e., a set of equations that are able to reproduce with sufficient accuracy the electrical behavior of the structure.

Different macromodeling strategies are needed for different structures. We consider three main structure types which can be found along a propagation path. First, we have drivers and receivers at the path terminations. These are usually buffers characterized by strong nonlinearities and relevant dynamic effects, for which we adopt parametric behavioral macromodels that provide excellent approximations of detailed transistor-level models, and lead to significant speedup in simulation time.

A second important class of structures includes interconnection elements characterized by a complex geometry, i.e., discontinuities such as packages, vias and via arrays, connectors, bends, etc. These discontinuities are treated as lumped multiports for which a passive macromodel based on a state-space representation is constructed from measured or simulated time-domain or frequency-domain port responses.

The last class of investigated structures includes segments of uniform transmission-line structures at chip, module, board level, and cables. Their macromodeling process, which is highly accurate and very efficient, involves a combination of delay extraction and rational approximation.

The proposed modeling strategy is illustrated via a case study, presented in Section 2. The three techniques leading to the construction of the macromodels for drivers/receivers, transmission lines, and 3D interconnects are outlined and benchmarked in Section 3. Finally, Section 4 reports some results on the system-level characterization of the critical net under investigation.

2. A Case Study

All the numerical results to be presented in this paper refer to a specific case study, depicted in Fig. 1. The structure involves a chip-to-chip communication through a coupled and complex interconnect path. The coupled path conducts the signals through various transmission lines and discontinuities along: last metal layer on first chip, a module, card 1, connector (a), board A, connector (b), board B, connector (c), board C, connector (d), card 2, module, and last metal on second chip, where the two receivers are located (data were provided under confidential agreement by IBM). A total of 42 transmission-line segments are present, each specified by frequency-dependent per-unit-length parameter matrices. Four connectors provide the link between cards and

Manuscript received March 30, 2005.
† The authors are with the Dipartimento di Elettronica, Politecnico di Torino, Corso Duca degli Abruzzi 24, 10129 Torino, Italy Contact e-mail: igor.stievano@polito.it

boards. Two specifications are available for these connectors: i) a large circuit with more than 40000 elements provided by the connector vendor, and ii) the frequency-domain scattering matrices up to 10 GHz. Finally, the terminals of the coupled interconnect are connected to two IC drivers (near-end side on card 1) and two IC receivers (far-end side on card 2). These components are known via their transistor-level description.

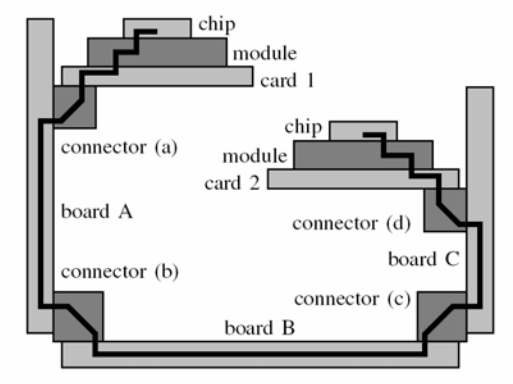

Fig. 1. Simplified view of the propagation path (the thick line) under investigation. The figure is not to scale and only illustrative of the overall complexity.

The complete simulation of the structure of Fig. 1 is a very challenging task, since all the data or even possible models characterizing each basic block comes from a different environment and can be hardly used together within the same simulation engine. In fact, a brute force SPICE simulation fails on a 2GB RAM PC due to the complexity of the various available models. As a possible solution to this problem, we construct simplified macromodels that are able to represent the behavior of each substructure with good accuracy, but require less CPU and memory resources.

3. Macromodels

In this Section, the most suitable methodologies for the development of accurate and efficient macromodels of buffers (i.e., drivers and receivers), transmission-lines and lumped complex 3D-interconnects are briefly outlined. Due to limited space, results will only be shown in Section 4 for the entire structure. Extensive validation of the single macromodeling techniques is available in the open literature (see the reference list).

3.1 Logic devices: M*π*log

In the distribution networks of digital signals, the terminations represented by the IC drivers and receivers are critical elements, since their intrinsic nonlinear and dynamic behavior can significantly affect the capacity of the propagation paths. Therefore, accurate and efficient macromodels are required.

In this Section, we briefly review the M*π*log (Macromodeling via Parametric Identification of LOgic Gates) approach [2], [19], providing an effective methodology for the construction of accurate and efficient behavioral models of logic devices. In this approach, output buffer constitutive relations are sought as dynamic nonlinear parametric two-piece models of the form

$$i(t) = w_1(t)i_1(v(t)) + w_2(t)i_2(v(t)),$$

relating the port voltage v and current i variables, where $i_1(t)$ and $i_2(t)$ are submodels describing the port behavior in the HIGH and LOW logic states, respectively, and $w_1(t)$ and $w_2(t)$ are weighting coefficients describing state transitions.

Parametric nonlinear relations and system identification methods like those involving the identification of mechanical systems, economic trends, etc. allow us to obtain improved nonlinear dynamic models for submodels $i_{1,2}(t)$ in the above representation, see [3]. Parametric models are usually expressed as sums of sigmoidal functions of the involved variables and their parameters are estimated by fitting the model responses to suitable transient responses of the input and output variables related by the model. In this case, the related variables are the voltage and current of the output port in fixed logic state and the model parameters are computed by minimizing a suitable error function between voltage and current waveforms of the model and real device. Specific algorithms are available to solve this problem, depending on the choice of the family of basis functions used to define the parametric models [4], [5].

Parametric models offer rigorous mathematical foundations, identifiability from external observations, good performances for the problem at hand as well as preserving the ability to hide the internal structure of the modeled devices. Finally, parametric models can be readily implemented according to standard industrial simulation tools like SPICE and VHDL-AMS [1]. In addition, such already-mentioned SPICE and VHDL-AMS implementations are completely compatible with the multilingual extension of IBIS (Input/output Buffer Information Specification), which is the most established standard for the behavioral description of IC ports. In fact, ver. 4.1 of IBIS specification [6] is an extension, recently devised to overcome some limitations of the original standard, allowing for more general models not necessarily based on simplified circuit interpretations.

Details on parametric modeling of single-ended CMOS devices can be found in [3], where the parametric

approach is applied to the modeling of input and output ports of commercial devices by means of the transient responses of their transistor-level models. The estimation of parametric models from measured transient responses is demonstrated in [7]. The extension of the methodology in order to take into account the device temperature, the power supply voltage, the power supply current drawn by buffers as well as to model tri-state devices is addressed in [2]. Recent advances on the modeling of receiver circuits, including the logic detection mechanism and the effects of power supply voltage fluctuations are in [8]. Finally, some results on the modeling of differential Low Voltage Differential Signaling (LVDS) devices are in [9].

The Mπ*log* methdology was tested on the case study of Section 2 by simulating the transmission of 700 bits using a SPICE-like solver. All transmission line segments were replaced with ideal (lossless and uncoupled) lines and all connectors were removed and shorted. The efficiency results obtained with different drivers/receivers models are collected in Table 1. The results show a significant speedup of the proposed macromodels with respect to the refererence transistor-level models of devices, thus leading to accurate predictions of device port responses (see [2], [3] for validation results on accuracy and efficiency of macromodels). Besides, it is worth noting that the proposed macromodels, turns out to be almost as efficient as simplified linear equivalents of devices, that provide rough approximations of device port responses [10].

Table 1: Efficiency of Drivers/Receivers models

DRV/RCV models	CPU time	Accuracy
Transistor-level	20.3 hours	Reference
Mπ*log*	11.6 minutes	very good, 1-3% of bit time, in timing
Linear (ideal)	7 minutes	poor

3.2 Transmission Lines: TOPLine

Uniform transmission lines are characterized by a cross section which is translation-invariant along the direction of propagation of the signals. This calls for models based on the Telegraphers equations with suitable per-unit-length matrices $\mathbf{L},\mathbf{C},\mathbf{R},\mathbf{G}$. Such parameters must be assumed to be frequency-dependent in order to capture all relevant signal degradation effects, and must be computed accurately via transverse 2D field simulation. Thus, the main difficulty in transmission-line modeling is the conversion of the intrinsic frequency-dependent and distributed line specification into a time-domain model.

The approach that we follow, denoted as TOPLine [19], is based on the well-known Method of Characteristics [11]. A detailed description of the proposed methodology is available in [12], [13], so only a brief outline is given here. A generic N-conductor line is represented as a 2N-port element, with terminal voltages and currents related in the Laplace domain as

$$\mathbf{Y}_c(s)\mathbf{V}_1(s)-\mathbf{I}_1(s)=\mathbf{H}(s)\left[\mathbf{Y}_c(s)\mathbf{V}_2(s)+\mathbf{I}_2(s)\right]$$
$$\mathbf{Y}_c(s)\mathbf{V}_2(s)-\mathbf{I}_2(s)=\mathbf{H}(s)\left[\mathbf{Y}_c(s)\mathbf{V}_1(s)+\mathbf{I}_1(s)\right]$$

where $\mathbf{Y}_c(s)$ is the characteristic admittance matrix (representing the matching load on both ends of the line) and $\mathbf{H}(s)$ is the propagation operator through the line (including delay, dispersion, losses, etc…). These matrices are readily computed from the per-unit-length parameters at all available frequencies ($s=j\omega$) via known expressions [13]. The conversion into a time-domain compatible model is performed by a modal delay extraction (using the infinite-frequency modes defined by the modal matrix $\mathbf{M}$) via definition of a delayless propagation operator

$$\mathbf{P}(s)=e^{s\mathbf{T}}\mathbf{M}^{-1}\mathbf{H}(s)\mathbf{M}$$

and by a combined frequency-domain rational approximation

$$\mathbf{Y}_c(s)=\mathbf{Y}_\infty+\sum_n\frac{\mathbf{Y}_n}{s-p_n},\quad \mathbf{P}(s)=\mathbf{P}_\infty+\sum_n\frac{\mathbf{P}_n}{s-q_n}$$

The explicit extraction of the line delay leads to smooth functions and consequently to very accurate rational approximations even with a small number of poles, typically less than 10. Extensive validations and application results are available in [12], [13].

Given the above representation, a model realization to be employed in transient simulations can be readily constructed. In fact, a direct equivalent circuit synthesis can be performed using standard SPICE elements. Basic circuit interpretation of the above expression requires only resistors, capacitors, controlled sources, and ideal transmission lines (to treat the extracted delay). This last step is exact and therefore no loss of accuracy may occur during the synthesis.

3.3 3D-Interconnects: IdEM

There are several interconnect structures that cannot be treated as uniform transmission lines. Examples can be vias, connectors, junctions, bends, power/ground structures, and discontinuities in general. These structures constitute one of the most challenging tasks for an accurate system-level characterization under SI and EMC standpoints. The only assumption that can be adopted is linearity, since no model structure can be assumed in the general case.

The modeling approach, denoted as IdEM (Identification of Electrical Macromodels) [19], is based on a sequence of well-defined steps. First, the electromagnetic behavior of the interconnect structure is determined via full-wave analysis and/or by direct

measurement. As a result of the characterization, a set of port responses in time or frequency domain are available, and constitute a possibly large amount of data to be processed to obtain a global macromodel. The most common representation, especially for signal links, is the scattering form, although admittance and impedance may be used as well. As for the transmission line structures, the key to conversion to time-domain is a rational approximation in the Laplace domain, which is here applied directly to the structure transfer (scattering) matrix

$$\mathbf{S}(j\omega) = \mathbf{S}_\infty + \sum_n \frac{\mathbf{S}_n}{j\omega - p_n}$$

Several schemes may be devised for the computation of this rational approximation. When the number of ports is not too large (few units), a common pole set may be used for all transfer matrix entries in a single fitting stage. Conversely, when the number of ports is too large, separate subset of port responses may be fitted independently with different poles. Some considerations may be found in [14].

The computation of poles and residues is performed via the powerful pole relocation algorithm known as Vector Fitting (VF). Depending on the nature of the characterization that was employed, either the standard frequency-domain VF [16] or its time-domain counterpart [15] may be adopted. In both cases, the poles and residues are obtained by iterative refinement of an initial (even random) guess of the poles. Each iteration step requires only the solution of a standard linear least squares problem.

A final remark on the model passivity. Since any interconnect structure is passive and unable to generate more energy than it is fed with, it is highly recommended to retain this important property in the rational model. In fact, a passivity violation may result in non-converging or exponentially unstable system-level simulations, since an arbitrary interconnection of stable but non-passive models is not guaranteed to remain stable. Our approach to this problem is based on a passivity check once the model has been constructed. If non-passive, the residues are recomputed including passivity constraints. The main tool allowing for this check and compensation is the so-called Hamiltonian matrix associated to the macromodel. The theory and applications developed in [17] and [18] show that existence of purely imaginary eigenvalues of this matrix is a symptom of passivity violation. When this happens, an iterative perturbation algorithm allows to displace these eigenvalues from the imaginary axis by inducing perturbations on the residues, thus leading to passivity enforcement. All details are reported in [18].

The proposed methodology was tested on the case study under investigation by performing a 700 bits simulation of the critical path with ideal (linear) drivers/receivers models and with ideal (lossless and uncoupled) transmission line models. The results obtained with diffrerent connector models, depicted in Table 2, show a significant gain in efficiency with respect to the original models, and only a 6X slowdown factor with respect to the simulation with all connectors removed.

Table 2: Efficiency of connector models

Connector models	CPU time
Shorted	21.5 minutes
IdEM	2 hours
Full circuit	42 hours

4. Results

We present here some results obtained from the global simulation of the structure depicted in Section 2 including all models of drivers/receivers, transmission lines, and 3D interconnects. All models were cast in a common SPICE format and a SPICE-like solver was used to run the simulations. The simulation is aimed at the characterization of safe digital transmission between the two ends of the path, to crosstalk evaluation, and to power/ground noise estimation. A pseudo-random sequence of 700 bits is used to drive the active line, leaving quiet the neighboring coupled path.

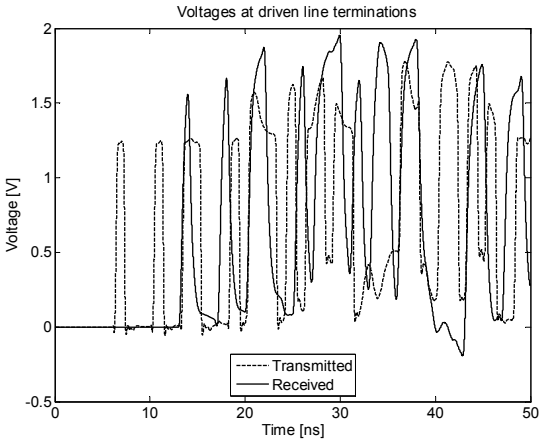

Fig. 2. Trasmitted and received signal on the active line.

The transmitted and received signals on the driven line are reported in Fig. 2. It should be noted that the delay of the propagation path is much larger than the bit time of 1 ns. Crosstalk waveforms at near and far end of victim line are given in Fig. 3, while the fluctuations of power and ground pins of the quiet driver are reported in Fig. 4. Finally, Fig. 5 shows the transmission eye diagram at the input port of the receiver obtained for the entire 700 bits sequence. The “open eye” shows that safe transmission

can be accomplished over the considered link at this bit rate.

The complete simulation required about 2 hours on a PC with 1.8 GHz CPU. Conversely, the simulation of the complete structure with the native models of each component (transistor-level models for drivers and receivers, full connector models, etc…) was not possible due to excessive complexity. This confirms the feasibility of the proposed approach for fast system-level SI and EMC analyses.

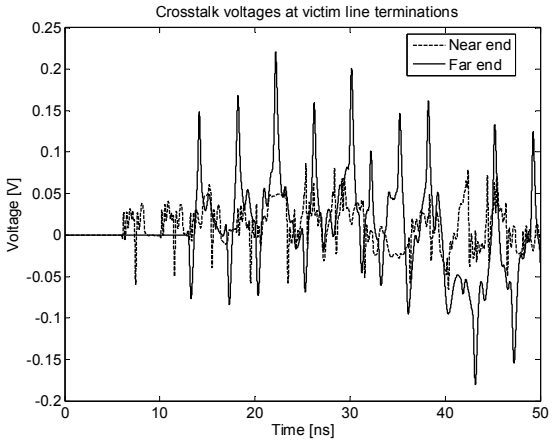

Fig. 3. Crosstalk voltage signals on the near- and far-end of the quiet line.

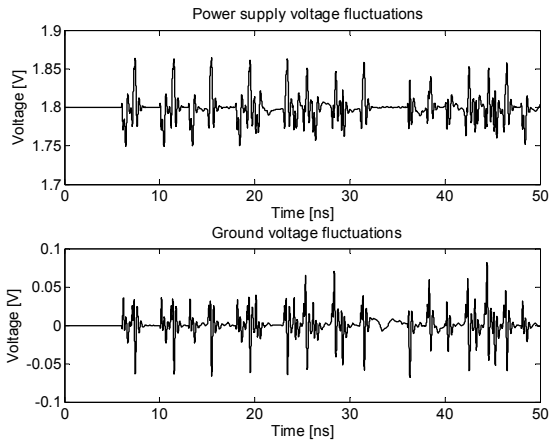

Fig. 4. Power and ground fluctuations at the quiet driver induced by switching of the active driver.

5. Conclusions

This paper addresses the system-level assessment of signal integrity and EMC effects of critical nets in high-speed communication and information systems. The proposed approach overcomes previous limitations of existing methodologies and amounts to developing accurate and efficient macromodels of each sub-structure composing the whole system, i.e., IC drivers and receivers, transmission lines and complex 3D interconnects. Suitable macromodels of the three types of structures are presented and cast in a common form as SPICE-like circuits or VHDL-AMS equation-based descriptions in order to be used together within the same simulation environment. The proposed approach has been demonstrated on a realistic case study, thus confirming the feasibility of the method for the system-level EMC predictions.

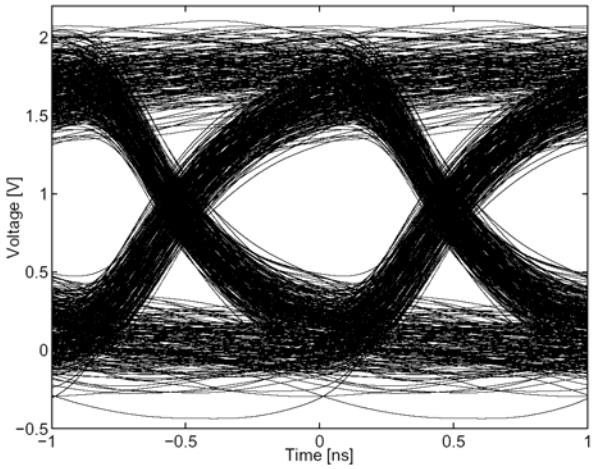

Fig. 5. Eye diagram for the complete transmission link at 1 Gbps.

Acknowledgments

The Authors are grateful to George Katopis and Erich Klink of IBM for providing the data of the system used for the application example. This work was supported in part by the Italian Ministry of University (MIUR) under a Program for the Development of Research of National Interest (PRIN grant #2004093025).

References

[1] Definition of Analog and Mixed Signal Extensions to IEEE Standard VHDL, IEEE Standard 1076.1-1999.

[2] I. S. Stievano, I. A. Maio, F. G. Canavero, "M*πlog* Macromodeling via Parametric Identification of Logic Gates," IEEE Transactions on Advanced Packaging, Vol. 27, No. 1, pp. 15–23, Feb. 2004.

[3] I. S. Stievano, F. G. Canavero, I. A. Maio, "Parametric Macromodels of Digital I/O Ports," IEEE Transactions on Advanced Packaging, Vol. 25, No. 2, pp. 255–264, May 2002.

[4] L. Ljung, System identification: theory for the user, Prentice-Hall, 1987.

[5] J. Sjoberg et al., "Nonlinear black-box modeling in system identify cation: a unified overview," Automatica, Vol. 31, No. 12, pp. 1691–1724, 1995.

[6] "I/O Buffer Information Specification (IBIS) Ver. 4.1," on the web at http://www.eigroup.org/ibis/ibis.htm.

[7] I. S. Stievano, I. A. Maio, F. G. Canavero, "Behavioral Models of I/O Ports from Measured Transient Waveforms," IEEE Transactions on Instrumentation and Measurement, pp. 1266–1270, Vol. 51, No. 6, Dec. 2002.

[8] I. S. Stievano, F. G. Canavero, I. A. Maio, "Behavioral Macromodels of Digital IC Receivers for Analog-Mixed Signal Simulations," Electronic Letters, 2005 (in press).

[9] I. S. Stievano, I. A. Maio, F. G. Canavero, C. Siviero, "Parametric Macromodels of Differential Drivers and Receivers," IEEE Transactions on Advanced Packaging, 2005 (in press).

[10] F. G. Canavero, S. Grivet-Talocia, I. Maio, I. Stievano, "Numerical Modeling of Digital Devices Impact on EMC/EMI," Proc. of *2001 IEEE EMC International Symposium*, Montreal, Canada, Aug. 13-17, 2001.

[11] F. H. Branin, "Transient Analysis of Lossless Transmission Lines", Proc. IEEE, Vol. 55, 1967, pp. 2012–2013.

[12] S. Grivet-Talocia, F. G. Canavero, "TOPLline: a delay-pole-residue method for the simulation of lossy and dispersive interconnects", in Digest of Electr. Perf. Electronic Packaging, Vol. 11, Monterey, CA, October 2002, pp. 359–362.

[13] S. Grivet-Talocia, H-M. Huang, A. E. Ruehli, F. Canavero, I. M. Elfadel, "Transient Analysis of Lossy Transmission Lines: an Effective Approach Based on the Method of Characteristics", IEEE Trans. Adv. Packaging, pp. 44–46, Vol. 27, No. 1, Feb. 2004.

[14] S. Grivet-Talocia, I.S.Stievano, F.G.Canavero, I.A.Maio, "A systematic procedure for the macromodeling of complex interconnects and packages," in EMC Europe 2004, International Symposium on Electromagnetic Compatibility, Eindhoven, The Netherlands, pp.414-419, September 6-10, 2004.

[15] S. Grivet-Talocia, "Package Macromodeling via Time-Domain Vector Fitting", IEEE Microwave and Wireless Components Letters, pp. 472-474, vol. 13, n. 11, November, 2003.

[16] B. Gustavsen, A. Semlyen, "Rational approximation of frequency responses by vector fitting", IEEE Trans. Power Delivery, Vol. 14, July 1999, pp. 1052–1061.

[17] S. Grivet-Talocia, "Enforcing Passivity of Macromodels via Spectral Perturbation of Hamiltonian Matrices" , 7th IEEE Workshop on Signal Propagation on Interconnects (SPI), Siena (Italy), pp. 33-36, May 11-14, 2003

[18] S. Grivet-Talocia, "Passivity enforcement via perturbation of Hamiltonian matrices", IEEE Trans. CAS-I, pp. 1755–1769, vol. 51, n. 9, September 2004.

[19] The modeling tools Mpilog, TOPLine, and IdEM are freely available for download from the official web site of the EMC Group at the Politecnico di Torino, Torino, Italy, http://www.eln.polito.it/research/emc

Flavio Canavero received the Laurea degree in Electronic Engineering from the Politecnico di Torino, Torino, Italy, in 1977, and the PhD degree from the Georgia Institute of Technology, Atlanta, USA, in 1986. Currently he is a Professor of Circuit Theory and Electromagnetic Compatibility with the Dipartimento di Elettronica, Politecnico di Torino. His research interests include interconnect modeling and digital integrated circuits characterization for signal integrity, field coupling to multiwire lines, and statistical methods in EMC. He is VP for Organization of his University, Editor-in-Chief of IEEE Transactions on Electromagnetic Compatibility, and Vice Chair of URSI Commission E. He has been the Organizer of the Workshop on Signal Propagation on Interconnects (SPI), from 2001 to 2003.

Stefano Grivet-Talocia received the Laurea degree and the Ph.D. degree in Electronic Engineering from the Politecnico di Torino, Torino, Italy, in 1994 and 1998, respectively. He joined in 1996 the EMC Group at the Politecnico di Torino, Torino, where he is currently Associate Professor of Circuit Theory. His research interests include modeling and simulation of lumped and distributed interconnects for Signal Integrity and Electromagnetic Compatibility. From 1999 to 2001 he served as Associate Editor of the international journal IEEE Transactions on Electromagnetic Compatibility.

Ivan A. Maio received the Laurea degree and the Ph.D. degree in Electronic Engineering from the Politecnico di Torino, Torino, Italy, in 1985 and 1989, respectively. Currently he is a Professor of Circuit Theory with the Dipartimento di Elettronica, Politecnico di Torino. His research interests are in the fields of Electromagnetic Compatibility and Circuit Theory, where he works on line modeling, and linear and nonlinear circuit modeling and identification.

Igor S. Stievano received the Laurea degree and the Ph.D. degree in Electronic Engineering from the Politecnico di Torino, Torino, Italy, in 1996 and in 2001, respectively. Currently he is an Assistant Professor of Circuit Theory with the Dipartimento di Elettronica, Politecnico di Torino. His research interests are in the field of Electromagnetic Compatibility, where he works on the macromodeling of linear and nonlinear circuit elements with specific application to the behavioral characterization of digital integrated circuits and linear junctions for the assessment of Signal Integrity and Electromagnetic Compatibility effects.