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RESEARCH ARTICLE

Modeling and Design of a Zero-Voltage Switching Battery Charger for Photovoltaic Applications

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ABSTRACT A novel solar-fed quasi-resonant battery charger operating in the Discontinuous Voltage Mode (DVM) is proposed and designed to achieve a high efficiency on a wide range of operating powers. The converter design procedure ensures the achievement of the Zero Voltage Switching of its MOSFETs on a wide range of operating conditions, thus reducing the switching losses. An analytical model of the converter operation and its static characteristic in its two operating modes is provided. A step-by-step design procedure for the converter is proposed for given battery and PV panel specifications. Measurements on a 100 W, 12 V-output prototype validate the accuracy of the modelling and highlight a high efficiency always above 90.9% with the input voltage ranging from 26.5 V and 28.5 V and an input power in the wide 20 W–100 W range.

INDEX TERMS Battery charging, discontinuous voltage mode, converter modelling, photovoltaic, quasi-resonant, zero voltage switching.

I. INTRODUCTION

Photovoltaic (PV) power systems are experiencing an increasing diffusion in the last few years, reaching a global installation capacity of 760 GW in 2020 [1]. Due to the intrinsic variability of the PV source, an increasing attention is devoted to the adoption of storage systems, to improve the reliability of generation plants for both grid-tied and off-grid applications [2]. The research and design of off-grid PV-storage interfaces is crucial to foster the installation of PV systems where the accessibility to the electrical grid is not straightforward, to meet the goals of the United Nations 2030 Agenda [3]. At the same time, off-grid PV-supplied charging systems are demanded in emerging green applications such as electrical light mobility [4], off-grid cooking systems [5] or green hydrogen production plants [6]. Fig. 1 shows a generic power conversion chain of an off-grid PV-fed charging station supplying a variety of DC or AC loads. Power converters designed for this application should be efficient and reliable, and should take into account both the requirements of the source (the intrinsic power variability of the PV generation) and of the battery (mainly, its lifetime).

The literature on solar-fed low-voltage battery chargers mainly focuses on two research branches: the design of innovative battery charge controllers at a systems level, and the exploration of new high-efficiency converter topologies. Within the first research branch, recent works have proposed multi-port battery chargers with different combinations of sources/loads: combined grid and PV module input ports [7], a flexible 3-outputs hybrid controller [8], a reconfigurable 2-modules charger [9]. Ad-hoc controllers are designed for an automatic management of the power flows. Other solutions specifically focus on the charging algorithm, as in [10], where the controller automatically switches between the float and bulk charging modes, or in [11], where a low conversion ratio of the PWM charge controller ensures the maximization of the conversion efficiency up to 98.5%, at the expense of working outside the Maximum Power Point (MPP). These works do not typically explore innovative power converter topologies solutions to address the high conversion efficiency requirement.

Within the second research branch, less recent works explore new PV-fed battery charger topologies, with the

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FIGURE 1. Typical power conversion chain of an off-grid PV-storage system supplying local DC or AC loads.

goal of ensuring a high conversion efficiency on a reasonable voltage gain and power range. Buck-derived resonant converters featuring Zero Voltage Switching (ZVS) [12] or Zero Current Switching (ZCS) [13] have been presented in literaure. Despite the soft commutation and the low component count, the increased voltage and current stresses of the semiconductor devices limit the conversion efficiency below 89% and 85%, respectively. A Single Ended Primary Inductor Converter (SEPIC) is designed for a battery charger in [14]. In this work, the desirable buck-boost capability of the converter increases the available voltage range and pushes the Maximum Power Point Tracking (MPPT) efficiency up to 99.2%, but no indication on the conversion efficiency is provided. Other solutions consider a parallel-load resonance [15] or a series-parallel resonance [16] to minimize the switching losses of the semiconductor devices. In both solutions, the strongly non-linear static characteristic allows to achieve a wide variation of operating powers in a restricted frequency range. However, these converters are typically optimized to work at a constant frequency (slightly above the resonance frequency), requiring an additional conversion stage [15] or exhibiting deteriorated efficiencies at other working points [16]. A generalized multi-stage resonant switched-capacitor converter is presented in [17], achieving a high and flat conversion efficiency (between 93.3% and 95.3% in the wide 10 W – 100 W range) thanks to the ZCS of the switches, at the expenses of a large number of components and of a fixed voltage conversion ratio.

In our previous work, a quasi-resonant (qR) battery charger for 24 V-rated PV panels was proposed [18]. The quasi-resonant converter operates in the Discontinuous Voltage Mode (DVM), already described in [19], but applied for the first time to PV applications. The present work extends [18] with a full analytical modelling of the converter in its two operating modes and its experimental validation. In addition, a step-by-step generalized design procedure is proposed. Finally, a 100 W prototype is tested on a wide range of operating powers to validate the performances, for different input and battery voltage conditions.

The remaining part of this paper is organized as follows: Section II presents the main features of the converter topology, while Section III analytically describes the converter operation within a switching cycle in its two operating regions. The equivalent circuit modelling and the step-by-step derivation of the static characteristic are provided as well. Section IV presents a generalized design flowchart and its application to a 100 W prototype compliant with a thin-film PV module and a 12 V lead-acid battery. Section V reports the

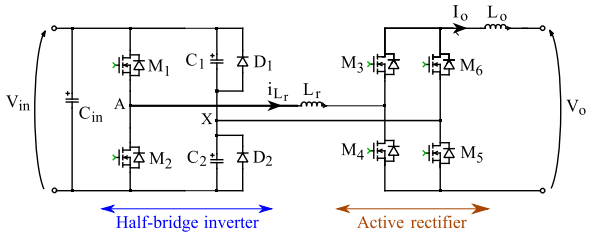


FIGURE 2. Schematic of the proposed quasi-resonant battery charger.

experimental validation of the prototype, while conclusions are drawn in Section VI.

II. PROPOSED CONVERTER TOPOLOGY

This section describes the proposed converter topology, outlining the distinctive features and novelties compared to the state of the art.

The grid-fed battery charger presented in [19] exploits a resonant inductance to achieve the soft commutation of the input MOSFETs, without increased voltage or current stresses on the semiconductor devices. The converter can be designed to achieve the ZVS on a wide input power range and thus it represents an interesting candidate for PV-fed battery chargers.

The converter topology is shown in Fig. 2 and consists in a frequency-modulated half-bridge inverter (MOSFETs M_1 and M_2 and capacitors C_1 and C_2, with $C_1 = C_2 = C$) followed by an active rectifier.

M_1 and M_2 are controlled with 180° phase shift and 50% duty cycle, so as to ensure a symmetric operation of the converter in the two half switching periods. To avoid cross-conduction, the conduction times of the MOSFETs are separated by a dead time t_{dead}.

Two clamping diodes D_1 and D_2 are connected in parallel to C_1 and C_2, respectively.

An input capacitor C_{in} at the input port helps stabilizing the working point of the PV source, whereas the output inductor L_{o} filters the high-frequency harmonics of the output current I_{o} to provide a smooth charging of the battery.

The active rectifier, consisting of MOSFETs M_3, M_4, M_5 and M_6, provides a full-wave rectification of the intermediate AC voltage generated between nodes A and X. Despite the additional driving complexity, an active rectifier eliminates the voltage drops of a diode bridge, which reduce the conversion efficiency especially at low voltage loads.

The inductor L_{r}, originally present in [19], is connected to the switching node A to assist the ZVS turn-ON of M_1 and M_2, by resonating with their output parasitic capacitances.

Unlike in conventional half-bridge converters, C_1 and C_2 are not supposed to keep a stable voltage at node X. They are designed to be alternately charged and discharged between 0 V and V_{in} by the output current I_{o}. The clamping action of D_1 and D_2 limits the maximum energy that each capacitor can store and release in a switching cycle. The result is that the voltage at node X features a distinctive trapezoidal shape, giving the name to the DVM [19].

Despite the similarities with the converter topology presented in [19], the proposed one does not include a transformer, adopts an active rectifier and is specifically designed to operate with high efficiency over a wide frequency and input power range, as demanded to meet the requirements of PV-fed battery chargers under variable operating conditions. In addition, the mathematical modelling of the converter operation is extended to another working mode, not previously explored. The proposed modelling represents the basis for the implementation of a closed-loop MPPT controller.

III. CONVERTER OPERATION AND MODELLING

For the sake of the converter analysis in a switching cycle, the following assumptions are made:

- the input capacitor C_{in} maintains a constant DC input voltage V_{in};
- the output filter inductor L_o maintains a constant DC output current I_o;
- the half-bridge MOSFETs M_1 and M_2 are ideal, except for their output parasitic capacitances C_{s1} and C_{s2} (with $C_{s1} = C_{s2} = C_s$);
- the forward voltage drops of the clamping diodes and MOSFETs body diodes are neglected;
- the reactive components C_1, C_2, C_{in}, L_r and L_o are lossless and ideal.

The operating mode of the converter depends on the switching frequency of the half-bridge MOSFETs. At sufficiently low frequencies, the converter operates in the DVM and its temporal behaviour in a half period can be split in 3 phases. Given the symmetric operation of the converter, an equivalent analysis can be performed for the other half period. Above a certain boundary frequency $f_{boundary}$, as it will be discussed later, the converter exits the DVM. The analytical derivation of $f_{boundary}$ is provided in this work. For the sake of clarity, the two operating modes will be referred to as *Low frequency* (LF) and *High frequency* (HF) modes.

A. LOW FREQUENCY MODE: CONVERTER OPERATION

1) POWER TRANSFER PHASE (PT, FIG. 3a)

During this phase, M_1, M_3 and M_5 are ON and conduct the constant output current I_o, whereas M_2, M_4 and M_6 are OFF. At node X, I_o splits equally, gradually charging C_2 and discharging C_1. As a result, V_X increases linearly from 0 V to V_{in}. Assuming a constant I_o, no voltage drop appears across L_r and the rectifier primary voltage V_p assumes a triangular behaviour:

$$V_p(t) \approx V_{DS2} - V_X = V_{in} - \frac{I_o}{2C}t. \tag{1}$$

The rectifier secondary voltage V_s coincides with V_p for the entire half-period, becoming $-V_p$ in the other half. This phase ends when $V_X = V_{in}$.

2) CURRENT CIRCULATING PHASE (CC, FIG. 3b)

M_1, M_3 and M_5 are still ON. In this phase, the clamping diode D_1 gets forward biased and clamps V_X to V_{in}. The rectifier primary voltage V_p becomes zero and forces the body diodes of M_4 and M_6 to turn ON, at zero current. A free-wheeling current path for the inductor current i_{L_r} is created and no power is temporarily drawn from the supply nor transferred to the battery.

3) CROSSOVER RESONANT PHASE (CR, FIG.3c to 3e)

When M_1 is turned OFF and the dead time begins, L_r starts resonating with the MOSFETs parasitic capacitances C_{s1} and C_{s2}, as shown in Fig. 3c. As a result, V_{DS2} starts decreasing towards 0 V. This behaviour only occurs if the energy stored in the tank inductor L_r is sufficient to charge C_{s1} up to the input voltage. This condition translates into a lower boundary for L_r:

$$L_r > \frac{2C_s V_{in}^2}{I_o^2}. \tag{2}$$

If (2) is satisfied, V_{DS2} reaches 0 V and the body diode of M_2 gets forward-biased, as shown in Fig. 3d. The voltage V_X (almost constant during this short phase) induces a linear discharge of i_{L_r}:

$$i_{L_r} = I_o - \frac{V_{in}}{L_r}t. \tag{3}$$

The difference between i_{L_r} and I_o flows through the body diodes of M_4 and M_6. From the currents balance at the input and output nodes of the rectifier, the rectifier MOSFETs source-to-drain currents derive consequently:

$$i_{M_3} = i_{M_5} = \frac{I_o}{2} + \frac{i_{L_r}}{2} \tag{4}$$

$$i_{M_4} = i_{M_6} = \frac{I_o}{2} - \frac{i_{L_r}}{2}. \tag{5}$$

If the dead time t_{dead} is sufficiently short, M_2 is turned ON while its body diode is still conducting, at zero voltage. The maximum allowed dead time $t_{dead,max}$ to achieve ZVS is limited by the time required for the full discharge of C_{s2} (denoted by t_1), plus the time for i_{L_r} to become null. After this time, indeed, L_r starts resonating again with C_{s1} and C_{s2}, and the ZVS condition is lost. Assuming a linear current discharge:

$$t_{dead,max} \approx t_1 + \frac{L_r I_o}{V_{in}}. \tag{6}$$

Together with M_2, also M_4 and M_6 are turned ON (Fig. 3e) at zero voltage. With an accurate control of the driving signals, as suggested by (4), M_3 and M_5 can be turned OFF at zero current when $i_{L_r} = -I_o$. The CR phase is concluded when M_3 and M_5 are turned OFF.

Fig. 4 shows the main converter waveforms in a complete switching cycle, in the LF mode. It is important to observe that the duration of the CR phase is exaggerated in the figure for a better visualization. In practical cases, the CR phase represents just a small fraction of the half period (2% or less).

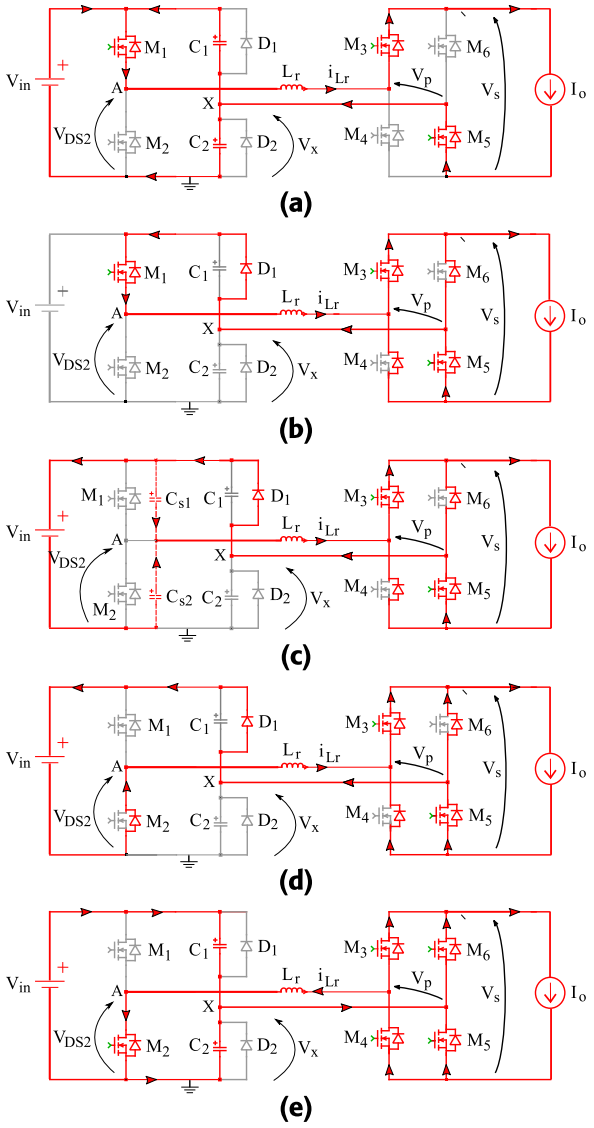


FIGURE 3. Equivalent circuits of the qR charger during a half-period, in the LF region. (a) PT mode. (b) CC mode. (c) CR mode: L_r resonates with the output parasitic capacitances of M_1 and M_2. (d) CR mode: the body diode of M_2 starts conducting. (e) CR mode: M_2 is turned ON and L_r is forced to be discharged.

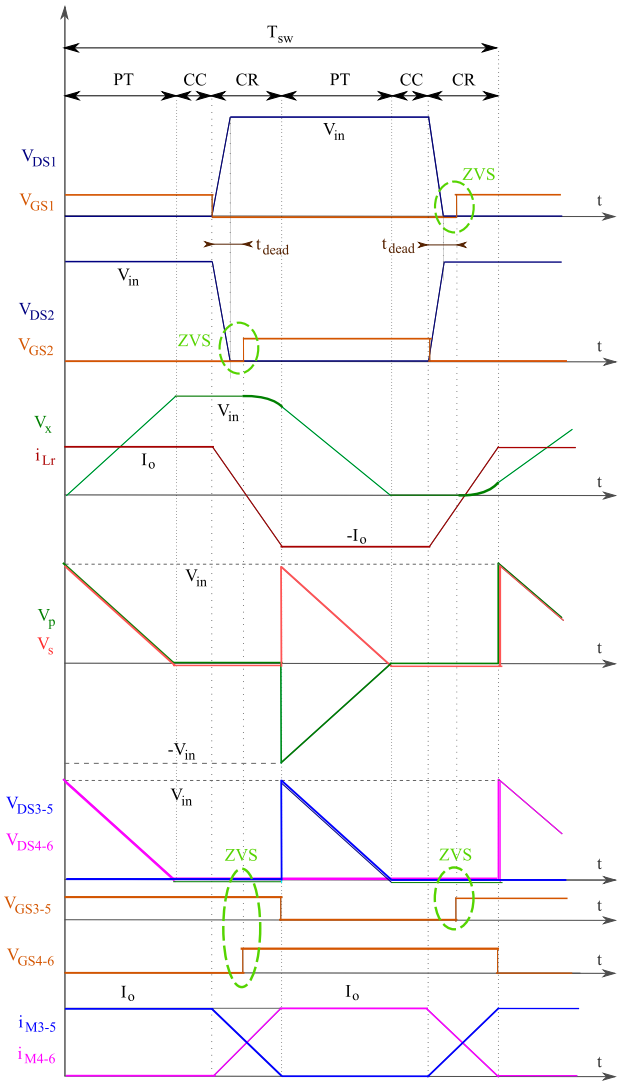


FIGURE 4. Main voltage and current waveforms in a switching period, in the LF region.

B. LOW FREQUENCY MODE: CONVERTER MODELLING

In the LF mode, the capacitors C_1 and C_2 always store and release in a period the same amount of energy, defined by:

$$\mathscr{E}_C = \frac{1}{2} C V_{in}^2. \tag{7}$$

As a consequence, as derived in [19], the transferred power P_{out} exhibits a linear dependence on the switching frequency:

$$P_{out} = 2 C V_{in}^2 f_{sw}. \tag{8}$$

Assuming no power loss in the rectifier and a constant voltage source V_{batt} model for the battery, the converter can be modelled as a voltage- and frequency-dependent current generator:

$$I_o \approx \frac{2 C f_{sw} V_{in}^2}{V_{batt}}. \tag{9}$$

At steady-state, assuming no voltage drop across L_o, the average value of the triangular-shaped V_s coincides with the charging voltage of the battery. As a consequence, to ensure a positive power flow, the following voltage constraint holds:

$$V_{in} > 2 V_{batt}. \tag{10}$$

C. HIGH FREQUENCY MODE: CONVERTER OPERATION

1) POWER TRANSFER PHASE (PT, FIG. 5a)

The operating principle of this phase is equivalent to the one described for the LF region. The constant output current I_o, flowing through M_1, M_3 and M_5, charges C_2 and discharges C_1. In the HF region, however, the DVM is not achieved and the CC phase does not exist. As a consequence, the initial

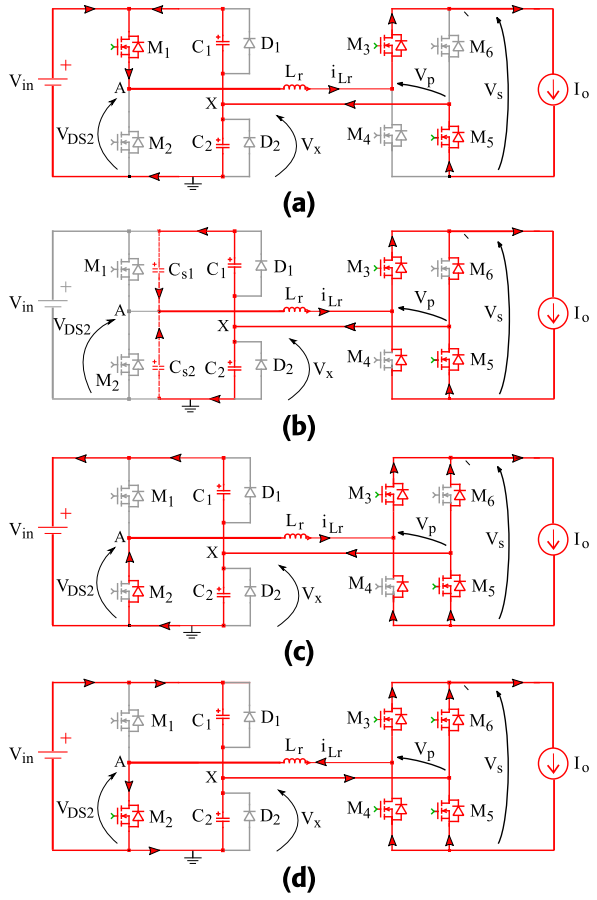


FIGURE 5. Equivalent circuits of the qR charger during a half-period, in the HF region. (a) PT mode. (b) CR mode: L_r resonates with the output parasitic capacitances of M_1 and M_2. (c) CR mode: the body diode of M_2 starts conducting. (d) CR mode: M_2 is turned ON and L_r is forced to be discharged.

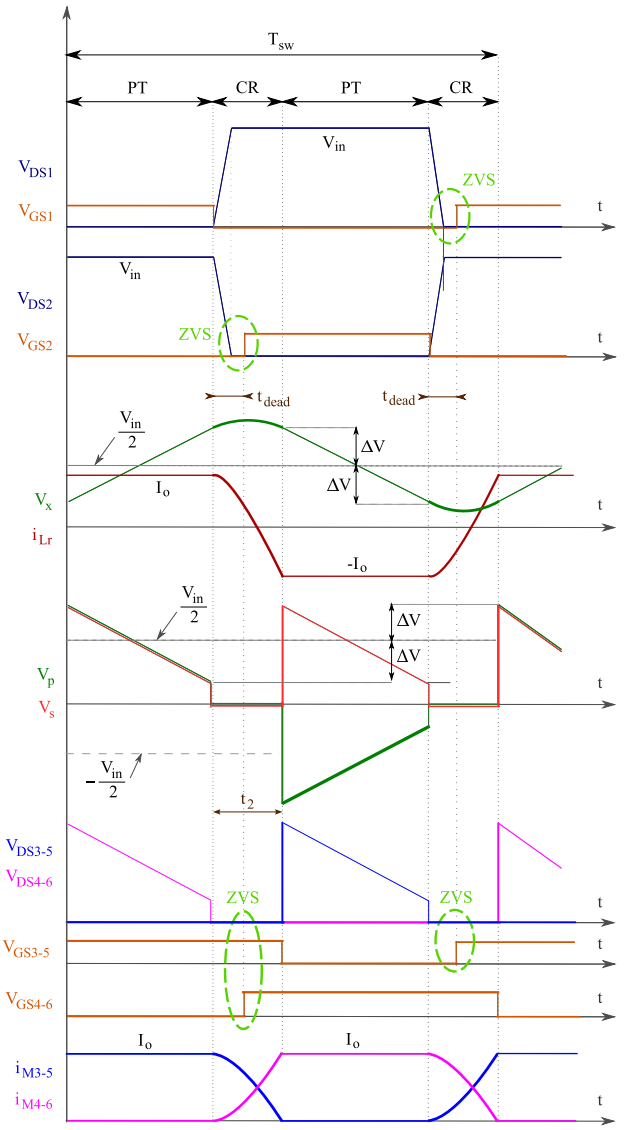


FIGURE 6. Main voltage and current waveforms in a switching period, in the HF region.

voltage at node X, contrarily to the LF region, is no more 0 V, but a certain positive voltage:

$$V_X(0) = \frac{V_{in}}{2} - \Delta V. \tag{11}$$

ΔV is not known a-priori, but is uniquely determined once the input voltage, the battery voltage and the switching frequency are known; the analytical evaluation of ΔV is proposed in Section III-D and is the basis for the derivation of the static characteristic. The voltage V_X linearly increases with slope $\frac{I_o}{2C}$. Meanwhile, V_p decreases linearly:

$$V_p(t) \approx V_{DS2} - V_X = \frac{V_{in}}{2} + \Delta V - \frac{I_o}{2C}t. \tag{12}$$

At the end of the PT phase, when M_1 is turned OFF, it can be assumed by the symmetry of operation that the node X voltage is $\frac{V_{in}}{2} + \Delta V < V_{in}$.

2) CROSSOVER RESONANT PHASE (CR, FIG. 5b to 5d)

When M_1 turns OFF, as in the LF region, L_r resonates with C_{s1} and C_{s2}, causing the voltage V_{DS2} to decrease until the body diode of M_2 gets forward biased (Fig. 5b). Again, this condition can occur only if (2) is satisfied. V_X is assumed constant during the fall of V_{DS2}.

The body diodes of M_4 and M_6 get forward biased during this phase and start sinking current from L_r, as in the LF region. Both V_p and V_s are null.

Once the body diode of M_2 gets forward biased and clamps V_{DS2} to 0 V, L_r starts resonating with C_1 and C_2 (Fig. 5c). The resonant mode is described by the linear system (13):

$$\begin{cases} 2C\dfrac{dV_X}{dt} - i_{L_r} = 0 \\ V_X + L_r\dfrac{di_{L_r}}{dt} = 0, \end{cases} \tag{13}$$

whose resonance frequency is $\omega_{res} = \frac{1}{\sqrt{2CL_r}}$. In practical cases, the duration of the CR phase is short enough to allow

a first-order Taylor approximation of the solutions of (13):

$$\begin{cases} V_{\mathrm{X}}(t) \approx \dfrac{V_{\mathrm{in}}}{2} + \Delta V \\ i_{\mathrm{L_r}}(t) \approx I_{\mathrm{o}} - 2C\omega_{\mathrm{res}}^2 \left(\dfrac{V_{\mathrm{in}}}{2} + \Delta V\right) t. \end{cases} \tag{14}$$

The distribution of the currents in the rectifier devices is once again described by (4) and (5). As in the LF region, the ZVS of M_2 can be achieved if it is turned ON while its body diode is still in conduction. The maximum allowed dead time can be computed as in (6). After the dead time, M_2, M_4 and M_6 are turned ON (Fig. 5d), all of them at zero voltage, minimizing the switching losses.

The time t_2 required by $i_{\mathrm{L_r}}$ to completely reverse (from I_{o} to $-I_{\mathrm{o}}$) can be explicitly computed in the approximation of linear fall of $i_{\mathrm{L_r}}$, from (14):

$$t_2 \approx \frac{2I_{\mathrm{o}}}{2C\omega_{\mathrm{res}}^2 \left(\frac{V_{\mathrm{in}}}{2} + \Delta V\right)} = \frac{2L_{\mathrm{r}}I_{\mathrm{o}}}{\frac{V_{\mathrm{in}}}{2} + \Delta V}. \tag{15}$$

Fig. 6 shows the main converter waveforms in a complete switching cycle, in the HF mode.

D. HIGH FREQUENCY MODE: CONVERTER MODELLING

Differently from the LF region, where the electrical charge stored and released by C_1 and C_2 is only dependent on the input voltage ($C \cdot V_{\mathrm{in}}$), in the HF it exhibits a more complex and non-linear expression.

The derivation of the static characteristic $P_{\mathrm{out}}(f_{\mathrm{sw}})$ in the HF region can be carried out by averaging the trapezoidal output voltage of the rectifier, that coincides with the charging voltage across the battery. As described, V_{s} exhibits the following behaviour:

$$V_{\mathrm{s}}(t) = \begin{cases} \dfrac{V_{\mathrm{in}}}{2} + \Delta V - \dfrac{I_{\mathrm{o}}}{2C}t & \text{if } t \in \text{PT phase} \\ 0 & \text{if } t \in \text{CR phase.} \end{cases} \tag{16}$$

Assuming that the CR phase duration coincides with t_2, the average value of V_{s} becomes:

$$\begin{aligned} \overline{V_{\mathrm{s}}} &= \frac{2}{T_{\mathrm{sw}}} \int_0^{\frac{T_{\mathrm{sw}}}{2}} V_{\mathrm{s}}(t)\, dt = \frac{2}{T_{\mathrm{sw}}} \frac{V_{\mathrm{in}}}{2} \left(\frac{T_{\mathrm{sw}}}{2} - t_2\right) \\ &= \frac{V_{\mathrm{in}}}{2} - Z_{\mathrm{eq}} I_{\mathrm{o}}, \end{aligned} \tag{17}$$

where:

$$Z_{\mathrm{eq}} = \frac{2V_{\mathrm{in}}L_{\mathrm{r}}f_{\mathrm{sw}}}{\frac{V_{\mathrm{in}}}{2} + \Delta V}. \tag{18}$$

The equivalent averaged circuit model of the output side of the converter reduces to a resistive loop, as shown in Fig. 7, in which Z_{eq} is linked to the reactive impedance of L_{r}, R_{ext} combines the resistive losses in the output loop (such as the filter inductor, rectifier and cables losses), and R_{batt} is the battery internal resistance. For compactness of notation, the total ohmic losses are embedded in $R_{\mathrm{ohm}} = R_{\mathrm{ext}} + R_{\mathrm{batt}}$.

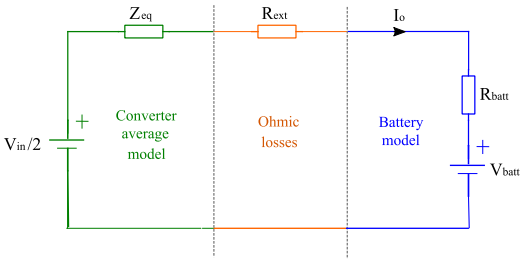


FIGURE 7. Averaged simplified equivalent circuit of the converter in the HF region.

The current flowing in the output loop can be expressed as function of the unknown ΔV:

$$I_{\mathrm{o}}(\Delta V) = \frac{\frac{V_{\mathrm{in}}}{2}(1 - \alpha_{\mathrm{V}})}{Z_{\mathrm{eq}}(\Delta V) + R_{\mathrm{ohm}}}, \tag{19}$$

where $\alpha_{\mathrm{V}} = \frac{2V_{\mathrm{batt}}}{V_{\mathrm{in}}}$. Once again, the converter transfers power to the battery only when (10) is satisfied. To explicitly evaluate I_{o} and ΔV, an additional equation needs to be set. This can be derived recalling that, during the PT phase, the node X voltage increases by $2\Delta V$ under the effect of the output current:

$$I_{\mathrm{o}}(\Delta V) = 2C \frac{2\Delta V}{\frac{T_{\mathrm{sw}}}{2} - t_2}. \tag{20}$$

Combining (19) and (20), a third-order equation is obtained in ΔV:

$$P_3 \Delta V^3 + P_2 \Delta V^2 + P_1 \Delta V + P_0 = 0, \tag{21}$$

where:

$$\begin{cases} P_3 = \dfrac{4R_{\mathrm{ohm}}^2}{V_{\mathrm{in}}} \\ P_2 = R_{\mathrm{ohm}} \cdot \left[4\left(R_{\mathrm{ohm}} + 4L_{\mathrm{r}}f_{\mathrm{sw}}\right) - \dfrac{1 - \alpha_{\mathrm{V}}}{4Cf_{\mathrm{sw}}}\right] \\ P_1 = V_{\mathrm{in}}\left(R_{\mathrm{ohm}} + 4L_{\mathrm{r}}f_{\mathrm{sw}}\right)^2 + \dfrac{V_{\mathrm{in}}L_{\mathrm{r}}}{2C}(1 - \alpha_{\mathrm{V}})^2 \\ \qquad - \dfrac{R_{\mathrm{ohm}} + 2L_{\mathrm{r}}f_{\mathrm{sw}}}{2Cf_{\mathrm{sw}}} \dfrac{V_{\mathrm{in}}}{2}(1 - \alpha_{\mathrm{V}}) \\ P_0 = -\left(\dfrac{V_{\mathrm{in}}(1 - \alpha_{\mathrm{V}})}{2}\right)^2 \cdot \left[\dfrac{R_{\mathrm{ohm}} + 4L_{\mathrm{r}}f_{\mathrm{sw}}}{4Cf_{\mathrm{sw}}(1 - \alpha_{\mathrm{V}})} + \dfrac{L_{\mathrm{r}}}{C}\right]. \end{cases} \tag{22}$$

Eq.(21) could be solved by recurring to the Cardano's method for third-order equations. However, when the ratio of the second and third order terms $P_2(f_{\mathrm{sw}})/P_3$ is proved to be much larger than the maximum value that ΔV can assume (i.e. V_{in}), the third-order term can be neglected from (21) and the explicit solution becomes:

$$\Delta V = \frac{-P_1 + \sqrt{P_1^2 - 4P_2P_0}}{2P_2}. \tag{23}$$

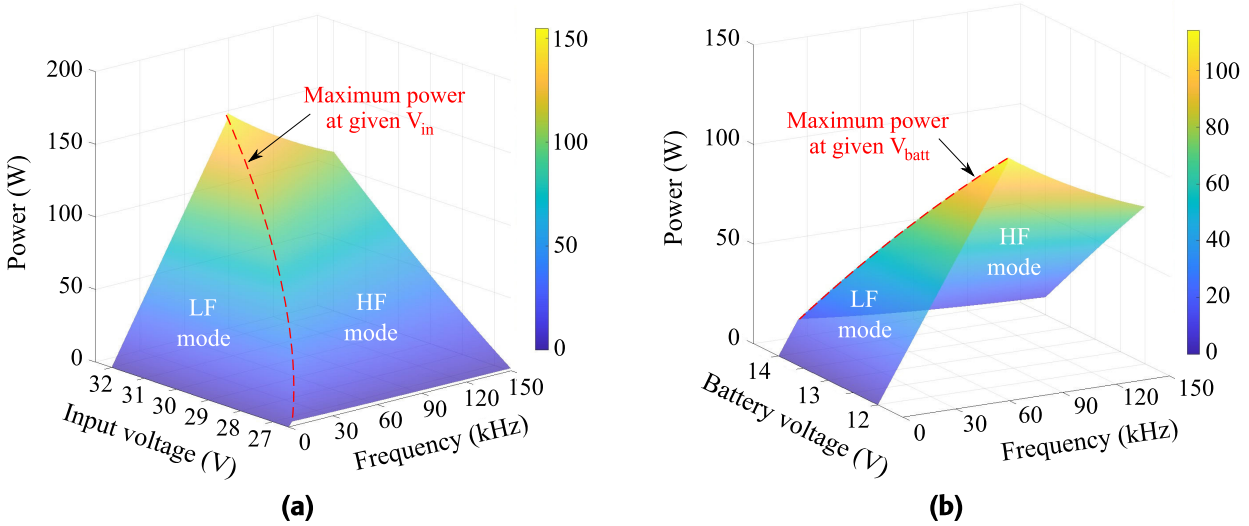


FIGURE 8. Analytical 3-D plots of the static characteristic of the proposed converter. (a) Output power as function of V_{in} and f_{sw}, at $V_{batt} = 13.2\,V$; (b) Output power as function of V_{batt} and f_{sw}, at $V_{in} = 28.5\,V$.

After computing ΔV, $I_o(f_{sw}, V_{in}, V_{batt})$ follows from (19), and the charging power transferred to the battery becomes:

$$P_{out,HF} = I_o \cdot (V_{batt} + R_{batt} I_o)\,. \tag{24}$$

According to (24), the resulting behaviour of the output power in the HF mode is approximately hyperbolic with f_{sw}. At fixed frequency operation, the increase of battery voltage leads to an automatic output power reduction: this is a substantial difference with the LF region, where the output power does not depend on the battery voltage.

The boundary frequency $f_{boundary}$, defining the transition from the LF to the HF mode, can be derived imposing the continuity of the output power:

$$P_{out,LF}(f_{boundary}) = P_{out,HF}(f_{boundary}). \tag{25}$$

The resulting second-order equation leads to the explicit solution:

$$f_{boundary} = \sqrt{\left(\frac{R_{ohm}}{4L_r}\right)^2 + \frac{\alpha_V\,(1-\alpha_V)}{16CL_r}} - \frac{R_{ohm}}{4L_r}. \tag{26}$$

Since $f_{boundary}$ is the switching frequency at which the maximum power can be transferred, it can be adopted as a design parameter for sizing the converter according to given specifications, as it will be explained in Section IV.

Figs.8a and 8b show the 3-D plots of the static characteristic of the converter as function of frequency and of the input and battery voltage, respectively. The dashed lines represent the boundary between the LF and HF modes. Following (26), it is clear that an increase of V_{in} or reduction of V_{batt} move $f_{boundary}$ at higher frequencies and larger powers can be achieved. On the contrary, an increased battery voltage during the charging process causes an automatic limitation of the transferred power. Notice that, due to the hyperbolic-like behaviour of the static characteristic in the HF mode, a much wider frequency sweep is required to cover the same power window.

TABLE 1. Target specifications and design parameters of the converter.

Design specification	Value	Design parameter	Value
$V_{in,rated}$	28.5 V	$f_{rated,min}$	60 kHz
$V_{batt,min} - V_{batt,max}$	12 V − 13.5 V	η_{target}	90%
P_{rated}	100 W	$P_{min,ZVS}$	30 W

IV. CONVERTER DESIGN

In this section, the design procedure adopted for a 100 W prototype is illustrated. The whole design process starts from the definition of the target battery specifications, specifically the minimum charging voltage $V_{batt,min}$, the maximum charging voltage $V_{batt,min}$, the rated charging current I_{rated} and the battery internal resistance R_{batt}. Reminding the voltage constraint imposed by (10), not all the PV modules are equally suited for any battery selection. In this work, a lead-acid 12 V-battery was targeted and, as a consequence, only 24 V-rated PV modules can be chosen. Specifically, to ensure the possibility to extract the maximum power P_{rated} and to ensure a positive net power flow over the entire recharge cycle, the panel rated voltage $V_{in,rated}$ and open-circuit voltage V_{OC} should satisfy (27) and (28), respectively.

$$V_{MPP} > 2V_{batt,min} \tag{27}$$

$$V_{OC} > 2V_{batt,max} \tag{28}$$

In this design, the components selection was tuned for the panel and battery specifications reported in Tab.1. Suitable PV panels for this application are, for instance, Copper Indium Gallium Selenide (CIGS) modules Bluesun BSM-FLEX-130N [20] or Unisun FLEX-03N [21]. Once selecting the target source and load, the worst-case voltage and current stresses can be computed for each component.

All MOSFETs conduct the output current for approximately half switching period (neglecting the duration of the CR phase). As a consequence, all of them exhibit the same RMS current ($I_o/2$) and peak current (I_o). While the maximum drain-to-source voltage of M_1 and M_2 is bounded by V_{in}, the rectifier MOSFETs are subjected to large voltage spikes immediately after their turn-OFF. The reason is that, when a couple of MOSFETs turns OFF at the end of the half switching period, the residual current $I_o - i_{L_r}$ flows in their parasitic capacitances, causing large resonant voltage spikes. Based on simulations, a conservative value larger than $2V_{in,rated}$ is recommended for the breakdown voltage of M_{1-4}. Since all the MOSFETs turn ON at zero voltage, minimizing the switching losses, a low conduction resistance $R_{DS,ON}$ is needed to reduce the conduction losses as well. An additional desired feature for the MOSFETs is a low switching time (both in turn-ON and OFF), given the need to control with precision the dead time period to achieve the ZVS. 100 V − 92 A MOSFETs were selected, driven by three half-bridge gate drivers. The MOSFETs C_s, which constraints the achievement of the ZVS, was computed as the charge-equivalent output capacitance storing the same amount of charge of the non-linear datasheet C_{oss} at a given output voltage v_{DS} [22]:

$$C_s(v_{DS}) = \frac{\int_0^{v_{DS}} C_{oss}(v')dv'}{v_{DS}}. \tag{29}$$

The design procedure for C and L_r is illustrated in Fig. 9. The combined choice of $C - L_r$ depends on multiple design parameters (reported in Tab.1) and affects both the achievement of the ZVS of $M_1 - M_2$ on a desired power range and the possibility to harvest the rated power.

A lower bound for L_r derives by imposing the ZVS condition in (2) for a minimum output power $P_{min,ZVS}$:

$$L_r > 2C_s \left(\frac{V_{in,rated} V_{batt}}{P_{min,ZVS}} \right)^2. \tag{30}$$

The other constraint on L_r derives from the actual possibility to harvest the rated power at the rated panel voltage. Since the static characteristic of the converter exhibits the absolute maximum at $f_{boundary}$, it is necessary to impose:

$$2CV_{in,rated}^2 \cdot f_{boundary}(R_{ohm}, \alpha_V, C, L_r) \geq P_{rated}. \tag{31}$$

Notice that α_V is computed at $V_{in,rated}$ and at a desired battery voltage ($V_{batt} = 12.5$ V), whereas a conservative value of R_{ohm}, linked to the total resistive losses in the converter, can be set from the desired target efficiency $\eta_{target} = 90\,\%$ at rated power:

$$R_{ohm} = (1 - \eta_{target}) \frac{P_{rated}}{I_{rated}^2}. \tag{32}$$

From (26) and (31), an upper bound of L_r follows:

$$L_r < C \cdot R_{in,rated}^2 \left(\frac{\alpha_V(1-\alpha_V)}{4} - \frac{R_{ohm}}{R_{in,rated}} \right), \tag{33}$$

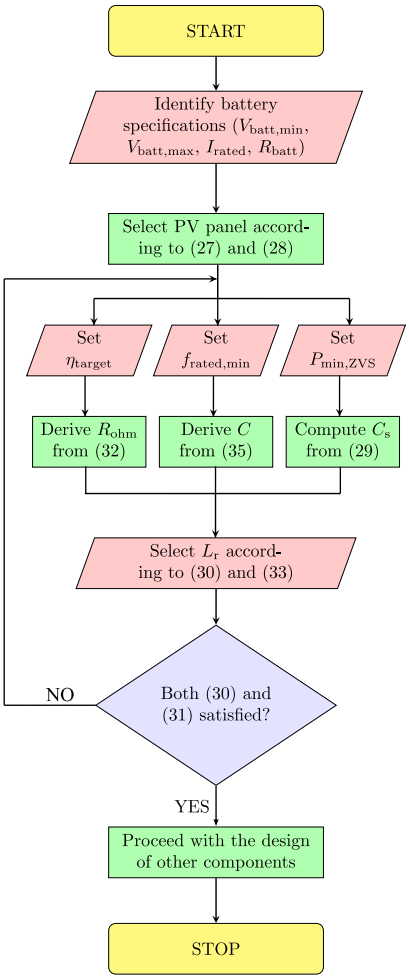


FIGURE 9. Generalised design flowchart for the qR battery charger.

where, for compactness of notation:

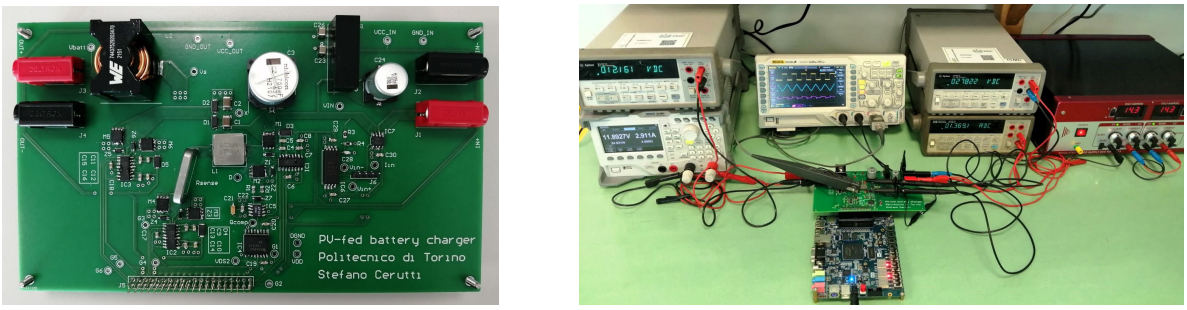
$$R_{in,rated} \triangleq \frac{V_{in,rated}^2}{P_{rated}}. \tag{34}$$

A preliminary selection of C can be done by imposing a minimum switching frequency $f_{rated,min} = 60$ kHz at which the rated power is harvested in the LF mode, to relax the filtering requirements of the output inductor L_o:

$$C = \frac{P_{rated}}{2f_{rated,min} V_{rated}^2}. \tag{35}$$

From (35), the maximum capacitance C is $\approx$ 1 µF. From (30) and (33), L_r should be selected in the 349 nH − 468 nH range. As illustrated in Fig. 9, the selection of C and L_r is iterated until both (30) and (31) are satisfied. In some cases, it may be necessary to relax $P_{min,ZVS}$ or select MOSFETs with lower C_s.

C_1 ad C_2 are subjected to a $I_o/2$ current stress and V_{in} voltage stress. An additional desirable feature is a stable capacitance towards frequency variations. Multi-Layer Ceramic Capacitors (MLCC) were selected, with 940 nF capacitance, 50 V rated voltage and 12 A rated current.



(a) (b)

FIGURE 10. Pictures of the experimental setup: (a) Top layer view of the PCB prototype; (b) Picture of the testbench.

L_r conducts a pure-AC square-wave current whose RMS value is $\approx I_o$. A ferrite-core 330 nH inductor was selected, exhibiting low DC resistance (1.3 mΩ), 36.5 A rated current for 40 °C temperature increase, and 62 A saturation current for a 20% inductance decrease. The selected inductance value is slightly outside the computed range, meaning that the ZVS condition will be ensured from output powers slightly above the designed $P_{\text{min,ZVS}}$.

The clamping diodes D_1 and D_2 should be chosen so that their breakdown voltage is larger than V_{in} and they conduct, only in the LF mode, the average current expressed in (36):

$$\overline{I_{\text{diode}}} \approx \frac{I_o}{2} - 2Cf_{\text{sw}}V_{\text{in}}. \tag{36}$$

Schottky-barrier diodes with 8 A rated current and 45 V breakdown voltage were selected.

The input capacitor C_{in} should be sized to suppress the fluctuations in the input current. A fluctuating working point, indeed, decreases the maximum harvested power from a PV panel. The authors in [23] propose a model-based analytical relation between the output power decrease and the AC current ripple superimposed to the average MPP current. A 8% AC current ripple superimposed to the MPP current causes, for instance, almost 7% power reduction. In [24], an analogous approach recommends to limit the voltage ripple across a PV panel below the 8.5 $\%V_{\text{MPP}}$ in order to maintain the average extracted power above the 98 $\%P_{\text{MPP}}$. These constraints should be coupled with the small-signal equivalent resistance of the target PV panel at the MPP [25]: the capacitor should provide a lower impedance path for the pulsed input current. By considering the worst case input current ripple, the input capacitor ESR should be maintained below $\approx$ 540 mΩ. From the balance of currents at the input node, the RMS capacitor current results:

$$I_{\text{C}_{\text{in}},\text{RMS}} \approx 2Cf_{\text{sw}}V_{\text{in}}\sqrt{\frac{V_{\text{in}}}{2V_{\text{batt}}} - 1}. \tag{37}$$

At the rated operating condition, $I_{\text{C}_{\text{in}},\text{RMS}} \approx 1.3$ A. An Aluminum electrolytic capacitor was selected with 63 V rated voltage, 750 µF, 68 mΩ ESR and 2.5 A rated ripple current.

The output filter inductor L_o was designed to limit the current ripple superimposed to I_o below the safety limit recommended by [26] for Valve-Regulated Lead-Acid (VRLA) batteries. The integration of the voltage waveform of L_o results in an approximately parabolic ripple current whose amplitude is expressed by:

$$\Delta I_o \approx \frac{V_{\text{in}}}{16f_{\text{sw}}L_o}. \tag{38}$$

Considering, as an example, a 50 A h battery, the ripple current should be limited to 2.5 A and the minimum inductance ensuring this constraint at the rated conditions is 10.8 µH. The inductor rated current should be larger than $I_{\text{o,max}}$.

The selected ferrite-core inductor exhibits 47 µH inductance, 8.8 mΩ DC resistance, 13 A saturation current (associated to 30% inductance decrease) and 17.5 A maximum current (associated to a temperature increase of 40 °C). The selected inductance allows to limit the ripple current below 2.5 A down to 15 kHz. The selected parts for the prototype are summarized in Tab.2.

TABLE 2. Main converter components for the physical prototype.

Component	Value	Part number
L_r	330 nH	IHLP5050CEERR33M01
$C_1 - C_2$	940 nF	C1812C944J5JLC7805
C_{in}	750 µF	UCZ1J751MNS1MS
L_o	47 µH	74437529203470
$M_1 - M_6$	N/A	TPH4R10ANLL1Q
$D_1 - D_2$	N/A	V8PAL45HM3_A/I

TABLE 3. Experimental test conditions.

Parameter	Range
V_{in}	26.5 V − 28.5 V
V_{batt}	12 V − 13.5 V
P_{rated}	100 W
f_{sw}	10 kHz − 165 kHz

V. EXPERIMENTAL VERIFICATION

A 2-layer PCB was designed for the validation of the modelling and to test the performance of the proposed converter. The top-layer view of the prototype is shown in Fig. 10. The layout design focused on the minimization of the gate-source

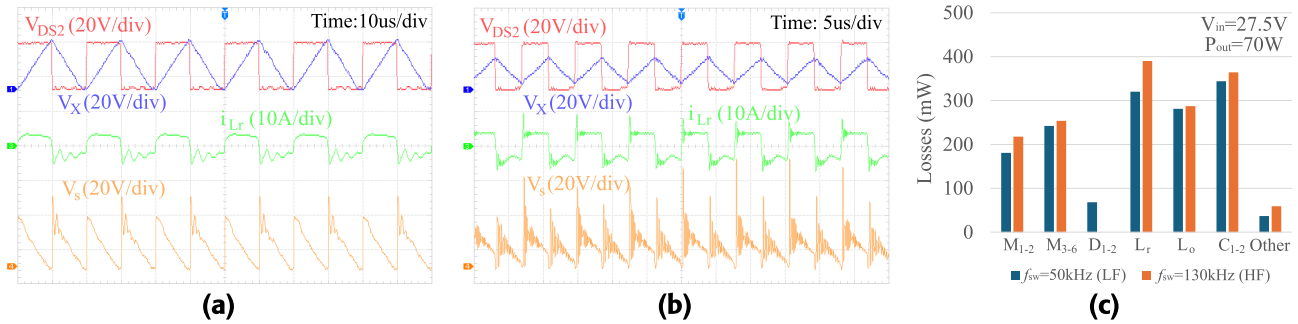


FIGURE 11. Main experimental waveforms and simulated power budget of the converter at $V_{in} = 27.5\,V$ and $V_{batt} = 12\,V$, in the LF and HF modes: (a) Waveforms in the LF mode ($f_{sw} = 50\,kHz$); (b) Waveforms in the HF mode ($f_{sw} = 130\,kHz$); (c) Comparison of simulated power budget in the LF ($f_{sw} = 50\,kHz$) and HF modes ($f_{sw} = 130\,kHz$). The total power losses are 1.57 W in the LF mode and 1.58 W in the HF mode.

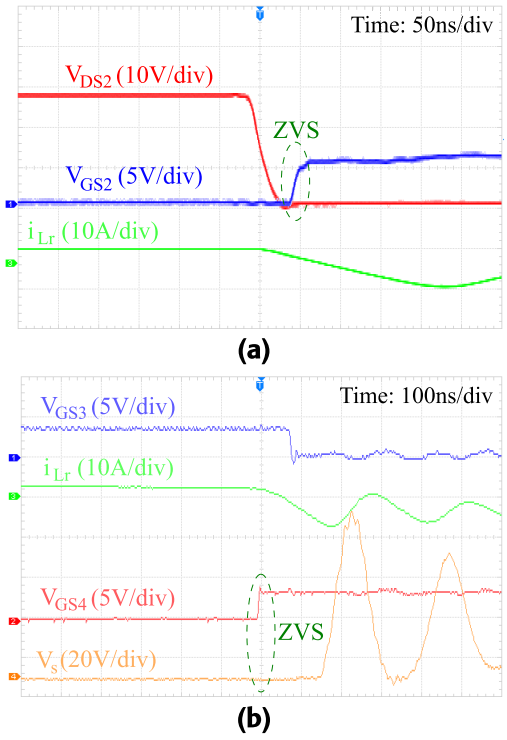


FIGURE 12. Details of the soft commutation of M_2 and M_4 for $V_{in} = 27.5\,V$, $V_{batt} = 12\,V$, $f_{sw} = 50\,kHz$). (a) ZVS turn ON of M_2. (b) ZVS turn ON of M_4.

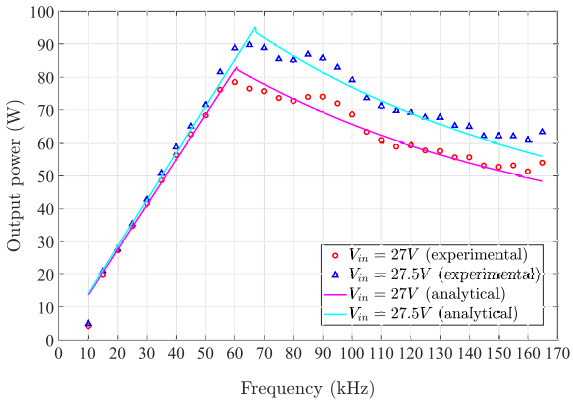


FIGURE 13. Comparison of experimental and analytical static characteristics for two different input voltage conditions ($V_{in} = 27\,V$ and $V_{in} = 27.5\,V$) and fixed battery voltage ($V_{batt} = 12\,V$).

loops at the interface between gate drivers and MOSFETs and the adoption of multiple Vertical Interconnect Accesses (VIAs) for the connections to the ground planes, to minimize the parasitic inductances and optimize the signal integrity. The driving signals for the MOSFETs were generated by an external FPGA Terasic Cyclone V SoC on a De1-SoC board. An open-loop control was developed to modify the switching frequency and MOSFETs dead time.

The complete experimental setup is shown in Fig. 10b. A DC power supply and a DC electronic load were adopted to replace the PV panel and the low voltage battery. The tested input and battery voltage ranges, and the rated power are reported in Tab.3.

A. CONVERTER OPERATION

Figs.11a and 11b show some of the relevant waveforms of the converter, namely the voltage V_X, the switching node voltage V_{DS2}, the resonant inductor current i_{L_r} and the rectifier output voltage V_s, in a LF and HF mode condition, respectively. The two operating conditions can clearly be distinguished by the triangular waveform of V_X, which sweeps from 0 V to V_{in} only in the LF mode. In both cases, the duration of the CR mode is too short to be appreciated. Notice that i_{L_r} exhibits, in the second half of the switching period, an unexpected $\approx$ 330 kHz oscillation superimposed to the square-wave behaviour, probably due to a spurious resonance of the filter inductor with the rectifier MOSFETs and layout parasitics.

A simulated estimation of the power budget of the converter is presented in Fig. 11c. The simulations were performed in LTSpice XVII and refer to the same operating conditions of Figs.11a and 11b, at 70 W output power. Despite the losses in the clamping diodes in the LF mode, the increased frequency causes larger dissipation in all the other components in the HF mode. The rectifier MOSFETs exhibit lower switching losses compared to the half-bridge switches, thanks to the ZVS turn ON and the nearly-ZCS turn OFF.

Fig. 12 shows some details of the soft commutation of the converter MOSFETs, for the following operating conditions:

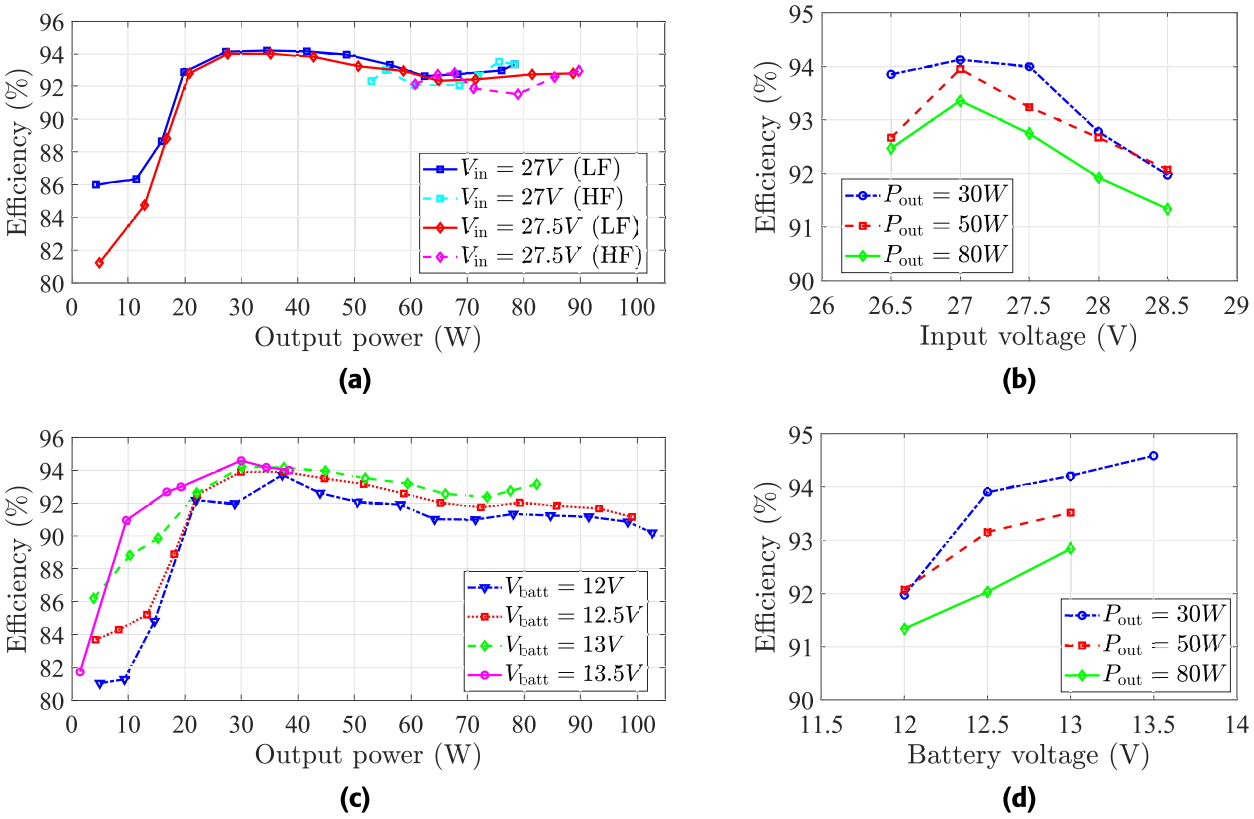


FIGURE 14. Experimental efficiency plots at various input voltage, battery voltage and output power conditions. (a) Efficiency VS power at constant $V_{batt} = 12$ V, at different V_{in} (27 V and 27.5 V); (b) Efficiency VS V_{in} at constant $V_{batt} = 12$ V, at different power conditions (30 W, 50 W and 80 W); (c) Efficiency VS power at constant $V_{in} = 28.5$ V, at different V_{batt} (from 12 V and 13.5 V); (d) Efficiency VS V_{batt} at constant $V_{in} = 28.5$ V, at different power conditions (30 W, 50 W and 80 W).

TABLE 4. Comparison of the proposed converter with the state of the art.

Reference	[7]	[12]	[13]	[14]	[15]	[16]	[17]	[19]	**Proposed**
Switching technique	Hard	Soft	Soft	Hard	Soft	Soft	Soft	Soft	**Soft**
Fixed/variable gain	Variable	Variable	Variable	Variable	Fixed	Variable	Fixed	Fixed	**Variable**
Control variable	Duty cycle	Switching frequency	Switching frequency	Duty cycle	Uncontrolled	Switching frequency	Uncontrolled	Uncontrolled	**Switching frequency**
Tested input voltage range	13.3 V - 14.7 V	24 V	17 V - 19 V	10 V - 22 V	24 V	40 V	48 V	230 V (RMS)	**26.5 V - 28.5 V**
Tested power range	3 W - 27 W	5 W - 20 W	4 W - 48 W	10 W - 80 W	80 W - 90 W	35 W - 60 W	10 W - 100 W	15 W - 65 W	**20 W - 100 W**
Min / max efficiency	83.3% / 89%	81% / 84%	57% / 85%	N/A	87% / 92%	84.4% / 90% (sim.)	93.3% / 95.3%	80% / 87%	**90.9% / 94.6%**

$V_{in} = 27.5$ V, $V_{batt} = 12$ V, $f_{sw} = 50$ kHz, 80 ns dead time. Fig. 12a highlights the ZVS turn ON of M_2, whereas Fig. 12b shows the ZVS turn ON of M_4 (V_s temporarily coincides with V_{DS4} during its turn ON).

B. STATIC CHARACTERISTIC

Fig. 13 compares the measured output powers and the analytical static characteristics, derived by (8) and (24). The plots refer to two combinations of input and output voltages (27 V/12 V and 27.5 V/12 V) selected to clearly identify the two operating modes.

In the LF mode, the experimental behaviour is optimally fitted by (8). Below 15 kHz, the resonant tank consisting of L_o and the half-bridge capacitors (resonance frequency around 16.9 kHz) induces undesired oscillations in the output current: as a consequence, the converter exits the DVM and the output power can no more be described by a linear function. In the HF mode, the experimental output power correctly

follow a hyperbolic-like behaviour. The values of R_{ohm} ensuring the best fitting were 173 mΩ (for the 27 V case) and 165 mΩ (for the 27.5 V case). Notice that, relying on (23), the expression of the output power in the HF mode can be derived explicitly, without recurring to non-linear equations solvers. The HF characteristic shows small deviations around the nominal curve which are probably related to the previously mentioned spurious resonance. According to (8), it is possible to observe that the load curve in the LF mode reduces to a purely resistive and load-independent expression:

$$R_{converter,LF} \triangleq \frac{V_{in}}{I_{in}} = \frac{1}{2Cf_{sw}}. \quad (39)$$

The intersection of the converter load curve with the PV module I-V characteristic represents the system working point. The derived model is suited for the construction of an ad-hoc MPPT controller.

C. CONVERSION EFFICIENCY

Fig. 14 presents relevant conversion efficiency plots referred to different operating conditions, to estimate the performance of the PV-fed converter in an outdoor environment. The measurements of input and output powers include the gate driving losses, while excluding the quiescent power of the integrated circuits. The dead time was set to 80 ns, which maximizes the achievement of the ZVS of the input MOSFETs in most of the operating conditions.

Fig. 14a shows two efficiency plots as function of the output power at two input voltage conditions (27 V and 27.5 V) and fixed battery voltage, 12 V. The transition from the LF to the HF mode is highlighted. From previous considerations, the covered power window in the HF mode is limited, unless very high switching frequencies are employed. The graphs appear flat for output powers between 20 W and 90 W, with less than 2% efficiency drop. For the same output power, the HF mode exhibits generally lower efficiencies, due to the increased losses at higher frequencies. At low frequency operation ($f_{sw} < 15$ kHz), when the transferred power is below 20 W, the undesired resonance between C_1, C_2 and L_o degrades the performances and prevents the ZVS of the half-bridge MOSFETs.

Fig. 14b reports three efficiency curves as function of the input voltage at three power conditions (30 W, 50 W and 80 W) and $V_{batt} = 12$ V. The switching frequency is adjusted to achieve the desired output power. The peak 94% efficiency is obtained at $V_{in} = 27$ V and 30 W. The efficiency decreases at higher input voltages because of the hard-switching losses of M_1 and M_2 at turn OFF [28], and at higher working powers for the larger conduction losses.

Fig. 14c shows some efficiency curves as function of the output power at various battery voltage conditions (between 12 V and 13.5 V) and rated input voltage, 28.5 V. The results show that the efficiency, for all the cases, is always above 90% for operating powers above 20 W. As the battery voltage increases, $f_{boundary}$ is pushed at lower frequencies according to (26), representing a self-limitation of the charging power.

Fig. 14d reports three efficiency curves as function of the battery voltage at three power conditions (30 W, 50 W and 80 W) and $V_{in} = 28.5$ V. As expected, for the same power, the efficiency increases with V_{batt}, due to the lower conduction losses. The peak 94.6% efficiency is obtained at 30 W and $V_{batt} = 13.5$ V.

Tab.4 compares the proposed converter with the state of the art PV-fed battery chargers in the literature. A specific focus is devoted to the tested range of operating powers and the minimum and maximum efficiency measurements in that range. What emerges is that the proposed converter solution exhibits the highest efficiency on the widest power range among the other variable gain converters, confirming the initial claim of a high and flat efficiency curve.

VI. CONCLUSION

A quasi-resonant battery charger is proposed in this work for off-grid outdoor PV applications. The converter operation is based on the Discontinuous Voltage Mode, applied to a new topology suited for a PV application. The full mathematical description of the converter operation in its two operating modes and the analytical derivation of the static characteristic are provided and validated experimentally. A generalized design flowchart is outlined to guide the components selection based on the target source/load and the power range at which the ZVS of the input MOSFETs is desirable. The design is applied to a 100 W prototype and the experimental results show the accuracy of the mathematical modelling and satisfactory efficiency results. Thanks to the soft commutation of the MOSFETs, the converter exhibits a high efficiency with reduced drop over a wide range of operating powers, desirable feature for outdoor PV applications. At the rated 28.5 V input voltage, the efficiency is always larger than 90% in the wide 20 W − 100 W power range, reaching an efficiency peak of 94.6% at 13.5 V battery voltage.

The reduced voltage stresses of the input components, the soft commutation of all the power devices and the low output current ripple are among the main benefits of the converter, making it suitable for a MPPT battery charger for PV applications. The main limitations of the converter are the voltage constraint on the input PV panel and the AC losses of the resonant inductor.

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