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***Abstract* — In this paper, the design of a basic self-biased stacked cell using a customized common-gate small-signal model is presented. The model extraction procedure is detailed in the paper and applied to a 0.1-µm GaAs pHEMT with 4x40-µm periphery, which is used as basic element for the design of the stacked cell. Measurements in common-source configuration together with electromagnetic simulations are used to extract an accurate model of the common gate, that is then validated against measurements in common-gate configuration. Eventually, the design of a 2-transistor stacked cell is reported, together with the simulation results. The designed cell nearly achieves the ideal 3-dB output power improvement with respect to the single device.**

***Keywords* — GaAs HEMTs, Power Amplifier, Device Modeling, MMIC, Stacked Amplifier.**

I. Introduction

Millimeter-wave (mm-wave) bands are a highly attractive solution to overcome the issues associated with the crowding of the low-frequency spectrum, to achieve communications with higher data rates, resorting to more efficient modulation schemes [1]-[3].

Achieving high performance for the analog front-end at mm-wave frequencies, in particular medium-high output-power levels from the power amplifier (PA), as well as high integration, is particularly challenging. For developing multifunctional monolithic microwave integrated circuits (MMIC) at Ka-band and above, short-gate length GaAs pHEMT technology is still very competitive. Compared to Silicon processes, it provides better linearity and noise, thanks to lower substrate loss, and higher breakdown voltages, which in turn allow for higher power density. Despite not achieving the power densities of GaN counterparts, it features higher gain at higher frequency, as well as better linearity.

The main challenges in implementing high-performance MMIC power amplifiers (PAs) at high frequencies are related to parasitic reactances that must be minimized, which requires reducing the size of individual transistors in a PA, as wider gate area implies higher intrinsic capacitances and gate sheet resistance. Moreover, larger devices show higher inductive effect and possible current imbalance among fingers that sensibly degrade performance. Consequently, achieving high output power requires stacking multiple devices.

There are three power-combining topologies that can be employed: 1- parallel connection (open circuit power combining), 2- series connection (short-circuit power combining), and 3- power combining with an arbitrary impedance to merge power from individual cells. Classical amplifier topologies rely on parallel power combinations, summing up the devices drain currents. This solution, however, requires a relatively large chip area, thus increasing cost, and reducing the optimum source and load impedances, already typically low at mm-wave, with a detrimental effect on impedance matching. Series power combination represents an alternative approach, summing up devices drain-source voltages: a solution known as stacked PA [3]. Device stacking allows for a higher drain supply voltage, representing a big advantage in low-breakdown technologies, and increases the optimum load impedance also enabling very compact layout [4]. Hence, a noteworthy advantage of the stacked PA is that it can be profitably adopted as a basic high-power and high-gain cell to be further employed in more complex PA architectures, from classical parallel combined PAs to complex architectures such as corporate PAs [5], Doherty PAs [6], etc.

Being the stacked PA composed of a common source (CS) and common gate (CG) transistor, an accurate model for both transistor configurations is needed. While foundry models are typically very accurate in predicting CS transistor performance, an ad-hoc CG model should be extracted to have a reliable design at high frequencies.

This work presents the design of a basic self-biased stacked cell based on a customized measurement-based common-gate small-signal model. The stacked cell has been designed at 27 GHz, adopting the 0.1-µm GaAs pHEMT technology from United Monolithic Semiconductors (UMS).

II. Common-Gate Model-Extraction Procedure

In the stacked cell, a common source (CS) stage is cascaded by one or more common gate (CG) stages (more details in Section III). As often happens, the foundry does not provide a dedicated common-gate model in the Process Design Kit (PDK), but what is typically available is a two- or three-terminal model based on the common-source CS configuration. This leads to inevitable inaccuracies of the CS model which is not able to accurately reproduce the CG behavior.

The main reason for inaccuracies in predicting CG behavior by CS-based model is that, in the CS, the extrinsic parasitic network of the transistor (defined at the intrinsic gate-source and drain-source reference planes) could be very different from that of the CG [7],[8], as highlighted in Fig. 1. Therefore, these inaccuracies at transistor level might limit the success of circuit design at the first foundry run.

To address this issue, we propose a procedure to extract a custom model of the CG transistor. The idea is to start with the extraction of the small-signal model of the CS transistor (i.e., extrinsic parasitic network, intrinsic capacitances and current generator parameters) by means of conventional techniques based on S-parameter measurements [9].

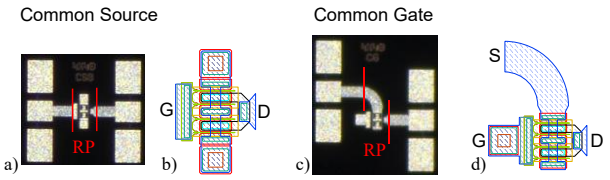

Fig. 1 Picture of the (a) common-source and (c) common-gate configurations, and (c), (d) correspondent layout. RP is the measurements Reference Plane.

After that, we can use the CS intrinsic model as the intrinsic model also of the CG transistor, whereas for the linear extrinsic parasitic network (EPN), we relied on EM simulations of the CG access structures, which were properly simulated and then connected to the intrinsic common-gate model to build the complete small-signal CG model, as shown in Fig. 2.

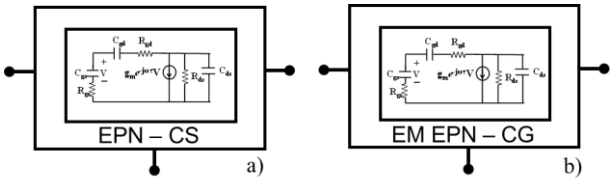

Fig. 2 (a) Common source and (b) common gate models.

To apply this procedure, we realized samples of the transistors in both CS and CG configurations, as shown in Fig 1 a) and c), to be characterized. The procedure has been applied to a 4×40-µm device, which is the size chosen for the design of the stacked cell. S-parameter measurements have been carried out over a wide bias grid, including cold-FET conditions, used to extract the EPN, and nominal bias point, used to extract the small-signal model parameters [8]. TRL calibration has been performed so that the measurement reference plane (RP) lays at the end of the half-thru (see Fig 1). After that, EM simulations of the access structure of the CG, including the "half-curve" used to connect the source, were performed up to 35 GHz. In particular, we split the access structures into three parts: the gate manifold, the drain manifold and the via and finger region. The corresponding scattering parameters resulting from the simulations were then directly used in the schematic together with the small-signal model of the CS to build the CG small-signal model. Eventually, the CG model is validated against the measurements of the CG transistor (see Fig. 1). The comparison between measurements and simulations is shown in Fig. 3. During measurements, port 1 of the VNA is connected to the source and port 2 is connected to the drain of the CG transistor. As can be seen, there is a good agreement between measurements and simulations, which confirms the effectiveness of the proposed modeling procedure. The three-terminal foundry model predictions are also reported in Fig. 3. It is evident how such a model is not able to accurately reproduce the CG measurements. Then, the proposed CG model has been used in the design of the stacked-cell as shown in the next section.

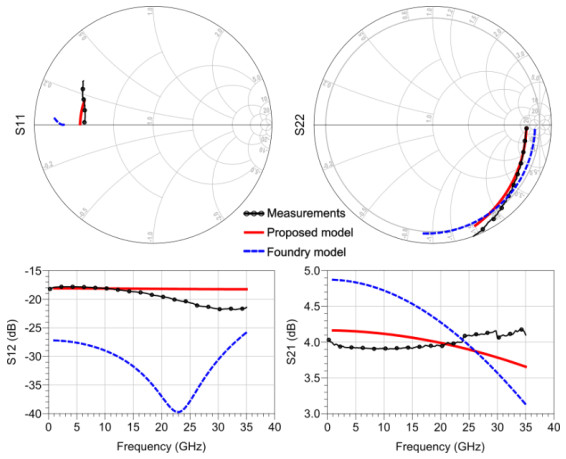

Fig. 3. Measured (symbols) and simulated (lines) S-parameters form 1 GHz to 35 GHz at the nominal bias condition for the common gate configuration. Solid red line is the proposed CG model. Dashed blue line is the CS foundry model.

III. STACKED ANALYSIS AND DESIGN FLOW

A simple *N*-device stacked PA schematic is shown in Fig. 4. It is made up of two basic stages: a CS and $(N-1)$ Pseudo-CG. The latter differs from a standard CG due to the gate capacitance function, which is not simply providing a short-circuit at the operating frequency, as in cascode PAs; instead, it plays a crucial role in device inter-stage matching. In this way every transistor in the stack should be able to provide its maximum output power, hence increasing the total gain and power of a factor *N*.

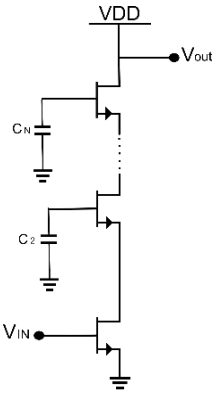

Fig. 4. *N*-device stacked cell PA topology.

The maximum number of devices that can be stacked at a specific operating frequency f is limited by the cutoff frequency of the technology f_T, according to equation (1) [3]:

$$N_{max} = \left\lfloor \frac{1}{\ln\left(1+\frac{f}{f_T}\right)} \right\rfloor \qquad (1)$$

With the selected technology, at 27 GHz, it is possible to stack more than 2 devices; however, we have chosen to adopt only 2 devices in this work due to several practical

considerations. First, this study serves as a preliminary validation of the proposed model. Additionally, while the theoretical model provides a guideline, practical limitations such as stability concerns, impedance matching challenges, and potential degradation in gain and efficiency must be carefully evaluated.

Class-AB operation is proposed due to its simplicity, lower quiescent current, and higher efficiency compared to Class-A. In the stacked structure, all the transistors must be biased at the same quiescent point to generate in-phase V_{DS} voltages. Since the stages share the same DC drain current, each transistor should have the same V_{GS}. A resistive divider is employed to provide the DC bias for CG from the cell drain supply, which is set at N times the individual transistor V_{DS}. In this way, the DC routing is simplified, allowing for considering the stacked cell as a 3-terminal device. Based on load-line theory, the desired I_D = 15 mA quiescent current requires V_{GS} = -0.15 V, when the transistors V_{DS} is set to 3 V. As shown in Fig. 5 (a), the device is inherently unstable up to around 60 GHz. To stabilize the device at all frequencies, the stability network (SN) presented in Fig. 5(b) is used, embedded with the CS gate bias network to minimize the area.

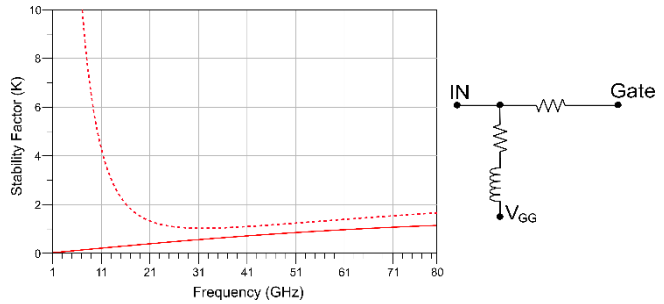

Fig. 5. (a) K stability factor, without (solid) and with SN (dashed), (b) Stabilization and gate-bias network with ideal components.

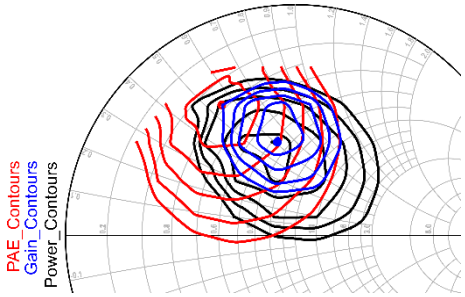

Fig. 6. Output power (black), Gain (blue) and PAE (red) load-pull contours at 1dB compression point of the 4×40-µm device at 27 GHz.

Load-pull simulation results for the 4 × 40 µm device at 27 GHz at chosen bias are shown in Fig. 6. Different optimum loads can be found for the highest output power, gain, or PAE, respectively, thus the adopted load is Z_{optCS} = (24.7 + j23.1) Ω, selected to have a good trade-off among all the performance parameters.

The Harmonic Balance (HB) simulation results of the CS device with the selected optimum load are reported in Fig. 7: at the maximum PAE of 37 %, the saturated output power is 17 dBm, while the associated gain is 9.4 dB.

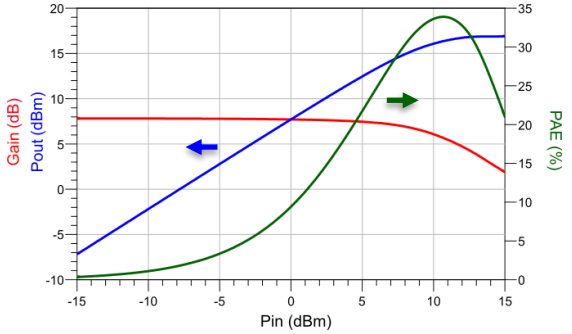

Fig. 7. HB simulation of the CS transistor with the selected optimum load: output power (blue), power gain (red) PAE (green).

We then proceeded to stack 2 transistors (i.e., CS and CG) of the same size. The custom model is used for the common-gate stage to have an accurate assumption of the parasitic elements. As anticipated, a resistive voltage divider is employed to provide the DC bias of the common gate, as shown in Fig. 8.

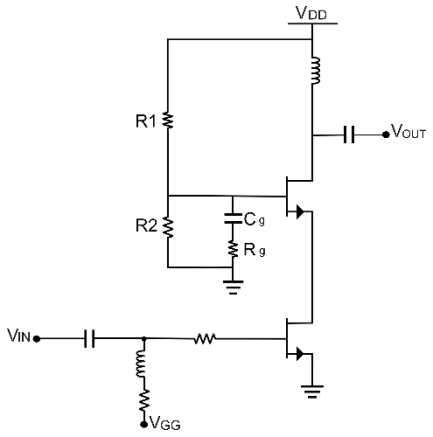

Fig. 8. Stacked cell with resistive self-bias.

To get the maximum output power, it is important to provide the proper load. In particular, the CS device should be matched to its optimum load (Z_{optCS}), found from the previous load-pull simulations.

As the CS stage load is represented by the input impedance of the CG, to obtain Z_{optCS} we must provide stacking proper value of the gate capacitance C_g (see Fig. 8).

It is worth noticing that, as the voltage at the CG drain is doubled compared to that of the CS transistor, the load should be higher (namely twice), in order to guarantee current continuity, power balance, and impedance matching.

At such a high operating frequency, the reactive part of the optimum load is not negligible, thus it is difficult to manually calculate the optimum gate capacitance for the CG to be used. Consequently, the C_g value is optimized by simulation, hence taking into account all the parasitic effects, aiming at guaranteeing the best possible inter-stage matching, i.e., providing both the CS and the CG stages with a load impedance close to the optimum value as shown in Fig. 9 (C_g = 145 fF).

A small resistance has been also added in series with C_g to enhance the cell stability.

In Fig. 9 the black cross is Z_{optCS}, while red and blue circles are CG and CS loads (with power sweep), respectively.

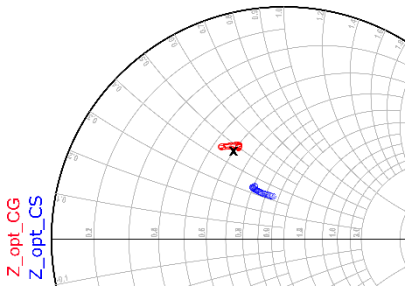

Fig. 9. Loads of the CS (blue circles) and CG (red circles) stages compared to the common source optimum load (black cross).

Fig. 10 and 11 show the layout and the overall 2-stage stacked cell performance at 27 GHz: 19.6 dBm of saturated output power with power gain and PAE above 12 dB and 41.3 % respectively are achieved. As it can be noticed, the power and gain boost are close to the theoretical value of 3 dB, demonstrating the effectiveness of device stacking.

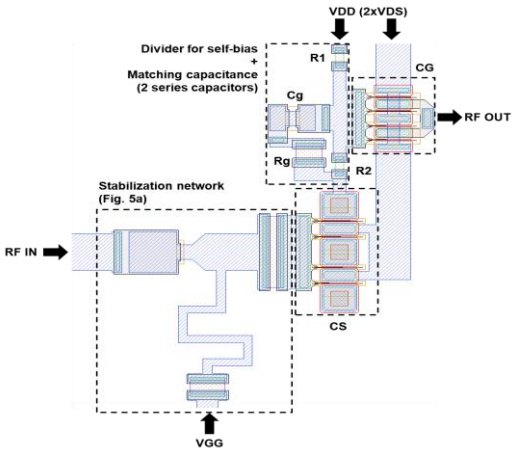

Fig. 10. Layout of the 2-stage stacked cell: the gate network of the CG stage is sharing the via hole with the CS transistor to save space. On the contrary, the stabilization network is clearly not optimized for compactness in this preliminary work.

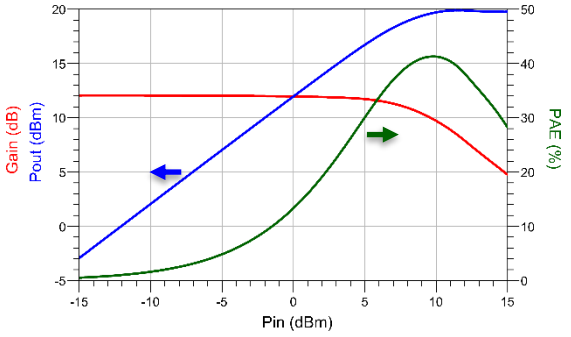

Fig. 11. HB simulation at 27 GHz of the 2-stage stacked cell: output power (blue), power gain (red) and PAE (green).

IV. Conclusion

In this work, the preliminary design of a stacked cell based on a customized measurement-based small-signal model by employing 0.1-µm GaAs pHEMT technology has been proposed. The model is capable to accurately reproducing the device behavior in common-gate configuration, which is of paramount importance for the design of the stacked cell. As a demonstrator, a 2-stage cell has been designed at 27 GHz, providing nearly ideal results in simulations, namely output power in excess of 19.6 dBm with power gain and PAE above 12 dB and 41.3 %, respectively.

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