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Doctoral Dissertation
Doctoral Program in Computer and Control Engineering (37.th cycle)

Computational Intelligence for Computer-Aided Design

Machine Learning Techniques for Microcontrollers Performance Screenings

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Summary

Microcontrollers (MCUs) have become essential components in a wide range of electronic applications, from home automation to aerospace systems. In safety-critical domains like automotive and medical devices, ensuring quality and reliability standards is essential. A key component of quality control for MCUs is performance screening, which assesses the maximum operating frequency of these devices under challenging conditions, such as extreme temperatures and voltages. Traditionally, this has been achieved through speed-binning, a process that sorts devices into performance categories (e.g., "fast" or "slow"). While effective, speed-binning is both costly and time-consuming. This thesis introduces a Machine Learning (ML)-based framework designed to enhance—not replace—traditional performance screening methods by providing additional insights to streamline testing.

The proposed ML framework leverages on-chip speed monitors (SMONs), which are ring oscillators embedded within the device used to measure internal speed characteristics. SMON frequencies serves as a foundation for developing predictive models that estimate maximum operating frequency and identify potential underperforming devices early on. By using this data, the framework can optimize the screening process, providing additional perspectives that reduce the need for exhaustive testing across the full spectrum of conditions.

This ML framework is a multi-stage process covering data collection, preprocessing, and model selection to support MCU performance prediction. First, it addresses data quality by performing data cleaning and outlier detection, ensuring only representative samples are used in training. Given the complexity of assessing maximum operating frequency across multiple functional tests, the framework leverages multi-task regression to enable the model to predict multiple failing frequency for different testing programs simultaneously. This also enhance the prediciton on the *critical pattern*, thus the minimum maximum operating frequency among the tested programs. To address the high cost of labeled data in ML model training, the framework incorporates Active Learning (AL), which selectively prioritizes labeling the most informative samples. This reduces the number of labeled samples required to reach target accuracy, decreasing both time and

cost compared to traditional random sampling approaches.

The framework explores semi-supervised learning, allowing models to leverage the unlabeled production data that is readily available. This improves prediction accuracy by training on a broader dataset without requiring extensive additional labeling. Transfer learning further enhances the framework's adaptability by enabling models trained on one MCU family to apply to others with minimal adjustments, making it highly flexible across product lines.

Feature selection is used to identify the most informative SMONs early in the production process, reducing the number of features needed without compromising accuracy.

The framework introduced in this thesis contributes to the MCU production field by enhancing traditional testing methods with predictive analytics, helping reduce costs and improve accuracy in performance screening. As MCUs continue to grow in complexity, this framework can be an integral addition to existing screening techniques, offering insights that improve production efficiency while maintaining high standards.

Future research may explore additional ML techniques to refine the predictive accuracy further, including advanced feature engineering and interpretability methods to improve transparency. Additional studies could also apply this framework to other embedded systems, helping extend its benefits across a broader array of electronic components.

In conclusion, this thesis demonstrates that ML can be used to augment traditional speed-binning processes, offering a scalable and flexible framework to help optimize MCU performance screening, reduce screening costs, and increase reliability across production lines.

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