Politecnico di Torino

ScuDo
Scuola di Dottorato ~ Doctoral School
WHAT YOU ARE, TAKES YOU FAR

PRIMA ELECTRO
CUSTOM DESIGNED ELECTRONICS
GROUPE SYNOV

PEIC
Power Electronics Innovation Center

Doctoral Dissertation

Doctoral Program in Electrical, Electronics and Communications Engineering
(XXXVIII cycle)

Innovative Control Algorithms for Grid-Tied Inverters

By

Alessandro Roveri

******

Supervisor(s):
Prof. Radu Bojoi, Supervisor
Dr. Fabio Mandrile, Co-Supervisor

Doctoral Examination Committee:
Prof. Paolo Mattavelli, Referee, Università di Padova
Prof. Luca Solero, Referee, Università Roma Tre

Politecnico di Torino
2026

Declaration

I hereby declare that, the contents and organization of this dissertation constitute my own original work and does not compromise in any way the rights of third parties, including those relating to the security of personal data.

Alessandro Roveri
2026

* This dissertation is presented in partial fulfillment of the requirements for **Ph.D. degree** in the Graduate School of Politecnico di Torino (ScuDo).

Be brave

Acknowledgements

After entering the industrial sector as an R&D engineer, returning to academia as a PhD student to pursue my aspirations required a *brave* decision. From the beginning, I knew that this dual commitment, though fascinating and intellectually stimulating, would entail moments of difficulty and sustained effort. It required *bravery* and determination to set aside hesitation, trust in my own abilities and embark on this demanding yet extraordinary journey. While only a small part of this *bravery* came from within, a far greater part was inspired by extraordinary people who supported me throughout this endeavor.

I therefore extend my special thanks to my academic supervisors, Radu and Fabio. You have been guides who have always listened to me and supported me, enriching me not only with technical knowledge but also on a human level.

I would also like to express my sincere gratitude to my manager and industrial supervisor, Remo, who did not hesitate to endorse my ambitions when I entered his office to propose myself as an industrial PhD candidate.

I wish to acknowledge Prima Electro S.p.A., the entire R&D team and in particular the Peiretti family, who placed their trust in me and invested in my professional development.

I would like to thank all the Poli guys and especially you, Vic. So many times you helped me late into the evening in the lab and so many times you had to put up with me.

Matteo and Sandro, thank you for that beer at the St. Martin pub, where you encouraged me to take this path. I truly would not have made it this far without that conversation.

Thank you, Mom and Dad, and thank you, Franci and Bea, my dear sisters, for your constant support, your encouragement and for always standing by me in every decision I have made. You have always believed in me more than I have ever believed in myself.

And finally, my deepest and most heartfelt thanks go to my beloved Michi. Throughout these years, more than anyone else, you have been my emotional pillar. You have been my anchor in the storm and without you I would have sunk long before this milestone.

Abstract

Recent international reports indicate that the accelerating energy transition, driven by the increasing electrification of end users and the growth of renewable generation, is resulting in a substantial rise in grid-connected power electronic converters. This proliferation of power electronics–interfaced loads and generators challenges the reliable operation of power systems, due both to higher and often unpredictable peak power demands and to the increased risk of instabilities caused by the reduction of total inertia.

To ensure the stability of future power systems and avoid frequent grid disruptions, renewable energy source (RES) plants must be able to provide ancillary services analogous to those traditionally delivered by synchronous generators (SGs). Moreover, high-power loads equipped with local energy storage can also enhance grid stability by making part of the stored energy available to the power system, thus mitigating peak power flows and contributing to power system resilience by providing ancillary services, similarly to RES plants.

In this context, two established approaches for enabling static converters to provide ancillary services and improve power quality are the virtual synchronous machine (VSM) control algorithms and the active power filters (APFs). The VSM concept implements an algorithm within the control unit of a grid-tied inverter to emulate the behavior of a SG, thus providing the full spectrum of ancillary services, including frequency and voltage regulation, inertial support, fault current injection and harmonic compensation. APFs, on the other hand, are effective in canceling the distorted currents injected into the grid by non-linear loads, thus ensuring power system compliance with international power quality standards.

The goal of this PhD thesis is thus to design control strategies for grid-tied inverters that enable the proper provision of grid ancillary services, making them more grid-friendly rather than potential sources of instability. Accordingly, innovative control algorithms for both VSM and APF applications have been developed, along with systematic design

procedures addressing key hardware aspects of grid-tied converters. This thesis is structured into two main parts.

The first part focuses on the VSM concept, describing and classifying existing VSM models and introducing a conventional one that highlights their key features. The power coupling phenomenon in VSMs is analyzed and a feedforward-based decoupling method is proposed to limit current stress on hardware components and prevent power fluctuations from propagating to the DC-connected storage during grid support. A dedicated grid impedance estimator for VSM-driven inverters is proposed, which is noise-immune, fully tunable and easily integrable into any VSM model, overcoming existing methods in the literature that rely on the adaptation of algorithms originally designed for grid-following converters.

The second part addresses innovative control and hardware solutions for APFs. It first presents the industrial case study considered in this thesis, which involves APFs installed in a production facility and operating in parallel with regenerative systems for AC–AC converter testing. Then, a dedicated discontinuous pulse-width modulation (DPWM) technique for APFs is proposed, which is insensitive to power line noise and therefore particularly suitable for industrial environments. Compared to conventional space vector pulse-width modulation (SVPWM), it better exploits existing hardware, minimizes losses and allows a doubled switching frequency, reducing the APF high-frequency current ripple injected into the grid. Finally, a dedicated design procedure for the differential-mode (DM) LCL filter interfacing the APF with the grid is proposed, accounting for both APF operating conditions and the compensated load characteristics, thus ensuring compliance with harmonic distortion standards while minimizing the filter volume, weight and cost.

Contents

Chapter 1

Motivation and Goal of the Work

1.1 Penetration of Grid-Tied Power Converters

According to the recent international technical reports [1], the energy transition toward electrification is advancing at an accelerated pace, driven by the increasing electrification of end users in key sectors such as buildings, industry and transport. Indeed, electricity demand is rising, meeting needs for heating, cooling, mobility, as well as powering motors and appliances. Instead, final consumption from fossil fuels is expected to decline in the coming years, even under the most pessimistic scenarios (Fig. 1.1).

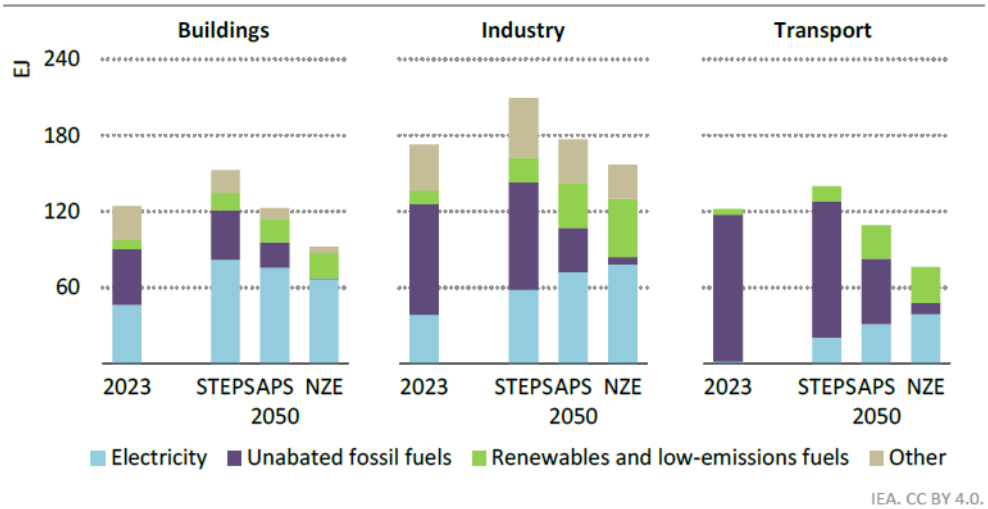


Fig. 1.1 Total final consumption by energy source in buildings, industry and transport by different scenarios (STEP, APS and NZE), 2023 and 2050. Source: IEA [1].

This energy gap in electricity request will be primarily filled by generation from renewable energy sources (RESs), such as solar photovoltaic (PV), hydropower and wind (Fig. 1.2).

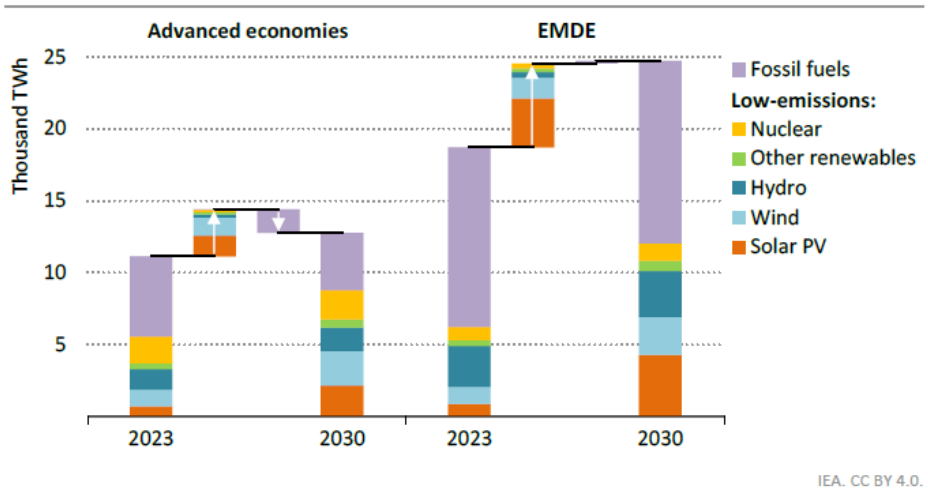


Fig. 1.2 Electricity generation by source in advanced and emerging (EMDE) economies, 2023 and 2030. Source: IEA [1].

The increasing direct reliance of end users on electricity, together with the expansion of renewable generation, is driving an exponential growth in the number of power electronic converters connected to the grid. The rising penetration of power electronics–interfaced loads and generators pose a challenge to the proper operation of the existing electrical system not only because of the higher peak power demands that must be managed by the system operators, but also due to the potential instabilities that the increasing number of grid-connected converters can introduce.

This section therefore discusses the latest application areas involving grid-interfaced power electronic converters. Then, the impact of these applications on the operation of the power system will be investigated in next sections of this chapter.

1.1.1 Renewable Energy Sources

RESs provide a sustainable alternative to fossil fuels, contributing to climate change mitigation by reducing the carbon dioxide (CO_2) emissions (Fig. 1.3). Over the past decade, the integration of RESs into the electric grid has been increasing globally and the

transition to clean energy is expected to continue at a rapid pace in the coming years, with installed capacity projected to double by 2030 compared to current levels. (Fig. 1.3).

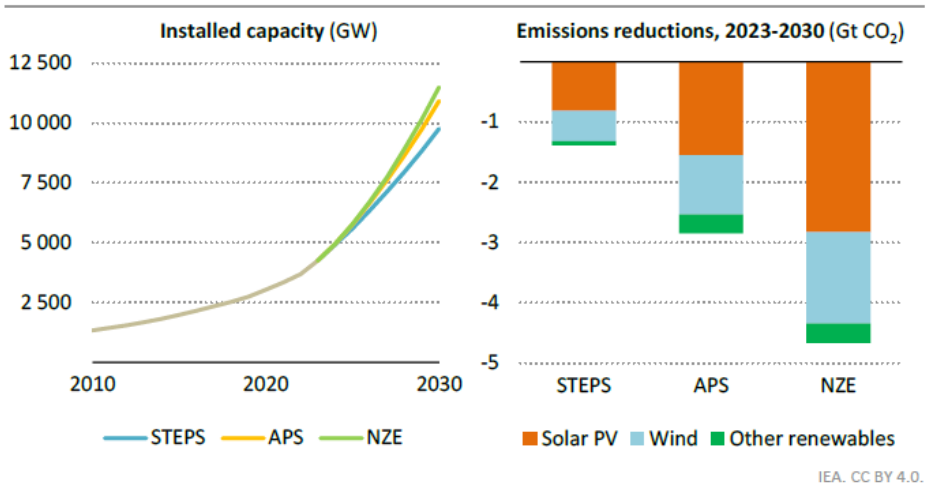


Fig. 1.3 Global installed capacity of renewables, 2010-2030, and emissions reductions by scenario, 2023-2030. Source: IEA [1].

The most promising RESs are wind and solar energy.

Wind Energy

Wind power plants convert the kinetic energy of the wind into electrical energy by means of wind turbines. Both onshore and offshore wind farms harness this resource to generate electricity. The global expansion of wind power has been rapid, driven by technological advancements, supportive regulatory frameworks and declining costs. Wind turbines can be deployed across a wide range of terrains, from open plains to coastal waters, providing a scalable and reliable solution for the ongoing transition to renewable energy [2].

A wind turbine is normally connected to the grid by means of static power converter, according to the principle scheme of Fig. 1.4 [3]. The turbine blades extract the wind kinetic energy and make it available to a rotating shaft. The mechanical power flows through a a gear-box and is delivered to an electric generator (G in Fig. 1.4), which converts mechanical energy into electrical energy: Finally, a two-stage AC-DC and DC-AC power converter manages the power flow and adapts the current waveforms injected into the grid. The DC-AC stage is commonly known as inverter.

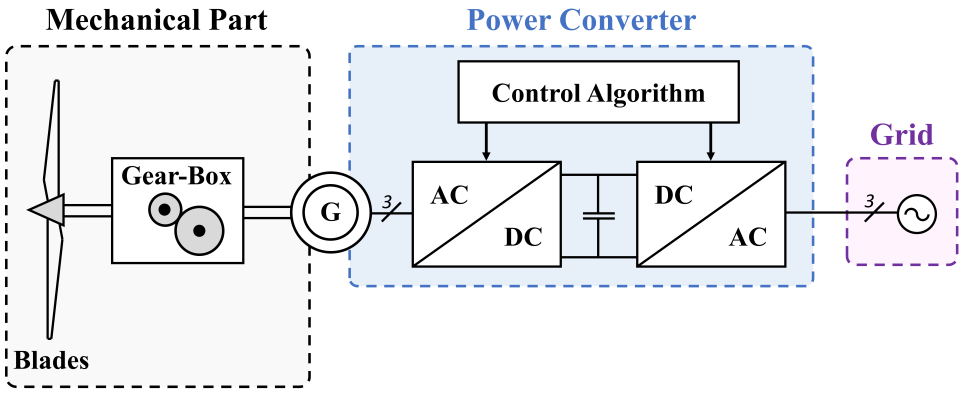


Fig. 1.4 Conventional scheme of connection of a wind turbine to the grid by means of a power converter.

Solar Energy

Solar energy exploits the sun abundant radiation through two primary technologies: PV panels and concentrated solar power (CSP) systems. PV panels directly convert sunlight into electricity, while CSP systems focus solar radiation via mirrors or lenses to generate electricity or produce heat. Continuous technological improvements have dramatically lowered costs, making solar energy increasingly competitive with conventional energy sources. Additionally, rooftop solar installations allow households and businesses to produce electricity on-site, reducing dependence on centralized grids and lowering building energy expenses [4].

A schematic of a conventional PV plant connected to the grid is shown in Fig. 1.5 [5].

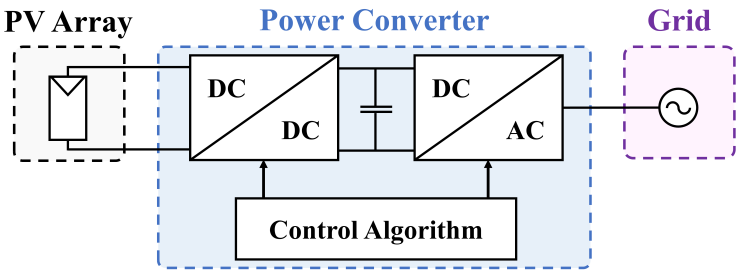


Fig. 1.5 Conventional scheme of connection of a PV array to the grid by means of a power converter.

Two conversion stages are utilized to connect PV plant to the grid: a first boost DC-DC stage and an inverter. Depending on the grid configuration, the PV inverter can have either a single-phase or a three-phase structure. The maximum power point tracking (MPPT)

algorithm [6] is among the most widely adopted control strategies in PV applications, ensuring system efficiency ≥ 99 % under steady-state conditions.

1.1.2 High-Power Loads: The Case of Ultra-Fast DC Chargers

Ultra-fast DC chargers constitute a case-study of high-power loads that are rapidly expanding in line with the electrification of the transport sector [1]. In recent years, targeted governmental policies have been driving the global deployment of public charging stations to keep pace with the growing electric vehicle (EV) market. The global number of ultra-fast charging points, with power ratings up to 150 kW, increased by about 50 % between 2023 and 2024 and an exponential growing trend is still expected in the coming years. Indeed, on a global scale, the public charging capacity for light-duty EVs would need to increase nearly nine-fold by 2030 to support EV sales implied by current stated policies [7].

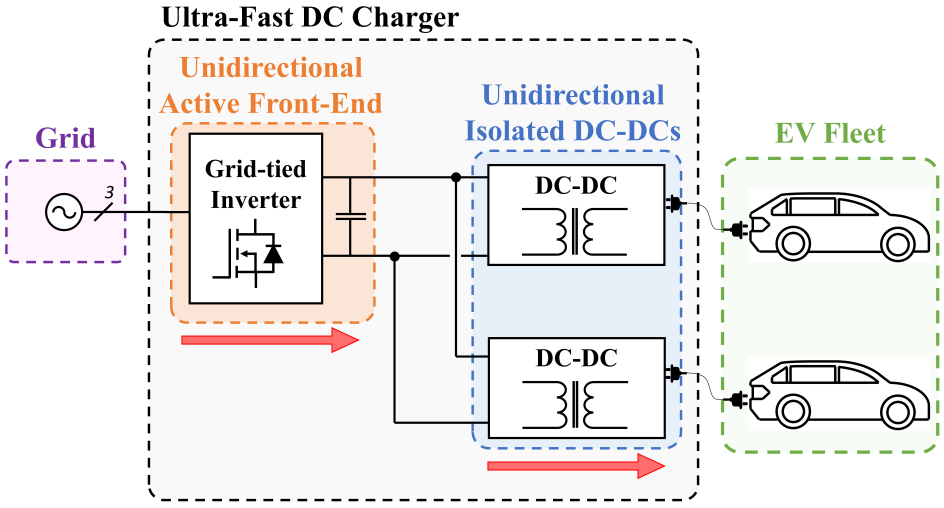


Fig. 1.6 Simplified scheme of an unidirectional ultra-fast DC charging system.

Among the EV charging systems, on-board AC chargers have limited power ratings (≤ 22 kW) and are suitable for overnight charging. In contrast, high-power off-board DC chargers offer higher power ratings, in the range of 50–350 kW. These chargers deliver DC current directly to the battery pack through a galvanically insulated power converter installed outside the EV, as shown in Fig. 1.6. The power is drawn from the grid by an AC-DC converter, known as active front-end (AFE). The next generations of ultra-fast DC chargers rated at 350 kW and above [8], [9] will provide EV refueling times similar to

those of gasoline vehicles, thus enabling faster and longer trips with EVs and encouraging mass-market consumers switch to electric mobility [10].

1.2 Stability of the Electric Grid

1.2.1 Paradigm of Power Systems

The century old paradigm of the electric grid consists in a centralized power generation from programmable sources (i.e., hydroelectric and thermoelectric power plants) by means of conventional synchronous generators (SGs), using the transmission lines to deliver the energy in a unidirectional way, thus balancing the load electricity demand [11]. For a proper power system operation, SGs must guarantee: constant grid frequency, constant voltage amplitude, sinusoidal voltage supply with low harmonic distortion and protection in case of faults. The SGs act to ensure the aforementioned conditions by providing the so-called grid ancillary services.

Constant Grid Frequency

The power system is designed to ensure the balance between active power demand and consumption by keeping the grid frequency around its nominal value. When the power balance is perturbed by generation or load variations, the grid frequency drops or rises. Conventional SGs operates to minimize these frequency deviations in case of transient power imbalances with the mechanism described in Fig. 1.7.

During a power imbalance, the kinetic energy stored in SGs plays a pivotal role. Indeed, when power demand increases or generated power reduces, the SGs rotors speed decreases, injecting inertial active power into the grid. The SGs inertial response contributes to raise the frequency nadir (i.e., the minimum frequency value reached during transient) and mitigating the rate of change of frequency (ROCOF), thus reducing the likelihood of activating frequency protection relays. After this initial response, which lasts approximately 1–4 seconds, primary frequency control adjusts the power output from programmable sources to meet the new load conditions in a time of period of few minutes. Finally, secondary frequency control restores the nominal frequency (e.g., 50 Hz in Europe and 60 Hz in USA) on a timescale of tens of minutes [11].

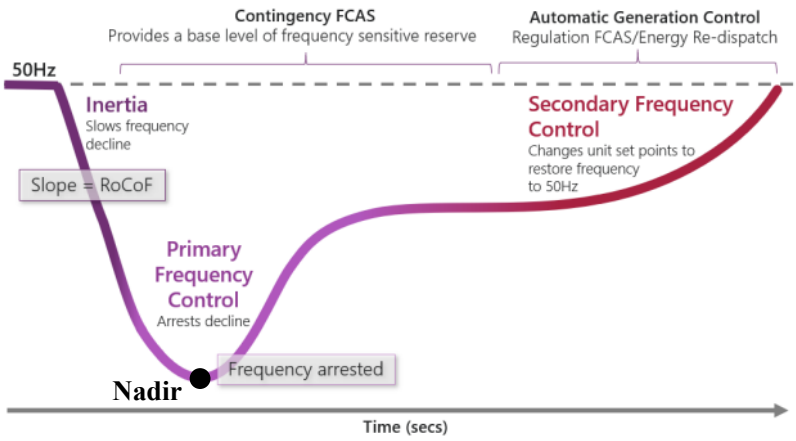


Fig. 1.7 Frequency profile and frequency control steps after a power imbalance due to a generation reduction or an increased absorption by loads. Source: [12].

Constant Voltage Amplitude

SGs must maintain a stable voltage level for the proper power system operation. Voltage amplitude must be kept within established standards. Its variations are closely related to the injection or absorption of reactive power, especially in predominantly inductive power systems.

Low Harmonic Distortion

The electric grid requires a sinusoidal voltage with low distortion in steady-state conditions. Indeed, the presence of harmonics and interharmonics in the supply voltage may lead to the circulation of distorted current components, with subsequent overheating of the supplying line cables and electrical equipment, increasing risk of triggering of the line protection devices and malfunctioning of the loads connected to the grid. Due to the above-mentioned side effects, international standards [13] provide harmonic distortion limitations to mitigate the adverse impacts of distorted currents on power system.

Owing to their electromechanical construction, SGs are able to generate a voltage with a very low total harmonic distortion (THD). Furthermore, in the event of distorted voltage on the power lines, SGs inherently inject harmonic currents, thus counteracting the voltage distortion, as their stator provides a low impedance path for frequency components other than the fundamental.

Power System Protection during Faults

The structure of the power system must withstand, detect and clear short circuits. The power lines are protected by breakers to isolate faulty sections of the grid and clear the faults. SGs are well suited to trigger such protections, since they inherently inject a fault current in the event of voltage reduction at their terminals, as it occurred in the case of a grid short-circuit. The magnitude of the injected current depends on the electrical distance from the fault location. For faults in close proximity, SGs can inject short circuit currents several times their rated value (e.g., 5 pu) without triggering their thermal protections, due to their high thermal time constant. Consequently, they can remain connected to the grid and ride through the fault, thus contributing to grid stability under abnormal conditions.

1.2.2 Impacts of Renewable Energy Sources on Power Systems

Energy production by RESs offer a sustainable alternative to fossil fuels and is frequently associated with distributed generation, promoting energy independence for communities and individuals and reducing reliance on centralized power production, thus minimizing the risk of outages [14].

On the other hand, RESs can introduce stability challenges to the power system. Indeed, RES plants rely on static converters for injecting the generated energy into the grid and inherently lack the inertial capabilities of SGs, which arise from the kinetic energy stored in their rotating components [15], [16]. The continuous increase in RESs connections to the electric grid, combined with the simultaneous decommissioning of thermal plants due to decarbonization policies [1], is leading to a progressive decrease in the total inertia of power systems. This reduction results in higher ROCOF and lower frequency nadir during power imbalances (Fig. 1.7), thus compromising the overall grid frequency stability.

Conventional control algorithms for RESs, such as MPPT for PV plants, do not provide any of the grid ancillary services described above, which therefore remain the exclusive domain of SGs.

1.2.3 Impacts of High-Power Loads on Power Systems

The energy transition [1] is leading to a rise in high-power, unpredictable and discontinuous loads connected to the power system, such as ultra-fast DC chargers. The large scale

deployment of such loads is increasing the daily peak demand on the utility. Moreover, their complete lack of flexibility and predictability poses significant challenges for the power system stability.

Most of the issues mentioned above can be mitigated by installing local energy storage in proximity to, or directly integrated with, such loads [17], [18]. In the case of ultra-fast DC chargers, local storage can be also provided by the batteries of the EVs being charged, making bidirectional the DC-DCs interfaced to the EVs and the AC-DC power converter stage (Active Front End - AFE), as shown in Fig. 1.8.

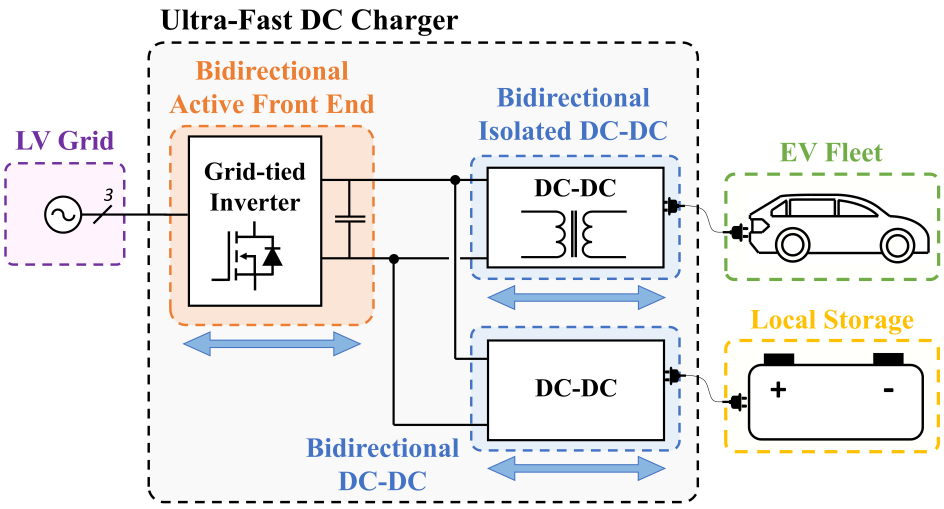


Fig. 1.8 Simplified scheme of a bidirectional ultra-fast DC charging system with installed local storage.

Indeed, local storage can serve as an energy reserve that can be made available to the power system, useful for addressing unexpected large imbalances between power demand and generation, thus reducing the risk of grid instabilities [19], [20]. Moreover, the installation of local storage enables full power decoupling between the power drawn by the end load (such as EVs) and the power drawn from the grid, thus allowing for intra-day load shifting and minimizing the power flow on transmission and distribution lines [18], [21].

Local storage can be employed for the same purposes in RES plants, thus decoupling the generated energy from the energy injected into the grid in accordance with load demand [22].

1.2.4 Case Study: The 2025 Iberian Peninsula Blackout

A current and relevant case of a blackout event occurred in Spain and Portugal on April 28, 2025 [23]. Shortly before the blackout, energy production from RESs, such as solar and wind, was significant throughout Spain (Fig. 1.9). This resulted in the Iberian Peninsula equivalent total inertia constant H, a parameter related to power system stability [11], being low, in the range 2.19–2.69 s.

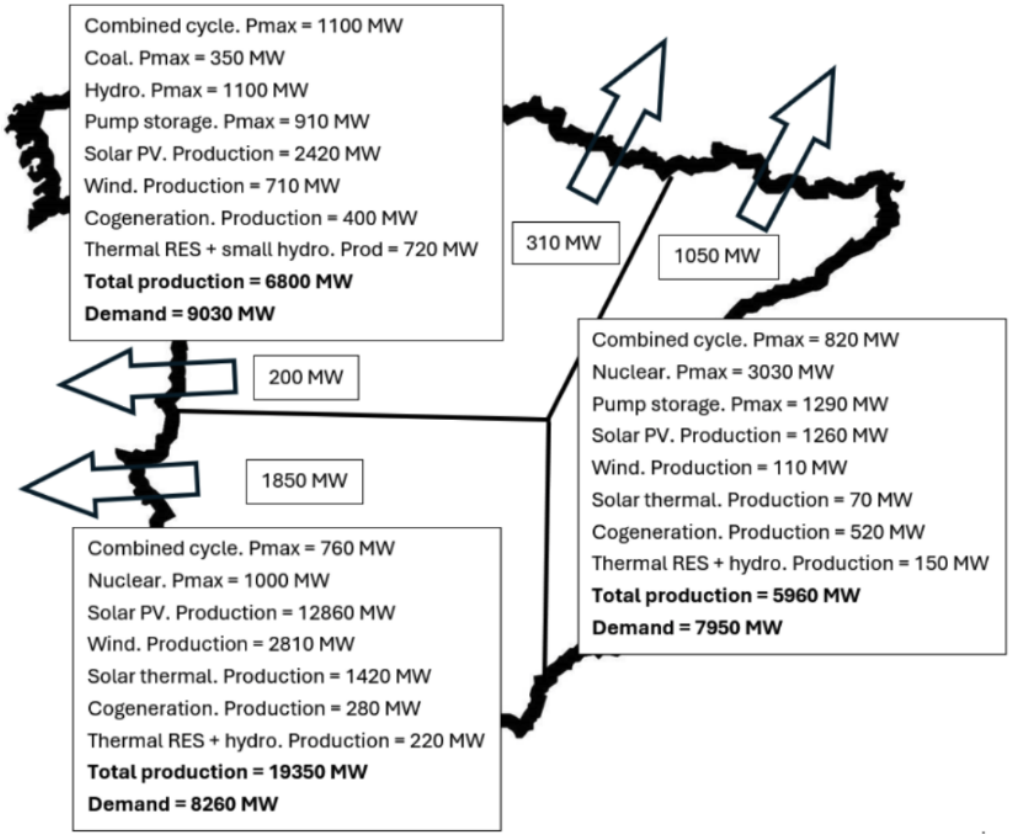


Fig. 1.9 Geographic distribution of production and load in Spain before the blackout. Source: [23].

Initially, increases in power system electric load were observed, attributed to the loss of small-scale distributed renewable generation. Subsequently, within a time window of approximately one minute and twenty seconds prior to the blackout event, cascading losses of renewable generation occurred, exceeding a total of 4000 MW. As a result, the Spanish and Portuguese power systems began to lose synchronization with the rest of the European continental grid, leading to the disconnection of the Iberian system firstly from Morocco and then from France. This marked the onset of the collapse, which unfolded within just

a few seconds from the initial loss of synchronism (Fig. 1.10). The currently available preliminary data indicates that the above-described sequence of events took place after a voltage increase in the Spanish power system [23].

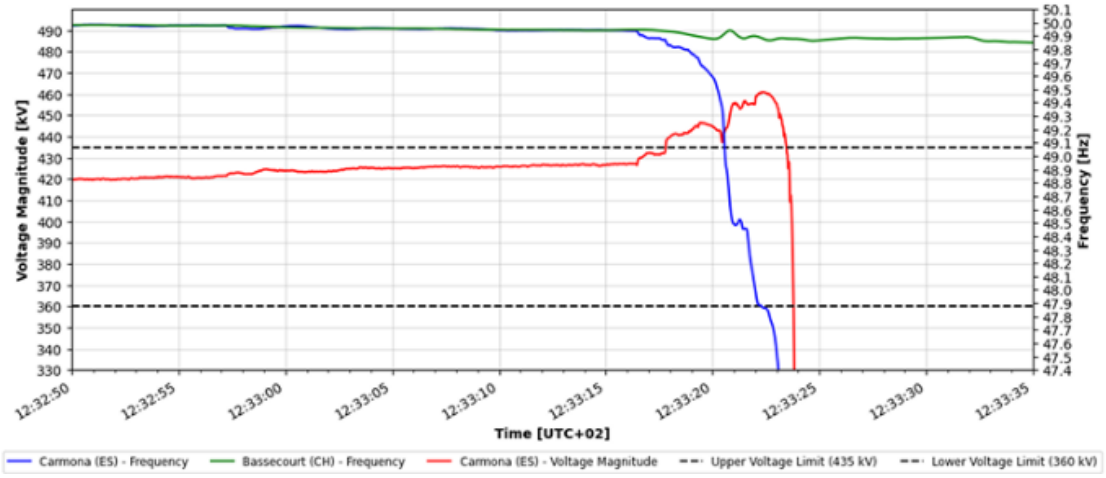


Fig. 1.10 Evolution of the frequency (blue curve) and the voltage (red curve) in Spain and of the frequency in the rest of Continental Europe (green curve) during the incident. Source: [23].

The Iberian Peninsula blackout is a concrete demonstration of how the decommissioning of thermal power plants, together with the increasing penetration of converter-interfaced RESs, is reducing the total power system inertia, thus compromising the stability of the grid. According to recent technical reports [15], the equivalent total inertia constant H of power systems in various European countries is expected to decrease below the critical value of 2 s, compared with the desired ideal value of over 4 s (Fig. 1.11). This is expected to result in a higher frequency of catastrophic events, such as the Iberian Peninsula blackout, if no measures are taken.

Moreover, the proliferation of unpredictable and intermittent high-power loads associated with the energy transition process, such as ultra-fast DC chargers, will constitute additional perturbing factors, further weakening power system stability.

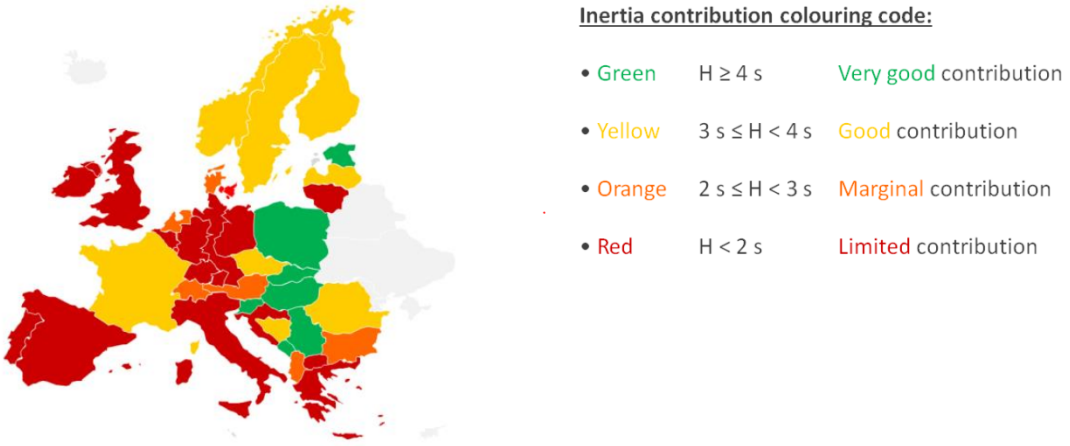


Fig. 1.11 Indicating expected contribution of each transmission system operator (TSO) in Europe to the power system equivalent total inertia constant H by 2030. Source: [15].

1.3 Ancillary Services Through Static Converters

To ensure the stability of future power systems and avoid frequent disruptions in the grid, RES plants will need to be enabled to provide ancillary services similarly to SGs. Regulatory authorities and transmission system operators (TSOs) across various countries are actively moving in this direction to enable RES plants to contribute to grid support [15], [16], [24], [25].

Nevertheless, even high-power loads with installed local storage can play a role, actively contributing to grid stability by making part of the stored energy available to the TSO. Indeed, the presence of local storage with installed bidirectional hardware enables these loads to also participate in the provision of ancillary services. For these users, such as the EV charging station operators, the provision of ancillary services can represent an additional source of revenue, achieved by exploiting the already installed hardware, after mutual agreement with the TSO [24], [25], [26], [27]. More specifically, solutions reported in the literature have demonstrated that ultra-fast DC chargers can be enabled to provide the full spectrum of grid ancillary services, including primary frequency regulation [28], [29], [30], voltage regulation [19], [29], [30], [31], inertial support [28], [29], [30], [31], fault current injection [31] and harmonic compensation [30], [31].

This section thus introduces two well-known solutions in the field of grid-tied power converters, aimed at enabling the partial or full provision of grid ancillary services and

improving power quality through static converters, i.e., the virtual synchronous machine (VSM) control algorithms and the active power filters (APFs).

1.3.1 Virtual Synchronous Machines

The concept of VSM consists in implementing into the grid-tied inverter control unit a dedicated algorithm that enables the static converter to emulate the behavior of SGs [32]. This approach ensures the converter capability to provide the full spectrum of ancillary services, i.e., grid frequency and voltage regulation, inertial support, short-circuit current injection during faults and harmonic compensation. Indeed, a VSM-driven inverter can preserve the advantageous characteristics of traditional SGs, such as the inherent provision of ancillary services, while potentially overcoming some of their limitations. For instance, a VSM is fully tunable to meet specific application requirements, while physical parameters in SGs, such as the inertia constant H, are not adjustable.

Over the past 15 years, numerous different solutions of VSMs have been proposed in the literature, each providing distinct operational characteristics [33], [34].

1.3.2 Active Power Filters

APFs are an effective solution for mitigating the issue of distorted currents injected into the grid by non-linear loads, such as diode or thyristor front-end rectifiers [35], [36], [37]. The distorted current components lead to an overall increase in the RMS current drawn from the grid, resulting in overheating of the supply cables, a higher risk of triggering line protection devices and potential interference with nearby sensitive electronic equipment. APFs are thus able to perform the harmonic compensation ancillary service by canceling the harmonic distortion and making the power system compliant with international regulations [13].

Among the various types of APFs, shunt-type APFs are the most industrialized [38]. They are connected in parallel to the distorted load, thus injecting non-sinusoidal currents to make the overall grid current sinusoidal at unity power factor.

1.4 Goal of the Thesis

The goal of this PhD thesis is the design of control strategies that enable grid-tied inverters to provide grid ancillary services, thus making them more grid-friendly, rather than posing challenges to the grid stability. To this end, both algorithms related to VSMs and APFs control have been developed. Nevertheless, certain aspects more closely related to the hardware design of grid-tied inverters have been investigated, with the aim of establishing component design procedures.

The research activities presented in the thesis have mainly focused on developing solutions aimed at enhancing the reliability and field performance of grid-tied inverters in industrial applications. All the investigated control and hardware solutions have been implemented in industrial products of Prima Electro S.p.A., the company that has funded the industrial PhD program.

1.5 Thesis Outline & Main Contributions

This thesis is structured into two main parts: one focusing on the VSM concept and the other on APF applications.

Virtual Synchronous Machines

The first part (Chapters 2, 3 and 4) deals with the VSM concept:

- **Chapter 2:** This chapter is a general introduction, where the nomenclature adopted in the following chapters is introduced. Moreover, VSM models available in the literature are described and classified according to their operating principle. A conventional VSM model is also presented, highlighting the main features common to the various VSM implementations;
- **Chapter 3:** This chapter investigates the power coupling phenomenon in VSM models, a relevant issue especially for high-power loads that employ their hardware to provide ancillary services through the implementation of VSMs in their AFE units. Indeed, the power coupling phenomenon causes a reactive power injection when the AFE is requested to provide a grid ancillary service associated with active

power provision and vice versa. This leads to unnecessary current overstress on the installed hardware and can result in the propagation of power fluctuations from the AFE AC-side to the DC-stage and, consequently, to the DC-connected batteries, potentially reducing their lifetime. A straightforward feedforward-based solution directly implemented in the VSM model is thus proposed to ensure complete active-reactive power decoupling while the AFE provides grid support [C4], [J3];

- **Chapter 4:** This chapter addresses the topic of grid impedance estimation in VSM-driven inverters. The knowledge of the grid impedance is essential for the proper tuning of the main functional blocks of a VSM algorithm and of the inverter current controllers, thus ensuring the correct provision of grid ancillary services. The grid impedance estimation methods available in the literature have been primarily developed for grid-following power converters. When applied to VSM applications, these approaches are typically adapted and therefore exhibit certain limitations. This chapter thus proposes a dedicated VSM-based grid impedance estimator that can be integrated into any VSM model, inherently rejecting measurement noise typically present on power lines in industrial environments and fully tunable with respect to the desired estimation time and accuracy [C1], [C2], [J2].

Active Power Filters

The second part (Chapters 5, 6, and 7) focuses on innovative control and hardware solutions for applications in the field of APFs:

- **Chapter 5:** The chapter introduces the nomenclature adopted in the following chapters, presents the control algorithm of the APF used in the experimental validation tests and describes the industrial case study considered in this thesis, i.e., the installation of APFs in a production facility, operating in parallel with regenerative systems used for the final functional testing of AC–AC power converters;

- **Chapter 6:** This chapter presents a dedicated discontinuous pulse-width modulation (DPWM) technique for APFs. Compared to other solutions reported in the literature, the proposed method is insensitive to the noise circulating on the power lines and acquired by the current sensors of the APF. This makes it particularly suitable for APFs installed in industrial environments, such as production facilities, where current and voltage disturbances are normally present. Moreover, compared to conventional

space vector pulse-width modulation (SVPWM), the proposed technique allows better exploitation of the existing hardware, minimizing losses in power devices and enabling the switching frequency to be doubled, thus reducing the high-frequency current ripple injected into the grid by the APF due to converter switching [C3], [J1];

- **Chapter 7:** This chapter proposes a dedicated design procedure for the differential-mode (DM) LCL filter used to interface the APF with the grid. Unlike previous methods reported in the literature, the proposed design methodology takes into account not only the operating conditions of the APF but also the characteristics of the compensated non-linear load. In this way, the current distortion standards at the point of common coupling (PCC), where both the APF and the compensated load are connected, are met, while the filter volume, weight and cost are minimized [J1].

The thesis ends with **Chapter 8**, which outlines the main conclusions and directions for future work.

1.6 List of Publications

The research activities undertaken during this PhD have culminated in the publication of the following papers:

Journals

[J1] A. **Roveri**, V. Mallemaci, F. Mandrile and R. Bojoi, "Design Guidelines for Active Power Filters Operating in Disturbed Industrial Environments," in IEEE Open Journal of Industry Applications, vol. 7, pp. 216-237, 2026, doi: 10.1109/OJIA.2026.3658742.

[J2] A. **Roveri**, V. Mallemaci, F. Mandrile and R. Bojoi, "Enhanced Virtual Synchronous Machine With Online Grid Impedance Estimation," in IEEE Open Journal of Industry Applications, vol. 6, pp. 427-444, 2025, doi: 10.1109/OJIA.2025.3584050.

[J3] A. **Roveri**, V. Mallemaci, F. Mandrile and R. Bojoi, "Power Decoupling Methods for Grid Support Provided by Ultra-Fast Bidirectional Chargers," in IEEE Open Journal of Industry Applications, vol. 6, pp. 107-119, 2025, doi: 10.1109/OJIA.2025.3529042.

Conferences

[C1] A. **Roveri**, F. Campanelli, F. Mandrile and R. Bojoi, "Improved Virtual Synchronous Machine with Grid Impedance Estimator for Islanding Detection," PCIM Conference 2026; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nürnberg, Germany, 2026, *Accepted for Publication*.

[C2] A. **Roveri**, V. Mallemaci, F. Mandrile and R. Bojoi, "A Virtual Synchronous Machine Based Algorithm for Online Grid Impedance Estimation," 2024 IEEE Energy Conversion Congress and Exposition (ECCE), Phoenix, AZ, USA, 2024, pp. 740-747, doi: 10.1109/ECCE55643.2024.10861752.

[C3] A. **Roveri**, F. Mandrile, V. Mallemaci and R. Bojoi, "Discontinuous PWM Modulation for Active Power Filters Operating in Disturbed Environments," 2023 IEEE Energy Conversion Congress and Exposition (ECCE), Nashville, TN, USA, 2023, pp. 6429-6436, doi: 10.1109/ECCE53617.2023.10362487.

[C4] A. **Roveri**, V. Mallemaci, F. Mandrile and R. Bojoi, "Power Decoupling Method for Grid Inertial Support Provided by Ultra-Fast Bidirectional Chargers," 2023 IEEE Energy Conversion Congress and Exposition (ECCE), Nashville, TN, USA, 2023, pp. 6544-6546, doi: 10.1109/ECCE53617.2023.10362280.

Moreover, the following paper was co-authored:

Conferences

[C5] A. Camboni, A. **Roveri**, F. Mandrile and R. Bojoi, "Simple Active Damping Solution for Industrial Grid-Tied Inverters using LCL Filters," 2025 IEEE Energy Conversion Congress and Exposition (ECCE), Philadelphia, PA, USA, 2025, pp. 1-7, doi: 10.1109/ECCE58356.2025.11260345.

Co-inventorship has been formally recognized in the registration of two national patents:

Patents

[P1] A. **Roveri**, V. Mallemaci, F. Mandrile and R. Bojoi, "Metodo per Stimare in Tempo Reale l'Impedenza di Rete per Mezzo di una Macchina Sincrona Virtuale", Application Number 102024000022908.

[P2] A. Camboni, A. **Roveri**, F. Mandrile and R. Bojoi, "Metodo Attivo di Smorzamento delle Risonanze in Filtri LCL per Inverter Connessi alla Rete Elettrica", Application Number 102025000024463.

Finally, as part of complementary activities, contributions include co-supervision of two Master's theses:

Master Thesis Co-Supervised

[T1] D. Lanfranco, Design of Active Power Filters for Power Quality Improvement, 2024. Supervisors: F. Mandrile (Politecnico di Torino), A. **Roveri** (Prima Electro S.p.A.).

[T2] G. Imperiale, Real-Time Grid Parameters Estimation for Stability Improvement of Ultra-Fast Charging Stations, 2024. Supervisors: R. Bojoi (Politecnico di Torino), A. **Roveri** (Prima Electro S.p.A).

Chapter 2

Virtual Synchronous Machines

This chapter consists of the following sections containing:

- Description of the reference hardware for VSM implementation, suitable for both RES generation plants and industrial load applications, such as the AFE of an ultra-fast DC charger;
- Investigation and systematic classification of the various VSM solutions reported in the literature, based on their implementation characteristics;
- Proposal of a conventional VSM model with analysis of the features commonly shared across different VSM implementations. This model will be integrated with the additional VSM features developed in this thesis, which will be presented in the subsequent chapters.

2.1 General Structure of the Hardware on Study

The reference hardware employed to study and implement the VSM solutions is presented in Fig. 2.1. The power converter is interfaced to the grid through an LCL filter, which represents the conventional approach for interfacing static converters to the grid [39]. The filter consists of an inverter-side inductor L_f, a filter capacitor C_f with in series a damping resistor R_f and a grid-side inductor L_{fg}. The inverter is supplied by an ideal DC source, which can represents both the generation from RESs (Fig. 1.4 and Fig. 1.5) or the local storage in a high-power load (Fig. 1.8). By idealizing the DC-side, the discussion can be

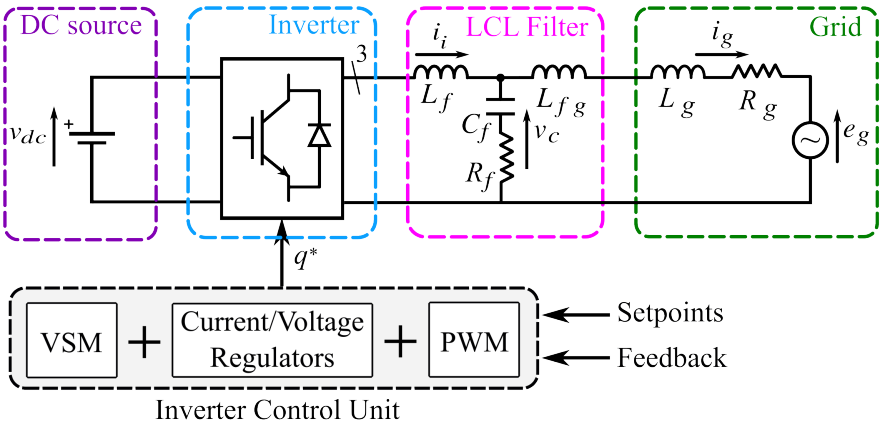


Fig. 2.1 Hardware block scheme for the considered VSM solutions.

thus focused on the control of the grid-tied inverter. The grid is modeled as an equivalent Thevenin circuit with a grid inductance L_g and resistance R_g.

In the described system, e_g and i_g are respectively the equivalent Thevenin grid voltage and current, v_c is the grid measured voltage across the filter capacitor branch, while i_i is the measured inverter output current.

The inverter control provides the commands q^* to the inverter switches, according to the external setpoints and the measured current and voltage feedback. The inverter control consists of the VSM algorithm, optional current and/or voltage regulators and the pulse-width modulator (PWM).

2.2 Current-Source and Voltage-Source VSMs

As shown in Fig. 2.2 and Fig. 2.3, a VSM algorithm is a higher-level controller, which receives as inputs the power references P_v^*-Q_v^* and either the measured grid voltage v_c (Fig. 2.2) or the inverter output current i_i (Fig. 2.3), thus providing the current i_i^* (Fig. 2.2) or voltage v_c^* (Fig. 2.3) references to the lower-level inverter controller [40]. Depending on whether the VSM provides i_i^* or v_c^* to the inverter controller, it can be defined as a current-source or voltage-source VSM.

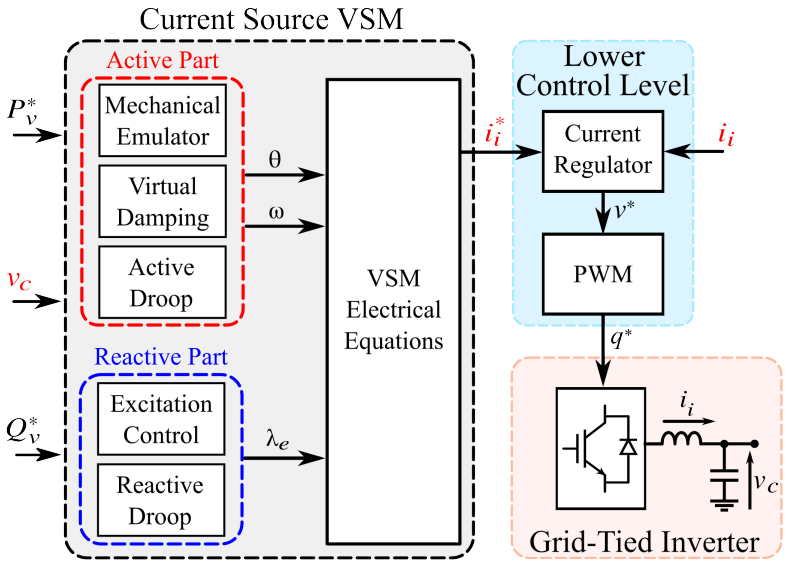


Fig. 2.2 Control scheme of a grid-tied inverter embedded with generic current source VSM. The VSM receives as inputs power references P_v^*-Q_v^* and the measured grid voltage v_c, thus providing the output current reference i_i^* to the inverter lower control level, consisting in a current regulator. The computed voltage reference v^* is thus the input of the pulse-width modulator (PWM), which finally provides the commands q^* to the inverter switches.

2.2.1 Current-Source VSMs

In current-source VSMs (Fig. 2.2), the inverter lower-level controller consists of a current regulator, which computes the inverter voltage reference v^*, that is then converted into the switching commands q^* by the PWM block. Some examples of this type of VSM configuration are the first VSG model proposed in 2007, i.e., the VISMA [41], its first simplified version VISMA I [42], the SPC [43], the VSYNC [44], the KHI [45], the S-VSC [46] and the latest version of Synchronverter [47].

2.2.2 Voltage-Source VSMs

On the other hand, voltage-source VSM models (Fig. 2.3) can be further classified according to the management of the VSM voltage output reference by the inverter lower control level. In some models, the lower-level control is not implemented, resulting in an open loop voltage control, as in the original Synchroconverter [48], the Osaka model [49] and the VISMA II variant [50]. Otherwise, as in CVSM [51] a cascaded dual loop control can be implemented. The first voltage loop compares the VSM reference voltage v_c^* with v_c

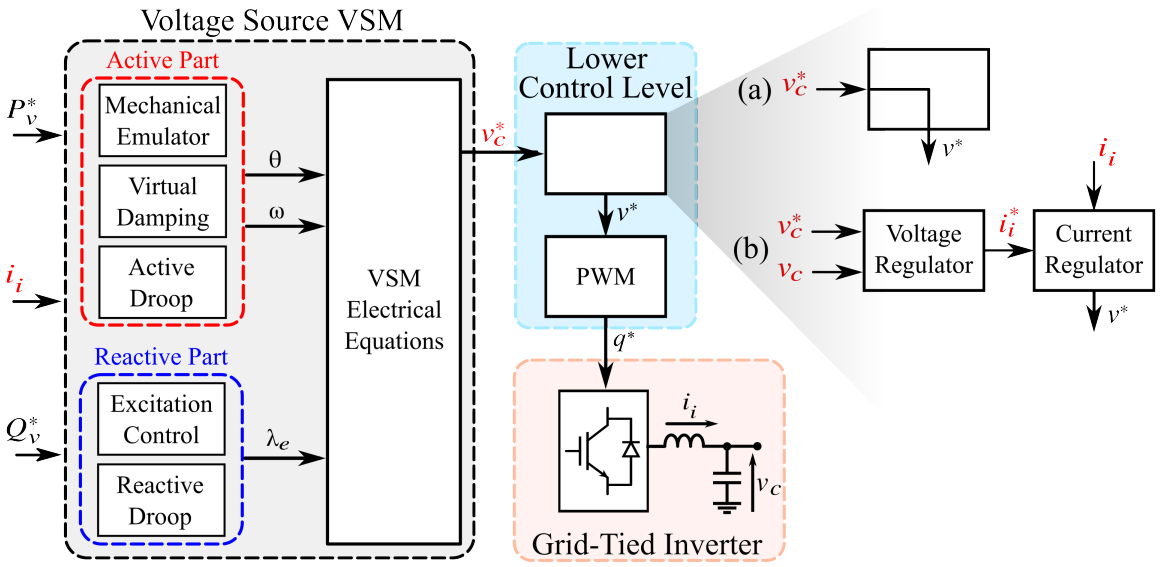


Fig. 2.3 Control scheme of a grid-tied inverter embedded with generic voltage source VSM. The VSM receives as inputs power references P_v^*-Q_v^* and the measured inverter output current i_i, thus providing the grid voltage reference v_c^* to the inverter lower control level, wich can consist in an open loop voltage control (a) or in a cascaded dual loop voltage and current control (b). The computed voltage reference v^* is thus the input of the pulse-width modulator (PWM), which finally provides the commands q^* to the inverter switches.

to generate i_i^*, which is then tracked by means of a current regulator, whose output v^* is provided to the PWM block.

As can be observed by comparing Fig. 2.2 and Fig. 2.3, current-source and voltage-source VSMs differ only in terms of implementation. Indeed, both are capable of providing the same functionalities related to active and reactive power control, which will be exhaustively detailed in the following section of this chapter.

2.3 Conventional VSM Model

The conventional VSM model adopted in this thesis is the current-source VSM depicted in Fig. 2.4. The VSM provides its computed current i_v as current reference i_i^* to the inverter controller, thus injecting the desired active and reactive powers P_v-Q_v into the grid.

The VSM model consists of the following functional blocks:

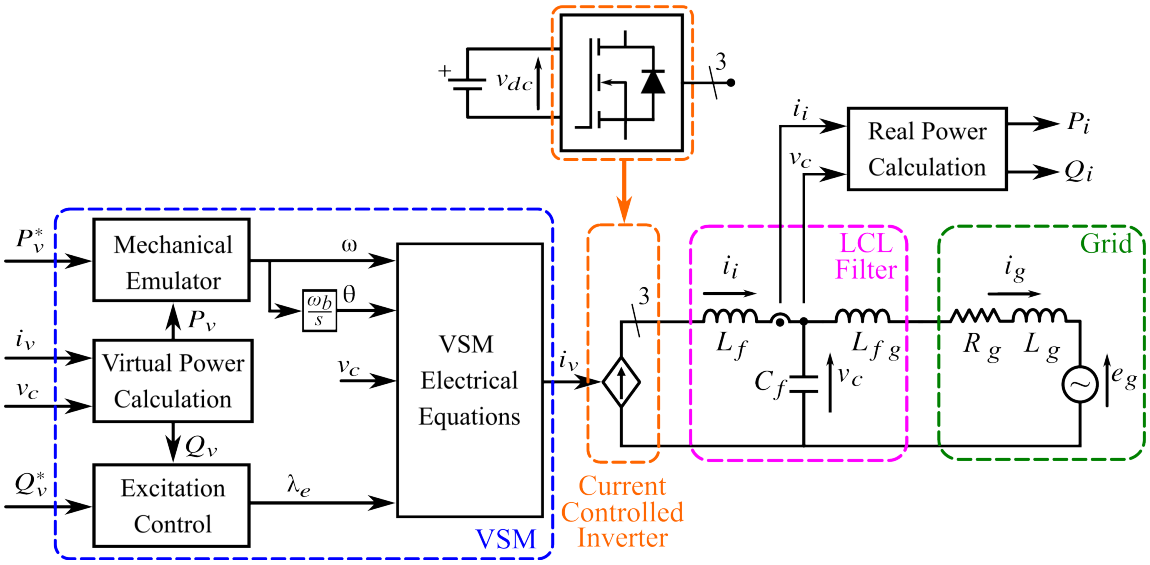


Fig. 2.4 Control scheme of the adopted current-source VSM model.

- **Virtual Power Calculation:** This block computes the VSM virtual powers P_v and Q_v by multiplying the VSM virtual current i_v with the measured grid voltage v_c;
- **Mechanical emulation:** It emulates the mechanical behavior of the VSM, by embedding the swing equation of conventional SGs [11]:

$$P_v^* - P_v = 2H\frac{d\omega}{dt} \tag{2.1}$$

  where H is the inertia constant and ω is the virtual rotor speed.

  Furthermore, any of the damping solutions in the literature must be integrated into this block to suppress the low frequency oscillations [43], [52], [53];

- **Excitation Control:** This function receives as inputs the reactive power reference Q_v^* and the virtual reactive power Q_v, providing as output the excitation flux λ_e, which is thus regulated to provide the desired reactive power exchange with the grid. Different design solutions are available in the literature for the excitation control feature, such as the excitation winding model of a real SG [41], a simple droop-based proportional gain controller [54], a purely integral [46] or proportional-integral [43] regulator, a feedforward-based solution [55];
- **Electrical Equations:** The resistive and inductive behavior of the VSM stator is emulated by implementing a virtual inductance L_v and resistance R_v. The electric

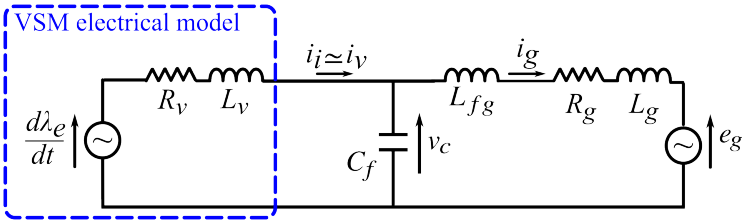


Fig. 2.5 Single phase electrical circuit of the VSM interfaced to the grid [57].

model receives as inputs v_c, the resulting virtual rotor speed ω and excitation flux λ_e and the virtual rotor position θ.

The presented VSM model does not embed active-reactive droop controllers to perform primary frequency and voltage regulation features. Nevertheless, these functionalities can be enabled by simply implementing two external proportional regulators, thus generating the droop references P_d^* and Q_d^* to be added to P_v^* and Q_v^*, as in [56]:

$$P_d^* = \frac{\omega^* - \omega}{b_p} \tag{2.2}$$

$$Q_d^* = \frac{\hat{V}_c^* - \hat{V}_c}{b_q} \tag{2.3}$$

where ω^* and $\hat{V}_c^*$ are the grid speed and voltage amplitude references, while b_p and b_q are the droop coefficients.

The single phase equivalent circuit of the conventional VSM interfacing the grid is depicted in Fig. 2.5. Since the internal current controller response is several order of magnitude faster than the one of the VSM algorithm, its transfer function can be ideally assumed with a unity gain during the discussion. Consequently, the inverter output current i_i is considered equal to the reference $i_i^* = i_v$, while the inverter output powers P_i and Q_i are assumed equal to the virtual powers P_v and Q_v.

The proposed VSM conventional model serves as the foundation for the following discussion. It will be integrated with the innovative algorithms related to VSMs, which are presented in the subsequent Chapters 3 and 4.

Chapter 3

Power Decoupling Methods for VSMs during Grid Support

This chapter aims to propose an active–reactive power decoupling solution directly integrated into the VSM algorithm, thus enhancing the provision of grid ancillary services by VSM-driven inverters under all operating conditions. An outline of the chapter is provided below:

- The introductory section provides a detailed discussion of the power coupling issue in VSM applications, emphasizing its impact on the quality of ancillary services provision. Existing power decoupling strategies for grid-forming power converters reported in the literature are then reviewed, highlighting their limitations and thus motivating the development of a decoupling algorithm specifically designed to improve the grid support provision by VSMs;
- The conventional VSM of Chapter 2 is enhanced with the proposed decoupling solution;
- The VSM linearized electrical model used to investigate the P-Q coupling issue is obtained. It serves as the basis for deriving the presented decoupling method. Then, the operation of the proposed decoupling solution is explained in detail;
- The sensitivity of the proposed decoupling algorithm to the grid parameters is investigated;

- The operation of the S-VSC, i.e., the implemented VSM model used for the experimental validation of the proposed decoupling solution, is described in detail;
- Experimental results are provided, thus validating the proposed method in performing the decoupling during inertial support and grid faults. Moreover, the power coupling suppression during power transients due to variation of VSM power references is investigated;
- A final section provides the conclusions and highlights the main contributions.

The results of this chapter are presented in the publications [57] and [58].

3.1 Power Coupling Issue in VSMs

The control algorithms designed for grid-forming power converters (e.g., VSMs) typically rely on the assumptions that active power linearly depends on the load angle (P-δ) and that reactive power depends solely on the voltage amplitude (Q-V) [11]. This assumption holds true in the case of a purely inductive transmission line and a VSM operating with small load angle. However, in many practical scenarios, such as low-voltage networks and microgrids, the grid and VSM resistances, as well as the load angle, cannot be neglected. Consequently, the active and reactive power are coupled (i.e., a variation in active power also induces a change in reactive power and vice versa) [59]. The main consequences include degraded dynamic performance, steady-state errors and an increased risk of system instability.

Moreover, the VSM capability in providing dynamic ancillary services, such as inertial support or fault current injection, is affected as well. Indeed, a larger amount of current is required to provide grid transient support. Furthermore, an additive fluctuating power flow can propagate from the grid to the DC-side of the inverter. Such oscillatory power behavior may adversely affect the lifespan of batteries, including those in EVs in the case of ultra-fast DC charging applications [19], [60], which are connected to the DC-side of the inverter as illustrated in Fig. 1.8. Consequently, particularly in the case of VSMs implemented in the AFEs of high-power loads, the integration of decoupling solutions must be considered to limit current stress on the hardware and to prevent ancillary services provision from interfering with the primary function of the application, e.g., the charging process.

To address the coupling issue, numerous power decoupling solutions have been proposed in the literature for grid-forming power converters, such as VSM-driven inverters [61], [62], [63], [64], [65], [66], [67], [68], [69], [70], [71], [72], [73], [74]. The virtual impedance method [61], [62], [63], [64] is one of the most widely adopted solutions. However, its decoupling capability is limited, as demonstrated in [63]. Furthermore, this method only compensates for the coupling due to the line resistive behavior, while the error introduced by the small load angle assumption is not considered [59]. In addition, it ensures decoupling only under steady-state conditions, as is also the case for the virtual power method [64], [65] and the feedforward-based algorithms in [66], [67], [68].

More recent works have specifically addressed the issue of dynamic power coupling in VSM controls [69], [70], [71], [72], [73], [74]. The VSM model proposed in [69] aims to mitigate the impact of reactive power variations on active power control. However, the reverse coupling is not considered. In addition, the compensation achieved is only partial, since the line is assumed to be purely inductive and only the deviation caused by large load angle is addressed. Instead, the method in [70] embeds the excitation control loop with a grid voltage estimator, which compensates for the line voltage drop and decouples the reactive power from the active power response.

Other recent works have introduced feedforward terms into the VSM active loop [71], [72] to enhance the VSM dynamic response. However, these methods primarily focus on improving power reference tracking and oscillation damping, while the power coupling phenomena are only treated as a secondary aspect. A VSM model combining a simplified virtual steady-state impedance with a current reference modification is proposed in [73] to mitigate power coupling. While this approach ensures both active and reactive power decoupling, it is tailored to a specific VSM model in which the virtual admittance is algebraically implemented. An enhanced feedforward-based method is proposed in [74], achieving full active–reactive decoupling, while immunity to grid impedance deviations is ensured through a power coupling observer. However, the accuracy of the algorithm is limited by errors in load angle estimation. In conclusion, all the aforementioned methods address power coupling primarily to improve VSM dynamic response and converter stability, without assessing its impact on the provision of ancillary services, such as inertial support or fault current injection.

Motivated by the lack of discussion on this topic in the literature, a straightforward decoupling solution, based on the implementation of feedforward terms in the conventional VSM model (Fig. 2.4) is presented in this chapter. The proposed solution ensures complete

active–reactive power dynamic decoupling while providing grid support, offering the following advantages:

- Feedforward terms are integrated into the VSM excitation control loop to cancel the reactive power injection during grid frequency deviation events. As a result, the current stress on the AFE during inertial support is minimized;
- The implementation of decoupling terms in the VSM swing equation (2.1) eliminates active power fluctuations, which could otherwise propagate from the AC-side to the DC-stage during reactive power support in the event of grid faults, thus potentially degrading the batteries connected to the DC-side.

Nevertheless, the designed algorithm guarantees a fully decoupled dynamic response in the case of VSM power reference variations. This method has a high degree of generality, as it can be implemented in any VSM with excitation control loop and mechanical emulation block, such as the conventional VSM model described in Chapter 2.

3.2 VSM Embedded with the Proposed Decoupling Algorithm

The conventional VSM model of Chapter 2 embedded with the proposed feedforward decoupling solution is depicted in the block diagram of Fig. 3.1.

Compared to the conventional VSM model, the following blocks are added:

- **Q-Decoupling:** This block cancels reactive power deviations caused by active power transients. Specifically, it computes the feedforward term $\lambda_{e,dec}$, which is added to the excitation flux λ_e^0 computed by the excitation control. The term λ_e is thus obtained and used as input for the VSM electrical model;
- **P-Decoupling:** This feature mitigates active power deviations induced by reactive power transients. In particular, it calculates the feedforward term ω_{dec}, which is added to the virtual rotor speed ω^0 computed by the mechanical emulator. The term ω is thus yielded and provided as input to the VSM electrical model.

The two algorithms are alternately enabled or disabled via the external command q_{dec}.

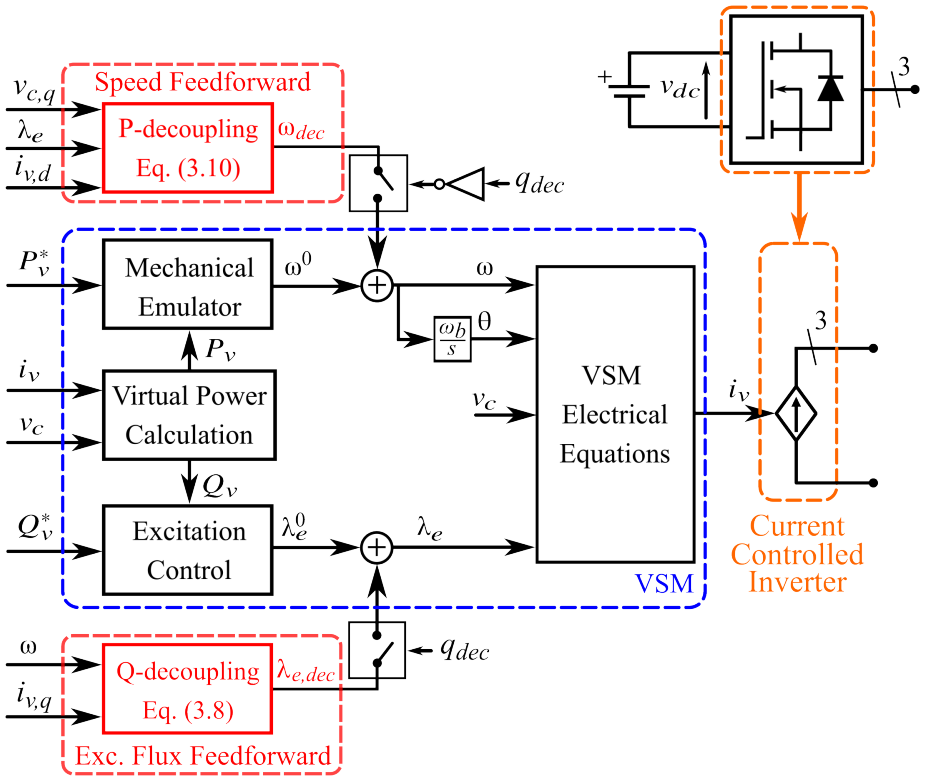


Fig. 3.1 Control scheme of the conventional VSM model embedded with the proposed feedforward-based power decoupling algorithm.

3.3 Proposed Decoupling Algorithm

The steady-state equivalent circuit in the (d,q) reference frame rotating at ω is obtained by neglecting the derivatives of currents and fluxes, as illustrated in Fig. 3.2. In the proposed model, λ_e is aligned with the d-axis (Fig. 3.3), while the VSM is assumed to operate under nominal conditions, i.e., $\omega \simeq \lambda_e \simeq 1$ pu. The grid inductance L_g and the grid-side LCL filter inductance L_{fg} can be combined into an equivalent series inductance $L_{g\ eq}$. Under these assumptions, the steady-state VSM and grid electrical equations in the (d,q) reference frame are given by (3.1)–(3.4):

$$v_{c,d} = \omega L_v i_{v,q} - R_v i_{v,d} \tag{3.1}$$

$$v_{c,q} = \omega \lambda_e - \omega L_v i_{v,d} - R_v i_{v,q} \tag{3.2}$$

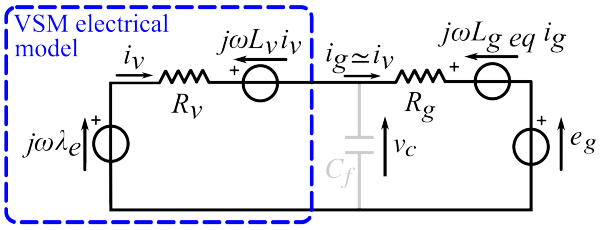


Fig. 3.2 Steady-state equivalent circuit in the (d,q) reference frame rotating at ω. C_f is neglected and an equivalent $L_{g\ eq} = L_g + L_{fg}$ is considered [57].

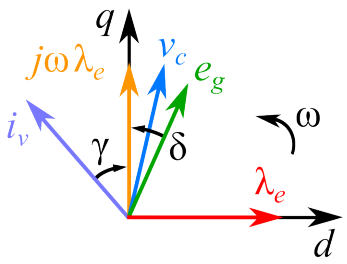


Fig. 3.3 Vector diagram of the VSM excitation flux λ_e, the VSM electromotive force $j\omega\lambda_e$, the measured voltage v_c, the grid voltage e_g and the virtual current i_v in the adopted (d,q) reference frame rotating at ω. δ is the load angle, while γ is the phase shift between i_v and $j\omega\lambda_e$ [75].

$$e_{g,d} = \omega L_{g\ eq} i_{g,q} - R_g i_{g,d} + v_{c,d} \tag{3.3}$$

$$e_{g,q} = -\omega L_{g\ eq} i_{g,d} - R_g i_{g,q} + v_{c,q} \tag{3.4}$$

The grid current i_g can be approximated as equal to i_v by neglecting the LCL filter capacitance C_f [39]. Consequently, the equivalent q-axis electrical equation is obtained by combining (3.2) and (3.4):

$$e_{g,q} = \omega\lambda_e - \omega L_{tot} i_{v,d} - R_{tot} i_{v,q} \tag{3.5}$$

where the total system inductance L_{tot} is given by the sum of L_v and $L_{g\ eq}$, while the total resistance R_{tot} is the sum of R_v and R_g.

3.3.1 Excitation Flux Feedforward

The q-axis electrical model given in (3.5) is linearized around the system operating point as follows:

$$\Delta e_g cos\delta - e_g sin\delta\Delta\delta = \Delta\omega\lambda_e + \Delta\lambda_e\omega - \Delta\omega L_{tot} i_{v,d} - \omega L_{tot}\Delta i_{v,d} - R_{tot}\Delta i_{v,q} \tag{3.6}$$

where δ is the load angle.

For small speed variations around the operating point, with low reactive current injection into the grid, the term $\Delta\omega L_{tot} i_{v,d}$ can be considered negligible. The term $\sin\delta\Delta\delta$ depends on both the load angle ($\sin\delta$) and its deviation ($\Delta\delta$). It is therefore significantly smaller than the other terms associated with ω and λ_e. In case of stable grid voltage amplitude ($\Delta e_g \simeq 0$), the q-axis linearized equation is simplified as:

$$\Delta\omega\lambda_e + \Delta\lambda_e\omega - \omega L_{tot}\Delta i_{v,d} - R_{tot}\Delta i_{v,q} = 0 \tag{3.7}$$

The relationship between the virtual speed, the excitation flux and the VSM current variations is thus established. Furthermore, the roles of the virtual and real impedances in the power coupling phenomenon are highlighted.

Since λ_e is aligned with the d-axis, v_c is predominantly oriented along the q-axis (Fig. 3.3). Consequently, the active power depends primarily on the $i_{v,q}$ current component (i.e., $P_v \approx v_{c,q} \cdot i_{v,q}$), while the reactive power depends on $i_{v,d}$ (i.e., $Q_v \approx v_{c,q} \cdot i_{v,d}$). During variations of P_v–$i_{v,q}$, such as those occurring in inertial support, undesired Q_v–$i_{v,d}$ components may be injected into the grid, as indicated by (3.7). This effect can be mitigated by introducing a feedforward term $\lambda_{e,dec}$ to the excitation flux, thus limiting deviations in $i_{v,d}$ and, consequently, the reactive power injection. The feedforward term is derived from (3.7) by enforcing $\Delta i_{v,d} \simeq 0$ and assuming $\omega \simeq \lambda_e \simeq 1$ pu:

$$\lambda_{e,dec} = -\Delta\omega + R_{tot}\Delta i_{v,q} \tag{3.8}$$

The term $\lambda_{e,dec}$ compensates for power coupling arising from the total system resistance and speed variations, and, consequently, from transient deviations in the load angle.

3.3.2 Speed Feedforward

Similar to the previous subsection, the Q_v–$i_{v,d}$ injection during grid support under fault conditions induces undesired P_v–$i_{v,q}$ variations. However, e_g varies significantly during voltage dips or swells, invalidating the main assumptions of (3.7) and rendering it unsuitable for computing a P-decoupling term. Nevertheless, an equivalent speed feedforward term can be derived by linearizing and simplifying the q-axis VSM electrical equation (3.2):

$$\Delta v_{c,q} = \Delta\omega\lambda_e + \Delta\lambda_e\omega - \omega L_v \Delta i_{v,d} - R_v \Delta i_{v,q} \tag{3.9}$$

The decoupling term is derived by enforcing $\Delta i_{v,q} \simeq 0$ and assuming $\omega \simeq \lambda_e \simeq 1$ pu:

$$\omega_{dec} = \Delta v_{c,q} - \Delta\lambda_e + L_v \Delta i_{v,d} \tag{3.10}$$

where $\Delta v_{c,q}$ compensates for grid voltage variations, while the remaining terms mitigate the P–Q coupling within the VSM.

3.3.3 Decoupling Feature Selection

Both ω_{dec} and $\lambda_{e,dec}$ mitigate P–Q coupling by reducing the mutual $i_{v,d}$–$i_{v,q}$ interaction and their dependence on virtual speed, excitation flux and grid voltage on the q-axis. Consequently, the two decoupling algorithms cannot be enabled simultaneously, as doing so would result in mutual interference and potential VSM instability. The desired decoupling function is selected via the external command q_{dec}:

- **Q-decoupling:** It is enabled by setting $q_{dec} = 1$. It limits the Q_v deviation during active power transients, such as the provision of inertial support, or variations in the inverter active power reference P_v^*. To achieve this, the additional term $\lambda_{e,dec}$, is added to the excitation flux λ_e^0 provided by the excitation control (Fig 3.1);
- **P-decoupling:** It is enabled when $q_{dec} = 0$ and effectively suppresses P_v fluctuations during reactive power transients, such as in the event of grid faults or variations in Q_v^*. The feedforward term ω_{dec} is added to ω^0, which is computed from the swing equation (2.1) in the mechanical emulator block (Fig 3.1).

The proposed decoupling algorithm is depicted in the flowchart of Fig. 3.4. The decoupling feature selection (either P-decoupling or Q-decoupling) can be executed in real time at each sampling period T_s by updating the decoupling variable q_{dec}. The VSM initial condition values $i_{v,i}$, $v_{c,i}$, $\lambda_{e,i}$, ω_i are thus saved and used to compute the small-signal deviation terms $\Delta i_{v,d}$, $\Delta i_{v,q}$, $\Delta v_{c,q}$, $\Delta\lambda_e$ and $\Delta\omega$. Accordingly, the decoupled terms ω_{dec}-$\lambda_{e,dec}$ are obtained by linearizing the VSM model around the updated steady-state operating point. Furthermore, when the corresponding decoupling algorithm is disabled, the reference values λ_e^0-ω^0 are enforced to be equal to λ_e-ω. In this way, the feedforward residuals are directly integrated into the outputs of the VSM electromechanical blocks, thus ensuring continuity in both the excitation flux and the virtual speed computation. Furthermore, the system initial values are periodically refreshed and the decoupling algorithms are reinitialized even when a steady-state condition is maintained for a predefined duration (e.g., 0.1 s).

3.4 Algorithm Sensitivity to Grid Impedance Estimation

While the P-decoupling feedforward term ω_{dec} remains unaffected by the grid impedance, the Q-decoupling component $\lambda_{e,dec}$ is sensitive to the accuracy of the grid resistance R_g estimation according to (3.8). Therefore, an accurate online computation of R_g is required to achieve full compensation of the reactive power coupling. To this end, several techniques for grid impedance estimation have been proposed in the literature [76], enabling real-time updates of the Q-decoupling algorithm. The reactive current error term, denoted as $\Delta i_{v,d,err}$, arising from an incorrect estimation of R_g, can be analytically derived from (3.7). Its expression is given by:

$$\Delta i_{v,d,err} = \frac{\tilde{R}_g - R_g}{L_v + L_{g\ eq}} \Delta i_{v,q} \tag{3.11}$$

where $\tilde{R}_g$ is the estimated grid resistance.

This spurious current component is influenced by the grid parameters, the error in the grid resistance estimation, the VSM inductance and the magnitude of the active current deviation $\Delta i_{v,q}$. Considering that $P_v \approx v_{c,q} \cdot i_{v,q}$ and $Q_v \approx v_{c,q} \cdot i_{v,d}$, the ratio between the excess reactive power $\Delta Q_{v,err}$ and the active power deviation ΔP_v can be computed from (3.11).

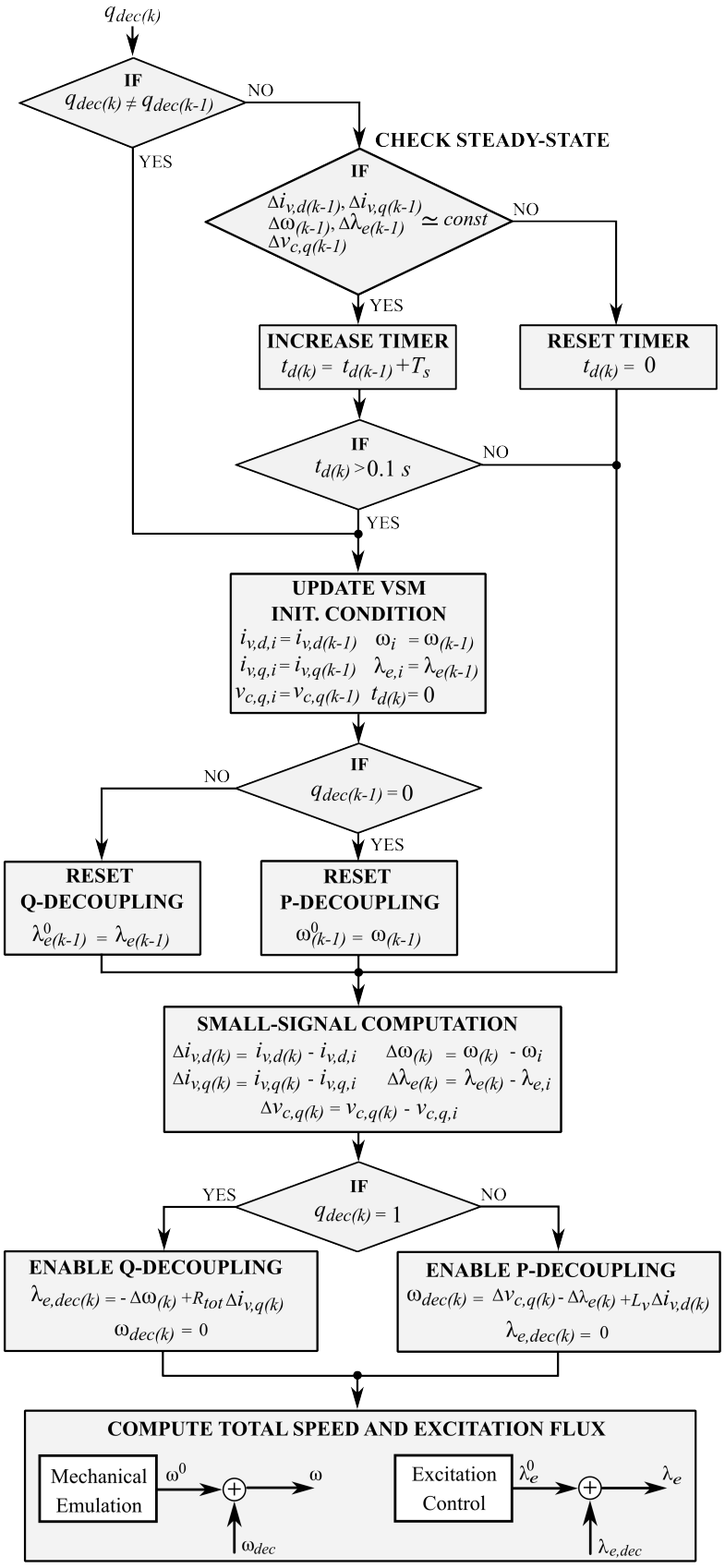


Fig. 3.4 Flowchart of the proposed power decoupling algorithm executed at sampling period k. T_s is the sampling time [57].

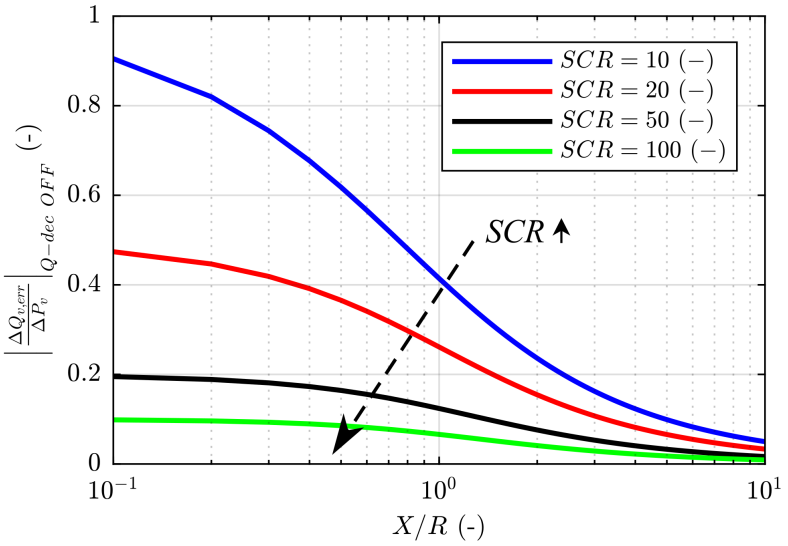


Fig. 3.5 Extra reactive power $\Delta Q_{v,err}$ injected into the grid when an active power variation ΔP_v occurs and Q-decoupling algorithm is not performed. The x-axis is in logarithmic scale [57].

This ratio can be expressed as a function of the short-circuit ratio (SCR), the X/R ratio, the virtual inductance L_v and the relative resistance estimation error $\epsilon_{R_g} = (\tilde{R}_g - R_g)/R_g$:

$$\frac{\Delta Q_{v,err}}{\Delta P_v} = \frac{\epsilon_{R_g}}{(\frac{X}{R}) + L_v \cdot SCR\sqrt{1 + (\frac{X}{R})^2}} \tag{3.12}$$

The uncompensated reactive power is thus proportional to ΔP_v and linearly dependent on ϵ_{R_g}, while it decreases when the VSM is connected to a low-impedance grid (high SCR) with predominantly inductive characteristics (high X/R). Therefore, special attention is required in the case of operation in ultra-weak or highly resistive grid conditions.

When an active power variation occurs and the Q-decoupling is disabled, the corresponding drawn reactive power can be calculated from (3.12) by setting $\tilde{R}_g = 0$, which results in $\epsilon_{R_g} = -1$:

$$\left|\frac{\Delta Q_{v,err}}{\Delta P_v}\right|_{Q-dec\ OFF} = \frac{1}{(\frac{X}{R}) + L_v \cdot SCR\sqrt{1 + (\frac{X}{R})^2}} \tag{3.13}$$

The variation of $\left|\Delta Q_{v,err}/\Delta P_v\right|_{Q-dec\ OFF}$ as a function of the X/R ratio for different SCR values is illustrated in Fig. 3.5. The VSM virtual inductance L_v is user-defined and it

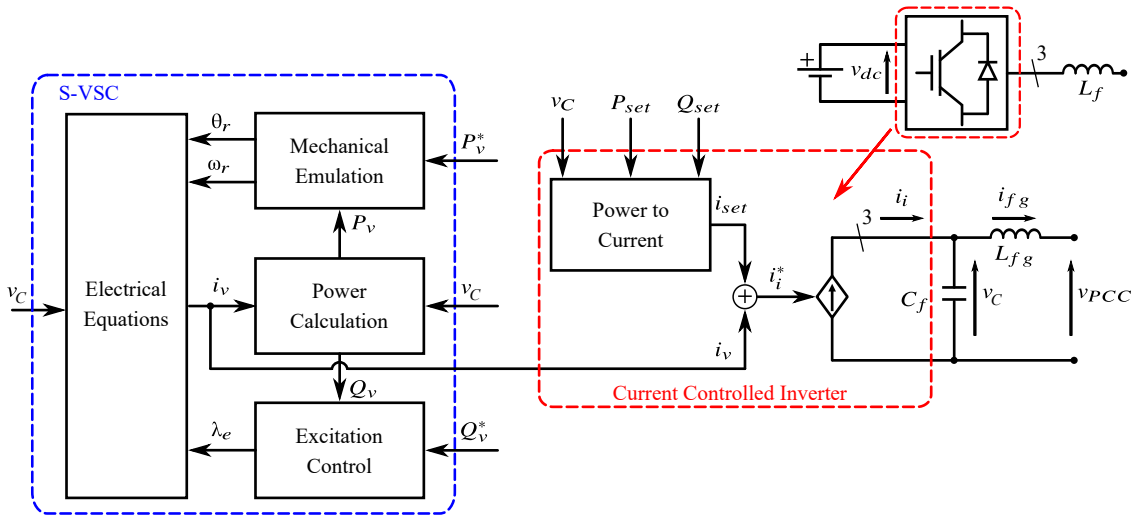


Fig. 3.6 S-VSC block control scheme [56].

is set to a typical value of 0.1 pu in this case study. In case of a weak and predominantly resistive grid with $SCR = 10$ and $X/R = 0.1$, the undesired reactive power resulting from the coupling effect is nearly equal in magnitude to the active power variation, with $\Delta Q_{v,err} = -0.9 \cdot \Delta P_v$. Conversely, the power coupling effect becomes negligible when the SCR exceeds 100 or the X/R ratio is greater than 10.

3.5 Implemented VSM Model

To perform experimental validation, the proposed decoupling solution is integrated into the VSM model known as S-VSC, a current-source VSM implemented at the Politecnico di Torino [46], [56]. A block diagram of the S-VSC is presented in Fig. 3.6. The main functional blocks of the S-VSC are analogous to those of the conventional VSM model described in Chapter 2.

The distinctive feature of the S-VSC is that it is implemented as an add-on feature operating in parallel with the conventional inverter current control structure. The latter includes a Power-to-Current block, which computes the current regulator reference i_{set} based on the active and reactive power setpoints P_{set} and Q_{set}, together with the grid voltage v_c [46]. In this way, the S-VSC can operate in two distinct modes: virtual synchronous generator (VSG) (Fig. 3.7) or virtual synchronous compensator (VSC) (Fig. 3.8). In VSG mode the reference power P^* - Q^* are provided as inputs to the VSM model by imposing $P_v^* = P^*$ and $Q_v^* = Q^*$. Conversely, $P_{set} = Q_{set} = 0$, resulting in $i_{set} = 0$ and

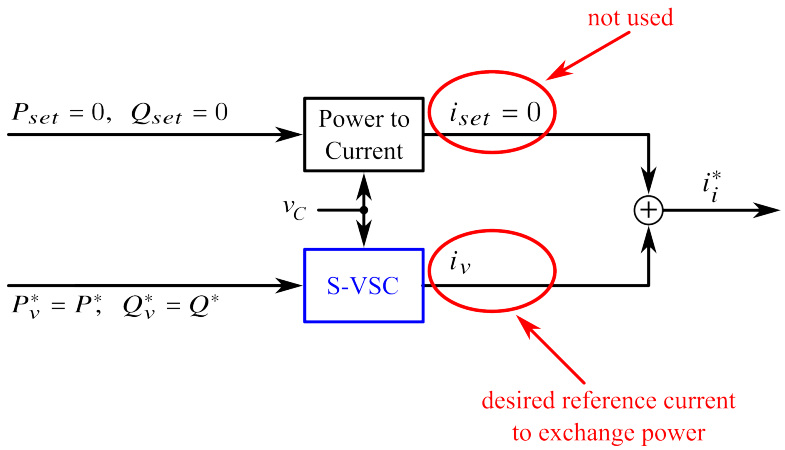


Fig. 3.7 Scheme of the S-VSC in VSG mode [77].

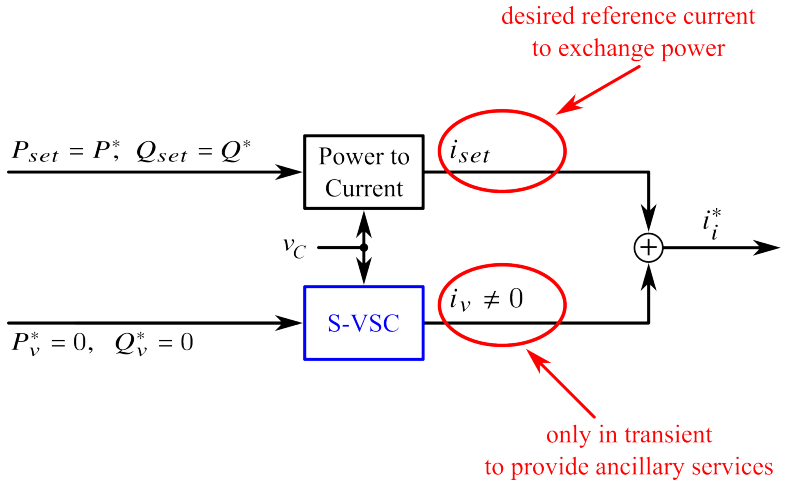


Fig. 3.8 Scheme of the S-VSC in VSC mode [77].

the inverter reference current i_i^* is thus equal to i_v. In this operating mode, the VSM model is responsible for providing dynamic support to the grid as well as managing the active–reactive power exchange. On the other hand, in VSC mode the S-VSC power references P_v^* - Q_v^* are kept equal to zero and the VSM is therefore active only during transient conditions to ensure the provision of grid services, such as inertial support and fault current injection, while remaining inoperative during steady-state operation. Instead, the continuous power exchange with the grid is managed by the conventional inverter control structure, by imposing $P_{set} = P^*$ and $Q_{set} = Q^*$. In this operating mode, the inverter reference current i_i^* is thus equal to the sum of the two terms i_v and i_{set}.

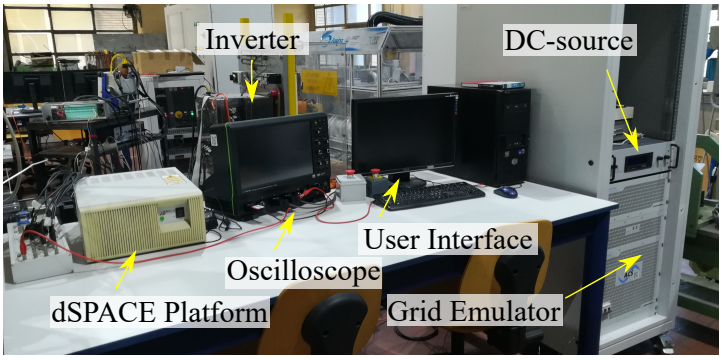


Fig. 3.9 Picture of the experimental setup [57].

The VSC mode is particularly suitable for VSM applications on high-power loads, such as ultra-fast DC chargers, where the charging operation represents the core functionality of the infrastructure and may require high-speed dynamics that can only be ensured by the traditional inverter current control on the millisecond timescale. Indeed, VSMs are normally tuned to ensure a dynamic response similar to that of SGs, i.e., on the order of hundreds of milliseconds to seconds.

In this work, since the S-VSC operating in VSG mode is, from an implementation standpoint, closer to the other current-source VSM models in the literature, this configuration was adopted for the experimental validation to provide a generalized framework for analyzing the proposed power decoupling algorithm.

3.6 Experimental Validation

The proposed feedforward decoupling algorithm was experimentally validated on a 15 kVA three-phase two-level inverter controlled by a dSPACE 1005 platform with switching f_{sw} and sampling f_s frequencies of 10 kHz. A picture of the experimental setup is shown in Fig. 3.9, while the corresponding system configuration is outlined in the block diagram of Fig. 3.10. The inverter is interfaced with a 50 kVA grid emulator through an LCL filter, which provides a 50 Hz, 120 V_{rms} phase voltage. The inverter DC-side is powered by a constant DC source, emulating a locally installed energy storage system. As grid impedance, a three-phase inductor and a three-phase resistor are inserted between the power converter and the grid emulator. The grid equivalent inductance is thus $L_{g\,eq} = L_{fg} + L_g = 0.046$ pu, $SCR = 7.58$ and $X/R = 0.37$.

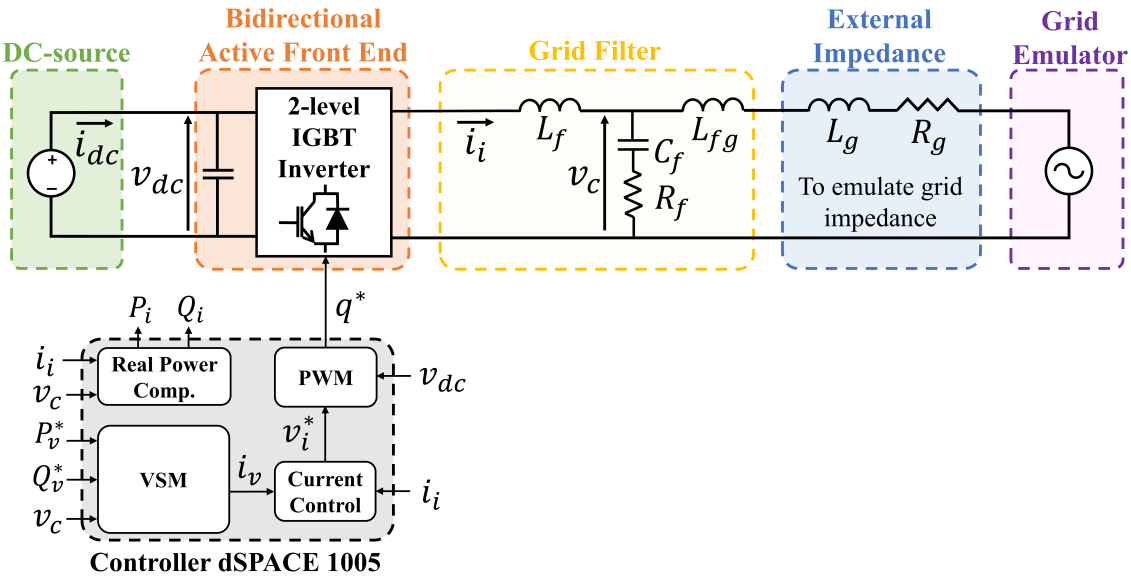


Fig. 3.10 Scheme of the system configuration used for tests.

As explained in the previous section, the S-VSC [46] is implemented in its VSG mode. Moreover, it is integrated with the VSM damping solution proposed in [53] to suppress VSM speed oscillations. The excitation control consists of an integral regulator. Consequently, the reactive power control behaves as a first-order system with a tunable excitation time constant τ_e.

The inverter nominal data, LCL filter and grid parameters, as well as the VSM parameters, are summarized in Table 3.1.

Five experimental tests were conducted to validate the proposed decoupling method:

- **Test 1:** The VSM inertial response is evaluated. The inverter is absorbing an active power $P_i = P_v^* = -0.25$ pu from the grid to store energy into the DC source when a triangular frequency variation in the range 49.5-50.5 Hz with a period of 2 s is imposed by the grid emulator. The inverter is expected to provide additional active power according to the VSM tuning and the frequency deviation. In contrast, the desired inverter reactive power Q_i is null. The effectiveness of the proposed decoupling algorithm in suppressing reactive power injection without affecting the inertial response is thereby demonstrated;

- **Test 2:** A grid frequency drop is imposed by the grid emulator to simulate a significant power imbalance during active power absorption by the inverter ($P_i = P_v^* = -0.5$

Table 3.1 Main data of the experimental setup [57].

Base Values		**Inverter**		**VSM**		**LCL Filter & Grid**	
S_b	15 kVA	S_n	15 kVA	L_v	0.1 pu	L_f	0.059 pu
V_b	170 V	I_n	59 A	R_v	0.02 pu	C_f	0.020 pu
f_b	50 Hz	V_{dc}	380 V	H	4 s	L_{fg}	0.013 pu
Z_b	2.9 Ω	f_{sw}	10 kHz	ζ	0.7	L_g	0.033 pu
L_b	9.2 mH	f_s	10 kHz	τ_e	0.1-1 s	R_g	0.124 pu
C_b	1.1 mF						

pu). The performance of the reactive power decoupling is then evaluated under this severe grid perturbation;

- **Test 3:** A 10 % voltage dip is applied by the grid emulator while the inverter operates in idle mode ($P_v^* = Q_v^* = 0$). This condition is expected to induce a reactive fault current. Simultaneously, the P-decoupling algorithm mitigates power fluctuations that could otherwise propagate to the DC-link, preventing undesired rapid charging and discharging of the DC-side connected storage;

- **Test 4:** The advantages of the proposed P–Q decoupling solution are assessed during the normal dynamic operation of the VSM. The VSM response to various step changes in active and reactive power references is analyzed both with and without the decoupling algorithm enabled;

- **Test 5:** The sensitivity of the Q-decoupling algorithm to grid resistance estimation is investigated under a step change in P_v^*, with the reactive power controller disabled. The steady-state error of Q_i is investigated for various values of relative estimation error ϵ_{R_g}.

3.6.1 Inertial Response

A linear variation of the grid frequency is imposed to assess the VSM performance during inertial support. The excitation controller is configured to yield a slow response ($\tau_e = 1$ s) in order to emphasize the advantages of the proposed decoupling solution. The expected active power injection is proportional to the virtual frequency derivative $\Delta f_r/\Delta t$ as given by:

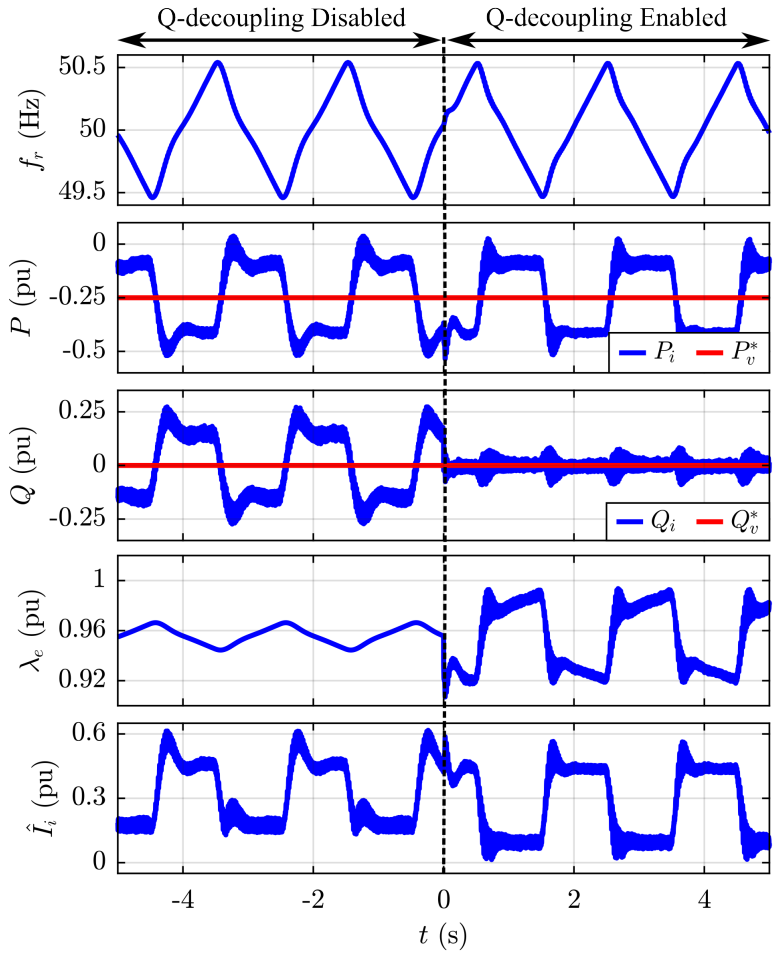


Fig. 3.11 Results of Test 1 (inertial behavior). From top to bottom: virtual frequency f_r, inverter active power P_i and virtual active power reference P_v^*, inverter reactive power Q_i and reactive power reference Q_v^*, excitation flux λ_e, output current peak $\hat{I}_i$ [57].

$$\Delta P_{inertial} = \frac{2H}{f_b} \cdot \frac{\Delta f_r}{\Delta t} = 0.16 \text{ pu} \tag{3.14}$$

This amount of power is superimposed on the absorbed power (-0.25 pu) that the inverter is already delivering to the DC source. In field applications involving high-power load, such as ultra-fast DC charging systems, $\Delta P_{inertial}$ is either supplied or absorbed by the locally installed off-board storage or directly by the EV batteries (Fig. 1.8). Initially, power decoupling is not applied, resulting in a maximum reactive power of 0.25 pu. As illustrated in Fig. 3.11, at time $t = 0$ s the Q-decoupling algorithm is activated, effectively suppressing the reactive power without impacting the inertial support feature. Indeed, the Q-decoupling algorithm provides $\Delta\lambda_e = \lambda_{e,dec}$ required to instantaneously compensate for

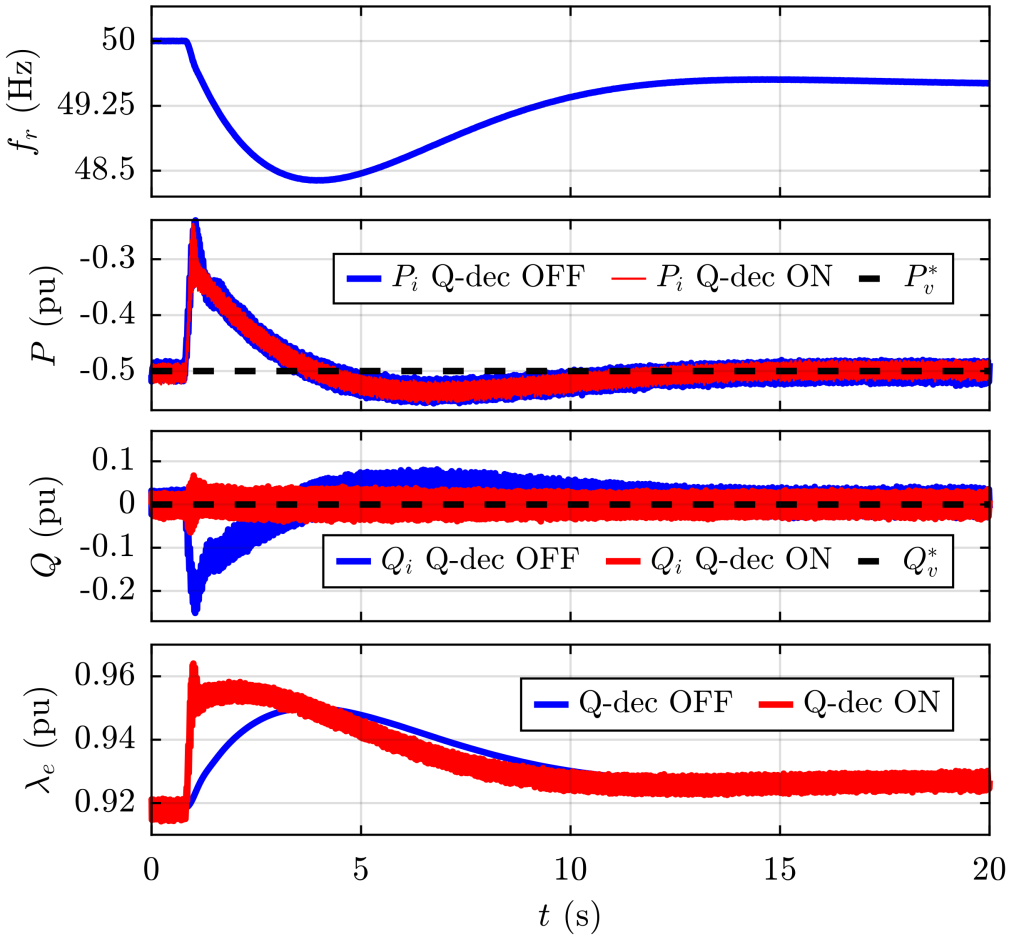


Fig. 3.12 Results of Test 2 (inertial behavior). From top to bottom: virtual frequency f_r, inverter active power P_i and virtual active power reference P_v^*, inverter reactive power Q_i and virtual reactive power reference Q_v^*, excitation flux λ_e [57].

the reactive power coupling. Furthermore, the peak current injected into the grid is reduced by 9.8 %, decreasing from 0.61 pu to 0.55 pu. Therefore, the current stress on the installed hardware required to perform grid support is significantly reduced.

3.6.2 Grid Frequency Drop

In Test 2 (Fig. 3.12), a severe grid frequency drop caused by a large power imbalance is emulated. Such a profile can occur in the event of a major generator disconnection from the grid. The grid frequency drops to a nadir of 48.39 Hz before stabilizing at a final value of 49.50 Hz. During this event, the inverter supplies 0.5 pu of active power to the DC source.

A deliberately severe frequency variation, with a low nadir, high initial slope and reduced post-fault value is applied to assess the effectiveness of the Q-decoupling algorithm. The test is performed both with and without the proposed feedforward decoupling, with the reactive controller set to $\tau_e = 1$ s in each case. The results obtained corroborate the findings of Test 1. Specifically, the proposed decoupling method preserves the inertial response while effectively limiting both the reactive power and the injected current during inertial support.

3.6.3 Voltage Dip

A 10 % voltage dip is applied to evaluate the performance of the P-decoupling algorithm under a short-circuit condition in the mains (Fig. 3.13). The fault occurs while the inverter is in idle mode ($P_v^* = Q_v^* = 0$), so that any power transfer from the DC source to the grid during the test is solely attributable to the power coupling effect. The excitation time constant τ_e is reduced to 0.1 s, thus intentionally accelerating the reactive control response. At $t = 0$ s, the voltage dip occurs. If the P-decoupling algorithm is not activated, an undesired amount of active power is injected into the grid, reaching a peak of 0.32 pu. Moreover, the resulting power fluctuations propagate through the inverter to the DC-side, causing a significant fluctuating current i_{dc} to be drawn from the DC-stage. This rapid peak current would initially be supplied by the DC-link capacitors, according to their energy capability. Then the current would be drawn from the local storage connected to the converter DC-stage, potentially affecting the battery lifetime. Conversely, when the P-decoupling algorithm is activated, the active power injection into the grid is nearly eliminated. Simultaneously, the DC-side operation is no longer affected by the provision of grid support during fault conditions. Furthermore, enabling the P-decoupling algorithm allows the desired fault current profile to be accurately attained. In fact, the behavior of the fault current Δi_{fault} can be described as follows:

$$\Delta i_{fault} = \frac{\Delta V_{dip}}{L_v + L_{g\ eq}} \cdot e^{-t/\tau_e} \tag{3.15}$$

where ΔV_{dip} denotes the amplitude of the voltage dip during the fault condition (0.1 pu in the present test).

Consequently, the VSM inductance and the excitation controller time constant can be tuned to meet the required support specifications during fault conditions. The amplitude of

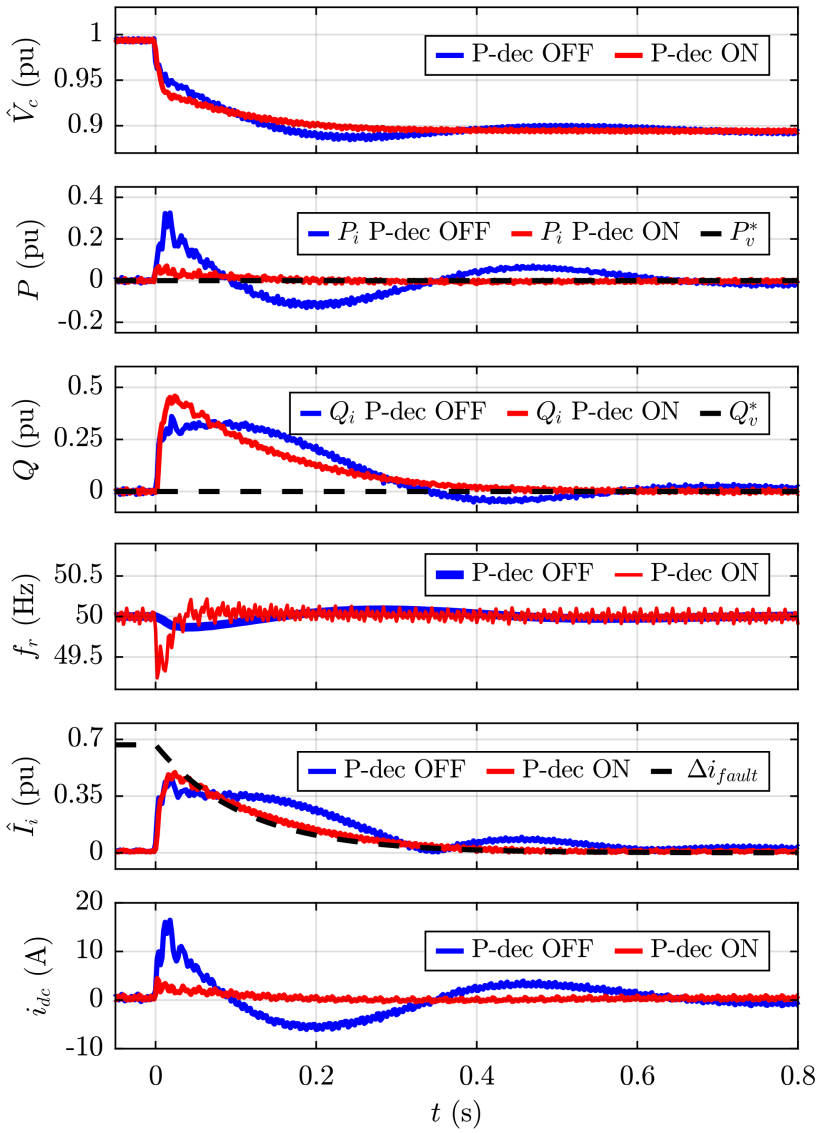


Fig. 3.13 Results of Test 3 (voltage dip) with the P-decoupling algorithm disabled and then enabled. From top to bottom: grid measured voltage peak $\hat{V}_c$, virtual active power P_v and active power reference P_v^*, reactive power Q_v and reactive power reference Q_v^*, virtual frequency f_r, inverter output current peak $\hat{I}_i$, current absorbed from the DC source i_{dc} [57].

the current injection is governed by L_v, whereas the duration of the event is determined by τ_e.

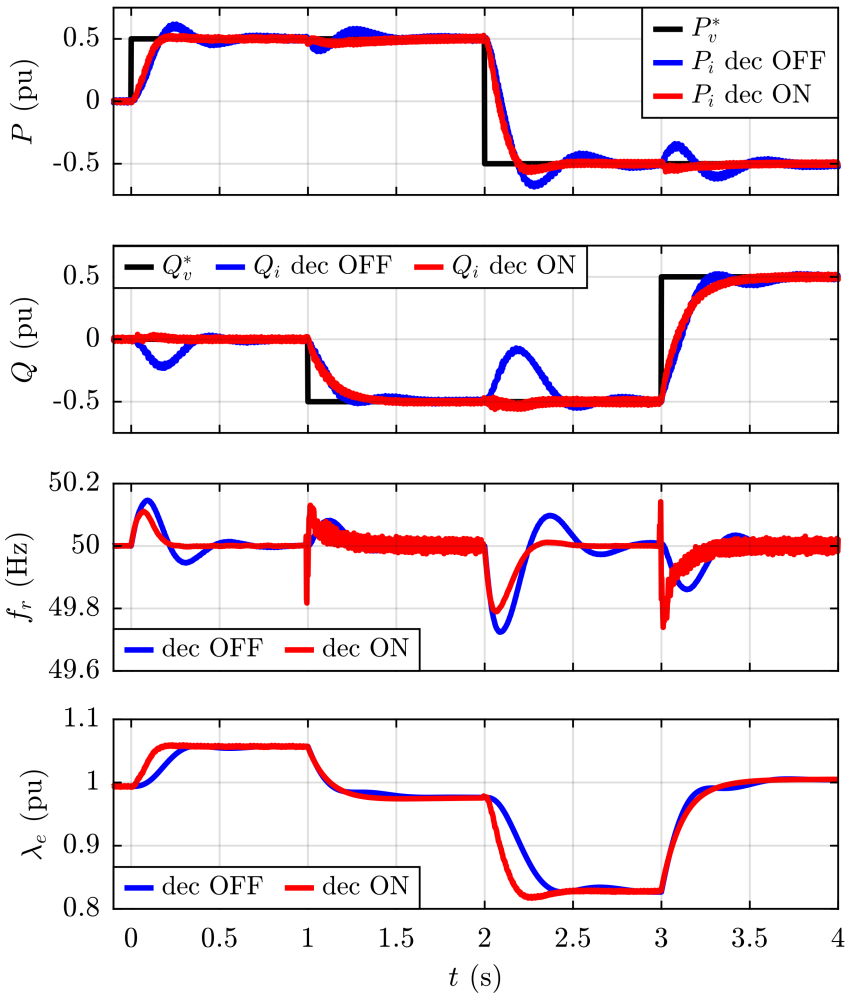


Fig. 3.14 Results of Test 4 (dynamic performance). From top to bottom: inverter active power P_i and virtual active power reference P_v^*, inverter reactive power Q_i and virtual reactive power reference Q_v^*, virtual frequency f_r, excitation flux λ_e [57].

3.6.4 Dynamical Operation

The dynamic performance of the VSM integrated with the proposed decoupling solution is evaluated by analyzing its response to various step changes in active and reactive power references (Fig. 3.14). The decoupling algorithm is selectively activated in correspondence with the power reference changes. Specifically, the P-decoupling algorithm is engaged by setting $q_{dec} = 0$ prior to a variation in Q_v^*, while the Q-decoupling algorithm is triggered by setting $q_{dec} = 1$ before a change in P_v^*. When one decoupling algorithm is enabled, the other is automatically disabled to prevent interference. The excitation time constant

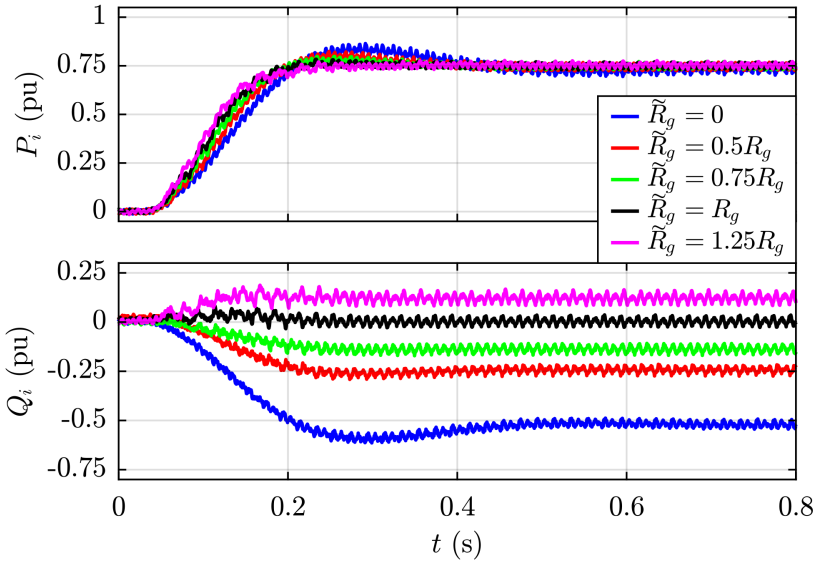


Fig. 3.15 Results of Test 5: effect of a wrong grid resistance estimation. From top to bottom: inverter active power P_i, inverter reactive power Q_i [57].

τ_e is set to 0.1 s to ensure comparable response times for both the VSM active and reactive control loops. Initially, the inverter operates with zero power references (i.e., $P_v^* = Q_v^* = 0$). At $t = 0$ s, a step change of $P_v^* = 0.5$ pu is requested. After 1 s, the reactive power reference is also step-changed to $Q_v^* = -0.5$ pu. Finally, the active and reactive power references are inverted at $t = 2$ s and $t = 3$ s, respectively. Under demanding test conditions, including step reversals of power references, the proposed P-decoupling and Q-decoupling algorithms effectively eliminate all power coupling effects during both P_v^* and Q_v^* variations. Specifically, Q_i fluctuations are fully suppressed when P_i changes and vice versa. Additionally, the power responses exhibit increased damping while preserving the original rise time.

3.6.5 Sensitivity to Grid Resistance Estimation

This test investigates the impact of R_g estimation on the effectiveness of the Q-decoupling algorithm. The reactive controller is disabled by setting its integral gain to zero, so that excitation flux variations are solely determined by the computed feedforward term $\lambda_{e,dec}$. A 0.75 pu step in active power is applied, and the resulting reactive power response is evaluated for various estimated grid resistance $\tilde{R}_g$ values, corresponding to 0 %, 50 %, 75 %, 100 % and 125 % of R_g (Fig. 3.15). The ΔQ_i deviations observed at the end of

Table 3.2 Comparison of the results of Test 5 with the theoretical values obtained with (3.12) [57].

$\tilde{R}_g/R_g$ (%)	ε_{R_g} (%)	ΔQ_i (pu)	$\Delta Q_{v,err}$ (pu)
0	-100	-0.52	-0.64
50	-50	-0.24	-0.32
75	-25	-0.14	-0.16
100	+0	+0.00	+0.00
125	+25	+0.12	+0.16

the transient response are then compared with the theoretical values $\Delta Q_{v,err}$ computed using (3.12). The results are summarized in Table 3.2 and indicate a strong agreement between measured and theoretical values. Notably, larger discrepancies are observed under significant estimation errors, such as when $\tilde{R}_g = 0$. These differences in the results can be attributed to the fact that $\Delta Q_{v,err}$ is derived using small-signal analysis, which assumes only minor variations around an operating point. In contrast, this test imposes a large active power change ($\Delta P_i = 0.75$ pu). Furthermore, when the R_g estimation is inaccurate, the resulting significant deviation of Q_i from the initial steady-state condition further affects the gap.

The results of Test 5 further validate the proposed Q-decoupling algorithm. When R_g is accurately estimated, reactive power injection is completely eliminated ($\Delta Q_i = 0$ pu), even for substantial variations in active power.

3.7 Conclusion

This chapter introduces a full decoupling strategy of active and reactive power for VSMs, aimed at compensating power coupling effects during rapid grid transients, including frequency fluctuations and voltage dips or swells. By enabling the Q-decoupling feature, feedforward terms are introduced at the output of the VSM excitation controller, thus canceling the reactive power injection during inertial support. By contrast, enabling the P-decoupling algorithm introduces feedforward terms into the VSM swing equation. As a

result, active power fluctuations are mitigated when the AFE injects short-circuit current into the grid during faults. Finally, the proposed decoupling solution guarantees a full-decoupled power response even in the event of power transients due to step-variations of VSM power references. The presented method thus limits the current effort required by the VSM algorithm to perform both ancillary services and fast power exchange variations with the grid, thus reducing losses and hardware stress on the inverter.

The selection between P-decoupling and Q-decoupling is performed by configuring the external command q_{dec}. When the user requests a variation in active or reactive power references, the appropriate decoupling feature can be pre-selected, ensuring correct power decoupling. In contrast, grid voltage and frequency perturbations are inherently unpredictable. Therefore, careful consideration is required when selecting the feature while the grid-tied inverter is operating in steady-state. The selection can be guided by agreements with the TSO concerning which ancillary services have to be provided by the VSM-driven inverter. Otherwise, additional considerations pertaining to the power converter hardware design may be taken into account.

The Q-decoupling algorithm limits the inverter current stress during inertial support. Therefore, a reduced rated current can be considered in the inverter design phase to ensure the capability to provide inertial behavior.

The P-decoupling algorithm eliminates both AC and DC power fluctuations when the inverter injects reactive current into the grid during voltage dips and swells. As this power would initially be drawn from the DC-link capacitors, the algorithm prevents the need for oversizing them in terms of energy.

Accordingly, the authors recommend enabling Q-decoupling by default if the inverter design did not account for additional current stress on the power switches due to power coupling phenomena. Alternatively, P-decoupling should be enabled by default to permit the installation of a DC-link with reduced energy capability.

Chapter 4

Online Grid Impedance Estimation through VSMs

This chapter presents a dedicated grid impedance estimator for VSM applications, which can be directly integrated into any VSM algorithm. The chapter covers the following topics:

- The need for accurate knowledge of grid impedance to ensure proper VSM tuning and operation, illustrated through selected examples;
- A comprehensive literature review of online grid impedance estimation methods for grid-following, grid-forming and VSM-driven inverters;
- The innovative contribution of the proposed VSM-dedicated grid impedance estimator, compared to existing methods in the literature;
- An outline of the functional blocks of the proposed VSM-based grid impedance estimator integrated into the conventional VSM model of Chapter 2;
- The linearized electrical model used to investigate the dependence of the VSM on grid parameters;
- The detailed description of the proposed VSM-based grid impedance estimator, built on the obtained linearized electrical model;
- The tuning procedure of the designed grid impedance estimator, along with its automation and sensitivity analysis to the deviations of the grid voltage and frequency;

- The experimental validation carried out on different hardware setups;
- A summary of the main findings and contributions.

The outcomes of this chapter contributed to the publication of [75], [78] and [79]. Moreover, the proposed grid impedance estimator is currently patented under the Italian patent law, under application number 102024000022908.

4.1 Influence of Grid Impedance on VSM Operation

Similar to SGs, the grid impedance affects VSM operation by limiting the converter power transfer capability and influencing both local stability and dynamic response [11]. Consequently, knowledge of the grid impedance is required to appropriately tune the main functional blocks of the conventional VSM discussed in Chapter 2 (Fig. 2.4), according to the following considerations:

- The damping strategies are typically implemented into the mechanical emulator block to suppress low-frequency power oscillations due to the interaction with the power system. These algorithms require knowledge of the grid reactance to ensure a proper algorithm tuning [43], [52], [53];
- Independent of the specific excitation control strategy adopted for the VSM, the reactive power dynamic response is inherently influenced by the grid inductance [55]. Consequently, this grid parameter must be explicitly incorporated into the tuning process of the excitation control. Otherwise, the capability of the VSM to provide adequate reactive support may be substantially impaired;
- As discussed in detail in Chapter 3, VSMs exhibit a coupling between active and reactive power responses when they are interfaced with a resistive power system [59]. Similarly to the power decoupling method proposed in this thesis [57], [58], other approaches in the literature rely on accurate grid resistance estimation to properly compensate for the resistive behavior of the power line [70], thus making the reactive power control insensitive to active power variations;
- Accurate grid impedance estimation is needed for the proper tuning of the lower-level inverter controller, thus enhancing the converter stability, which is strictly dependent on the grid stiffness [80], [81].

For the aforementioned reasons, accurate grid impedance estimation is essential for the real-time adjustment of VSM control parameters, thus ensuring stable operation and achieving the desired dynamic response.

4.2 Online Grid Impedance Estimation: Literature Review

The online estimation of local grid impedance through the grid-tied inverter control has been extensively investigated in the literature [76]. While several methods have been proposed for grid-following converters, only more recently solutions have been developed for grid-forming and VSM-controlled inverters.

4.2.1 Estimation through Grid-Following Converters

Grid impedance estimation methods for grid-following converters can be formally classified into passive and active approaches, based on whether the power converter deliberately injects a perturbation into the grid. Passive approaches exploit preexisting grid voltage and current harmonic distortions [82], [83] or natural grid transient events [84] to estimate the grid impedance. These methods typically exhibit a low signal-to-noise ratio [82], with estimation accuracy strongly dependent on the magnitude of the measured grid voltage and current distortion.

In contrast to passive approaches, active impedance estimation techniques rely on injecting controlled perturbations into the grid, followed by processing the resulting grid voltage and current responses. For example, certain methods introduce sinusoidal disturbances into the grid through either current [85], [86] or voltage [87], [88], [89] excitation at non-characteristic frequencies, i.e., frequencies that are not integer multiples of the fundamental. Other active approaches excite the grid by injecting impulsive disturbances, either through modifications of the inverter current references [80], [90], [91] or of the voltage commands [92]. This allows grid impedance estimation across a wide frequency range. Furthermore, pseudo-random binary [93], [94] and ternary sequences [95], as well as white noise disturbances [96], can be superimposed on the current references to perturb the power system. Although achieving high accuracy, all the aforementioned methods require the application of advanced data processing techniques, such as Fourier transforms [80], [85],

[87], [90], [91], [93], [94], [95], [96], [97], wavelet transforms [86], Kalman filters [88], [89], or recursive least squares (RLS) algorithms [92]. Furthermore, these techniques contribute to increase grid harmonic distortion, as they involve the injection of disturbances at frequencies other than the fundamental. As a result, compliance with international standards may be compromised [13].

Among active methods, P-Q reference variation algorithms are notable for their implementation simplicity. These techniques exploit variations in the active and reactive power references to change the operating point, thus extracting information on grid parameters, which are subsequently computed using algebraic computation [98], [99]. These methods cause minimal grid disruption while providing accurate estimation. However, P-Q reference variations inherently induce a load angle drift, resulting in a rotation of the adopted (d,q) synchronous reference frame. As a result, the measured current and voltage signals are referenced to different, misaligned (d,q) frames. This misalignment negatively affects the calculation of grid parameters, thus reducing the overall estimation accuracy [100]. The estimation accuracy can be improved by increasing the number of analyzed operating points, thus mitigating the effects of load angle deviation, albeit at the expense of additional execution time [101], [102].

4.2.2 Estimation through Grid-Forming Converters

Recent studies have focused on enabling grid impedance estimation through grid-forming power converters by adapting conventional P-Q variation methods [103], [104], [105]. A non-invasive technique is proposed in [103], where both grid inductance and resistance are computed in real-time using algebraic formulas. Additionally, a Kalman filter is employed to mitigate noise and measurement errors, thus enhancing estimation accuracy. The method proposed in [104] exploits the slow transient response of the grid-forming converter to trigger a RLS solver for grid parameter estimation. Instead, the approach presented in [105] requires only active power variations to estimate both inductance and resistance. As the grid impedance is determined via algebraic calculations, the authors recommend filtering current and voltage measurements to reduce sensitivity to disturbances. Although VSMs are control algorithms with grid-forming capabilities, all of these P-Q reference variation methods [103], [104], [105] cannot be directly implemented into VSM controls. This limitation arises because these estimation techniques do not account for the implementation of a virtual impedance, which is a common feature in VSM models [33], [34] as shown in Fig. 2.4, where the VSM electrical equations block is implemented.

4.2.3 Estimation through VSM-Driven Converters

Similar to grid-forming converters, existing recent studies allow VSM-controlled inverters to perform grid impedance estimation by incorporating conventional methods into their control. Specifically, a non-characteristic harmonic excitation method is integrated into the lower-level inverter current controller in [106], [107], increasing the overall control algorithm complexity and introducing the risk of interaction between the VSM control and the estimation procedure. Indeed, VSMs are capable of mitigating harmonic distortions in the grid [46], [108]. Consequently, they can react to external harmonic disturbances directly injected through the lower-level inverter controller, thus interfering with the impedance estimation process. In [109], a VSM is integrated with an RLS solver to estimate grid impedance using a non-intrusive approach. However, the proposed RLS method requires knowledge of the Thevenin equivalent grid voltage, which is not directly measurable. The authors assume it is known a priori and do not provide a procedure for its determination.

4.3 Novel Contribution to the Literature

Given the limitations of the estimation methods for VSM applications highlighted in the previous section and the sparse treatment of this topic in the literature, this chapter proposes a closed-loop grid impedance estimator, specifically designed for VSMs, that is directly integrated into the VSM model.

When an amount of current is directly injected into the grid through the inverter lower-level control, without being processed by the VSM algorithm, the VSM control is perturbed and its response depends on grid parameters. Therefore, a grid impedance estimation method is designed by leveraging the VSM sensitivity to these injected current disturbances.

The proposed estimator offers several advantages:

- It can be implemented in any VSM equipped with an excitation control loop [33], [34], as the conventional VSM model of Chapter 2;
- It inherently suppresses measurement noise, providing filtered results without requiring the implementation of advanced filtering solutions (e.g., Kalman filters);

- It can be easily tuned to balance the desired estimation time and filtering performance;
- It avoids the use of advanced mathematical processing (e.g., Fourier transform, Kalman filtering, RLS solvers) and relies only on basic algebraic computations to compensate for estimation errors due to load angle deviations during the estimation process, thus reducing algorithm complexity;
- It yields reliable results independently of the inverter operating conditions, the grid stiffness and the tuning of the VSM parameters.

4.4 VSM Embedded with the Proposed Estimator

The block diagram of the conventional VSM model of Chapter 2 embedded with the proposed grid impedance estimator is depicted in Fig. 4.1. The estimation procedure is triggered by the external commands q_{L_g} and q_{R_g}, which respectively enable the grid inductance and resistance estimation. Three additional blocks are integrated into the VSM to enable the grid impedance esimation:

- **Current Injection Block:** This block is used to introduce the external current perturbation required for grid parameters estimation. It provides the current i^*_{inj} to the lower-level inverter current controller, that is combined with i_v to compute i^*_i (i.e., $i^*_i = i_v + i^*_{inj}$). In this way, the desired current i_{inj} is injected into the mains during the grid parameters estimation process;
- **Estimation Block:** It represents the core function of the proposed estimation algorithm, combining the **Integral Estimator** and the **Data Compensator** sub-modules. The integral estimator controls the deviation of the virtual reactive current $i_{v,d}$ thus computing the terms $\Delta\lambda_{L_g}$ and $\Delta\lambda_{R_g}$, which are added to λ^0_e during grid inductance and resistance estimation, respectively. Finally, it outputs the preliminary values of grid inductance $\tilde{L}'_g$ and resistance $\tilde{R}'_g$. These raw values are then processed by the data compensator to yield the final estimations of grid inductance $\tilde{L}_{g\ eq}$ and resistance $\tilde{R}_g$. Once $\tilde{L}_{g\ eq}$ and $\tilde{R}_g$ have been determined, the estimated equivalent Thevenin grid voltage $\tilde{e}_g$ can also be readily computed;
- **Active Current Regulator:** This block is in charge of canceling the deviation of the virtual active current $i_{v,q}$ during grid impedance estimation by adding the additional

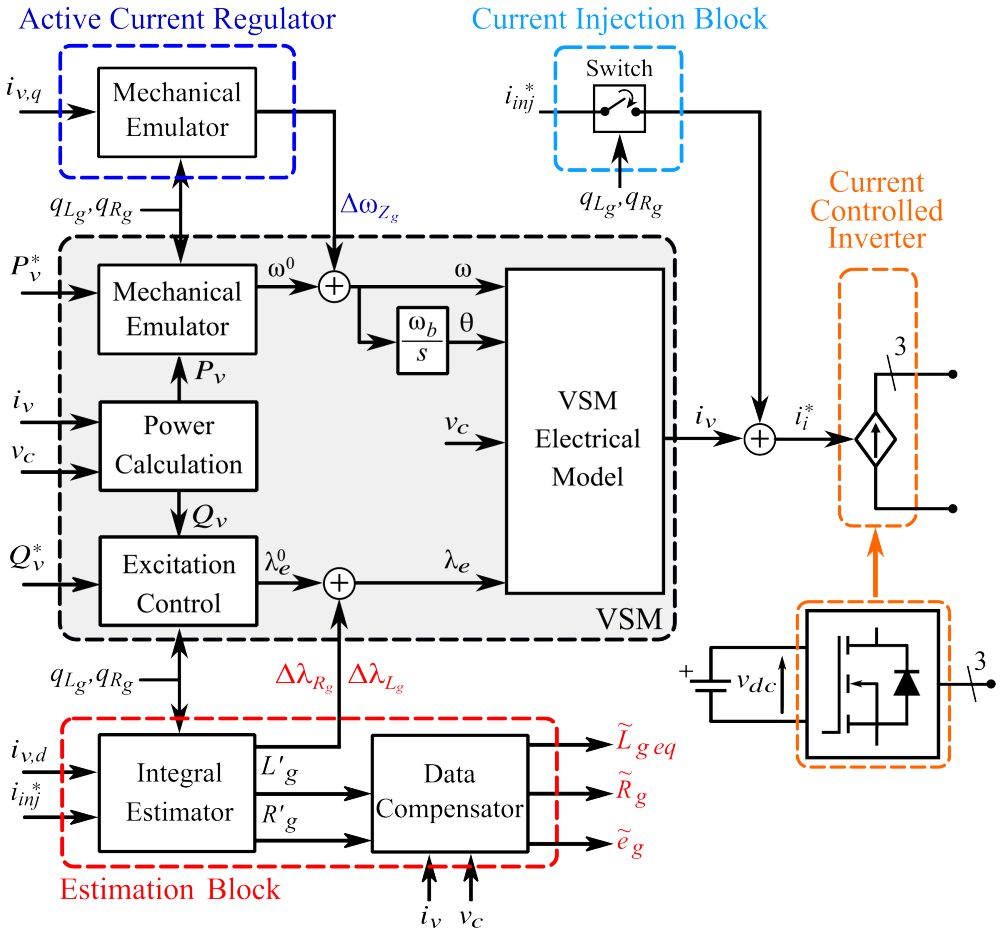


Fig. 4.1 Control scheme of the conventional VSM model embedded with the proposed VSM-based grid impedance estimator, which consists of three blocks: the estimation block (red highlight), the active current regulator (blue highlighted) and the current injection block (light blue highlighted).

term $\Delta\omega_{Z_g}$ to ω^0. It includes a module that replicates the mechanical emulator used to regulate P_v.

A detailed explanation of these additive functions will be presented in next sections.

As detailed in Chapter 2, the lower-level current control loop is several orders of magnitude faster than the VSM dynamic response and it can be simplified as ideal, with a unity gain transfer function. Therefore, the inverter output current i_i is assumed to match the reference $i_i^* = i_v + i_{inj}^*$ and the injected current is approximated as $i_{inj} \simeq i_{inj}^*$ in the discussion.

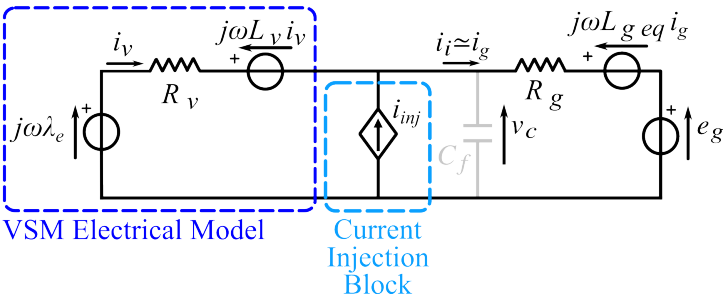


Fig. 4.2 Steady-state equivalent circuit in the (d,q) reference frame rotating at ω. C_f is neglected and an equivalent $L_{g,eq} = L_g + L_{fg}$ is considered [75].

4.5 Linearized VSM Electrical Model

The steady-state equivalent circuit in the (d,q) rotating reference frame of the VSM embedded with the proposed grid impedance estimator is obtained by neglecting the derivative terms (Fig. 4.2). The system steady-state equations (3.1)–(3.4), previously presented in Chapter 3, remain valid and can be reformulated according to the new VSM configuration by substituting i_g with $i_i = i_v + i_{inj}$ and neglecting the LCL filter capacitance C_f [39]. Moreover, $e_{g,d}$ and $e_{g,q}$ can be expressed as $e_g \sin\delta$ and $e_g \cos\delta$ (Fig. 3.3). Therefore, by combining and rearranging (3.1) with (3.3) and (3.2) with (3.4), the resulting equivalent electrical equations are obtained:

$$0 = (R_v + R_g) \cdot i_{v,d} + R_g \cdot i_{inj,d} - \omega(L_v + L_{g\,eq}) \cdot i_{v,q} - \omega L_{g\,eq} \cdot i_{inj,q} + e_g \sin\delta \tag{4.1}$$

$$\omega\lambda_e = (R_v + R_g) \cdot i_{v,q} + R_g \cdot i_{inj,q} + \omega(L_v + L_{g\,eq}) \cdot i_{v,d} + \omega L_{g\,eq} \cdot i_{inj,d} + e_g \cos\delta \tag{4.2}$$

Under the assumption of small deviations around the operating point ($\omega \simeq \lambda_e \simeq 1$ pu) and constant grid impedance ($\Delta R_g \simeq \Delta L_{g\,eq} \simeq 0$), the per-unit linearized electrical equations are derived as:

$$\begin{aligned} 0 = {} & (R_v + R_g) \cdot \Delta i_{v,d} + R_g \cdot \Delta i_{inj,d} - (L_v + L_{g\ eq}) \cdot \Delta i_{v,q} - L_{g\ eq} \cdot \Delta i_{inj,q} \\ & - [(L_v + L_{g\ eq}) \cdot i_{v,q} + L_{g\ eq} \cdot i_{inj,q}] \cdot \Delta\omega + \Delta e_g \sin\delta + e_g \cos\delta \cdot \Delta\delta \end{aligned} \tag{4.3}$$

$$\begin{aligned} \Delta\lambda_e = {} & (R_v + R_g) \cdot \Delta i_{v,q} + R_g \cdot \Delta i_{inj,q} + (L_v + L_{g\ eq}) \cdot \Delta i_{v,d} + L_{g\ eq} \cdot \Delta i_{inj,d} \\ & + [(L_v + L_{g\ eq}) i_{v,d} + L_{g\ eq} i_{inj,d} - 1] \cdot \Delta\omega + \Delta e_g \cos\delta - e_g \sin\delta \cdot \Delta\delta \end{aligned} \tag{4.4}$$

The expression of the load angle deviation $\Delta\delta$ can be obtained from (4.3):

$$\begin{aligned} \Delta\delta = {} & [-(R_v + R_g) \cdot \Delta i_{v,d} - R_g \cdot \Delta i_{inj,d} + (L_v + L_{g\ eq}) \cdot \Delta i_{v,q} + L_{g\ eq} \cdot \Delta i_{inj,q} \\ & + [(L_v + L_{g\ eq}) \cdot i_{v,q} + L_{g\ eq} \cdot i_{inj,q}] \cdot \Delta\omega - \Delta e_g sin\delta] \cdot \frac{1}{e_g \cos\delta} \end{aligned} \tag{4.5}$$

Therefore, by combining (4.4)–(4.5), the resulting equivalent electrical equation in the q-axis, with $\Delta\delta$ explicitly expressed, is derived:

$$\begin{aligned} \Delta\lambda_e = {} & [(L_v + L_{g\ eq}) + (R_v + R_g)\tan\delta] \cdot \Delta i_{v,d} \\ & + [(R_v + R_g) - (L_v + L_{g\ eq})\tan\delta] \cdot \Delta i_{v,q} \\ & + [L_{g\ eq} + R_g \cdot \tan\delta] \cdot \Delta i_{inj,d} \\ & + [R_g - L_{g\ eq} \cdot \tan\delta] \cdot \Delta i_{inj,q} \\ & + [(L_v + L_{g\ eq})(i_{v,d} - i_{v,q} \cdot \tan\delta) + L_{g\ eq}(i_{inj,d} - i_{inj,q} \cdot \tan\delta) - 1] \cdot \Delta\omega \\ & + \frac{\Delta e_g}{\cos\delta} \end{aligned} \tag{4.6}$$

As highlighted by (4.6), the VSM operation is affected by the injected current Δi_{inj}, along with the grid voltage and frequency deviations Δe_g and $\Delta\omega$.

When a $\Delta i_{inj,d}$ or $\Delta i_{inj,q}$ injection occurs, the response of the mechanical emulator to cancel the P_v perturbation would be sufficient to limit the $i_{v,q}$ deviation only if the VSM operates at low power or if the implemented L_v and R_v are negligible. Indeed, under these conditions, the voltage v_c can be considered primarily aligned with the q-axis (Fig. 3.3) and the active power is approximately linear with respect to $i_{v,q}$ (i.e., $P_v \simeq v_{c,q} \cdot i_{v,q}$ in

per-unit). However, for high power operation or when significant virtual impedance is implemented, this assumption no longer holds. Consequently, an additional block, i.e., the active current regulator shown in Fig. 4.1 must be integrated into the VSM to compensate for $\Delta i_{v,q}$ variations.

Instead, $\Delta i_{v,d}$ can be counteracted in (4.6) by adding an extra term $\Delta\lambda_e$ to the excitation flux λ_e. The term $\Delta\lambda_e$ is proportional to the injected currents $\Delta i_{inj,d}$ and $\Delta i_{inj,q}$ and it is influenced by the grid parameters R_g, $L_{g\ eq}$ and the load angle δ. Under the assumption of constant grid voltage and frequency ($\Delta e_g \simeq \Delta\omega \simeq 0$), the value of $\Delta\lambda_e$ required to cancel $\Delta i_{v,d}$ is:

$$\Delta\lambda_e = (L_{g\ eq} + R_g \cdot \tan\delta) \cdot \Delta i_{inj,d} + (R_g - L_{g\ eq} \cdot \tan\delta) \cdot \Delta i_{inj,q} \tag{4.7}$$

Two intermediate variables, associated with the actual grid parameters R_g and $L_{g\ eq}$ and the load angle δ are defined as follows:

$$L'_g = L_{g\ eq} + R_g \cdot \tan\delta \tag{4.8}$$

$$R'_g = R_g - L_{g\ eq} \cdot \tan\delta \tag{4.9}$$

where L'_g and R'_g denote the raw values of grid inductance and resistance, respectively.

Accordingly, two excitation flux terms are obtained by combining (4.7) with (4.8)–(4.9):

$$\Delta\lambda_{L_g} = L'_g \cdot \Delta i_{inj,d} \tag{4.10}$$

$$\Delta\lambda_{R_g} = R'_g \cdot \Delta i_{inj,q} \tag{4.11}$$

where $\Delta\lambda_{L_g}$ and $\Delta\lambda_{R_g}$ represent the additional excitation flux required to limit $\Delta i_{v,d}$ in the case of $\Delta i_{inj,d}$ and $\Delta i_{inj,q}$ injection, respectively.

If the VSM is connected to a stiff grid or operates at low power, the load angle becomes negligible, so that $\tan\delta \simeq 0$. In this case, $L'_g \simeq L_{g\ eq}$ and $R'_g \simeq R_g$. Consequently, (4.10)–(4.11) can be simplified as in [78]:

$$\Delta\lambda_{L_g}\big|_{\delta\to 0} \simeq L_{g\ eq}\cdot\Delta i_{inj,d} \tag{4.12}$$

$$\Delta\lambda_{R_g}\big|_{\delta\to 0} \simeq R_g\cdot\Delta i_{inj,q} \tag{4.13}$$

As a result, $L_{g\ eq}$ and R_g can be directly computed from (4.12) and (4.13), respectively.

However, when the VSM delivers high power while connected to a weak grid, the small load angle assumption no longer holds. In this case, additional algebraic manipulations are required to account for the effect of the load angle in (4.10)–(4.11), thus to derive $L_{g\ eq}$ and R_g in the general case. From Fig. 3.3, $\tan\delta$ can be expressed as:

$$\tan\delta = \frac{e_{g,d}}{e_{g,q}} \tag{4.14}$$

By substituting the steady-state grid electrical equations (3.3)–(3.4) into (4.14):

$$\tan\delta = \frac{v_{c,d} + L_{g\ eq}(i_{v,q}+i_{inj,q}) - R_g(i_{v,d}+i_{inj,d})}{v_{c,q} - L_{g\ eq}(i_{v,d}+i_{inj,d}) - R_g(i_{v,q}+i_{inj,q})} \tag{4.15}$$

Assuming a small external current injection, the effect of $i_{inj,d}$ and $i_{inj,q}$ on $\tan\delta$ can be neglected and (4.15) simplifies to:

$$\tan\delta \simeq \frac{v_{c,d} + L_{g\ eq}\cdot i_{v,q} - R_g\cdot i_{v,d}}{v_{c,q} - L_{g\ eq}\cdot i_{v,d} - R_g\cdot i_{v,q}} \tag{4.16}$$

Finally, the grid inductance and resistance are determined by combining (4.16) with (4.8)–(4.9):

$$e'_{g,d} = L'_g\cdot i_{v,q} - R'_g\cdot i_{v,d} + v_{c,d} \tag{4.17}$$

$$L_{g\ eq} = \frac{L'_g - R'_g \cdot \left(\frac{e'_{g,d}}{v_{c,q}}\right)}{1 + \left(\frac{e'_{g,d}}{v_{c,q}}\right)^2} \tag{4.18}$$

$$R_g = \frac{R'_g + L'_g \cdot \left(\frac{e'_{g,d}}{v_{c,q}}\right)}{1 + \left(\frac{e'_{g,d}}{v_{c,q}}\right)^2} \tag{4.19}$$

where (4.17) denotes the steady-state grid electrical equation in the d-axis, evaluated using the raw variables L'_g and R'_g instead of the real parameters $L_{g\ eq}$ and R_g.

In brief, a grid impedance estimation algorithm can be developed by exploiting the effect of grid parameters on the VSM excitation control response when a current i_{inj} is injected into the grid without being processed by the VSM. This approach enables a reliable estimation, independent of the grid stiffness or the VSM operating conditions, of both grid inductance and resistance by leveraging the relationships established in (4.10)–(4.11) and (4.18)-(4.19)

4.6 Proposed VSM-Based Grid Impedance Estimator

The estimation of grid inductance and resistance is triggered by the external commands q_{L_g} and q_{R_g}, which directly enable the injection of $i_{inj,d}$ and $i_{inj,q}$, respectively. The associated reference currents $i^*_{inj,d}$ and $i^*_{inj,q}$ are directly provided by the current injection block to the lower-level inverter current controller during the estimation process, as depicted in Fig. 4.1. Furthermore, whenever a grid parameter estimation is initiated by q_{L_g} or q_{R_g}, the most recent measurements of $i_{v,d}$, $i_{v,q}$, $v_{c,d}$ and $v_{c,q}$ are stored as the currents $i^0_{v,d}$–$i^0_{v,q}$ and voltages $v^0_{c,d}$–$v^0_{c,q}$. Specifically, by setting a high q_{L_g} or q_{R_g} at sampling instant k, the values are captured as $i^0_{v,d} = i_{v,d(k)}$, $i^0_{v,q} = i_{v,q(k)}$, $v^0_{c,d} = v_{c,d(k)}$ and $v^0_{c,q} = v_{c,q(k)}$. These stored current and voltage values are then utilized by the various blocks of the proposed estimator, as described below.

The core component of the proposed estimation tool is a closed-loop integral controller with an adjustable integral gain k_{est}, referred to as the integral estimator. It is responsible for regulating $i_{v,d}$ during the estimation process and for providing the preliminary estimation results, $\tilde{L}'_g$ and $\tilde{R}'_g$. The active current regulator block, on the other hand, is designed to

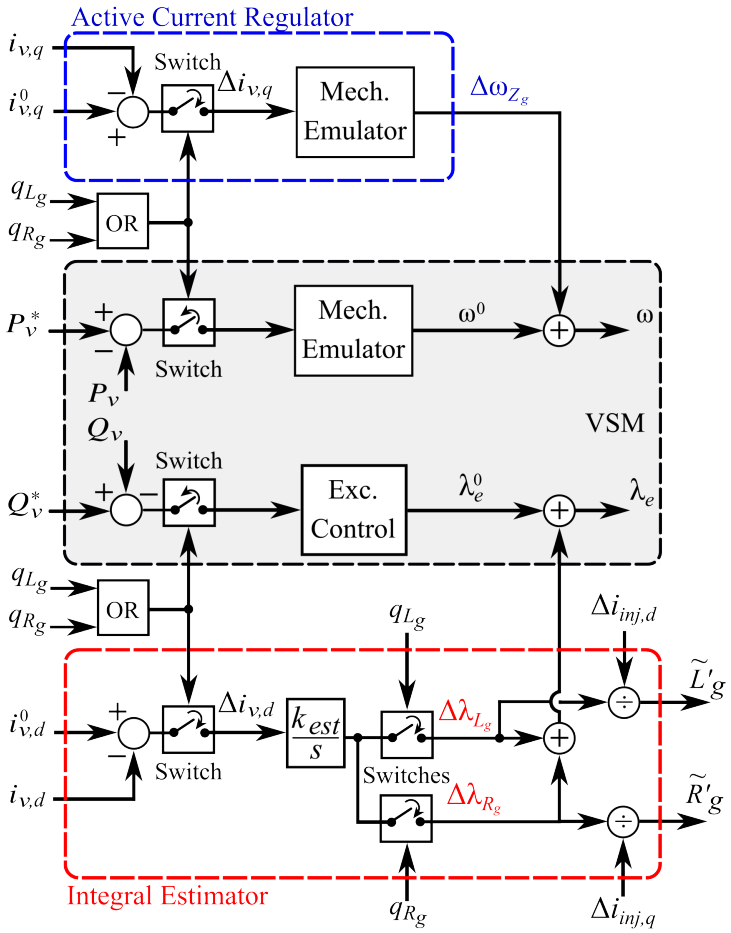


Fig. 4.3 Block diagram of the VSM excitation control and mechanical emulator integrating respectively the integral estimator (red highlighted) and the active current regulator (blue highlighted) [75].

replicate the mechanical emulator, controlling $i_{v,q}$ instead of P_v throughout the estimation process. The integral estimator and the active current regulator are integrated into the VSM model, as shown in Fig. 4.3.

During the estimation of grid inductance or resistance, the VSM excitation control and mechanical emulator are fully disabled, so that λ_e^0 and ω^0 remain fixed. At the same time, the integral estimator and the active current regulator are activated, assuming full control of $i_{v,d}$ and $i_{v,q}$, with $i_{v,d}^0$–$i_{v,q}^0$ set as the reference currents for the VSM. Consequently, they actively compensate for the virtual current deviations $\Delta i_{v,d} = i_{v,d} - i_{v,d}^0$ and $\Delta i_{v,q} = i_{v,q} - i_{v,q}^0$ induced by the injection of $i_{inj,d}$ or $i_{inj,q}$. When $i_{inj,d}$ is injected, the integral estimator generates the additional excitation flux $\Delta\lambda_{L_g}$ required to counteract the $i_{v,d}$ deviation. The raw grid inductance $\tilde{L}_g'$ is thus calculated according to (4.10). Likewise, during

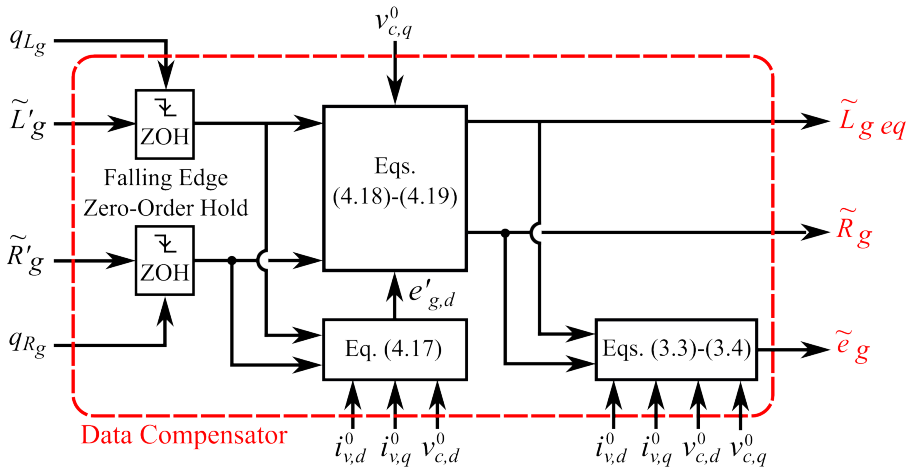


Fig. 4.4 Block diagram of the data compensator.

the injection of $i_{inj,q}$, $\Delta\lambda_{R_g}$ is determined, yielding the raw resistance $\tilde{R}'_g$ from (4.11). Simultaneously, the active current regulator computes the supplementary speed term $\Delta\omega_{Z_g}$ to limit $\Delta i_{v,q}$ for perturbations induced by both $i_{inj,d}$ and $i_{inj,q}$.

The last block to be described is the data compensator, which executes an algebraic correction within a single control period at the end of the estimation procedure. As depicted in Fig. 4.4, once the estimation concludes, the last calculated values of $\tilde{L}'_g$ and $\tilde{R}'_g$ are stored by the data compensator, which is responsible for correcting estimation errors caused by load angle deviations occurring during the estimation procedure. These stored values are then combined with $i^0_{v,d}$–$i^0_{v,q}$ and $v^0_{c,d}$–$v^0_{c,q}$ to produce the final values of estimated grid inductance $\tilde{L}_{g\ eq}$ and resistance $\tilde{R}_g$, according to (4.17)–(4.19). Finally, the estimated grid parameters $\tilde{L}_{g\ eq}$ and $\tilde{R}_g$ are utilized together with $i^0_{v,d}$–$i^0_{v,q}$ and $v^0_{c,d}$–$v^0_{c,q}$ to calculate the equivalent Thevenin grid voltage $\tilde{e}_g$, obtained by substituting these values into the grid electrical equations (3.3)–(3.4).

The operation of the proposed VSM-based grid impedance estimation algorithm at each control period k is summarized in the flowchart of Fig. 4.5. Generally, the raw grid inductance and resistance estimations must be performed in quick succession, as both $\tilde{L}'_g$ and $\tilde{R}'_g$ are needed to compute the refined values $\tilde{L}_{g\ eq}$ and $\tilde{R}_g$. However, when the VSM is connected to a stiff grid or operating at low power, data refinement can be skipped since $L'_g \simeq L_{g\ eq}$ and $R'_g \simeq R_g$, as shown in (4.12)–(4.13). In this case, the computations of $\tilde{L}_{g\ eq}$ and $\tilde{R}_g$ are fully decoupled, and only a single current injection ($i_{inj,d}$ or $i_{inj,q}$) is required to estimate the corresponding grid parameter.

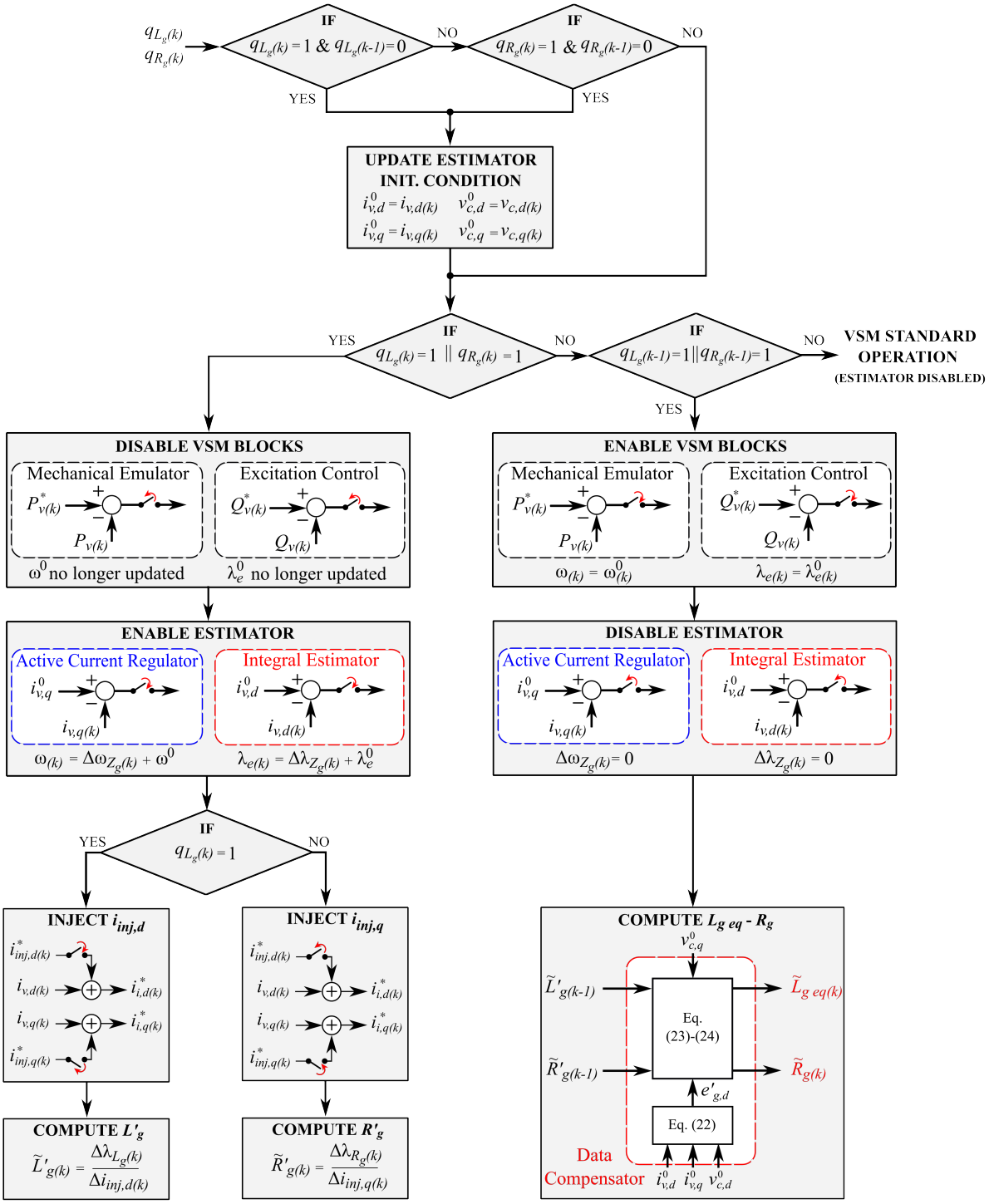


Fig. 4.5 Flowchart of the proposed VSM-based grid impedance estimator executed at sampling time k. The generic additional excitation flux $\Delta\lambda_{Z_g}$ provided by the integral estimator corresponds to $\Delta\lambda_{L_g}$ and $\Delta\lambda_{R_g}$ in case of L'_g and R'_g computation, respectively [75].

Once the estimation process is complete, both the integral estimator and the active current regulator are disabled. The VSM excitation control along with the mechanical emulator are thus reactivated (Fig. 4.5). The newly estimated values can then be used to adaptively update the gains of the VSM active [43], [52], [53] and reactive [55] power controllers, or to fine-tune the inverter current regulators [80], [81].

4.7 Tuning Procedure

While the dynamic response of the active current regulator is expected to closely match that of the mechanical emulator, the response of the integral estimator can be adjusted by appropriately tuning the closed-loop integral gain k_{est}. This tuning procedure is independent of whether L'_g or R'_g is being estimated. By considering the linearized q-axis electrical equation (4.6) and assuming small $i_{inj,d}$–$i_{inj,q}$ injections, the linearized feedback diagram of the excitation control is derived, as illustrated in Fig. 4.6. The closed-loop estimator acts as a low-pass filter, with its characteristic equation given by:

$$s \cdot [(L_v + L_{g\ eq}) + (R_v + R_g)\tan\delta] + k_{est} = 0 \tag{4.20}$$

The system is therefore characterized by a single pole, with the estimation time constant τ_{est} defined as:

$$\tau_{est} = \frac{(L_v + L_{g\ eq}) + (R_v + R_g)\tan\delta}{k_{est}} \tag{4.21}$$

The desired value of the time constant τ_{est} is achieved through proper tuning of k_{est}:

$$k_{est} = \frac{(L_v + \tilde{L}_{g\ eq}) + (R_v + \tilde{R}_g)\tan\tilde{\delta}}{\tau_{est}} \tag{4.22}$$

where $\tan\tilde{\delta}$ denotes the estimated value of $\tan\delta$.

Notably, the estimated grid inductance, resistance and load angle affect the calculation of k_{est}. Consequently, two distinct implementation strategies can be considered:

- The most recently computed values of $\tilde{L}_{g\ eq}$ and $\tilde{R}_g$, together with the current measurements of $v_{c,d}$, $v_{c,q}$, $i_{v,d}$, and $i_{v,q}$ are used to calculate $\tan\tilde{\delta}$ via (4.16). Sub-

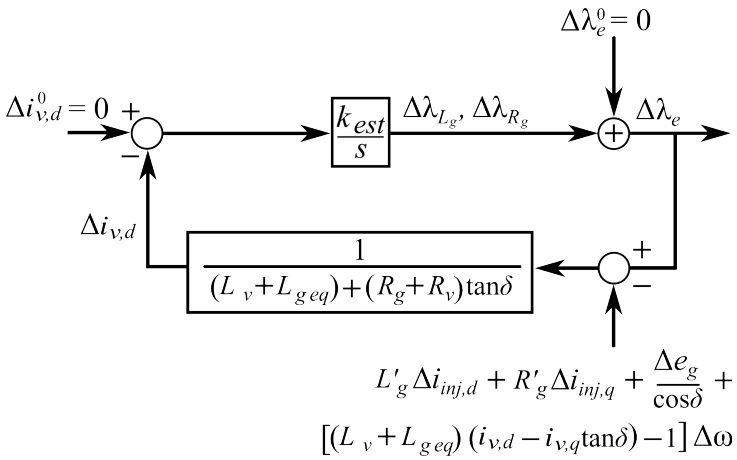


Fig. 4.6 Linearized model of the integral estimator regulating the reactive current $\Delta i_{v,d}$ [75].

sequently, $\tilde{L}_{g\ eq}$, $\tilde{R}_g$ and $\tan\tilde{\delta}$ are employed to determine k_{est} corresponding to the desired τ_{est};

- The load angle and the inductance estimation terms are considered negligible (i.e., $\tan\tilde{\delta} \simeq 0$ and $\tilde{L}_{g\ eq} \simeq 0$). Consequently, $k_{est} \simeq \frac{L_v}{\tau_{est}}$. This approach will be used to tune k_{est} during the experimental validation phase.

The real estimation time constant $\tau_{est,real}$ is therefore given by:

$$\tau_{est,real} = \frac{(L_v + L_{g\ eq}) + (R_v + R_g)\tan\delta}{(L_v + \tilde{L}_{g\ eq}) + (R_v + \tilde{R}_g)\tan\tilde{\delta}} \cdot \tau_{est} \tag{4.23}$$

Reducing the estimation time constant τ_{est} decreases the estimation execution time, while a larger τ_{est} improves noise attenuation. The estimator cut-off frequency is therefore given by:

$$f_{cut-off\ est} = \frac{1}{2\pi \cdot \tau_{est,real}} \tag{4.24}$$

Accordingly, a τ_{est} value in the range of 10-100 ms is selected for the experimental tests, balancing a short procedure duration with effective filtering of the estimated results.

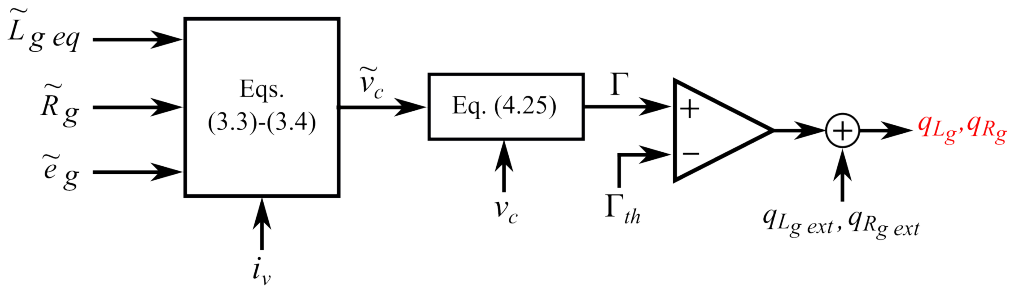


Fig. 4.7 Proposed estimation evaluation algorithm, wich enables the automatic execution of the estimation procedure when the error variable Γ exceeds the threshold Γ_{th}. The estimation procedure can be forced by the user, that can manually set the external commands $q_{L_{gext}}$ and $q_{R_{gext}}$.

4.8 Automation of the Estimation Procedure

Until now, the estimation procedure has been presented as being triggered by the commands q_{L_g} and q_{R_g} without specifying the method of their generation. These commands can be forced by an external user to execute the estimation at a desired instant. Alternatively, they can be produced automatically by an auxiliary algorithm, referred to as the estimation evaluation algorithm (Fig. 4.7). This feature uses the estimated equivalent grid inductance $\tilde{L}_{g\,eq}$, resistance $\tilde{R}_g$, equivalent Thevenin grid voltage $\tilde{e}_g$ and the VSM virtual current i_v to compute the estimated voltages $\tilde{v}_{c,d}$ and $\tilde{v}_{c,q}$ by applying the grid electrical equations (3.3)–(3.4). Ideally, in the case of correct grid parameters estimation, $\tilde{v}_{c,d} \simeq v_{c,d}$ and $\tilde{v}_{c,q} \simeq v_{c,q}$. Instead, in the event of a grid impedance or voltage variation the estimated voltage $\tilde{v}_{c,d}$ and $\tilde{v}_{c,q}$ deviate from the measured values $v_{c,d}$ and $v_{c,q}$ respectively. Therefore, an error variable Γ can be computed as follows:

$$\Gamma = \sqrt{(v_{c,d} - \tilde{v}_{c,d})^2 + (v_{c,q} - \tilde{v}_{c,q})^2} \tag{4.25}$$

In the event that Γ exceeds a predefined threshold Γ_{th}, the grid impedance estimation is automatically triggered by raising the q_{L_g} and q_{R_g} signals.

In summary, the implementation of the proposed estimation evaluation algorithm, similarly to other solutions reported in the literature [91], [102], [110], makes the estimator procedure an event-driven solution, suitable for applications requiring rapid detection of grid impedance variations, such as in unintentional islanding detection, for which international standards require the inverter to trip within 2 s of the formation of the island [111].

4.9 Estimator Sensitivity

As shown in Fig. 4.6, the integral estimator cannot distinguish whether $\Delta\lambda_e$ arises from the external current injections $\Delta i_{inj,d}$–$\Delta i_{inj,q}$ or from deviations in grid voltage Δe_g and frequency $\Delta\omega$. Although Δe_g and $\Delta\omega$ perturbations are typically small during normal grid operation and significant deviations are unlikely to occur within the short estimation period, their occurrence can affect the estimation results. Consequently, this section examines the sensitivity of the proposed estimation method to the variations of Δe_g and $\Delta\omega$.

4.9.1 Sensitivity to Grid Voltage

The impact of Δe_g on the computation of grid parameters is examined by analyzing the transfer function $\frac{\Delta\lambda_e}{\Delta e_g}$, derived from the block diagram shown in Fig. 4.6:

$$\frac{\Delta\lambda_e}{\Delta e_g} = \frac{\dfrac{k_{est}}{\cos\delta}}{s\cdot[(L_v + L_{g\ eq}) + (R_v + R_g)\tan\delta] + k_{est}} \tag{4.26}$$

The grid parameter estimation error ΔZ_{e_g} caused by Δe_g is identical for both L'_g and R'_g estimations. It can be determined by imposing $s \to 0$ (i.e., analyzing the stationary response to a step change) and dividing by the injected current Δi_{inj}, in accordance with (4.10)–(4.11):

$$\frac{\Delta Z_{e_g}}{\Delta e_g} = \frac{1}{\Delta i_{inj}} \cdot \left.\frac{\Delta\lambda_e}{\Delta e_g}\right|_{s\to 0}$$

$$\frac{\Delta Z_{e_g}}{\Delta e_g} = \frac{1}{\Delta i_{inj}\cdot\cos\delta} \tag{4.27}$$

where $\Delta i_{inj} = \Delta i_{inj,d}$ for the estimation of the raw grid inductance L'_g, while $\Delta i_{inj} = \Delta i_{inj,q}$ for the computation of the raw grid resistance R'_g.

As shown in (4.27), the effect of grid voltage variations on estimation accuracy grows with the load angle.

4.9.2 Sensitivity to Grid Frequency

Similarly, the influence of $\Delta\omega$ on the estimation of L'_g and R'_g can be analyzed by examining the transfer function $\frac{\Delta\lambda_e}{\Delta\omega}$:

$$\frac{\Delta\lambda_e}{\Delta\omega} = \frac{k_{est}\cdot[(L_v + L_{g\ eq})(i_{v,d} - i_{v,q}\cdot\tan\delta) - 1]}{s\cdot[(L_v + L_{g\ eq}) + (R_v + R_g)\tan\delta] + k_{est}} \tag{4.28}$$

The grid parameter estimation error ΔZ_ω resulting from $\Delta\omega$ is then calculated under the same assumptions used for ΔZ_{e_g} in (4.27):

$$\frac{\Delta Z_\omega}{\Delta\omega} = \frac{1}{\Delta i_{inj}}\cdot\frac{\Delta\lambda_e}{\Delta\omega}\bigg|_{s\to 0}$$

$$\frac{\Delta Z_\omega}{\Delta\omega} = \frac{(L_v + L_{g\ eq})(\sin\gamma - cos\gamma\cdot\tan\delta)\cdot i_v - 1}{\Delta i_{inj}} \tag{4.29}$$

where γ represents the phase shift between the VSM virtual current i_v and the electromotive force $j\omega\lambda_e$, as illustrated in Fig. 3.3.

For a given δ, the estimator maximum sensitivity to $\Delta\omega$ occurs when $\gamma = \delta - \pi/2$:

$$\frac{\Delta Z_\omega}{\Delta\omega}\bigg|_{\gamma=\delta-\frac{\pi}{2}} = -\frac{\frac{L_v + L_{g\ eq}}{\cos\delta}\cdot i_v + 1}{\Delta i_{inj}} \tag{4.30}$$

Therefore, according to (4.29)–(4.30), the effect of speed variations on estimation accuracy increases with both the load angle δ and the virtual current i_v.

According to (4.27) and (4.29), the sensitivity of the estimator to grid voltage and frequency variations can be mitigated by injecting a sufficiently large Δi_{inj}. However, the chosen magnitude of Δi_{inj} must remain small enough to avoid significant interference with the operation of the grid-tied power converter. Consequently, a value of $\Delta i_{inj} = \pm$ 0.1 pu is recommended.

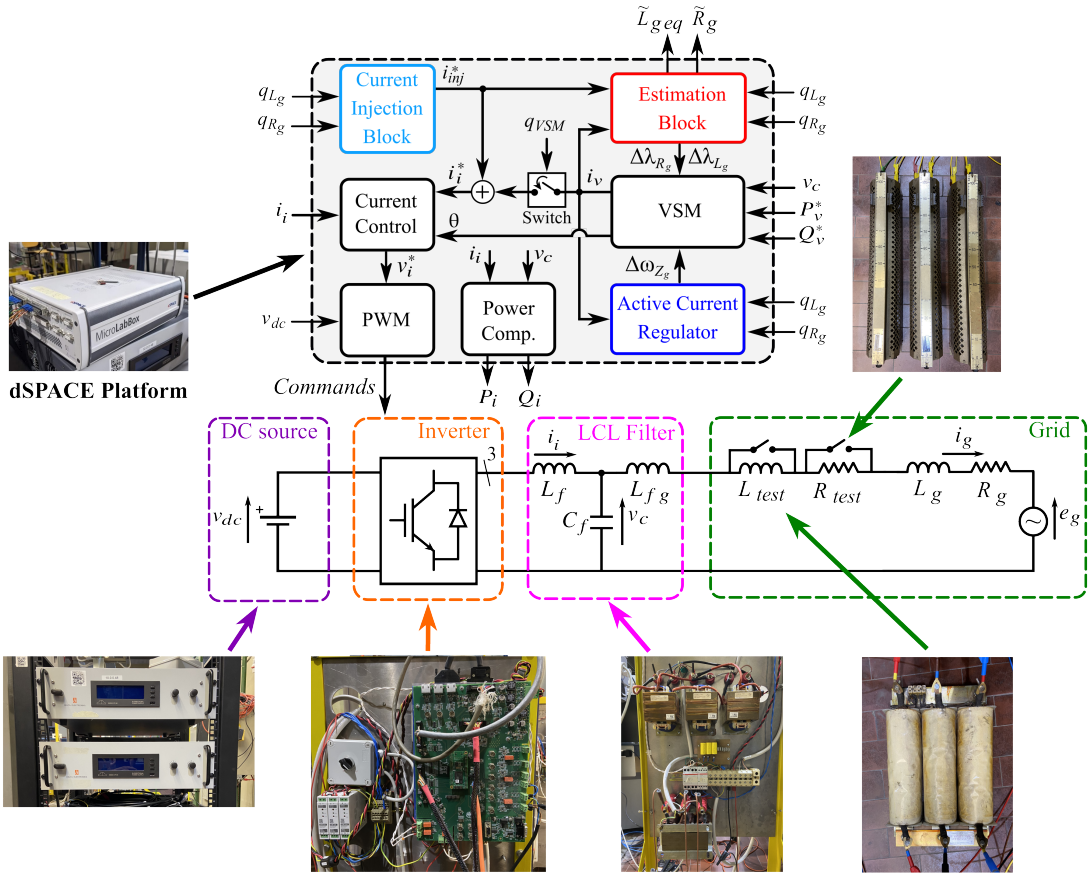


Fig. 4.8 Scheme and pictures of the hardware setup used for the experimental Tests 1-8 [75].

4.10 Experimental Validation: Accuracy of the Method

The system configuration employed for the experimental tests is shown in Fig. 4.8. The grid-tied converter is a 15 kVA, two-level, three-phase inverter, controlled via a dSPACE MicroLabBox platform with switching and sampling frequencies of 10 kHz. The inverter DC-link is powered by a constant voltage source.

The proposed estimation method has been implemented into the S-VSC [46] in its VSG configuration (Fig. 3.7), where the excitation control consists of a purely integral regulator. Instead, the lead-lag damping solution proposed in [53] is embedded within the mechanical emulator. The VSM electrical inductive and resistive parameters are set to $L_v = 0.3$ pu and $R_v = 0.1$ pu.

The VSM-controlled inverter is interfaced with a 50 Hz, 400 V_{rms} low-voltage grid via an LCL filter, featuring $L_f = 2$ mH, $C_f = 5$ µF, and $L_{fg} = 4.1$ mH. In addition, a 1.2 mH

Table 4.1 Main data of the experimental setup for Tests 1-8 [75].

Base Values		**Inverter**		**VSM**		**LCL Filter & Grid**	
S_b	15 kVA	S_n	15 kVA	L_v	0.3 pu	L_f	0.059 pu
V_b	400 V_{rms}	I_n	31 A	R_v	0.1 pu	$L_{f\,g}$	0.121 pu
f_b	50 Hz	V_{dc}	650 V	H	0.5 s	C_f	0.017 pu
Z_b	10.7 Ω	f_{sw}	10 kHz	ζ	0.7	L_{test}	0.035 pu
L_b	34.0 mH	f_s	10 kHz	τ_{est}	10-100 ms	R_{test}	0.023 pu
C_b	0.3 mF						

inductor L_{test} and a 250 mΩ resistor R_{test} can be inserted in series with the LCL filter to manually vary the grid equivalent inductance $L_{g\ eq}$ and resistance R_g. Table 4.1 lists all the key system parameters.

Several tests are carried out to experimentally verify the performance of the proposed grid impedance estimator:

- **Tests 1–3:** The grid impedance estimation is assessed with the VSM operating under various high-power conditions. In all three tests, the estimation is performed while the VSM delivers the same apparent power $S_i \simeq 0.7$ pu, but with different distributions between active P_i and reactive Q_i power. Specifically, in Test 1, the VSM provides only active power, $P_i = P_v^* = 0.7$ pu; in Test 2, it supplies only reactive power, $Q_i = Q_v^* = 0.7$ pu; in Test 3, it delivers both active and reactive power, with $P_i = P_v^* = 0.5$ pu and $Q_i = Q_v^* = 0.5$ pu;

- **Tests 4–5:** The impact of the estimator integral gain k_{est} on both the duration of the estimation process and the method noise rejection capability is examined, considering grid inductance estimation in Test 4 and grid resistance estimation in Test 5;

- **Tests 6–7:** The impedance estimation is performed while an external inductor L_{test} (Test 6) or resistor R_{test} (Test 7) is inserted in series with the LCL filter, thus modifying the grid impedance;

- **Test 8:** The impedance estimation is carried out at system startup, while the VSM output command remains disabled. Specifically, the VSM is already tracking the grid frequency and providing the position θ to the inverter current controller, but i_v

has not yet been applied as the inverter current reference i_i^*, as the VSM enabling signal q_{VSM} is kept low (Fig. 4.8).

For this set of tests, the impedance estimation is triggered manually by the external user, while the estimation evaluation algorithm (Fig. 4.7) remains disabled. For each experimental test, the estimation of the grid parameters using the proposed VSM-based algorithm is preceded by a non-characteristic harmonic current injection of 0.2 pu at 75 Hz, as proposed in [85]. The grid voltage and current signals acquired by the dSPACE controller during grid excitation are recorded and subsequently processed offline in MATLAB using the Fast Fourier Transform (FFT). This procedure yields a precise measurement of the complex grid impedance at 75 Hz, allowing the resistive and inductive components to be accurately determined. These experimentally obtained values serve as a benchmark for validating the results of the proposed estimation method. During the 75 Hz current injection, the inverter current reference i_i^* is held constant, while the VSM output signal i_v is deactivated by lowering q_{VSM} (Fig. 4.8). This prevents the VSM from counteracting the disturbance and ensures an accurate measurement of the grid impedance. All test results are summarized in Table 4.2, which reports both the expected and the estimated values of $L_{g\ eq}$ and R_g. The data reported for each experimental test consist of real-time samples acquired by the dSPACE platform.

4.10.1 Estimation during VSM High-Power Operation

The grid inductance and resistance are estimated while the VSM delivers $P_i = P_v^* = 0.7$ pu in Test 1 (Fig. 4.9), $Q_i = Q_v^* = 0.7$ pu in Test 2 (Fig. 4.10) and $P_i = P_v^* = 0.5$ pu with $Q_i = Q_v^* = 0.5$ pu in Test 3 (Fig. 4.11). For all tests, the estimation integral gain k_{est} is set to achieve a desired time constant $\tau_{est} = 50$ ms, neglecting the terms $\tilde{L}_{g\ eq}$ and $\tan\tilde{\delta}$ in (4.22). The estimation procedure is initiated at $t = 0.5$ s, when the raw inductance computation L_g' (highlighted in light blue) is activated by setting $q_{L_g} = 1$ and applying $i_{inj,d}^* = -0.1$ pu. Concurrently, the VSM excitation control and the mechanical emulator are disabled, while the active current regulator suppresses $\Delta i_{v,q}$ by adjusting ω and the integral estimator provides the additional excitation flux $\Delta\lambda_{L_g} = \lambda_e - \lambda_e^0$ required to counteract the $\Delta i_{v,d}$ deviation induced by the $i_{inj,d}$ injection. Then, at $t = 1.25$ s, the L_g' estimation phase is disabled ($q_{L_g} = 0$) and $i_{inj,d}$ injection is removed. Simultaneously, the raw resistance estimation R_g' (highlighted in pale orange) is initiated by setting $q_{R_g} = 1$, thus injecting $i_{inj,q} = i_{inj,q}^* = -0.1$ pu. Therefore, both the active current regulator and the integral

Table 4.2 Experimental results of grid parameters estimation [75].

Test n°	Notes	$\mathbf{L_{g\,eq}}$[1] [pu]	$\tilde{\mathbf{L}}_{\mathbf{g\,eq}}$ [pu]	$\mathbf{R_g}$[1] [pu]	$\tilde{\mathbf{R}}_{\mathbf{g}}$ [pu]
1	$i^*_{inj,d} = i^*_{inj,q} = -0.1$ pu, $P^*_v = 0.7$ pu, $Q^*_v = 0$ pu	0.143	0.142	0.040	0.035
2	$i^*_{inj,d} = i^*_{inj,q} = -0.1$ pu, $P^*_v = 0$ pu, $Q^*_v = 0.7$ pu	0.143	0.141	0.031	0.028
3	$i^*_{inj,d} = i^*_{inj,q} = -0.1$ pu, $P^*_v = Q^*_v = 0.5$ pu	0.141	0.141	0.036	0.031
4	$i^*_{inj,d} = -0.1$ pu, $P^*_v = Q^*_v = 0$ pu				
	- $\tau_{est} = 10$ ms	0.152	0.145		
	- $\tau_{est} = 50$ ms	-	0.146		
	- $\tau_{est} = 100$ ms	-	0.149		
5	$i^*_{inj,q} = -0.1$ pu, $P^*_v = Q^*_v = 0$ pu				
	- $\tau_{est} = 10$ ms			0.035	0.032
	- $\tau_{est} = 50$ ms			-	0.032
	- $\tau_{est} = 100$ ms			-	0.033
6	$i^*_{inj,d} = -0.1$ pu, $P^*_v = Q^*_v = 0$ pu, $\Delta L_{g\,eq}$ comp.	0.035	0.033		
7	$i^*_{inj,q} = -0.1$ pu, $P^*_v = Q^*_v = 0$ pu, ΔR_g comp.			0.023	0.025
8	$i^*_{inj,d} = i^*_{inj,q} = 0.1$ pu, $q_{VSM} = 0$ (VSM disabled)	0.150	0.145	0.029	0.029

[1] $L_{g\,eq}$-R_g are computed through the benchmark method in Tests 1-5 and 8. Instead, they are obtained from the nameplates of the external inductor L_{test} and the resistor R_{test} in Tests 6-7.

estimator remain active, ensuring the cancellation of $\Delta i_{v,d}$–$\Delta i_{v,q}$. In particular, the integral estimator provides $\Delta\lambda_{R_g} = \lambda_e - \lambda_e^0$ to compensate for the $\Delta i_{v,d}$ deviation induced by the $i_{inj,q}$ injection. Finally, at $t = 2$ s, the R'_g estimation phase is concluded ($q_{R_g} = 0$) and the injection of $i^*_{inj,q}$ is halted. Immediately afterward, the data compensator refines the preliminary values $\tilde{L}'_g$ and $\tilde{R}'_g$ to correct for the error introduced by the load angle variations during the estimation process. Through this compensation step, the final and reliable estimates of the grid inductance $\tilde{L}_{g\ eq}$ and resistance $\tilde{R}_g$ are obtained.

The proposed method allows the estimation of both grid inductance and resistance within a total duration of 1.5 s. Each raw parameter is computed over a 0.75 s interval, with the overall procedure time selected according to the chosen value of τ_{est}. The difference between $\tilde{L}'_g$–$\tilde{L}_{g\ eq}$ and $\tilde{R}'_g$–$\tilde{R}_g$ increases as the load angle δ deviates, in accordance with (4.8)–(4.9). In Test 1 (Fig. 4.9), $\delta = 17.6°$ with inductive estimates of $\tilde{L}'_g = 0.153$ pu and $\tilde{L}_{g\ eq} = 0.143$ pu, while the resistive estimated values are $\tilde{R}'_g = -0.009$ pu and $\tilde{R}_g = 0.035$ pu, with $\tilde{R}'_g$ even taking a negative value. Therefore, the data compensator implementation is necessary to achieve accurate estimation. The gap between raw and refined grid parameters becomes smaller in Test 3 (Fig. 4.11), where $\delta = 7.4°$. In this case, $\tilde{L}'_g = 0.145$ pu and $\tilde{L}_{g\ eq} = 0.141$ pu, whereas $\tilde{R}'_g = 0.012$ pu and $\tilde{R}_g = 0.031$ pu. Conversely, in Test 2 (Fig. 4.10), with $\delta = -4.2°$, the inductive values nearly coincide ($\tilde{L}'_g = 0.139$ pu and $\tilde{L}_{g\ eq} = 0.141$ pu, while the discrepancy between $\tilde{R}_g$–$\tilde{R}'_g$ further reduces ($\tilde{R}'_g = 0.038$ pu and $\tilde{R}_g = 0.028$ pu). In this latter case, the data compensator refinement is thus not strictly required.

The absolute estimation errors are contained for both grid inductance and resistance. In contrast, the relative errors for the grid resistance are significant, with ϵ_{R_g} equal to −12.5 % in Test 1, −9.7 % in Test 2 and −13.9 % in Test 3. In contrast, the grid inductance estimation shows minimal relative errors, with ϵ_{L_g} equal to −0.7 pu in Test 1, −1.4 % in Test 2 and +0.1 % in Test 3. As demonstrated in the previous sections of this chapter, the estimation errors induced by grid voltage variations (4.27) or frequency deviations (4.29) affect the absolute values of both L'_g and R'_g equally. Therefore, these errors propagate to the refined estimates $\tilde{L}_{g\ eq}$ and $\tilde{R}_g$, having a more pronounced impact on the relative error for smaller parameters, such as the grid resistance R_g of the grid used in these tests.

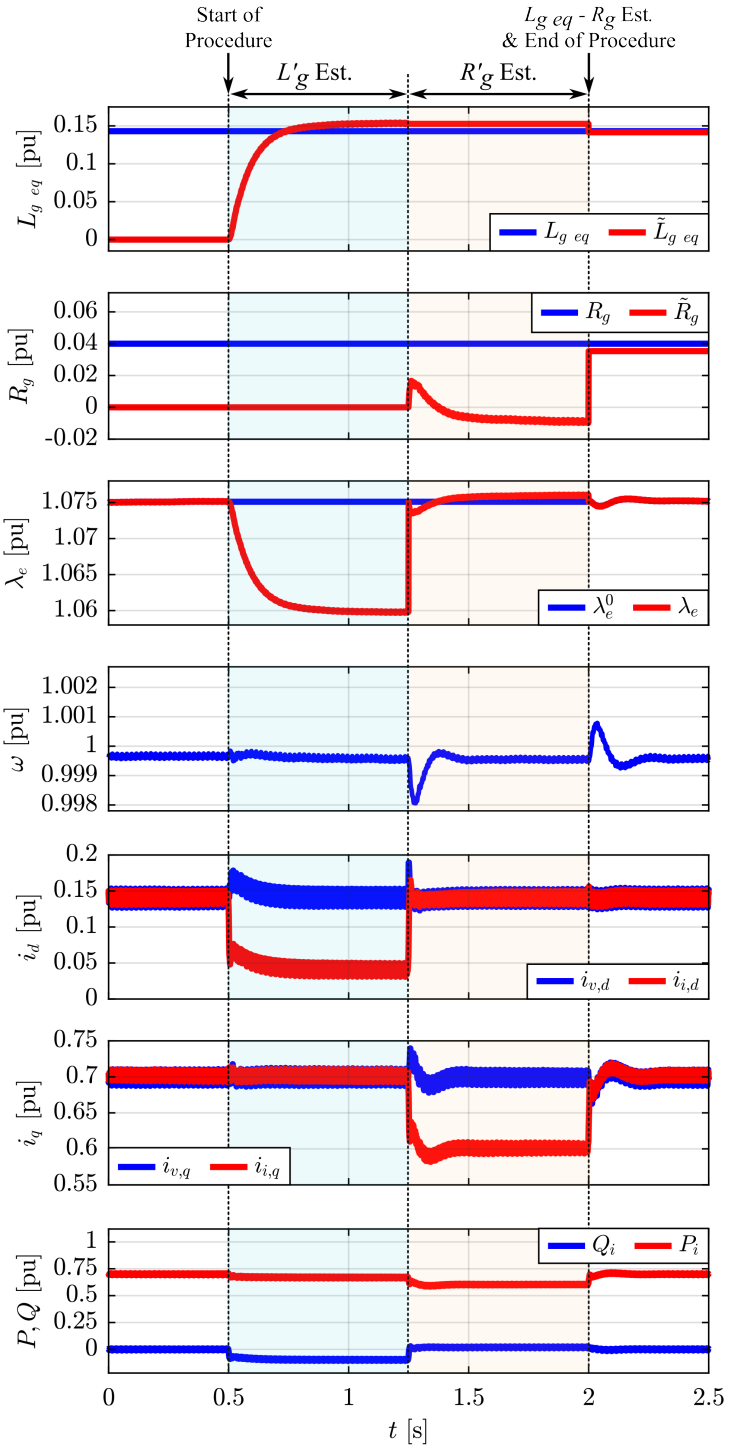


Fig. 4.9 Results of Test 1. From top to bottom: measured and estimated grid inductance $L_{g\ eq}$–$\tilde{L}_{g\ eq}$ and resistance R_g–$\tilde{R}_g$; excitation flux λ_e^0 and resulting λ_e; virtual rotor speed ω; dq-axes virtual and inverter currents $i_{v,d}$–$i_{i,d}$ and $i_{v,q}$–$i_{i,q}$; inverter output powers P_i–Q_i [75].

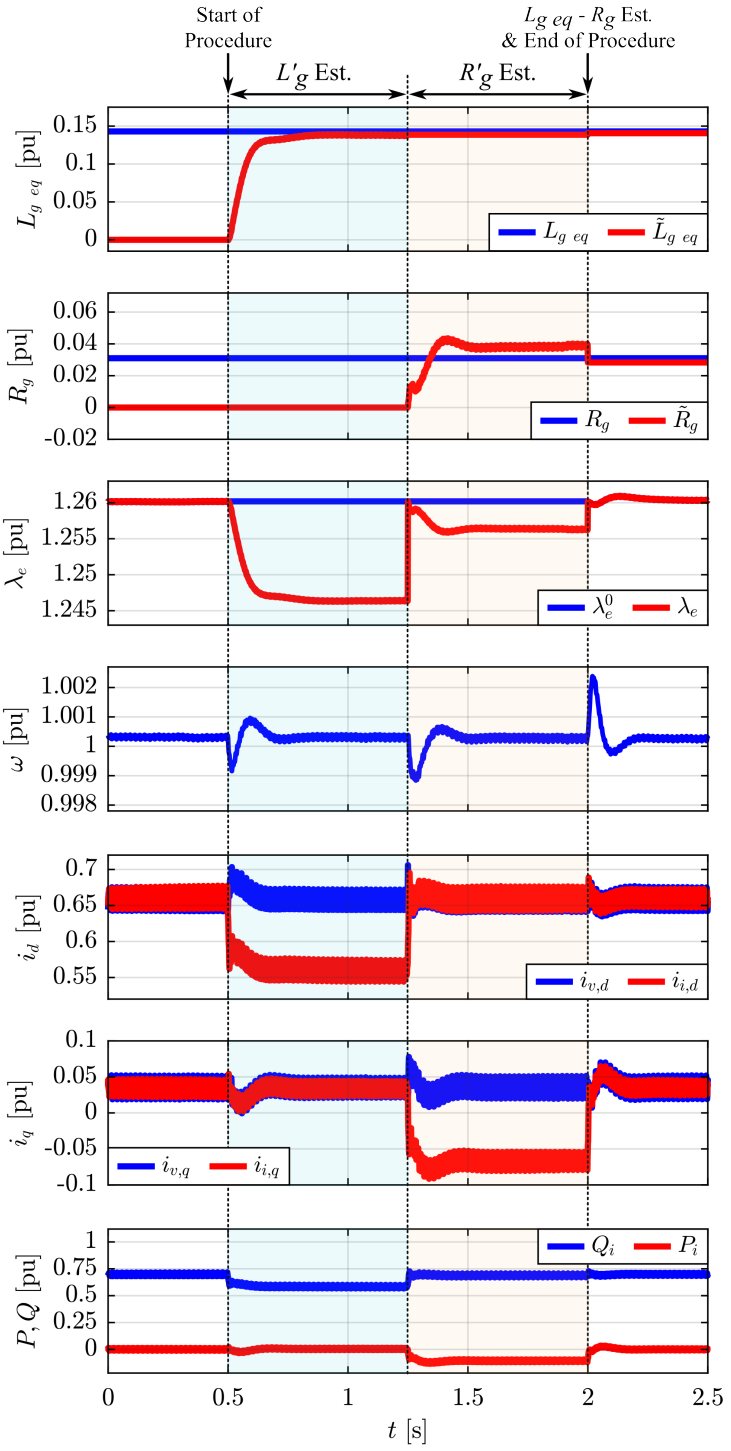


Fig. 4.10 Results of Test 2. From top to bottom: measured and estimated grid inductance $L_{g\ eq}$–$\tilde{L}_{g\ eq}$ and resistance R_g–$\tilde{R}_g$; excitation flux λ_e^0 and resulting λ_e; virtual rotor speed ω; dq-axes virtual and inverter currents $i_{v,d}$–$i_{i,d}$ and $i_{v,q}$–$i_{i,q}$; inverter output powers P_i–Q_i [75].

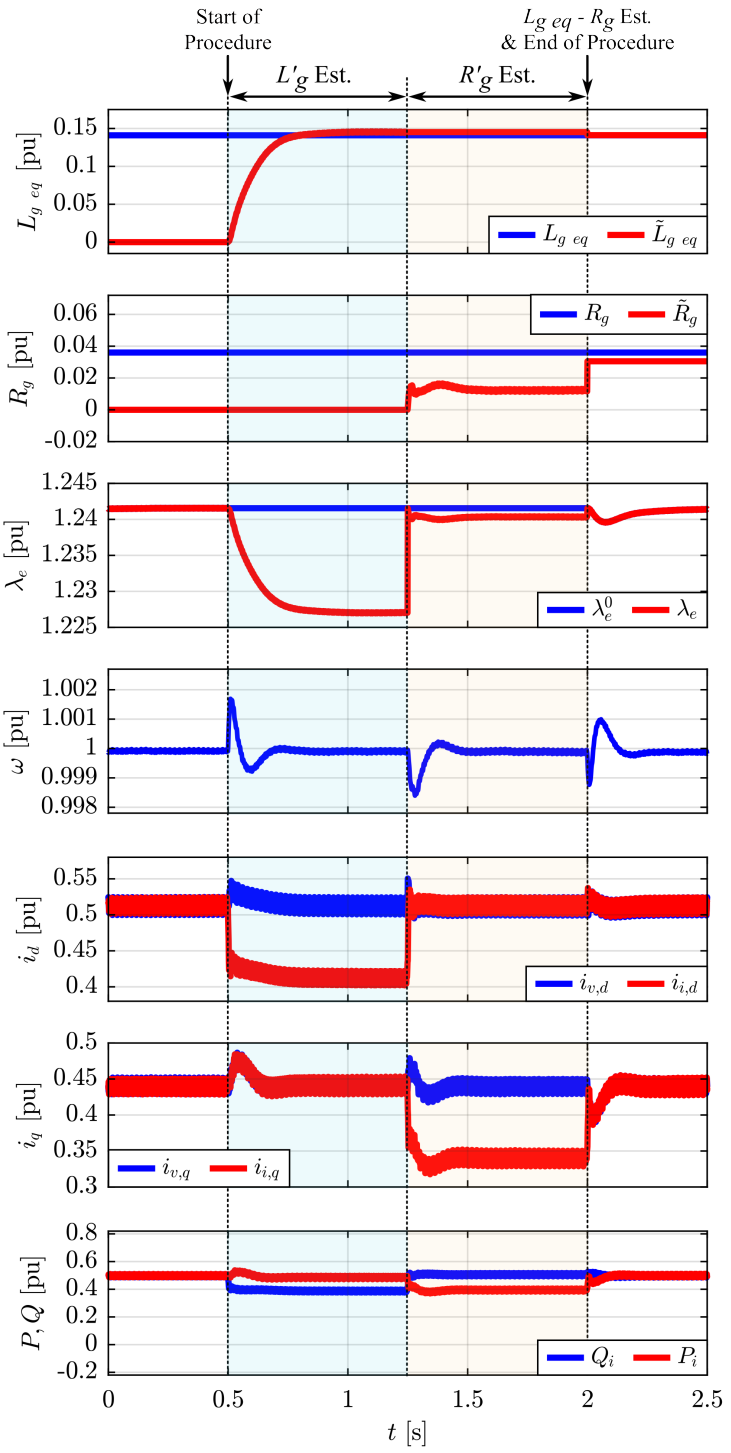


Fig. 4.11 Results of Test 3. From top to bottom: measured and estimated grid inductance $L_{g\,eq}$–$\tilde{L}_{g\,eq}$ and resistance R_g–$\tilde{R}_g$; excitation flux λ_e^0 and resulting λ_e; virtual rotor speed ω; dq-axes virtual and inverter currents $i_{v,d}$–$i_{i,d}$ and $i_{v,q}$–$i_{i,q}$; inverter output powers P_i–Q_i [75].

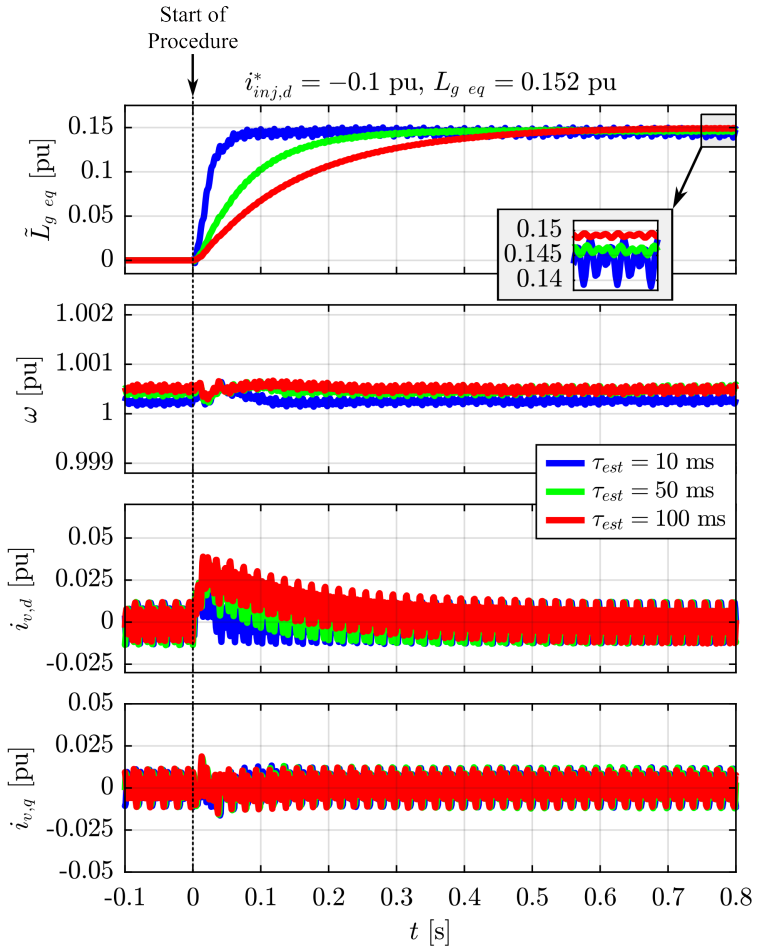


Fig. 4.12 Results of Test 4: grid inductance estimation for different values of estimation time constant τ_{est}. $i_{inj,d} = -0.1$ pu is injected, while the VSM is operating at null power. From top to bottom: estimated grid inductance $\tilde{L}_{g\ eq}$, virtual rotor speed ω, virtual currents $i_{v,d}$ and $i_{v,q}$ [75].

4.10.2 Estimation Duration and Noise Rejection

In Test 4 (Fig. 4.12) and Test 5 (Fig. 4.13), the grid inductance and resistance are respectively estimated by injecting $i_{inj,d} = -0.1$ pu and $i_{inj,q} = -0.1$ pu, while the VSM provides zero power ($P^*_v = Q^*_v = 0$ pu). The estimation procedure is repeated for different values of τ_{est} to evaluate the impact of the integral gain k_{est} on both the estimation duration and the estimator filtering performance. During VSM operation at zero power, $\delta = 0°$ and the raw values satisfy $L'_g \simeq L_{g\ eq}$ and $R'_g \simeq R_g$. Consequently, $L_{g\ eq}$ and R_g can be directly obtained from the integral estimator using (4.12)–(4.13), without requiring any data correction from the data compensator. A peak-to-peak ripple of approximately 0.025 pu is present on both $i_{v,d}$ and $i_{v,q}$. This current ripple originates from measurement noise on v_c, which

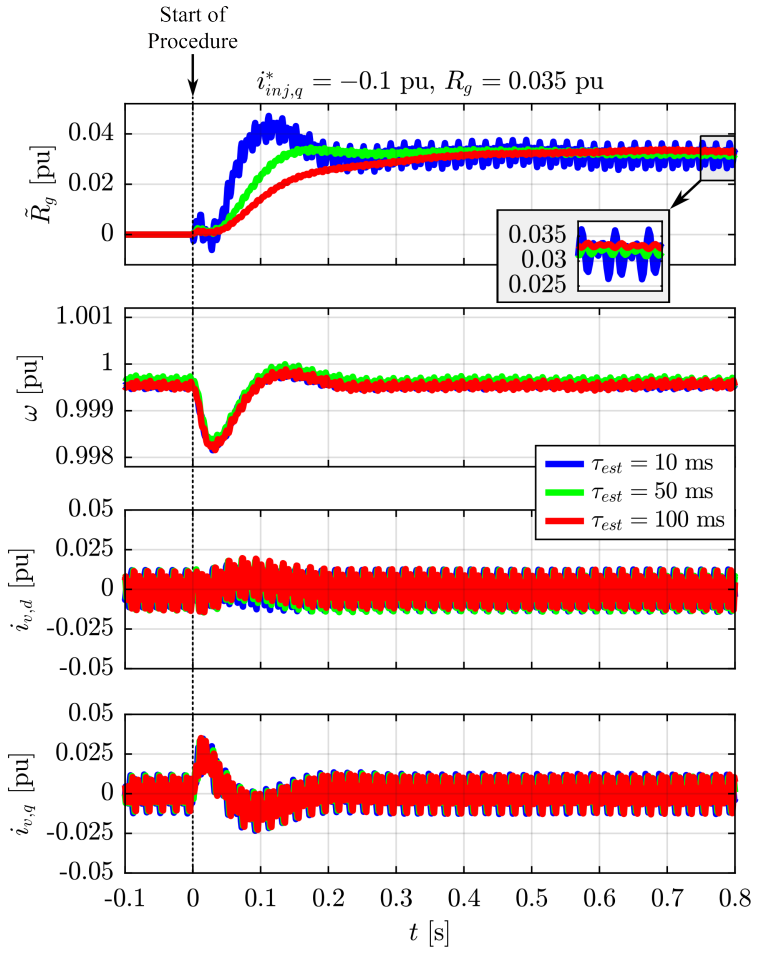


Fig. 4.13 Results of Test 5: grid resistance estimation for different values of estimation time constant τ_{est}. $i_{inj,q} = -0.1$ pu is injected, while the VSM is operating at null power. From top to bottom: estimated grid resistance $\tilde{R}_g$, virtual rotor speed ω, virtual currents $i_{v,d}$ and $i_{v,q}$ [75].

propagates through the VSM electrical model (Fig. 4.1) and affects the computed virtual currents.

The integral gain k_{est} is set according to the desired τ_{est}, neglecting the terms $\tilde{L}_{g\ eq}$ and $\tan\tilde{\delta}$ in (4.22). Consequently, from (4.23), the real estimation time constant $\tau_{est,real}$ exceeds the target τ_{est} by a factor of $\frac{L_v+L_{g\ eq}}{L_v} = 1.51$. The expected theoretical curves of estimated grid inductance and resistance during estimation process can be expressed as follows:

$$\tilde{L}_{g\ eq\ th} = L_{g\ eq} \cdot (1 - e^{-\frac{t}{\tau_{est,real}}}) \tag{4.31}$$

$$\tilde{R}_{g\ th} = R_g \cdot (1 - e^{-\frac{t}{\tau_{est,real}}}) \tag{4.32}$$

As shown in Fig. 4.12, the $\tilde{L}_{g\ eq}$ curves closely follow the pure exponential trend predicted by (4.31). In contrast, the $\tilde{R}_g$ curves in Fig. 4.13 deviate from the theoretical behavior of (4.32), displaying superimposed fluctuations caused by $\Delta i_{v,q}$ and $\Delta\omega$ variations during the estimation process. Indeed, the injection of $i_{inj,q}$ induces a sudden variation in the load angle δ, causing oscillations in $\Delta\omega$ and $\Delta i_{v,q}$, which are subsequently damped by the active current regulator. Both the transient $\Delta i_{v,q}$ and $\Delta\omega$ fluctuations influence $\Delta\lambda_{R_g} = \Delta\lambda_e$ according to (4.6), thus consequently propagating into the computation of R_g. Therefore, the response of the active current regulator can affect the overall duration of the estimation procedure. As τ_{est} decreases (i.e., with increasing k_{est}), the R_g estimation becomes more sensitive to fluctuations in $\Delta i_{v,q}$ and $\Delta\omega$.

The integral estimator, behaving as a low-pass filter, inherently attenuates noise on $i_{v,d}$, yielding filtered estimation results. Its cut-off frequency $f_{cut-off\ est}$ is determined by $\tau_{est,real}$ according to (4.24) and can be adjusted through the tuning of k_{est}. In Tests 4–5, setting $\tau_{est} = 10$ ms yields a cut-off frequency of $f_{cut-off\ est} = 11$ Hz, resulting in a 0.01 pu ripple on both $\tilde{L}_{g\ eq}$ and $\tilde{R}_g$. Increasing τ_{est} to 50 ms lowers $f_{cut-off\ est}$ to 2 Hz, reducing the ripple to 0.002 pu. Further increasing τ_{est} to 100 ms provides marginal additional improvement, with $f_{cut-off\ est} = 1$ Hz and ripple decreasing to 0.001 pu on both estimated parameters.

4.10.3 Estimation with Grid Impedance Variation

The proposed estimation method is validated by inserting an external inductor L_{test} (Test 6) or resistor R_{test} (Test 7) in series with the LCL filter during the estimation process. The estimation time constant is set to $\tau_{est} = 50$ ms, following the same assumptions as in the previous tests. Since the VSM operates at zero power during estimation, $L_{g\ eq}$ and R_g can be directly computed by the integral estimator, as described in (4.12)–(4.13).

The $L_{g\ eq}$ estimation during the insertion of L_{test} is shown in Fig. 4.14. The inductance estimation is initially enabled at $t < 0$ s by setting $q_{L_g} = 1$ and $i^*_{inj,d} = -0.1$ pu, providing the first computed value. At $t = 1$ s, $L_{test} = 0.035$ pu is inserted and with the integral estimator still active, the updated value of inductance is immediately computed. The resulting variation in grid inductance $\Delta\tilde{L}_{g\ eq} = 0.033$ pu is accurately calculated.

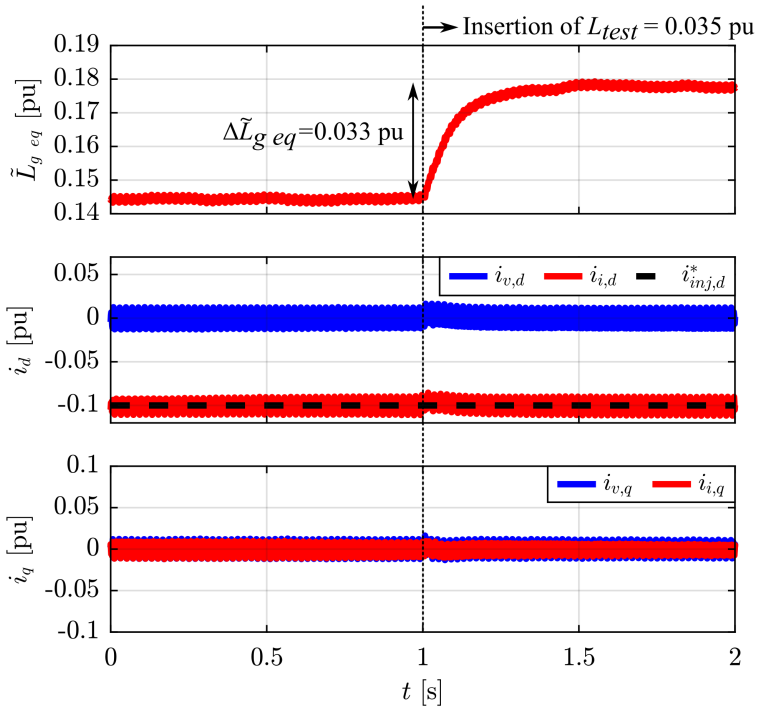


Fig. 4.14 Results of Test 6: grid inductance estimation while an external inductor L_{test} is inserted in series with the LCL filter and the VSM is providing null power. From top to bottom: estimated grid inductance $\tilde{L}_{g\ eq}$; d-axis virtual current $i_{v,d}$, inverter output current $i_{i,d}$ and injected current reference $i^*_{inj,d}$; q-axis virtual current $i_{v,q}$ and inverter output current $i_{i,q}$ [75].

A similar procedure is performed for grid resistance. The estimation of R_g is carried out while R_{test} is inserted, as shown in Fig. 4.15. An initial resistance estimation is obtained at $t < 0$ s by setting $q_{R_g} = 1$ and $i^*_{inj,q} = -0.1$ pu. At $t = 1$ s, the additional resistor $R_{test} = 0.023$ pu is inserted and the resulting grid resistance change $\Delta\tilde{R}_g = 0.025$ pu is accurately computed by the estimator.

4.10.4 Estimation at VSM Startup

In Test 8 (Fig. 4.16), the grid impedance estimation is performed at system startup, with the VSM only tracking the grid frequency and providing the position θ, while the virtual current i_v is not applied as the inverter current reference i^*_i (i.e., $q_{VSM} = 0$ in Fig. 4.8). At startup, the power converter is not delivering power. Therefore, the integral estimator can directly compute $L_{g\ eq}$ and R_g according to (4.12)–(4.13), rendering data refinement via the data compensator unnecessary. The proposed algorithm sequentially estimates the grid

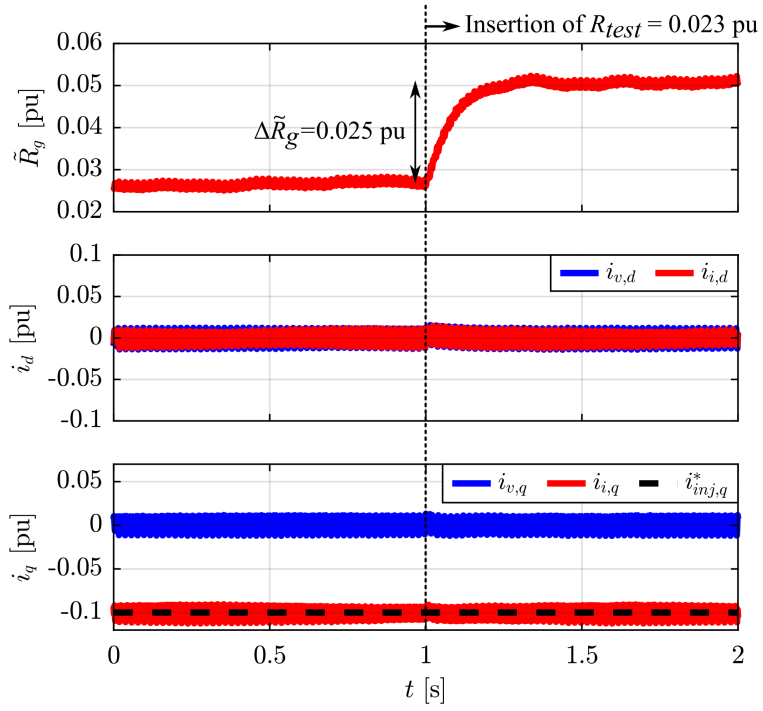


Fig. 4.15 Results of Test 7: grid resistance estimation while an external resistor R_{test} is inserted in series with the LCL filter and the VSM is providing null power. From top to bottom: estimated grid resistance $\tilde{R}_g$; d-axis virtual current $i_{v,d}$ and inverter output current $i_{i,d}$; q-axis virtual current $i_{v,q}$, inverter output current $i_{i,q}$ and injected current reference $i^*_{inj,q}$ [75].

inductance (light blue highlighted) and resistance (pale orange highlighted) with τ_{est} = 50 ms, following the procedure applied in Tests 1–3. The references $i^*_{inj,d}$ and $i^*_{inj,q}$ are set to +0.1 pu to validate the estimator also in the event of positive current injection into the grid through the current injection block. Since i_v is not used to compute the inverter current references, $i^*_i = i^*_{inj}$ during the estimation process and both the inverter output currents $i_{i,d}$ and $i_{i,q}$ accurately track the step variations of $i^*_{inj,d}$ and $i^*_{inj,q}$. Similar to Test 4, the $\tilde{L}_{g\ eq}$ curve follows an exponential trajectory. Likewise, as in Test 5, the $\tilde{R}_g$ curve shows oscillations superimposed on an exponential trend. Since $i_{v,q}$ is calculated but not injected into the grid ($q_{VSM} = 0$), these fluctuations are entirely due to $\Delta\omega$ deviations.

The results of Test 8 demonstrate that the proposed method can accurately estimate both grid inductance ($\epsilon_{L_g} = -3.3$ %) and resistance ($\epsilon_{R_g} = -1.4$ %), even when the VSM is solely used to track the grid position without controlling the inverter current. This functionality enables the safe tuning of the VSM functional blocks [43], [52], [53], [55], [57] even before the VSM is actively controlling the inverter, thus delivering power.

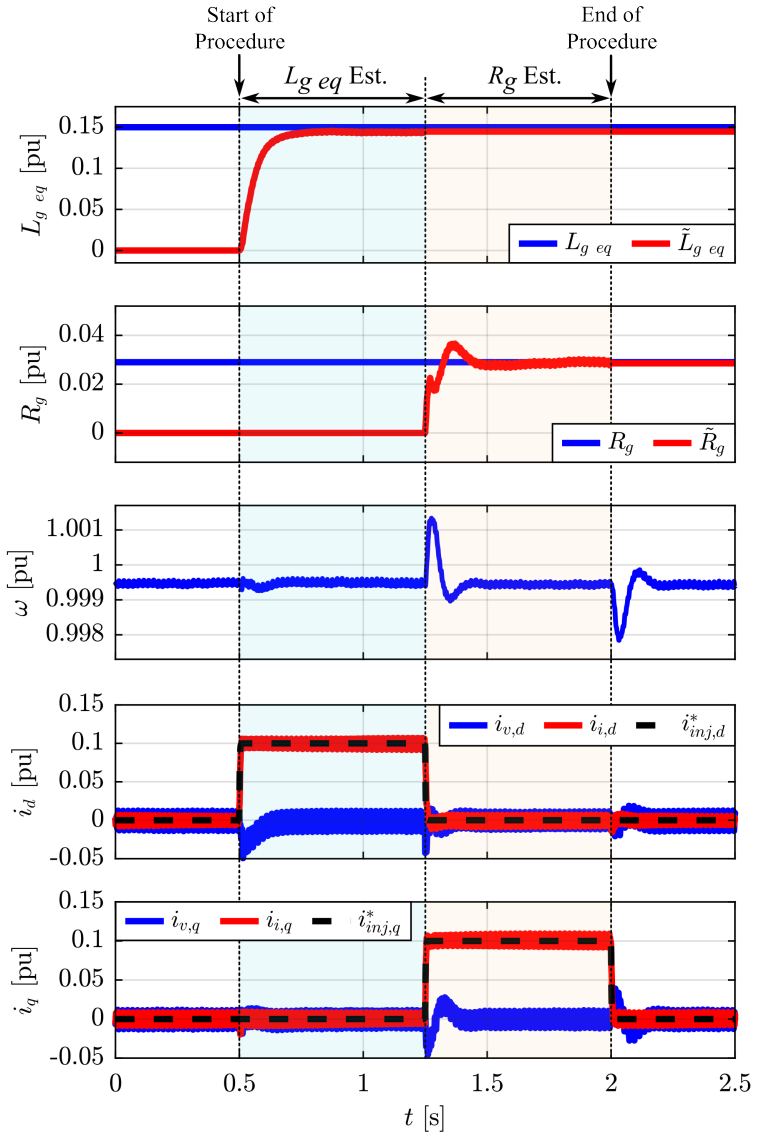


Fig. 4.16 Results of Test 8: grid inductance and resistance estimation when the VSM output command is disabled ($q_{VSM} = 0$), i.e., the VSM current i_v is not used as inverter current reference i_i^*. From top to bottom: measured $L_{g\ eq}$ and estimated $\tilde{L}_{g\ eq}$ grid inductance; measured R_g and estimated $\tilde{R}_g$ resistance; virtual rotor speed ω; d-axis virtual current $i_{v,d}$, inverter output current $i_{i,d}$ and injected current reference $i^*_{inj,d}$; q-axis virtual current $i_{v,q}$, inverter output current $i_{i,q}$ and injected current reference $i^*_{inj,q}$ [75].

4.11 Experimental Validation: Islanding Detection

The system configuration employed for the experimental tests is depicted in Fig. 4.17. A three-level neutral point clamped (NPC) 8 kVA VSM-driven inverter for applications in

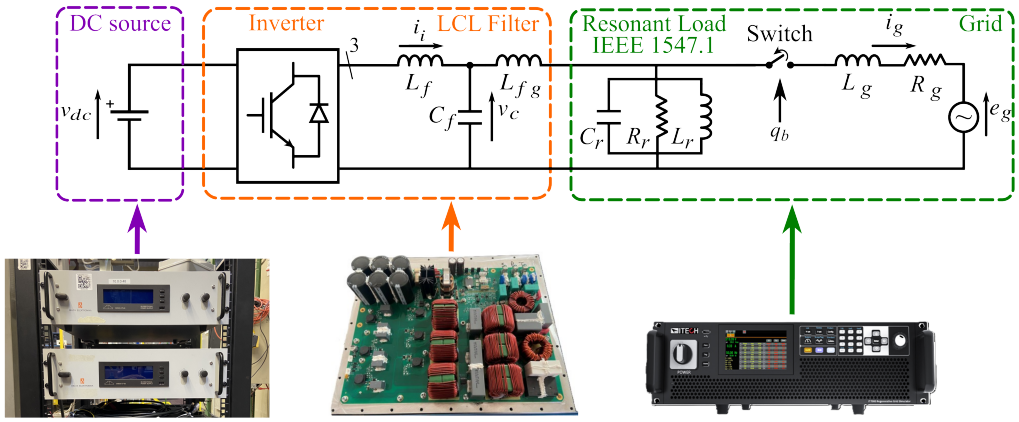


Fig. 4.17 Scheme and pictures of the hardware setup used for the experimental tests of unintentional islanding detection according to [112].

battery energy storage systems [21] is equipped with the proposed grid impedance estimator and the estimation evaluation algorithm (Fig. 4.7) to automate the estimation procedure, thus rapidly detecting significant grid impedance variations in the event of unintentional islanding. The inverter control system is based on an STM32G474 microcontroller and it operates with a switching frequency of 72 kHz and a sampling frequency of 18 kHz. The inverter DC-link is powered by a constant voltage source that emulates the behavior of the battery pack.

The implemented VSM model is the S-VSC [46], configured in its VSC mode (Fig. 3.8) and tuned according to the same parameter settings used in Tests 1–8, while the estimator time constant is set to $\tau_{est} = 5$ ms to accelerate the estimation process and the injected current references are $\Delta i^*_{inj,d} = \Delta i^*_{inj,q} = -0.05$ pu. An error evaluation threshold $\Gamma_{th} = 0.08$ pu is set for the estimation evaluation algorithm.

The VSM-driven inverter is connected to an ITECH 21 kVA regenerative grid simulator, able to emulate a 50 Hz, 400 V_{rms} grid with an RLC load connected in parallel. The inverter is interfaced to the grid emulator through an LCL filter with $L_f = L_{fg} = 250$ µH and $C_f = 6.8$ µF. The resonant load is tuned according to the IEEE unintentional islanding test specifications [112]: the resistance R_r is set to absorb the nominal active power of 8 kW (i.e., $R_r = 1$ pu), while the inductance L_r and the capacitance C_r exchange a reactive power of 8 kVar (i.e., $X_{L_r} = L_r = 1$ pu and $X_{C_r} = -1/C_r = -1$ pu), with an equivalent null load reactance as seen from the inverter. The inverter and the RLC load can be disconnected from the emulated grid by opening a virtual switch controlled through the q_b signal. Table 4.3 summarizes the main parameters of the system.

Table 4.3 Main data of the experimental setup for anti-islanding test.

Base Values		**Inverter**		**VSM**		**LCL Filter**		**Resonant Load**	
S_b	8 kVA	S_n	8 kVA	L_v	0.3 pu	L_f	0.004 pu	R_r	1.0 pu
V_b	400 V_{rms}	I_n	16 A	R_v	0.1 pu	$L_{f\,g}$	0.004 pu	L_r	1.0 pu
f_b	50 Hz	V_{dc}	650 V	H	0.5 s	C_f	0.043 pu	C_r	1.0 pu
Z_b	20 Ω	f_{sw}	72 kHz	ζ	0.7				
L_b	63.7 mH	f_s	18 kHz	τ_{est}	5 ms				
C_b	0.16 mF			Γ_{th}	0.08 pu				

As shown in Fig. 4.18, the inverter and the resonant load are isolated from the grid by commanding the switch opening through q_b at $t = 0$ s, while the inverter is providing $P_i = 1$ pu and $Q_i = 0$ pu. The estimation process is triggered by the proposed estimation evaluation algorithm, which requires around 100 ms to detect a potential unintentional islanding condition. The grid impedance estimator is thus enabled and detects a grid impedance variation compatible with an unintentional islanding condition, mainly due to the large grid resistance variation to $R_g = R_r = 1$ pu, while the estimated grid inductance is negligible, consistently with the system configuration. The estimation procedure therefore ends at $t = 1.39$ s with the triggering of the anti-islanding protection. In this test, the full estimation procedure is executed solely to illustrate the algorithm. Nevertheless, the anti-islanding protection can be enabled immediately after estimating $\tilde{R}_g$, once its significant variation is detected, i.e., at approximately $t = 0.3$ s. Anyway, the detection of the unintentional islanding occurs within the 2 s time limit imposed by the standards [111].

4.12 Conclusion

The knowledge of the grid impedance is essential for the proper tuning of the VSM control, thus ensuring the reliable operation of VSM-driven grid-connected inverters. This chapter introduces a dedicated VSM-based closed-loop estimator that exploits the intrinsic dependence of the VSM dynamic response on the grid parameters to determine both the equivalent grid inductance and resistance.

The proposed estimator represents an add-on functionality that can be integrated into any VSM model. It is activated when an amount of current not processed by the VSM is

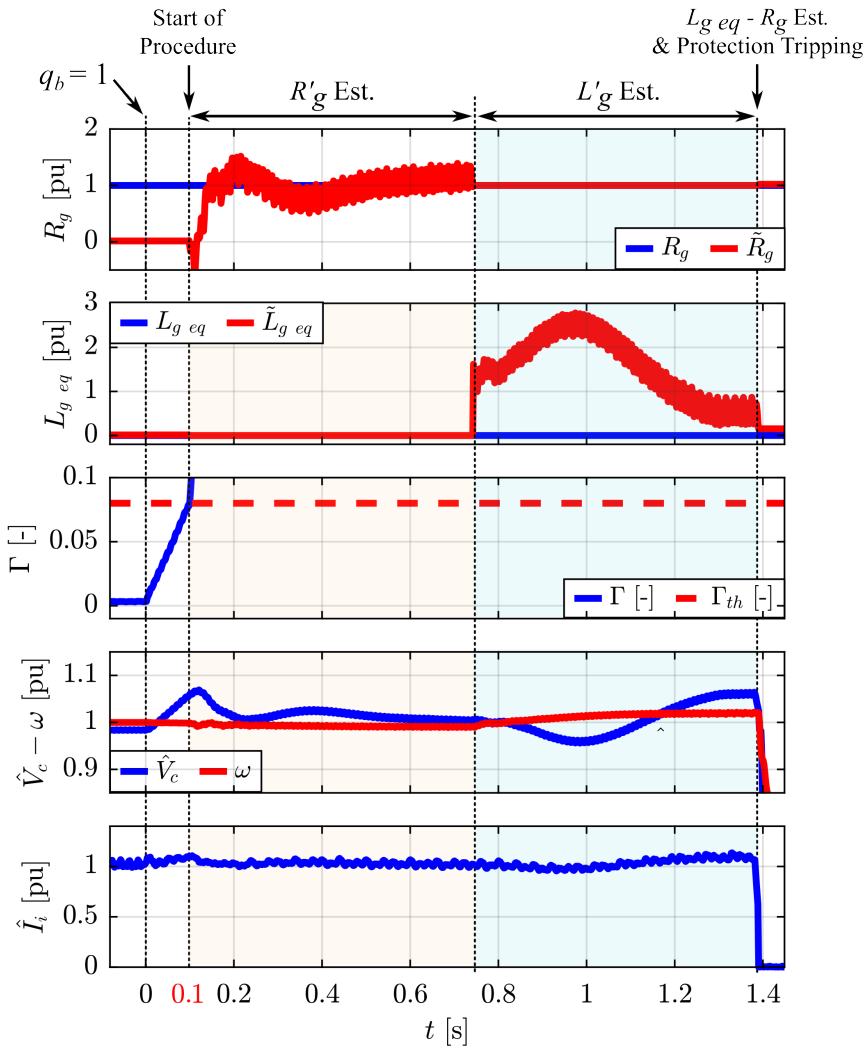


Fig. 4.18 Results of anti-islanding test: the grid resistance and inductance estimation is triggered by the proposed estimation evaluation algorithm. From top to bottom: real R_g and estimated $\tilde{R}_g$ grid resistance; real $L_{g,eq}$ and estimated $\tilde{L}_{g,eq}$ grid inductance; error variable Γ and its threshold Γ_{th}; measured grid peak voltage $\hat{V}_c$ and VSM speed ω; inverter peak output current $\hat{I}_i$.

directly injected into the grid via the lower-level inverter current controller. Only a small external current injection (±0.1 pu) is required to achieve accurate estimation results, while ensuring minimal perturbation of the power system during the estimation process.

The proposed method performs real-time grid parameter estimation using a basic integral estimator, eliminating the need for complex mathematical tools like Fourier Transform, Kalman filters, or RLS algorithms. At the end of the process, a simple algebraic adjustment compensates for the effects of load angle deviations on the estimated results.

Furthermore, the estimator intrinsically mitigates noise originating from voltage and current measurement disturbances, eliminating the need for advanced filtering techniques such as Kalman filters. This makes the proposed algorithm especially well-suited for field applications in disturbed environments. The estimator can be adjusted to achieve a desired response time and level of noise rejection, allowing the estimation duration to be shortened in less noisy conditions.

The estimation of grid inductance and resistance can be manually triggered by the user. Alternatively, the estimation procedure can be fully automated by implementing the estimation evaluation algorithm. This transforms the estimator into an event-driven solution, suitable for applications requiring rapid identification of grid impedance variations, such as the unintentional islanding detection.

The experimental results confirm that the proposed method provides accurate grid impedance estimation with effective noise filtering and fast dynamic response across different VSM operating conditions. Notably, accurate estimation is achieved even when the VSM is enabled and synchronized to the grid but its output commands are not used as inverter current references. This feature can be exploited during the startup phase to safely tune the VSM functional blocks. Nevertheless, the capability of the proposed algorithm to detect unintentional islanding conditions is also demonstrated.

Chapter 5

Active Power Filters in Industrial Environments

This chapter focuses on the following objectives:

- Illustration of the APF hardware architecture adopted in this thesis;
- Description of the APF control strategy implemented for the experimental tests presented in the following chapters;
- Presentation of the case study addressed in this thesis, i.e. the installation of APFs in end-of-line final functional testing systems of industrial power converters used in electric drive applications.

Accordingly, this chapter provides the background for the subsequent two chapters, which discuss the novel contributions of this thesis in the field of industrial APFs.

5.1 General Structure of the Hardware on Study

Among the various types of APFs, shunt-type APFs are the most widely industrialized [38]. They are connected in parallel with the distorted load, e.g., a diode or thyristor front-end rectifier, injecting compensating non-sinusoidal currents to ensure that the overall grid current remains sinusoidal and the system operates at unity power factor. Due to its extensive industrial deployment, this APF topology is adopted in this thesis.

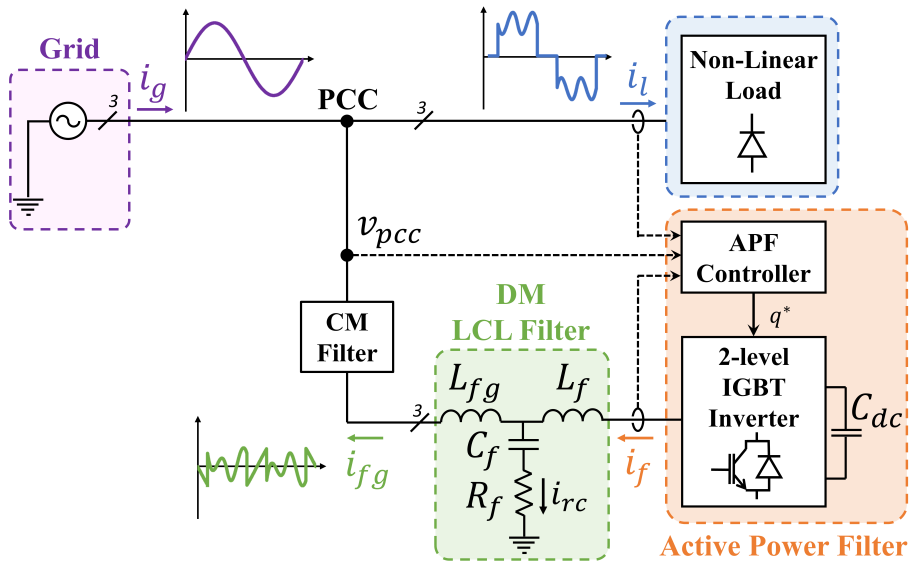


Fig. 5.1 Hardware block scheme for a shunt-type APF compensating for the distorted current injected by a non-linear load.

The reference hardware for the shunt-type APF operating in parallel to a non-linear load is depicted in Fig. 5.1. The APF consists of a grid-tied inverter with a floating DC-link, i.e., not supplied by any DC source. The inverter is connected to the PCC through two filtering stages:

- **Differential-mode (DM) LCL filter:** As in the other grid-connected inverter applications [39], DM LCL filter represents the conventional solution for interfacing APFs with the grid in applications rated above several kilowatts [113], [114], [115], [116]. Its function is to attenuate the current ripple produced by the inverter switching action, thus ensuring compliance with international harmonic distortion standards [13]. The DM LCL filter consists of an inverter-side inductor L_f, a filter capacitor C_f with in series a damping resistor R_f and a grid-side inductor L_{fg};
- **Common-mode (CM) filter:** It is in charge to limit the circulation of high-frequency CM currents [117], [118], [119] due to the presence of parasitic capacitances between the wires and the chassis of the converter and the ground. CM currents can cause grid current distortion, safety issues, increase of the system losses and electromagnetic interference with other equipment connected to the grid [120], [121], [122]. An in-depth analysis of this hardware component lies outside the scope of this thesis.

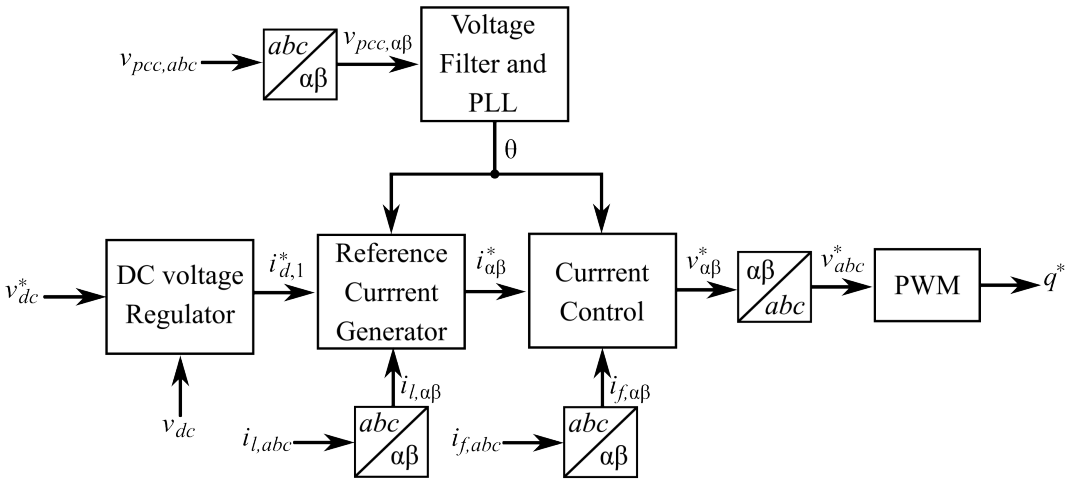


Fig. 5.2 Block diagram of the whole APF control system [123].

In the described system, i_g denotes the grid current, i_l the load current, v_{pcc} the grid phase voltage measured at the PCC, i_f the inverter output current flowing through L_f, i_{rc} the current in the RC branch and i_{fg} the APF current flowing through L_{fg} and injected at the PCC.

The APF controller determines the switching signals q^* to drive the inverter switches, thus compensating for the distorted and reactive components of the load current i_l.

5.2 Adopted Control Strategy

The adopted APF control method is the solution proposed in [123], whose overall block diagram is depicted in Fig. 5.2. The main blocks of the control are as follows:

- **Voltage Filter and PLL:** This block filters the measured PCC voltage in (α,β) reference frame $v_{pcc,\alpha\beta}$ through a sinusoidal signal integrator (SSI). The filtered outputs are then applied to a standard phase-locked loop (PLL) consisting of a proportional-integral (PI) regulator and an integrator. The PLL operates by locking the phase through nulling the voltage in the q-axis. It means that any current vector lying on the d-axis of the grid-synchronized (d,q) rotating reference frame corresponds to an active power exchange with the grid, whereas any current vector lying on the q-axis implies a reactive power exchange [124]. The grid position θ is

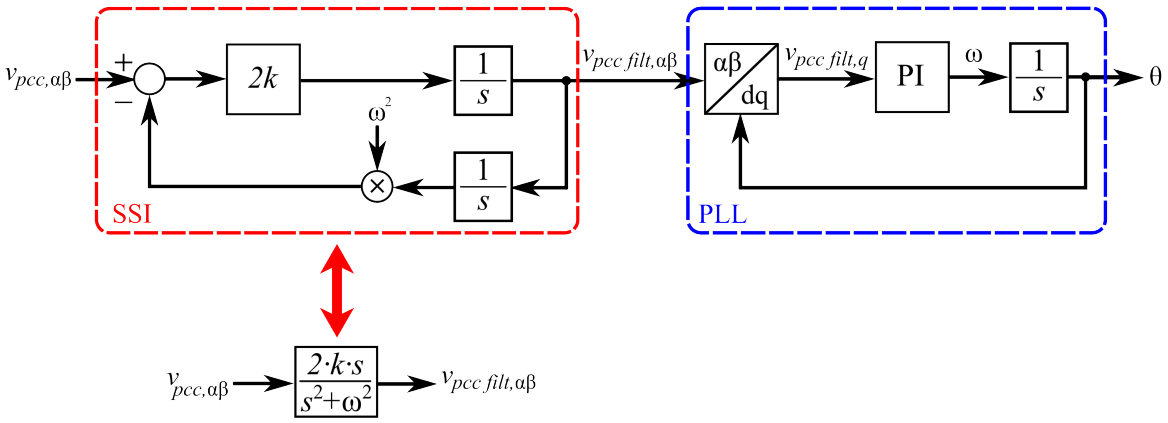


Fig. 5.3 Computation of the PCC voltage vector position.

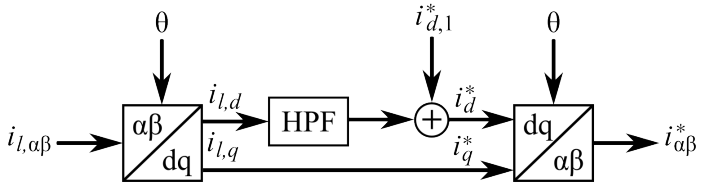


Fig. 5.4 APF reference current generation.

thus computed and used by the other control blocks. The operation of this control feature is depicted in detail in Fig. 5.3;

- **DC Voltage Regulator:** It is responsible for regulating the DC-link voltage v_{dc}. It consists of a simple PI regulator, whose output is the d-axis current reference $i^*_{d,1}$, corresponding to the active current component required to maintain the DC-link voltage level;

- **Reference Current Generator:** This block is in charge of computing the current references in stationary (α,β) reference frame $i^*_{\alpha\beta}$ (Fig. 5.4). The measured dq-load current $i_{l,dq}$ is first calculated by applying a rotational transformation to the αβ-load current $i_{l,\alpha\beta}$. Then, the d-axis current signal $i_{l,d}$ is processed by a high-pass filter (HPF) with a cut-off frequency of 20 Hz to remove the low-frequency term related to the active current absorbed by the load. The resulting signal is then summed with $i^*_{d,1}$ obtained from the DC-link voltage regulator and the d-axis reference current i^*_d is computed. Instead, the q-axis current signal $i_{l,q}$ is not processed, with the q-axis reference current $i^*_q = i_{l,q}$. Finally, $i^*_{\alpha\beta}$ is obtained with a rotational transformation.

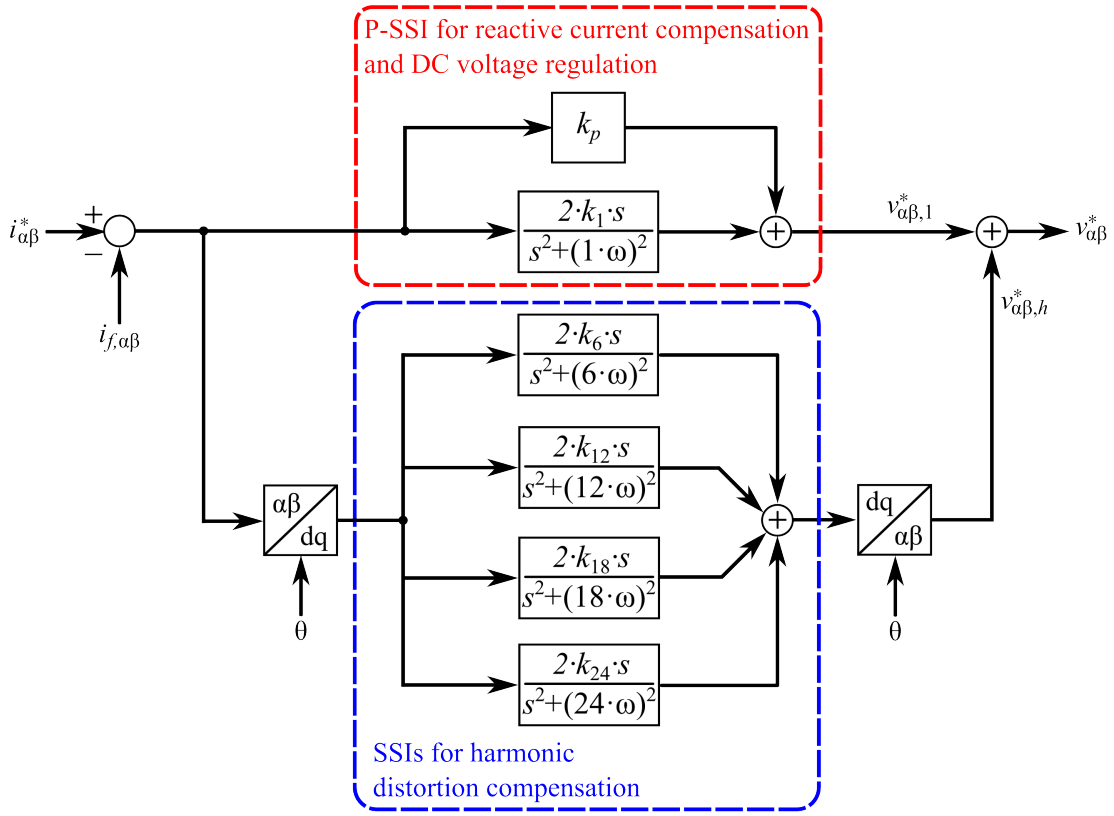


Fig. 5.5 Block diagram of the adopted APF current control.

- **Current Control:** The adopted current controller is depicted in Fig. 5.5. A proportional-sinusoidal signal integrator (P-SSI) regulator tuned at the grid fundamental frequency and operating in stationary (α,β) reference frame is in charge of performing the fundamental reactive current control and the DC-link voltage regulation. Instead, SSI regulators operating in synchronous (d,q) reference frame and rotating at the grid frequency are tuned at the harmonic orders $6k$, with $k = 1,2,3,4$. Each SSI regulator compensates for the $6k-1$ and $6k+1$ harmonics of negative and positive sequence, respectively, collapsing on the $6k$ harmonic in synchronous (d,q) reference frame. Thus, the controller computational effort to calculate the reference voltage $v^*_{\alpha\beta}$ and achieve the desired harmonic compensation is minimized, while the APF is able to compensate for current distortion components up to the 25$^{\text{th}}$ harmonic.

Finally, the computed reference voltages v^*_{abc} are provided to the pulse-width modulator (PWM), which generates the inverter commands q^* according to the adopted modulation technique (Fig. 5.2).

5.3 Case Study: APFs in Inverters Production Lines

With the increasing complexity of modern electronic equipment, the performance and reliability requirements for power electronic systems, along with those of their manufacturing processes, have become progressively more stringent. To satisfy these heightened demands, manufacturers of power converters commonly install regenerative testing systems within their production lines. These systems enable power converters end-of-line testing, thus reducing the likelihood of early-life failures while concurrently minimizing power drawn from the electrical grid and, as a result, decreasing the overall operational costs of the production facility [125], [126].

A possible regenerative testing methodology consists in evaluating the power converter by supplying a target motor mechanically coupled to a braking motor, which functions as a mechanical load emulator, within a back-to-back configuration (case (a) of Fig. 5.6) [127]. The power drawn by the braking motor can be returned to the grid only when it is driven by a bidirectional AC-AC power converter. However, when the converter under test has a high power rating, this testing approach becomes challenging. Specifically, the test bench, which comprises two motors and additional power electronics, becomes both bulky and costly [125]. Furthermore, a mechanical testing system necessitates additional safety protocols and maintenance, particularly when operating at high power and/or speed levels.

Owing to the limitations of the above-described approach, a more recent regenerative testing method, referred to as the virtual load [126] or virtual machine [128], has been proposed to reduce testing costs. In this approach, the electrical machines in the regenerative system are replaced by a single power electronic converter capable of bidirectional power flow, comprising two voltage source inverters arranged in a back-to-back configuration (case (b) of Fig. 5.6). The virtual load offers flexible controllability, enabling the testing of the converter under test (CUT) under a wide range of operating conditions, including variations in output current, voltage and frequency.

An alternative regenerative approach, suitable when space constraints are not a primary concern, involves incorporating a transformer within the regenerative loop with an appro-

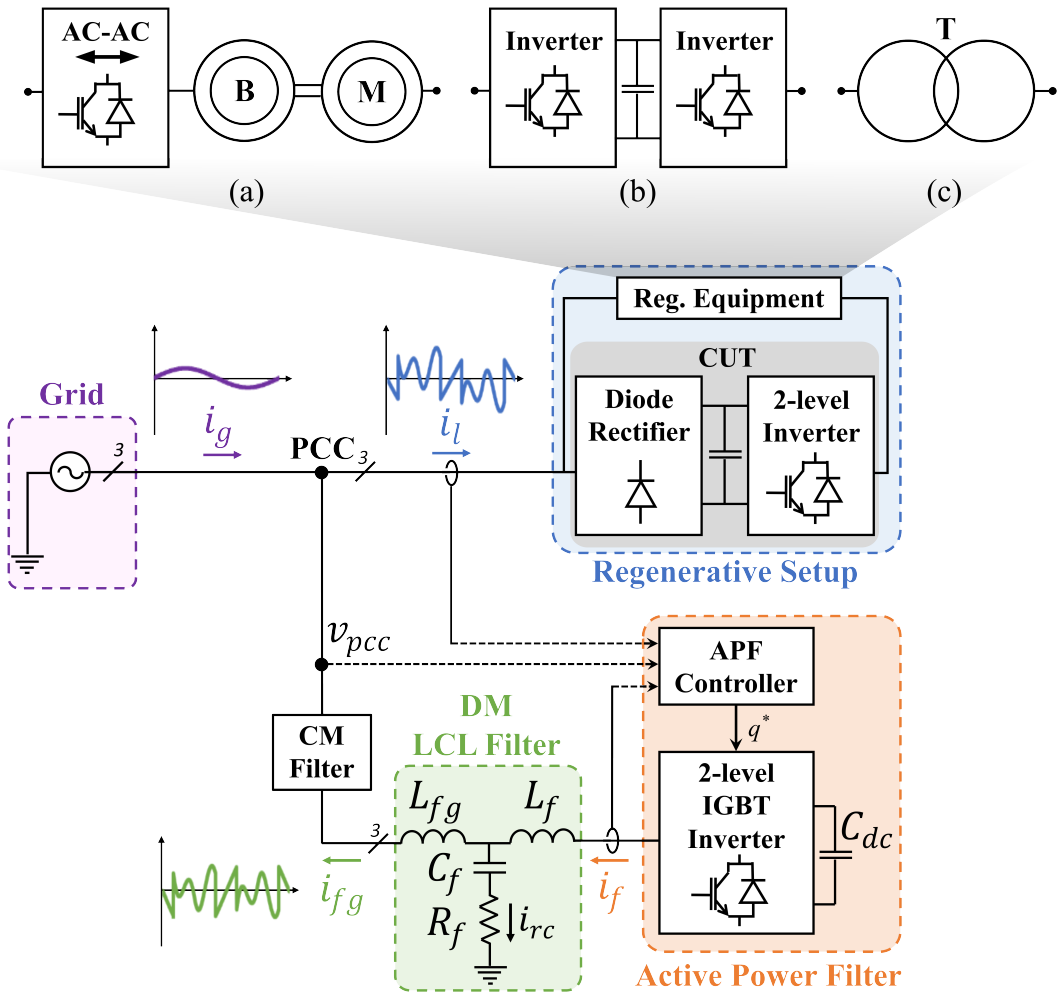


Fig. 5.6 Principle scheme of a shunt-type APF compensating for the distorted current injected by the passive front-end rectifier of the CUT during its final functional test in the regenerative system. The regenerative system equipment can include: a target motor (M) coupled with a breaking motor (B), which is interfaced to the grid through an inverter (a); a single power electronic converter with bidirectional power flow, comprising two voltage source inverters connected in a back-to-back configuration (b); a transformer (c).

priate turns ratio (case (c) of Fig. 5.6). This configuration reduces maintenance costs and eliminates the need to control additional converters beyond the CUT. However, it restricts testing to the fixed grid voltage and frequency. Consequently, this method is particularly well suited for evaluating converters that operate in the field at nearly constant operating points, such as those used in compressed air systems and vacuum pumps.

The CUT examined in this thesis is a power converter featuring an uncontrolled AC-DC input stage (e.g., thyristor or diode rectifier) and a DC-AC voltage source inverter at the

output stage. Regardless of the regenerative configuration employed, the active power recirculates within the regenerative system during testing. Consequently, the current drawn from the grid consists primarily of a small amount of active current to compensate for system losses, in addition to the distorted current produced by the CUT grid-side rectifier. With this type of configuration, the distorted current significantly exceeds the fundamental current drawn at the PCC, rendering the regenerative system a highly distorted non-linear load for the grid.

For these types of applications, the installation of a shunt-type APF in parallel to the regenerative system becomes essential to ensure compliance with international standards for harmonic distortion limitation [13]. In this context, the APF conceptually cancels the current drawn from the grid (Fig. 5.6), except for the active current associated with the CUT losses, thus providing substantial benefits in terms of the sizing, cost and efficiency of the facility power lines.

Chapter 6

Dedicated Discontinuous Pulse-Width Modulation for Industrial APFs

This chapter proposes an APF-dedicated generalized DPWM technique, referred to as APF-GDPWM, specifically designed for APFs operating in disturbed environments, such as industrial plants. This chapter presents the following contributions, which are addressed in dedicated sections:

- The introductory section explains the advantages of implementing DPWM techniques in grid-tied inverters. It also discusses why conventional DPWM solutions developed for AFEs and electrical drives are not suitable for APFs. Furthermore, the drawbacks of other APF-dedicated DPWM methods reported in the literature are highlighted, thus motivating the design of a new generalized DPWM solution for APFs (APF-GDPWM) that is suitable even for power converters operating in disturbed environments, such as industrial installations;
- The implementation of the proposed APF-GDPWM method is described in detail, emphasizing its advantages when operating in disturbed environments, in comparison with other APF-dedicated DPWM techniques reported in the literature;
- The conduction and switching losses of a two-level three-phase APF are analytically evaluated for both continuous pulse-width modulation (CPWM) techniques, such as SVPWM, and the proposed APF-GDPWM, as a function of the total harmonic distortion (THD_i) of the load current compensated by the APF;

- The PWM waveform quality of an APF implementing SVPWM and the proposed APF-GDPWM technique is examined. The analysis considers the APF compensating for distorted line currents with different THD_i levels. Furthermore, specific waveform quality indices associated with the PWM techniques are introduced to enable a comparative assessment between SVPWM and the presented APF-GDPWM;
- Experimental tests on a two-level TRL 9 industrial APF compensating a 260 kVA regenerative system are conducted to compare the performance of an APF implementing the proposed APF-GDPWM and the other dedicated DPWM solutions for APFs reported in the literature under different operating conditions of the CUT;
- Final considerations are provided in the concluding section.

The contributions presented in this chapter have resulted in the publication of [129] and [130].

6.1 Discontinuous Pulse-Width Modulation Techniques in APFs

While the installation of an APF enhances power quality, it also results in an increase in active power absorption at the PCC due to the inherent power converter losses. Therefore, maximizing the APF efficiency is essential to mitigate its impact on overall power line consumption. Conversely, the APF switching frequency is typically set as high as possible, at the expense of efficiency, to reduce the size and cost of the grid connection filters [39] and, simultaneously, to increase the converter control bandwidth, thus enhancing the APF harmonic compensation capability [131]. The use of DPWM techniques in two-level three-phase inverters is a well-established approach in the literature for reducing power converter switching losses by up to 50 %, or, alternatively, for increasing the switching frequency up to twice its value without adversely affecting the power converter thermal performance [132].

Each DPWM technique is optimized for a specific power factor value [133]. In all DPWM algorithms, the output of each inverter leg is clamped to either the positive or negative rail of the DC-link for one-third of the fundamental period (120°), thus eliminating the switching losses associated with the clamped phase. A uniform distribution of switching losses among the power devices is achieved by dividing the clamped region

into two symmetrical sub-intervals of 60°, ensuring that the leg output is clamped to both the positive and negative rails for equal duration. Moreover, the clamped intervals of each phase should be positioned near the positive and negative current peaks to maximize the reduction in switching losses [134]. In a three-wire power converter, an appropriate zero-sequence voltage is injected to achieve the desired DPWM [132].

Generalized DPWM strategies have been proposed in the literature to combine standard DPWMs according to the output power factor [132] or current [134]. However, these techniques are primarily designed for conventional applications, such as electrical drives [132], [134], [135] and AFEs [136], [137], [138], [139], where the low-order harmonic content of the current consists of the fundamental component. In such cases, the power factor and current vector position can be easily determined, allowing for the calculation of the optimal clamping interval for each phase. In contrast, an APF must inject multiple harmonic currents according to the non-linear load behavior. Consequently, its output current waveform deviates from a purely sinusoidal profile and multiple current peaks may occur within a single fundamental period. Therefore, accurately estimating the instantaneous phase shift between the APF voltage and current vectors becomes challenging. For this reason, generalized DPWM methods that rely on power factor or peak current estimation are not suitable for minimizing switching losses or increasing the switching frequency in APFs.

A generalized DPWM solution specifically designed for APFs was proposed in [140]. The algorithm operates at each control period, determining the phase to be clamped based according the instantaneous values of the three-phase reference voltages and currents. As a result, switching losses are minimized compared to conventional CPWM techniques, such as SVPWM. However, the proposed approach was validated only through laboratory experiments employing a three-phase diode rectifier as a non-linear load, where inductive or capacitive load behavior was emulated by modifying the DC output configuration. Consequently, several practical challenges associated with the deployment of APFs in industrial environments were not addressed. Indeed, this method is particularly sensitive to noise present in the line currents, which is common in disturbed environments where numerous grid-connected power converters can inject high-frequency disturbances into the grid. Such noise is captured by the APF line sensors, compromising the proper computation of the zero-sequence voltage. Unwanted and repetitive switching of the clamped phase may thus occur, leading to the following drawbacks:

- Decreased APF efficiency resulting from the increased number of switching events within a fundamental period;
- Degradation of the high-frequency quality of the APF output current, resulting in an increase in the THD_i of the current drawn at the PCC;
- A shift toward higher frequencies (above the kHz range) in the CM voltage harmonic spectrum of the components associated with zero-sequence voltage injection. The presence of CM voltage harmonics at elevated frequencies increases the sensitivity of the system to CM current circulation.

To overcome the limits of the methods available in the literature [140], this chapter proposes an improved generalized DPWM solution for APFs that is robust against line noise affecting APF operation in disturbed environments, such as industrial plants. Compared to [140], the proposed method (APF-GDPWM) improves the APF high-frequency output current distortion and limits the injection into the grid of CM voltage high-frequency components due to the zero-sequence, thus beneficially impacting on the design of the CM filter installed between the power converter and the grid (Figs. 5.1 and 5.6) to limit CM currents. Moreover, when applied to a standard 2-level IGBT inverter, it allows increasing the switching frequency up to two times with respect to the SVPWM without modifying the thermal design of the power converter. The doubling of the switching frequency has the significant benefit of the increase of the dynamic APF performance due to the higher regulation bandwidth, resulting in better compensation of the distorted currents [131]. Moreover, the DM LCL filter size and cost can be reduced, while meeting the harmonic attenuation requirements [13].

6.2 Proposed APF-GDPWM Algorithm

The computation of the zero-sequence voltage v^*_{cm} through the proposed APF-GDPWM solution is outlined in the flowchart of Fig. 6.1. The inputs of the algorithm consist of the reference voltages v^*_{abc} and currents i^*_{abc}. The reference voltages v^*_{abc} are obtained as output of the current control regulators (Fig. 5.5.), while the reference currents i^*_{abc} are computed as depicted in Fig. 5.4.

The reference voltage components v^*_a, v^*_b and v^*_c are compared to find which are the maximum v_x and the minimum v_y phase voltages. Consequently, their corresponding

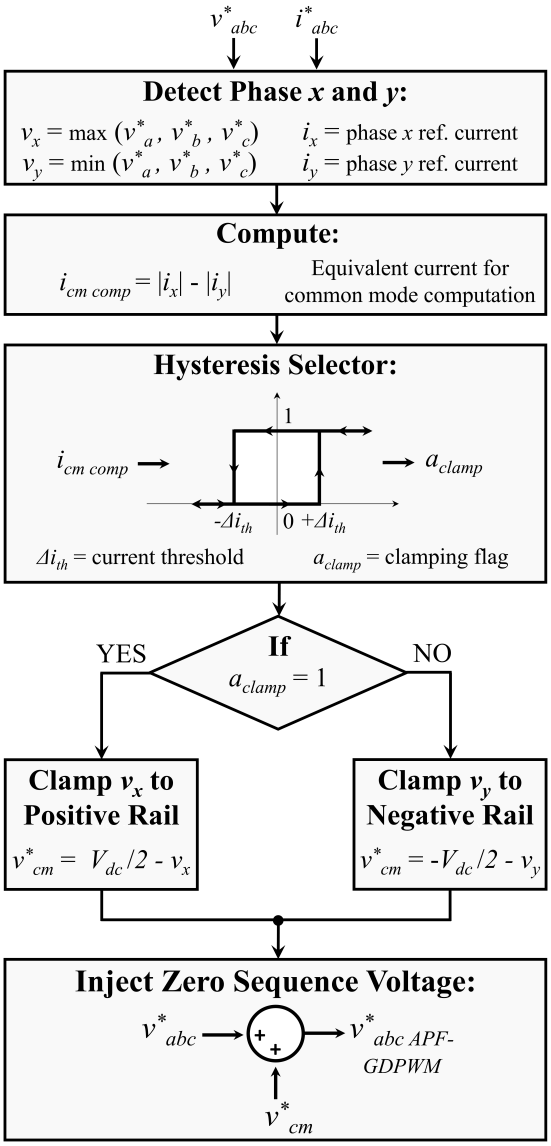


Fig. 6.1 Flowchart of the zero-sequence voltage v^*_{cm} computation with the proposed APF-GDPWM algorithm [129].

phase reference currents are defined as i_x and i_y. The voltages v_x and v_y can be clamped to the positive and negative rails of the DC-link, respectively. Whereas, the clamping of the remaining phase is not allowed, thus guaranteeing the maximum voltage linearity range for the APF-GDPWM. Indeed, by defining the modulation index as follows:

$$M = \frac{V^*}{V_{dc}/2} \tag{6.1}$$

where V^* is the magnitude of the reference voltage and V_{dc} is the DC-link voltage, the maximum value of M preserving linearity in the voltage formation process is $M_{max} = \frac{2}{\sqrt{3}}$ [133].

The maximum switching losses reduction is obtained in each control period if one of the phases v_x or v_y, operating with the highest reference current in terms of absolute value, is clamped to the positive ($\frac{V_{dc}}{2}$) or negative ($-\frac{V_{dc}}{2}$) DC rail. As shown in Fig. 6.2, six clamping sectors can be thus identified for the reference voltages v_a^*, v_b^* and v_c^*. The APF output phase voltage is assumed as sinusoidal, even if it provides multiple harmonic currents. Indeed, the fundamental components of the APF reference voltages are dominant, since they must balance the grid voltage that can be considered as sinusoidal. Only a small amount of voltage is provided to compensate for the higher current frequencies proportionally to the line impedance. For each sector, the phases allowed to be clamped to the positive and negative DC rails are reported in Table 6.1.

However, high frequencies current disturbances may circulate in power lines, e.g., the current ripple due to the switching of other grid-tied power converters in the surroundings. The frequencies of these current disturbances are often within the range defined by the APF control bandwidth and the sampling frequency. Therefore, they cannot be removed or compensated through software filtering. These high frequencies disturbances, combined with a non negligible sensitivity of the line current sensors, affect the current references i_{abc}^* and consequently the zero-sequence voltage computation. Indeed, when the absolute values of i_x and i_y are close to each other, a repetitive change of the clamped phase may occur. Therefore, a hysteresis selector is implemented into the APF-GDPWM algorithm to avoid the negative effect mentioned above. A resulting common-mode computation current $i_{cm\ comp}$ is defined as the difference between the absolute values of i_x and i_y. A change of the clamped phase is executed only if it exceeds a threshold $\pm\Delta i_{th}$, which is tuned considering the current sensors sensitivity and the disturbance amplitude.

The influence of noise on the zero-sequence voltage computation is exemplified in Fig. 6.3. In this scenario, a constant 4 kHz disturbance with an amplitude corresponding to 5 % of the peak reference current is injected into the power line, while the APF compensates for the 5^{th} and 7^{th} current harmonic orders produced by a nonlinear load exhibiting $THD_i = 102$ %. The power converter operates with a sampling frequency of 16 kHz. The clamping region n° 6 is grey highlighted and the algorithm computation in this interval is analysed. For a wide angular range, i_a^* and i_b^*, corresponding to i_x and i_y, respectively, have similar absolute values. Therefore, multiple zero crossings of $i_{cm\ comp}$

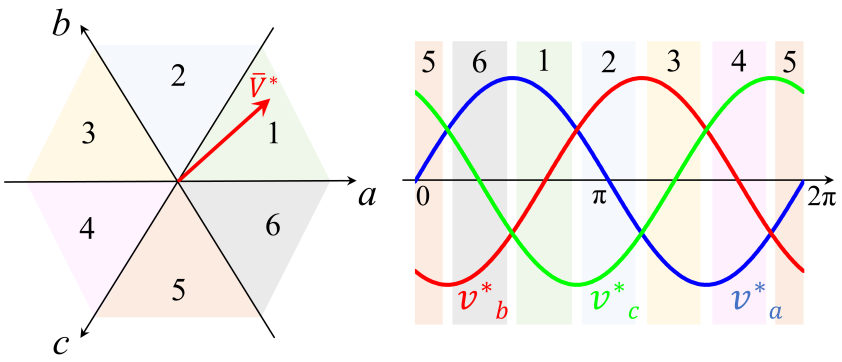


Fig. 6.2 Reference voltage space vector diagram divided in six clamping sectors [130].

Table 6.1 Phase voltage clamping sectors [130].

Sector	**Positive clamped phase v_x**	**Negative clamped phase v_y**
1	v^*_a	v^*_c
2	v^*_b	v^*_c
3	v^*_b	v^*_a
4	v^*_c	v^*_a
5	v^*_c	v^*_b
6	v^*_a	v^*_b

occur, resulting in a repetitive change of the clamped phase between v^*_a and v^*_b when Δi_{th} is null and the hysteresis selector is thus disabled. Instead, the side effect is completely eliminated by setting Δi_{th} to a comparable value with the noise amplitude ($\Delta i_{th} = 0.05$ pu). Therefore, the integration of the hysteresis selector into the APF-GDPWM improves the robustness of the algorithm to disturbances on the line currents, thus avoiding unnecessary changes of clamping phase and a consequent injection of high-frequency CM voltage related to the zero-sequence computation. Furthermore, the efficiency is increased since the number of switching transitions are minimized when the absolute values of i_x and i_y are similar.

By setting $\Delta i_{th} = 0$ pu and bypassing the hysteresis selector, the APF-GDPWM algorithm would be equivalent to the generalized DPWM technique for APFs proposed in

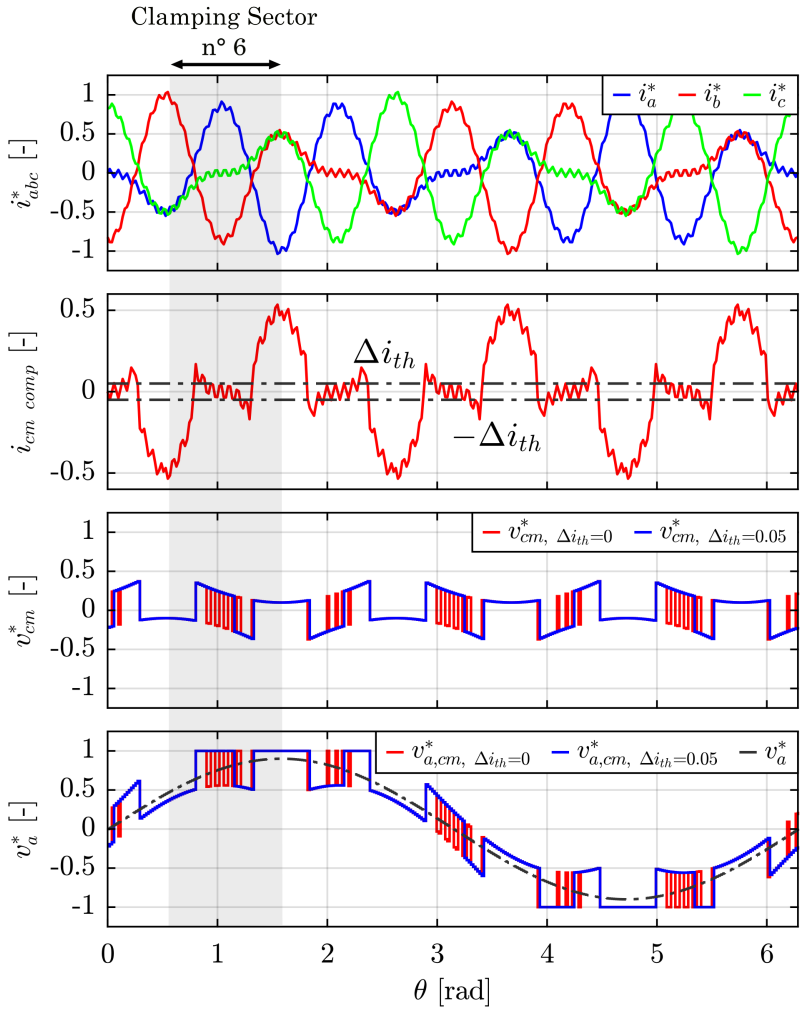


Fig. 6.3 APF operation with the proposed APF-GDPWM in presence of disturbances in the power lines. Currents and voltages are normalized. The clamping sector n° 6 is grey highlighted. From top to bottom: reference currents, common mode computation current, zero-sequence voltage and phase *a* reference voltage [130].

[140], which thus results particularly sensitive to high-frequency noise and consequently not suitable for field applications.

6.3 APF Conduction and Switching Losses

The conduction and switching losses of two-level three-phase PWM inverters used in electrical drives have been thoroughly analyzed in [132], [133]. However, these results

cannot be directly extended to an APF, which injects multiple harmonic current components rather than a single fundamental one. The mean conduction (P_c) and switching (P_{sw}) losses for a power device (either the switch or the freewheeling diode) in an APF are determined by integrating the instantaneous losses over one fundamental period. The corresponding expressions are presented in (6.2) and (6.3):

$$P_c = \frac{R_{on}}{2} \cdot I_{cell,x,rms}^2 + \frac{V_{th}}{2} \cdot I_{cell,x,m} \tag{6.2}$$

$$P_{sw} = \frac{E_{sw}}{V_{dc,n} \cdot I_n} \cdot f_{sw} \cdot V_{dc} \cdot k_{sw} \cdot I_{cell,x,m} \tag{6.3}$$

where R_{on} and V_{th} denote the on-state resistance and threshold voltage of the power device, respectively; E_{sw}, $V_{dc,n}$ and I_n represent the reference total energy loss, the nominal DC-link voltage and the nominal output current, as specified in the datasheet; f_{sw} is the switching frequency; V_{dc} is the actual DC-link voltage; $I_{cell,x,rms}$ and $I_{cell,x,m}$ are the RMS and mean currents in one of the two unidirectional switching cells into which each inverter leg can be subdivided. Specifically, $x = pos$ or $x = neg$ indicates whether the positive or negative unidirectional switching cell is considered, respectively (see Fig. 6.4). A detailed derivation of (6.2)–(6.3) is presented in the Appendix A.

The term k_{sw} denotes the switching loss factor [132], which relates the switching losses of the APF-GDPWM to those of standard CPWM techniques, such as SVPWM:

$$k_{sw} = \frac{P_{sw,APF-GDPWM}}{P_{sw,CPWM}} \tag{6.4}$$

Unlike in electric drive applications [133], P_c depends solely on the current flowing through the power devices. Indeed, neither the power factor, which is null, nor the output voltage (or modulation index M) influence the conduction losses. Conversely, the expression for P_{sw} remains unchanged. Nevertheless, the relationship between $I_{cell,x,rms}$ and $I_{cell,x,m}$ is not unique as in the case of single-harmonic control, but rather strictly determined by the specific characteristics of the non-linear load being compensated.

The form factor k_f, establishing the relationship between the mean and RMS values of the unidirectional switching cell current, is defined as:

$$k_f = \frac{I_{cell,x,m}}{I_{cell,x,rms}} \tag{6.5}$$

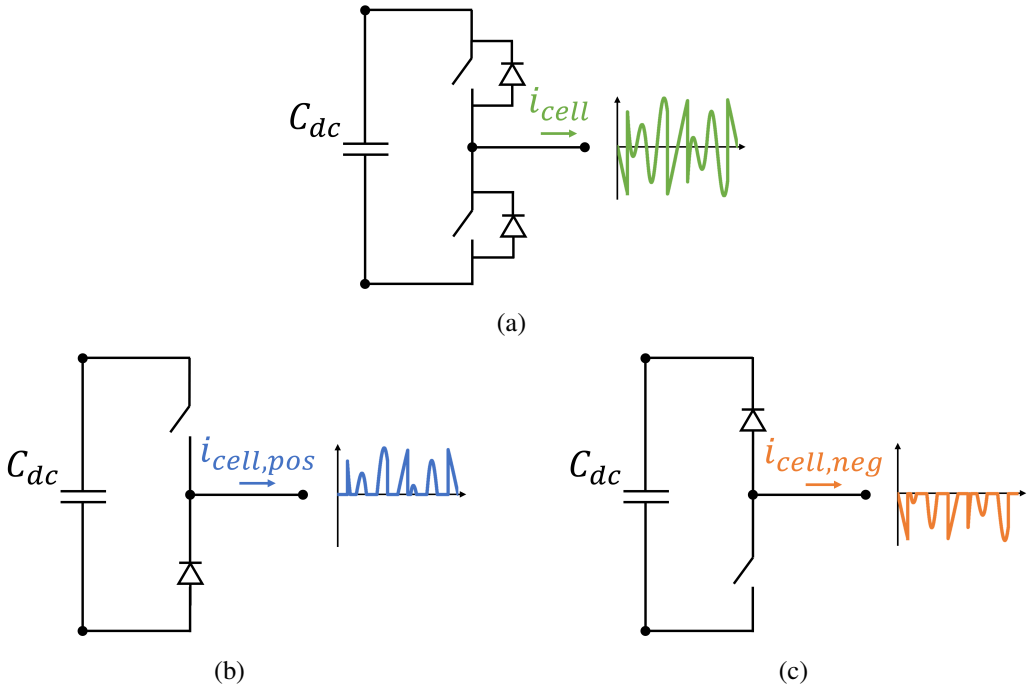


Fig. 6.4 The inverter leg of a two-level three-phase APF (a) is a bidirectional switching cell, which can be subdivided into two unidirectional cells. Each cell consists of a power switch (e.g., IGBT or MOSFET) with the related freewheeling diode. The unidirectional cells conduct respectively positive $i_{cell,pos}$ (b) and negative $i_{cell,neg}$ (c) currents. Instantaneously, the APF output current is $i_{cell} = i_{cell,pos} + i_{cell,neg}$ [129].

Conversely, the relationship between the APF RMS output current $I_{cell,rms}$ and the RMS current in the unidirectional switching cell $I_{cell,x,rms}$ is independent of the load being compensated:

$$I_{cell,rms} = \sqrt{2} \cdot I_{cell,x,rms} \tag{6.6}$$

Therefore, P_c and P_{sw} can be expressed as functions of the APF operating current $I_{cell,rms}$, the type of non-linear load, which influences k_f, and the implemented modulation technique, which affects k_{sw}:

$$P_c = \frac{R_{on}}{4} \cdot I_{cell,rms}^2 + \frac{V_{th}}{2\sqrt{2}} \cdot k_f \cdot I_{cell,rms} \tag{6.7}$$

$$P_{sw} = \frac{E_{sw}}{\sqrt{2} \cdot V_{dc,n} \cdot I_n} \cdot f_{sw} \cdot V_{dc} \cdot k_{sw} \cdot k_f \cdot I_{cell,rms} \tag{6.8}$$

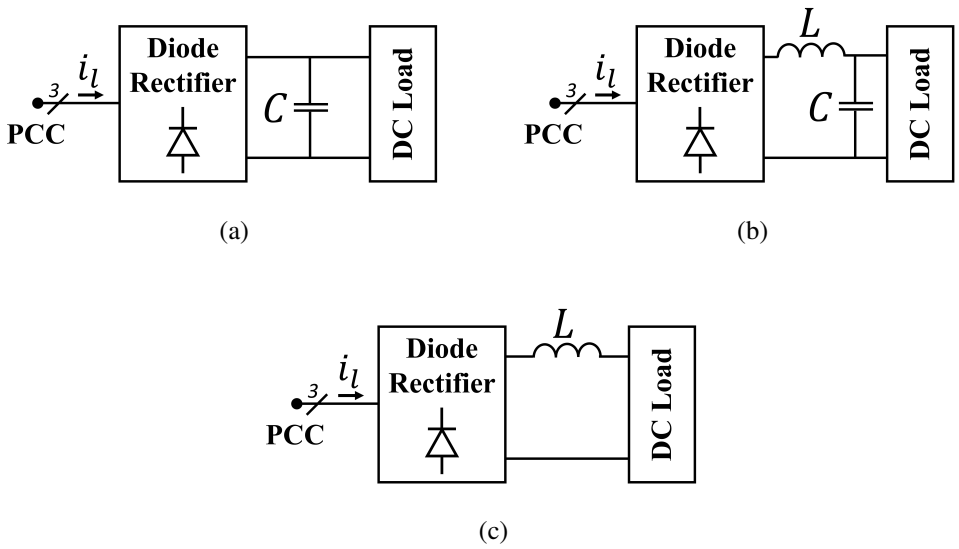


Fig. 6.5 Different examples of non-linear loads. Diode front-end rectifier with capacitive (a), inductive-capacitive (b) and inductive (c) output and supplying a generic DC load [129].

A common example of a three-phase non-linear load connected to the grid is the full-bridge diode front-end rectifier [141], [142]. The modeling of the current behavior of a diode rectifier is not unique, as the distortion introduced by the non-linear load is influenced in both magnitude and waveform by the type of output filter [38], [123], [141] and by the ratio between the inductance L and capacitance C of the output filter (Fig. 6.5).

Consequently, for the purposes of a standardized case study, an ideal diode rectifier is adopted, characterized as follows:

$$i_l(n,\theta,\tau) = \sum_{n=1}^{\infty} \frac{4\sqrt{3}}{n\pi} \cdot \sin\left(n \cdot \frac{\tau}{2}\right) \cdot \sin(n \cdot \theta) \cdot K(n) \tag{6.9}$$

$$K(n) = \begin{cases} -1, & n = 6k-1 \\ +1, & n = 6k+1 \\ 0, & \text{otherwise} \end{cases} \quad ,\forall k \in \mathbb{N} \tag{6.10}$$

where $\tau \in [0, \frac{\pi}{3}]$. The load exhibits non-linear capacitive behavior as $\tau \to 0$ and non-linear inductive behavior as $\tau \to \frac{\pi}{3}$ (Fig. 6.6).

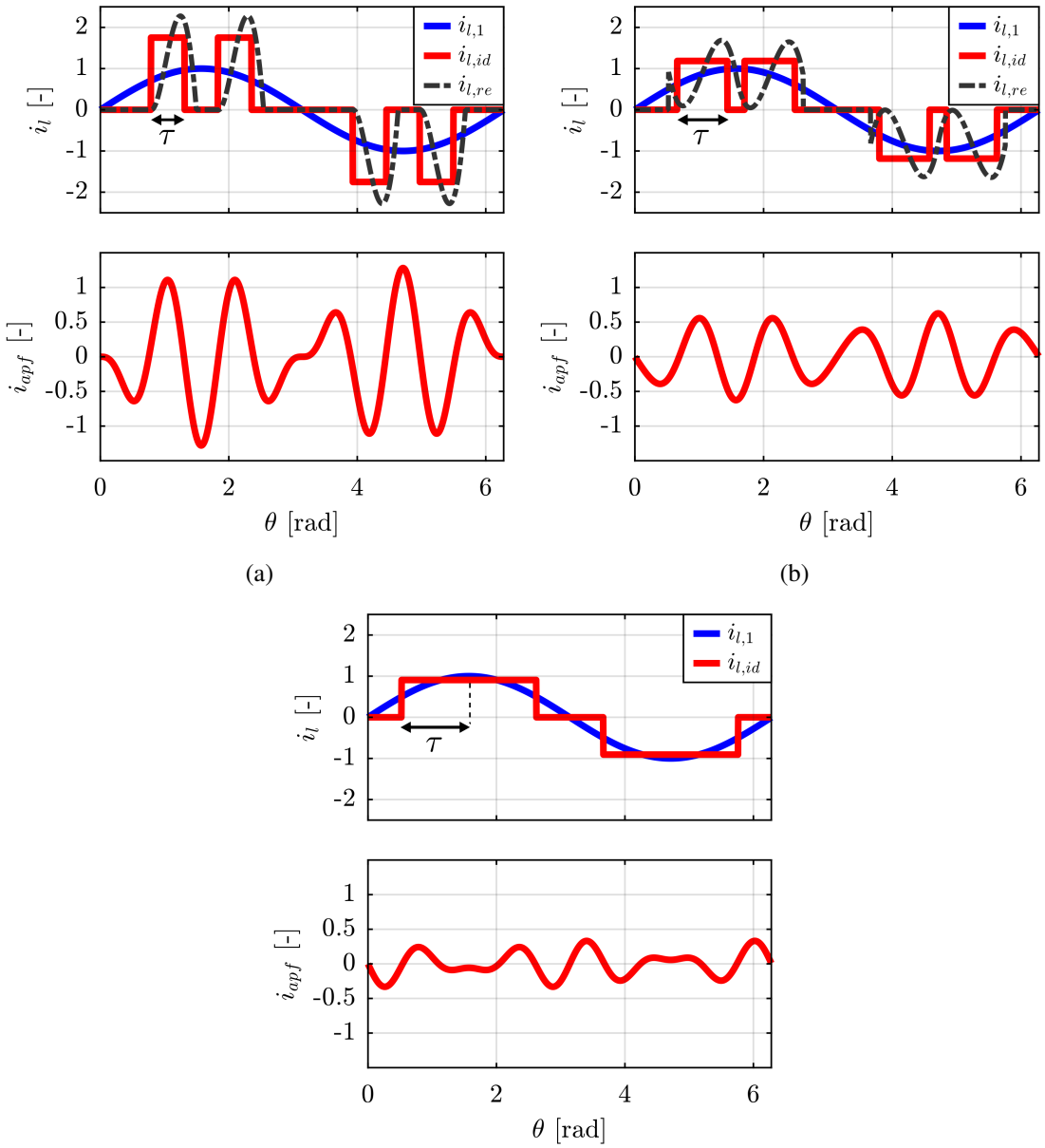


Fig. 6.6 5th and 7th harmonic compensation of a diode front-end rectifier. From top to bottom: ideal load current ($i_{l,id}$) and its fundamental component ($i_{l,1}$), APF output current (i_{apf}). The currents are normalized with respect to the peak of $i_{l,1}$. (a) Rectifier with capacitive output $\left(\tau = \frac{\pi}{6}\right)$ and input $THD_i = 102$ %. (b) Rectifier with LC output $\left(\tau = \frac{\pi}{4}\right)$ and input $THD_i = 63$ %. (c) Rectifier with inductive output $\left(\tau = \frac{\pi}{3}\right)$ and input $THD_i = 31$ %. A real rectifier input current $i_{l,re}$ with the same THD_i and RMS of $i_{l,id}$ is also reported for (a) and (b) [129].

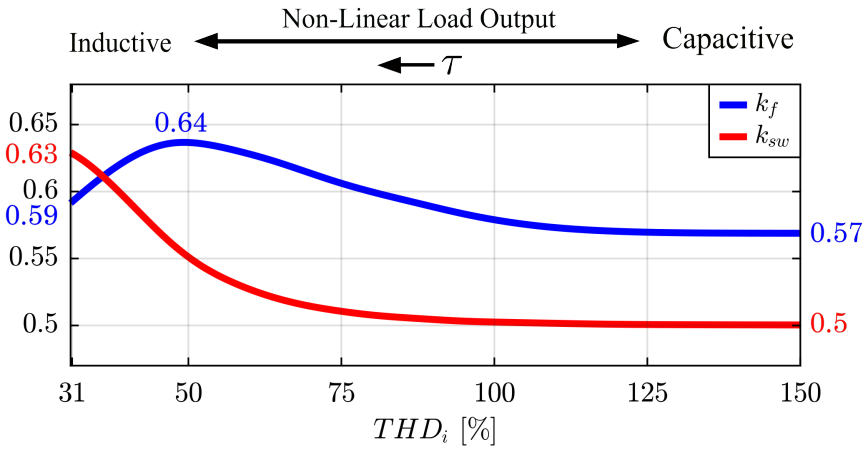


Fig. 6.7 The form factor k_f and the switching loss factor k_{sw} of an APF compensating for the 5$^{\text{th}}$ and 7$^{\text{th}}$ harmonic currents absorbed by an ideal diode rectifier. k_f and k_{sw} are expressed as a function of the non-linear load THD_i [129].

The impact of the APF-GDPWM on switching losses is analyzed for an APF compensating the 5$^{\text{th}}$ and 7$^{\text{th}}$ current harmonics provided by (6.9). As illustrated in Fig. 6.6, for the same fundamental current $i_{l,1}$ absorbed by the ideal rectifier, both the load current distortion THD_i and the corresponding compensation effort required from the APF increase in the event of capacitive output (i.e., as τ decreases). The dependence of the parameters k_f and k_{sw} on the input current distortion THD_i of the ideal rectifier is depicted in Fig. 6.7. The form factor k_f remains approximately constant (around 0.6) over the considered range of THD_i, reaching a maximum value of 0.64 for $THD_i \simeq 50$ %. The highest switching loss reduction, equal to 50 % ($k_{sw} = 0.5$), is achieved with capacitive loads (i.e., for large values of THD_i). Similarly, a significant switching loss reduction of 37 % is observed for inductive loads, corresponding to $k_{sw} = 0.63$ when $THD_i = 31\%$.

The computation of power device losses is carried out according to (6.7)–(6.8) using the commercial CM450DX-24T1 IGBT module, in order to demonstrate the effectiveness of the APF-GDPWM in reducing the overall inverter losses. The electrical characteristics of both the IGBT and its anti-parallel diode are obtained from the module datasheet [143] and are summarized in Table 6.2, together with the remaining system parameters. As illustrated in Fig. 6.8, the switching losses P_{sw} represent the main contribution to the total IGBT losses (Fig. 6.8a), whereas the conduction losses P_c are dominant in the diode (Fig. 6.8b). Consequently, the adoption of the APF-GDPWM instead of a CPWM proves more advantageous for the IGBT than for the diode, leading to a total loss reduction of 28.2–37.9 % and 16.8–22.4 %, respectively (Fig. 6.8). Given that the IGBT losses have a

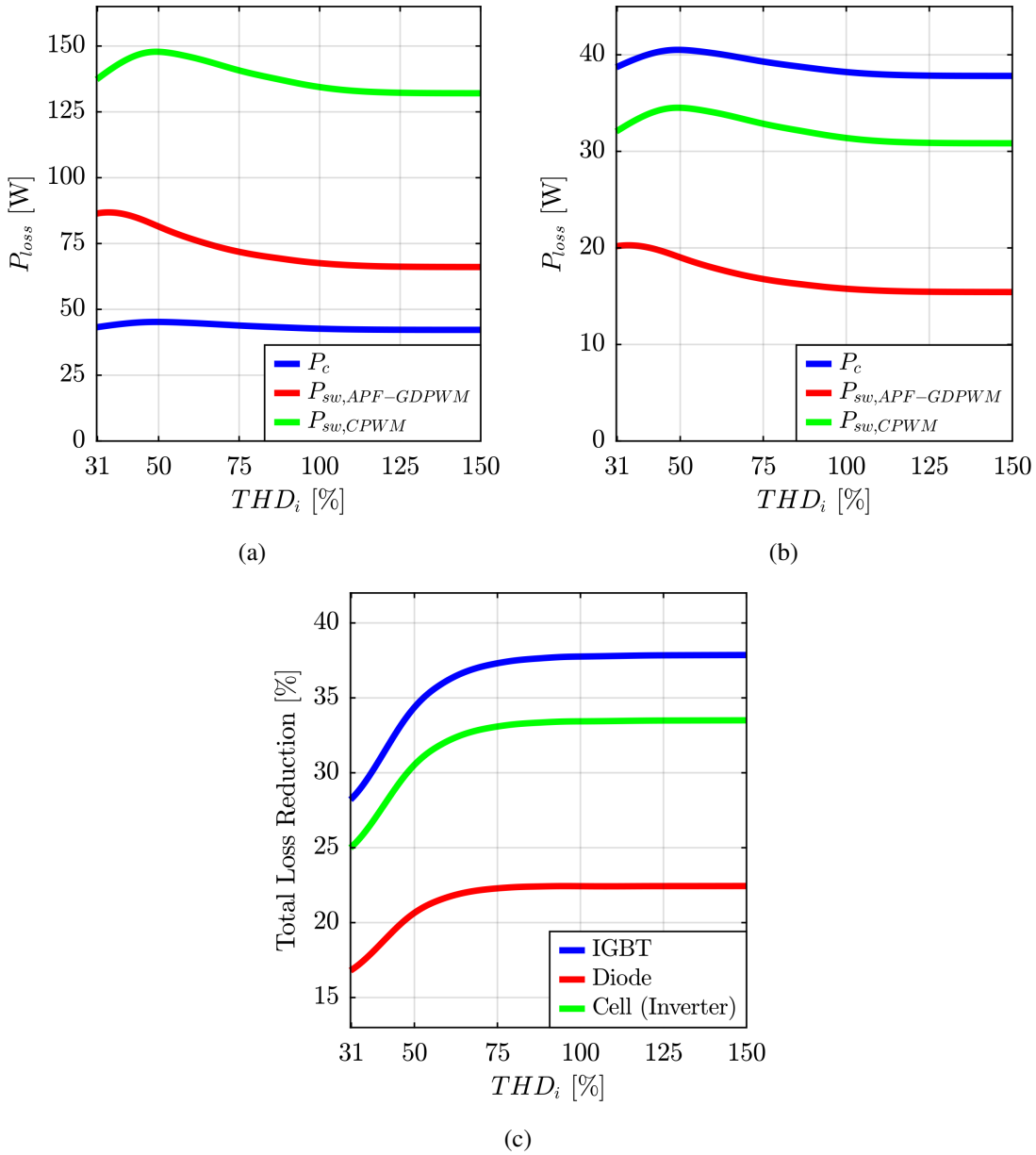


Fig. 6.8 Power devices losses for CM450DX-24T1 IGBT module according to the input THD_i of the ideal diode rectifier. The inverter is operating under the conditions described in Table 6.2. IGBT (a) and diode (b) conduction losses (P_c), switching losses with CPMWs ($P_{sw,CPWM}$) and APF-GDPWM ($P_{sw,APF-GDPWM}$). (c) IGBT, diode and switching cell total loss reduction obtained with APF-GDPWM with respect to CPWMs. The loss reduction for the switching cell also corresponds to the overall inverter loss reduction [129].

more significant influence on the overall converter efficiency, the switching loss reduction achieved by the APF-GDPWM translates into a substantial total loss decrease for both

Table 6.2 CM450DX-24T1 data and system parameters for power losses computation [129].

IGBT Module Data[a]				**System Parameters**	
$R_{on,IGBT}$	3.0 mΩ	$R_{on,diode}$	2.7 mΩ	$I_{apf,rms}$	150 A_{rms}
$V_{th,IGBT}$	0.84 V	$V_{th,diode}$	0.75 V	V_{dc}	750 V
$E_{sw,IGBT}$	98.5 mJ	$E_{sw,diode}$	23.0 mJ	f_{sw}	8 kHz
$V_{dc,n}$	600 V	I_n	450 A		

[a] Data for junction temperature $T_{v,j}$ = 150 °C and gate-emitter voltage $V_{g,e}$ = 15 V.

the switching cell and the entire inverter, ranging from 25.0 % to 33.5 %, with the best performance observed in the case of a diode rectifier with a capacitive output.

The capability of the APF-GDPWM to reduce switching losses with respect to CPWMs can be exploited either to enhance the converter efficiency or to increase the switching frequency, thus yielding additional benefits in the design of the DM LCL filter [39], [113], [114], [115], [116] and improving the harmonic compensation capability [131]. Indeed, for an equal total power loss condition, the switching frequency f_{sw} can be increased according to the following relation:

$$f_{sw,APF-GDPWM} = \frac{f_{sw,CPWM}}{k_{sw}} \tag{6.11}$$

6.4 Analysis of APF Output Current Distortion

The current ripple injected into the grid by the APF $i_{fg,h}$ is closely related with the flux ripple λ_h, which can be obtained by integrating the high-frequency component of the APF phase output voltage v_h generated by the inverter switching:

$$\lambda_h = \int_0^t v_h \, dt \tag{6.12}$$

$$i_{fg,h} = L_{eq} \cdot \lambda_h \tag{6.13}$$

where L_{eq} denotes the equivalent output inductance, which varies with the frequency and depends on both the DM LCL filter parameters and the grid impedance.

The analysis of λ_h instead of $i_{fg,h}$ provides a standardized framework for discussion, rendering it independent of the system electrical parameters. An indicator commonly employed in the literature to assess flux quality is the harmonic distortion factor (HDF) [144], which can be defined as follows:

$$HDF = 9 \cdot \frac{\lambda_{h,rms}^2}{\lambda_{b,rms}^2} \tag{6.14}$$

where $\lambda_{h,rms}$ represents the RMS value of the flux ripple and $\lambda_{h,b,rms}$ denotes the base value, defined as:

$$\lambda_{b,rms} = \frac{V_{dc}}{8 \cdot f_{sw}} \tag{6.15}$$

The analytical evaluation of $\lambda_{h,rms}^2/\lambda_{b,rms}^2$ for various modulation strategies, including SVPWM and DPWM algorithms, is presented in [133] for two-level inverter applications characterized by a single-frequency output voltage, such as electric drives. The results obtained are also applicable to APFs, provided that their low-frequency output voltage is assumed to be purely sinusoidal.

The HDF for APF-GDPWM is evaluated as a function of the modulation index M using MATLAB scripts, considering an APF that compensates for the 5^{th} and 7^{th} current harmonics drawn by the ideal diode rectifier described in (6.9). The resulting values are presented in Fig. 6.9 for different levels of non-linear load THD_i. The HDF curves corresponding to APF-GDPWM are observed to lie between those of DPWM1 and DPWM3, which represent, respectively, the DPWM strategies with the highest and lowest harmonic distortion characteristics [132], [133], [140], [144]. In particular, for a rectifier with inductive output ($THD_i = 31$ %), the waveform closely resembles that of DPWM3. The HDF for APF-GDPWM increases correspondingly with higher values of THD_i. Fig. 6.9 illustrates that, at the same switching frequency, APF-GDPWM exhibits a disadvantage relative to SVPWM in terms of harmonic distortion.

However, the HDF analysis can also be conducted under conditions of equal power losses. In this context, the switching frequency can be increased for APF-GDPWM in

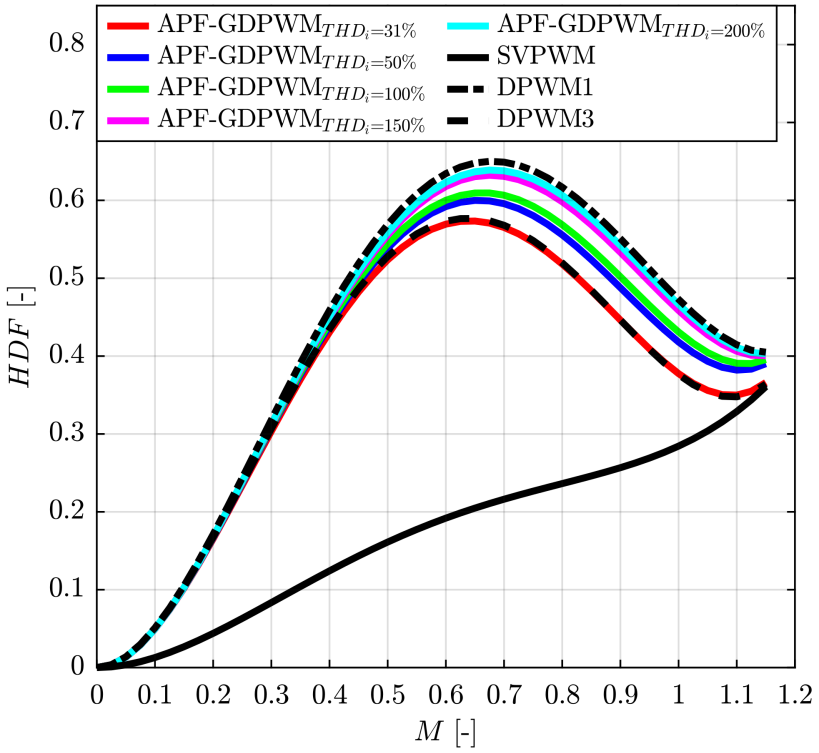


Fig. 6.9 Harmonic distortion factor under equal switching frequency (HDF) of an APF compensating for the 5$^{\text{th}}$ and 7$^{\text{th}}$ current harmonics drawn by an ideal diode rectifier (6.9) [129].

accordance with (6.11). Consequently, the harmonic distortion factor under equal inverter efficiency, denoted as HDF^{η}, is introduced:

$$HDF^{\eta} = k_{sw}^2 \cdot HDF \tag{6.16}$$

As illustrated in Fig. 6.10, under conditions of equal inverter losses, APF-GDPWM exhibits superior distortion performance compared to SVPWM, independent of the load THD_i. This behavior is particularly notable for $M \in [0.8, 1]$, which corresponds to typical modulation index values during APF steady-state operation, as these values ensure a sufficient voltage margin for output current control while simultaneously limiting the required DC-link voltage [140].

The HDF is a valuable metric for assessing the RMS value of the current (or flux) ripple injected into the grid by the APF. However, it does not convey information regarding the peak value of λ_h, which is a critical parameter for the proper design of the DM LCL filter inductors. Indeed, accurate knowledge of this peak value is essential to prevent flux

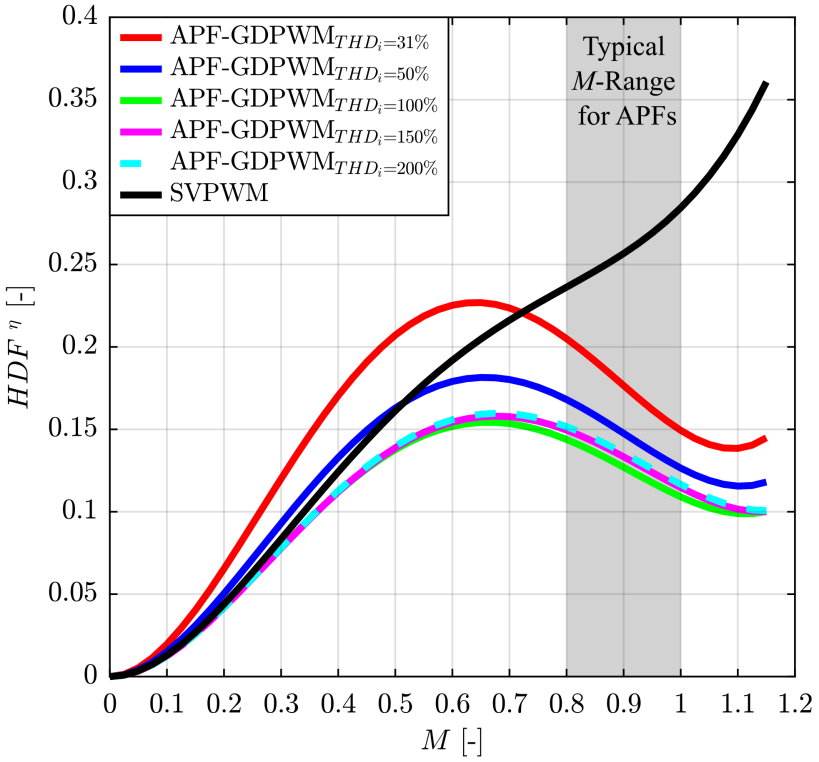


Fig. 6.10 Harmonic distortion factor under equal inverter efficiency (HDF^{η}) of an APF compensating for the 5$^{\text{th}}$ and 7$^{\text{th}}$ current harmonics drawn by an ideal diode rectifier (6.9) [129].

density saturation in the inductors. Therefore, the peak-to-peak maximum value of the flux ripple over a switching period $\lambda_{h,pp\ max}$ is computed as a function of M using MATLAB scripts, as in [145], [146]. The results obtained for both SVPWM and APF-GDPWM are presented in per-unit form in Fig. 6.11:

$$\lambda_{h,pp\ max,pu} = \frac{\lambda_{h,pp\ max}}{\lambda_{b,pp\ max}} \tag{6.17}$$

$$\lambda_{b,pp\ max} = \frac{V_{dc}}{6 \cdot f_{sw}} \tag{6.18}$$

where $\lambda_{h,pp\ max,pu}$ and $\lambda_{b,pp\ max}$ denote the per-unit and base values, respectively.

Unlike HDF, the per-unit peak-to-peak flux ripple $\lambda_{h,pp\ max,pu}$ obtained with APF-GDPWM is independent of the non-linear load current THD_i. Furthermore, the corre-

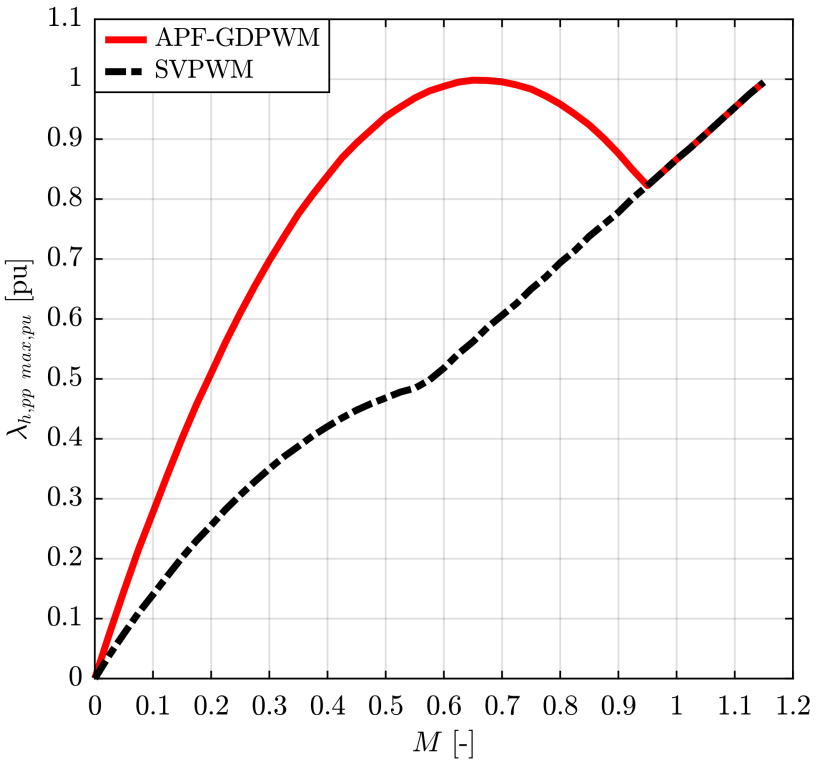


Fig. 6.11 Peak to peak maximum value of flux ripple under equal switching frequency ($\lambda_{h,pp\ max,pu}$) of an APF compensating for the 5$^{\text{th}}$ and 7$^{\text{th}}$ current harmonics drawn by an ideal diode rectifier (6.9) [129].

sponding curve lies above that of SVPWM for $M < 0.95$, while the curves coincide for $M \in [0.95, \frac{2}{\sqrt{3}}]$.

Similar to HDF, an analysis of $\lambda_{h,pp\ max,pu}$ can also be conducted under conditions of equal inverter efficiency. For this purpose, the corresponding indicator $\lambda^{\eta}_{h,pp\ max,pu}$ is introduced:

$$\lambda^{\eta}_{h,pp\ max,pu} = k_{sw} \cdot \lambda_{h,pp\ max,pu} \tag{6.19}$$

As illustrated in Fig. 6.12, under conditions of equal inverter losses, APF-GDPWM and SVPWM yield comparable peak-to-peak maximum flux ripple values for low M. Conversely, for high M, particularly within the typical operating range ($i.e., M \in [0.8, 1]$), APF-GDPWM ensures a lower $\lambda^{\eta}_{h,pp\ max,pu}$.

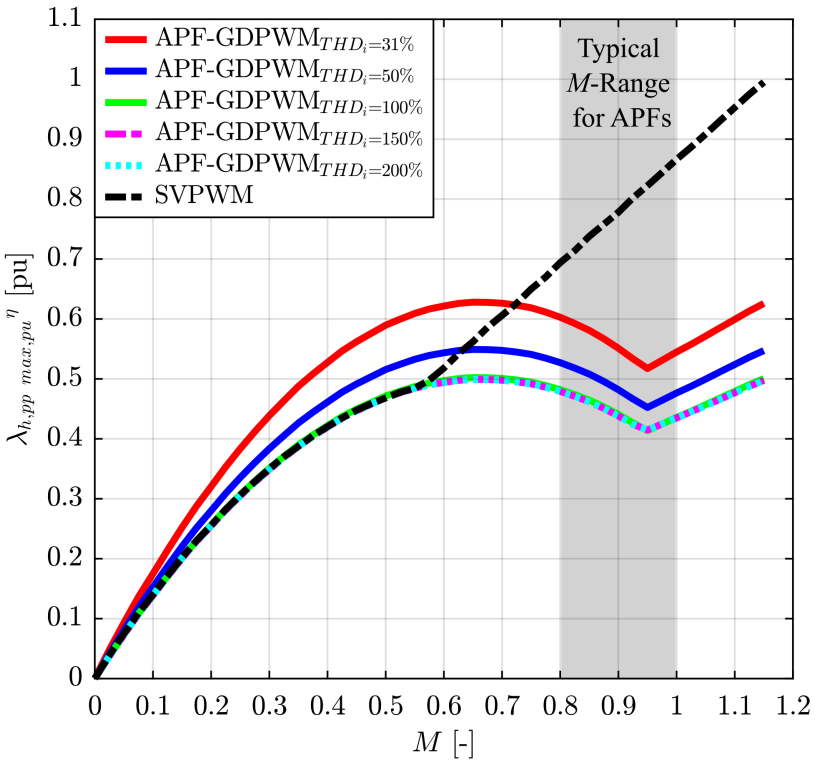


Fig. 6.12 Peak to peak maximum value of flux ripple under equal inverter efficiency ($\lambda^{\eta}_{h,pp\ max,pu}$) of an APF compensating for the 5$^{\text{th}}$ and 7$^{\text{th}}$ current harmonics drawn by an ideal diode rectifier (6.9) [129].

6.5 Experimental Validation

The case study of the non-linear load used in the experimental tests is a regenerative system employed for the final functional testing of the CUT at the end of the production line, as shown in Fig. 6.13. In the regenerative system, active power is recirculated through a line transformer. The CUT, rated at 260 kVA, is a power converter designed for electrical drives, featuring a three-phase diode rectifier with an output LC filter in the AC-DC stage (Fig. 6.5b) and a two-level three-phase IGBT inverter in the DC-AC stage. During full-power operation, the diode rectifier draws a current with a THD_i of 34.3 %.

A two-level APF is connected in parallel with the regenerative system (Fig. 6.13) to mitigate the current harmonics injected by the CUT grid-connected rectifier. It is interfaced to the grid through an LCL filter with L_f = 50 µH, C_f = 64 µF, R_f = 100 mΩ and L_{fg} = 15 µH. The APF is controlled according to the algorithms presented in Chapter 5 and the APF-GDPWM algorithm is implemented at f_{sw} = 16 kHz. It compensates for current

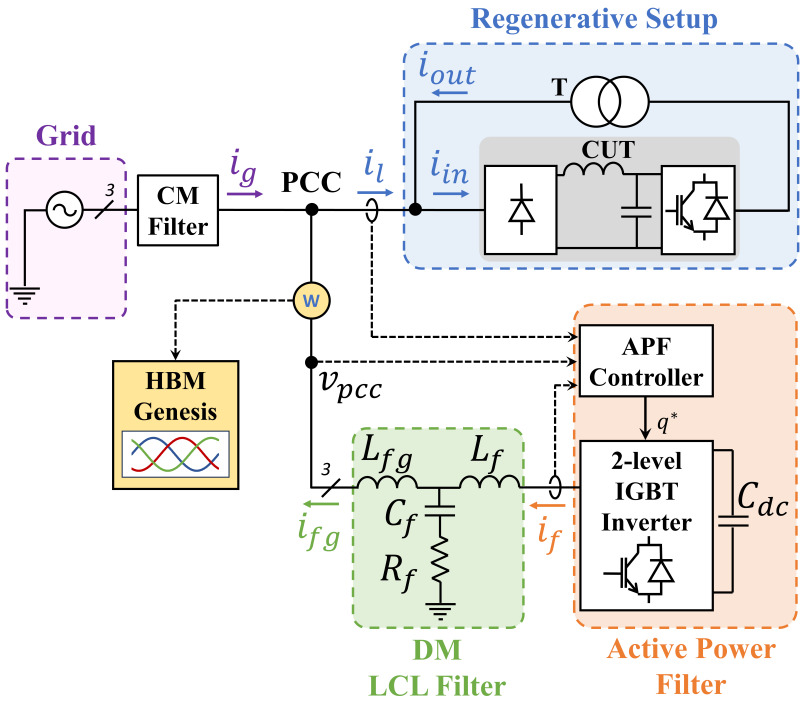


Fig. 6.13 Scheme of the shunt-type APF in parallel to a regenerative system used for the final functional tests of industrial inverters [129].

distortion up to the 25$^{\text{th}}$ harmonic, while its DC-link voltage is regulated to maintain a modulation index of approximately $M \simeq 0.9$ during APF operation. A HBM Genesis data recorder is connected between the LCL filter and the grid to collect electric data, thus evaluating the overall power converter losses, consisting in both the inverter and LCL filter losses (Fig. 6.13). The system setup is depicted in Fig. 6.14.

Figure 6.15 illustrates the system steady-state behavior under full-power operation. Without the APF, the grid current would reach $i_g = i_l = 170.0\ \text{A}_{\text{rms}}$. Instead, with compensation provided by the APF, i_g is markedly reduced to 32.8 A_{rms} (-80.7 %). The current injected back into the PCC by the CUT (i_{out}) leads the fundamental component of the current drawn by the CUT ($i_{in,1}$). This phase shift implies a reactive current absorption by the regenerative system at the fundamental frequency, which is compensated by the APF along with the harmonic components, resulting in a grid current i_g with a unity power factor. As shown in Fig. 6.15, i_{out} features a high-frequency current ripple caused by the switching of the CUT ($f_{sw,CUT} = 4$ kHz). This high-frequency component propagates to the PCC and is acquired on i_l by the APF controller. As previously explained in Section 6.2, this high-frequency noise can interfere with the computation of the zero-sequence voltage in APFs implementing the APF-GDPWM technique. The APF compensation

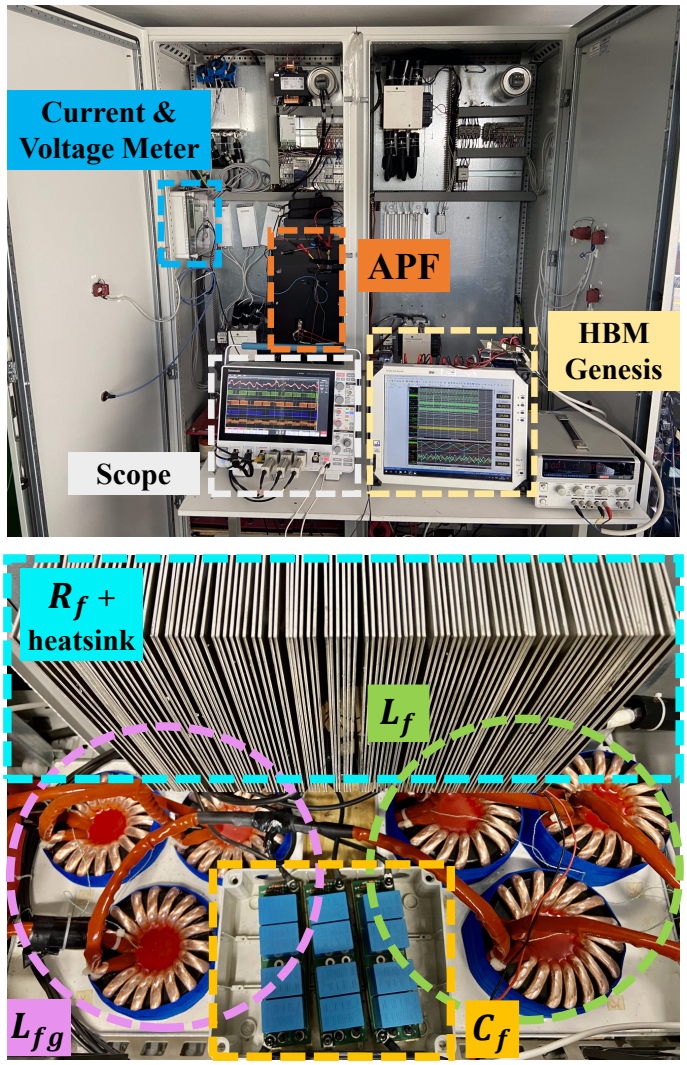


Fig. 6.14 System setup: APF cabinet with measuring equipment (top) and assembled differential mode LCL filter (bottom) [129].

performance, as well as the propagation of 4 kHz current noise on the power line, are further illustrated in Fig. 6.16, which presents i_l and i_g in the frequency domain.

The performance of the APF implementing the APF-GDPWM is evaluated under two conditions: proper tuning (i.e., Δi_{th} = 30 A) and with the hysteresis selector bypassed (i.e., Δi_{th} = 0 A). Disabling the hysteresis selector is equivalent to implementing the generalized DPWM technique for APFs presented in [140]. Evaluations are conducted while the

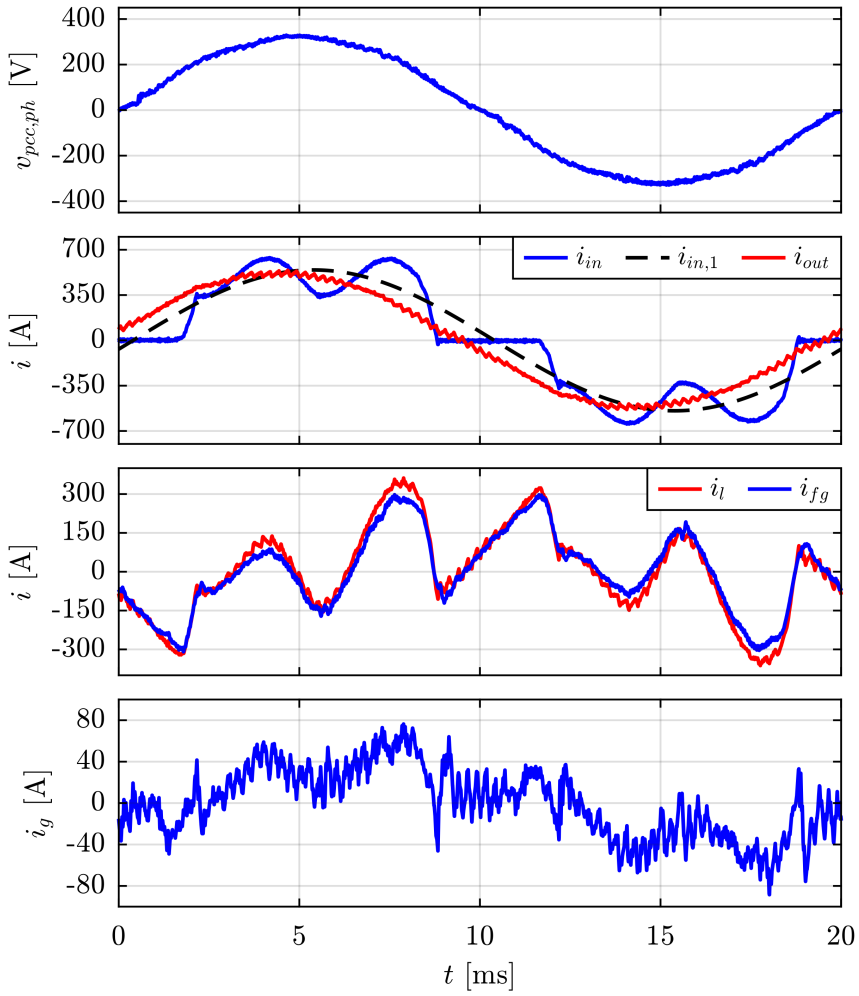


Fig. 6.15 Full-power operation of the regenerative system with connected in parallel the APF. From top to bottom: phase PCC voltage $v_{pcc,ph}$, CUT input current i_{in} and its fundamental component $i_{in,1}$, CUT output current i_{out}, current absorbed by the regenerative system i_l, current injected by the APF at the PCC i_{fg}, grid current i_g [129].

regenerative system is operating at full-power (P_{CUT} = 260 kW) in Test 1 (Figs. 6.17 and 6.18), half-power (P_{CUT} = 135 kW) in Test 2 (Figs. 6.20 and 6.21) and reduced power (P_{CUT} = 28 kW) in Test 3 (Figs. 6.23 and 6.24). Reducing P_{CUT} results in the CUT diode rectifier to behave more capacitively, leading to an increase in THD_i of the input current i_{in}, which reaches 34.3 % in Test 1, 43.9 % in Test 2 and 106.7 % in Test 3. Moreover, the current magnitude decreases and the sensitivity of the current sensors reduces, significantly affecting the computation of the zero-sequence voltage when the hysteresis selector is disabled (i.e., $\Delta i_{th} = 0$). Bypassing the hysteresis selector results

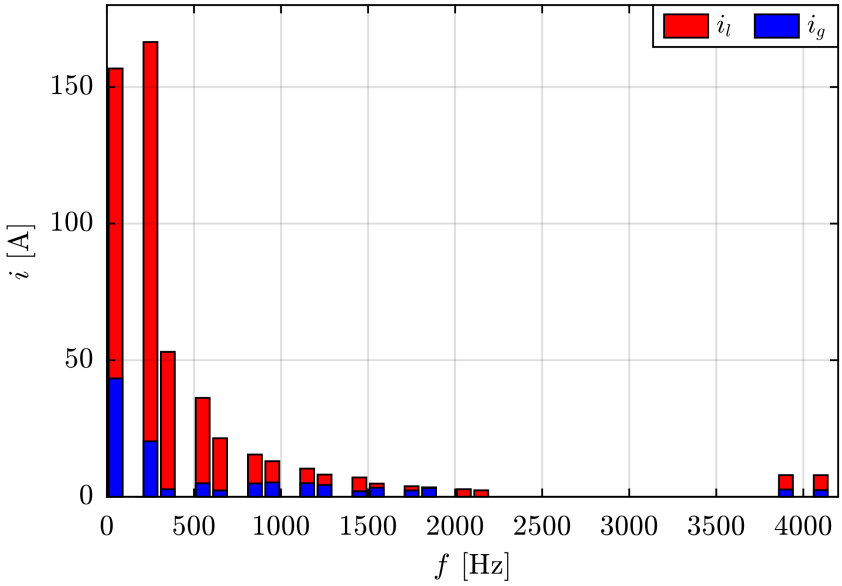


Fig. 6.16 Compensation capability of the APF, while the regenerative system is full-power operating. The currents i_l and i_g are shown in the frequency domain. A 4 kHz disturbance can be observed on i_l and, more attenuated, on i_g [129].

in multiple unwanted changes of the clamped phase within a single fundamental period, especially under the low-power conditions of Test 3 (Fig. 6.23). This side effect is fully eliminated by setting $\Delta i_{th} = 30$ A for all system operating conditions, with both the zero-sequence modulation index $m_c = \frac{v^*_{cm}}{Vdc/2}$ and the phase modulation index $m = \frac{v^*}{V_{dc}/2}$ exhibiting trends without repetitive abrupt deviations at the switching frequency. The primary advantage of implementing the hysteresis selector is the reduction of $i_{fg,h}$, thus mitigating the impact of the APF high-frequency ripple on the THD_i of the total current drawn at the PCC. Specifically, the RMS value of $i_{fg,h}$ decreases by 12.7 % in Test 1, 13.9 % in Test 2 and markedly by 41.5 % in Test 3.

The benefits of hysteresis selection on the CM voltage are illustrated in Fig. 6.19 for Test 1, Fig. 6.22 for Test 2, and Fig. 6.25 for Test 3. The harmonic spectrum is categorized into three distinct ranges:

- **Low frequency**: It contains the frequency components with $f \leq 1$ kHz, which are associated with the injection of the zero-sequence voltage;
- **Mid frequency**: It corresponds to the frequency range $f \in (1, 12]$ kHz, representing an intermediate region of the harmonic spectrum that typically exhibits low harmonic

content, as it is minimally affected by zero-sequence injection and lies below the switching frequency (f_{sw} = 16 kHz);

- **High frequency**: It includes all harmonics associated with the inverter switching, corresponding to $f > 12$ kHz.

Although the implementation of the hysteresis selector does not affect the overall CM RMS voltage V_{cm} and the high-frequency CM RMS voltage $V_{cm,hf}$, it influences the harmonic distribution within the low-frequency and mid-frequency ranges. Specifically, without the hysteresis selector, the low-frequency RMS content ($V_{cm,lf}$) decreases, as some harmonics associated with the zero-sequence injection shift to the mid-frequency range. Enabling the hysteresis selector confines these harmonics to the low-frequency range, thus reducing the system susceptibility to circulating CM currents. As a result, the mid-frequency CM RMS voltage ($V_{cm,mf}$) is reduced by 38.3 % in Test 1, 13.4 % in Test 2, and 72.9 % in Test 3.

The tests results are summarized in Table 6.3, which reports all relevant data for comparison in both absolute and relative terms.

6.6 Conclusion

This chapter introduces an enhanced discontinuous modulation technique (APF-GDPWM) specifically designed for APFs operating in disturbed environments. By incorporating a hysteresis-based selection mechanism into the zero-sequence voltage computation algorithm, the proposed approach effectively eliminates unwanted repetitive changes of the clamped phase, thus preventing side effects such as an increase of the high-frequency current ripple injected by the APF into the grid, the generation of high-frequency CM voltage components associated with zero-sequence voltage injection and the reduction of the converter efficiency.

The power device losses of the two-level APF are analytically evaluated based on the non-linear load THD_i and the APF operating current, considering both conventional CPWMs and the proposed APF-GDPWM. The analytical findings demonstrate that the proposed method effectively enhances the efficiency of the power converter, independently of the non-linear load characteristics.

Table 6.3 Experimental results with the method in [140] (i.e., Δi_{th} = 0 A) vs APF-GDPWM (i.e., Δi_{th} = 30 A).

Test	Notes	Quantity	Δi_{th} = 0 A	Δi_{th} = 30 A	
1	P_{CUT} =	**$I_{fg,h}$**	**7.9 A_{rms}**	**6.9 A_{rms}**	**-12.7 %**
	260 kW	$V_{cm,lf}$	137.9 V_{rms}	140.7 V_{rms}	+2.0 %
	THD_i =	**$V_{cm,mf}$**	**49.3 V_{rms}**	**30.4 V_{rms}**	**-38.3 %**
	34.3 %	$V_{cm,hf}$	193.4 V_{rms}	192.6 V_{rms}	-0.4 %
		V_{cm}	242.6 V_{rms}	240.5 V_{rms}	-0.9 %
2	P_{CUT} =	**$I_{fg,h}$**	**7.9 A_{rms}**	**6.8 A_{rms}**	**-13.9 %**
	135 kW	$V_{cm,lf}$	120.6 V_{rms}	122.4 V_{rms}	+1.5 %
	THD_i =	**$V_{cm,mf}$**	**58.2 V_{rms}**	**50.4 V_{rms}**	**-13.4 %**
	43.9 %	$V_{cm,hf}$	199.8 V_{rms}	201.1 V_{rms}	+0.7 %
		V_{cm}	240.5 V_{rms}	240.8 V_{rms}	+0.1 %
3	P_{CUT} =	**$I_{fg,h}$**	**9.4 A_{rms}**	**5.5 A_{rms}**	**-41.5 %**
	28 kW	$V_{cm,lf}$	56.3 V_{rms}	84.5 V_{rms}	+50.1%
	THD_i =	**$V_{cm,mf}$**	**89.4 V_{rms}**	**24.2 V_{rms}**	**-72.9 %**
	106.7 %	$V_{cm,hf}$	221.9 V_{rms}	227.7 V_{rms}	+2.6 %
		V_{cm}	245.8 V_{rms}	242.2 V_{rms}	-1.5 %

Subsequently, the high-frequency output current distortion of an APF implementing the APF-GDPWM is analyzed and compared with that obtained using SVPWM. The results indicate that, under equal inverter efficiency, the APF-GDPWM achieves a reduction in both the high-frequency peak-to-peak and RMS flux components, thus supporting a more effective and compact design of the DM LCL filter.

The experimental validation was carried out on a TRL 9 industrial two-level IGBT-based APF, compensating the distorted current drawn by a regenerative testing system of 400 V, 260 kVA industrial AC–AC power converters. Experimental tests conducted in a real disturbed industrial environment validate the effectiveness of incorporating a hysteresis selector within the APF-GDPWM scheme, as opposed to the method presented in [140], which lacks this feature. Indeed, compared to the solution in [140], the APF-GDPWM reduces both the APF current ripple injected into the grid and the high-frequency CM voltage components associated with the zero-sequence voltage, thus mitigating the risk of circulating CM currents.

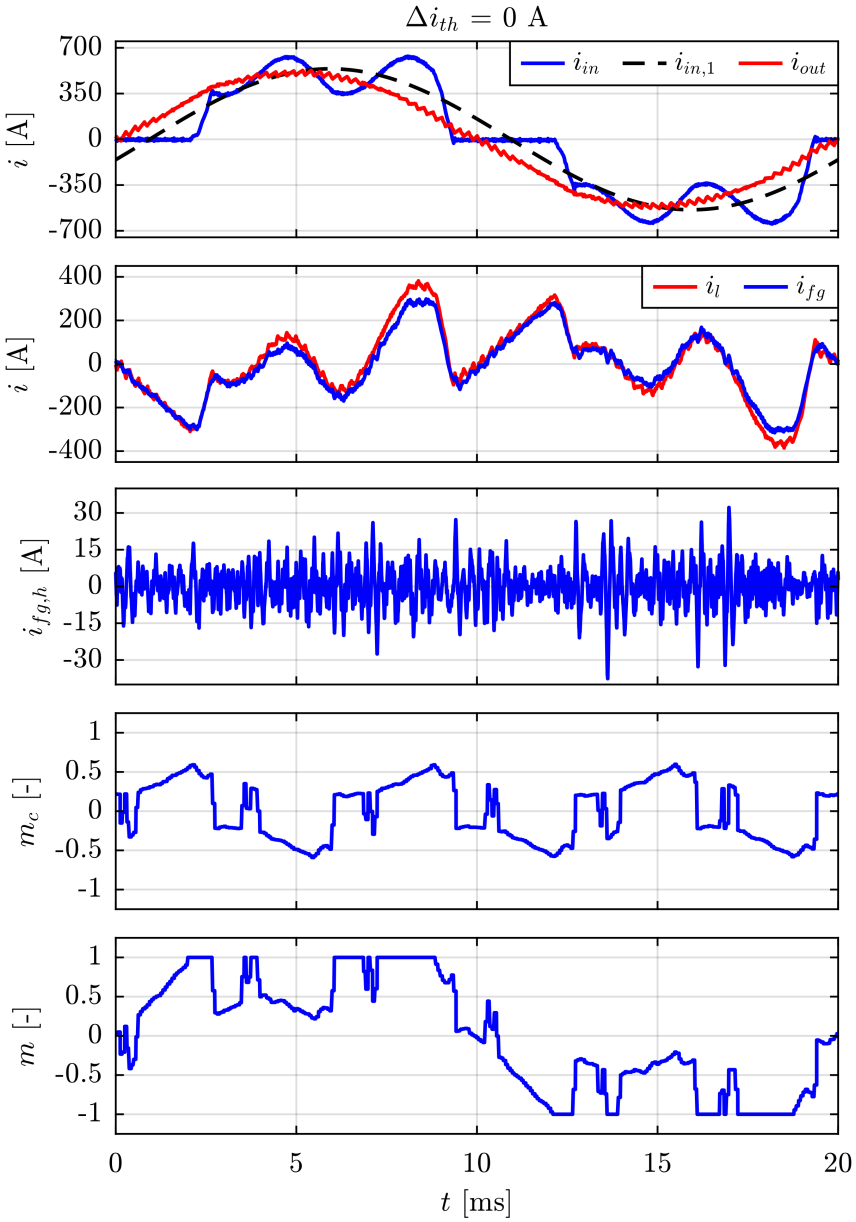


Fig. 6.17 Test 1: system steady-state operation while the CUT is providing full-power (P_{CUT} = 260 kW). The APF is implementing APF-GDPWM with f_{sw} = 16 kHz in the case of hysteresis selector disabled. From top to bottom: CUT input current i_{in} and its fundamental component $i_{in,1}$, CUT output current i_{out}, current absorbed by the regenerative system i_l, current injected by the APF at the PCC i_{fg}, residual APF current ripple injected at the PCC $i_{fg,h}$, zero-sequence modulation index m_c and phase modulation index m [129].

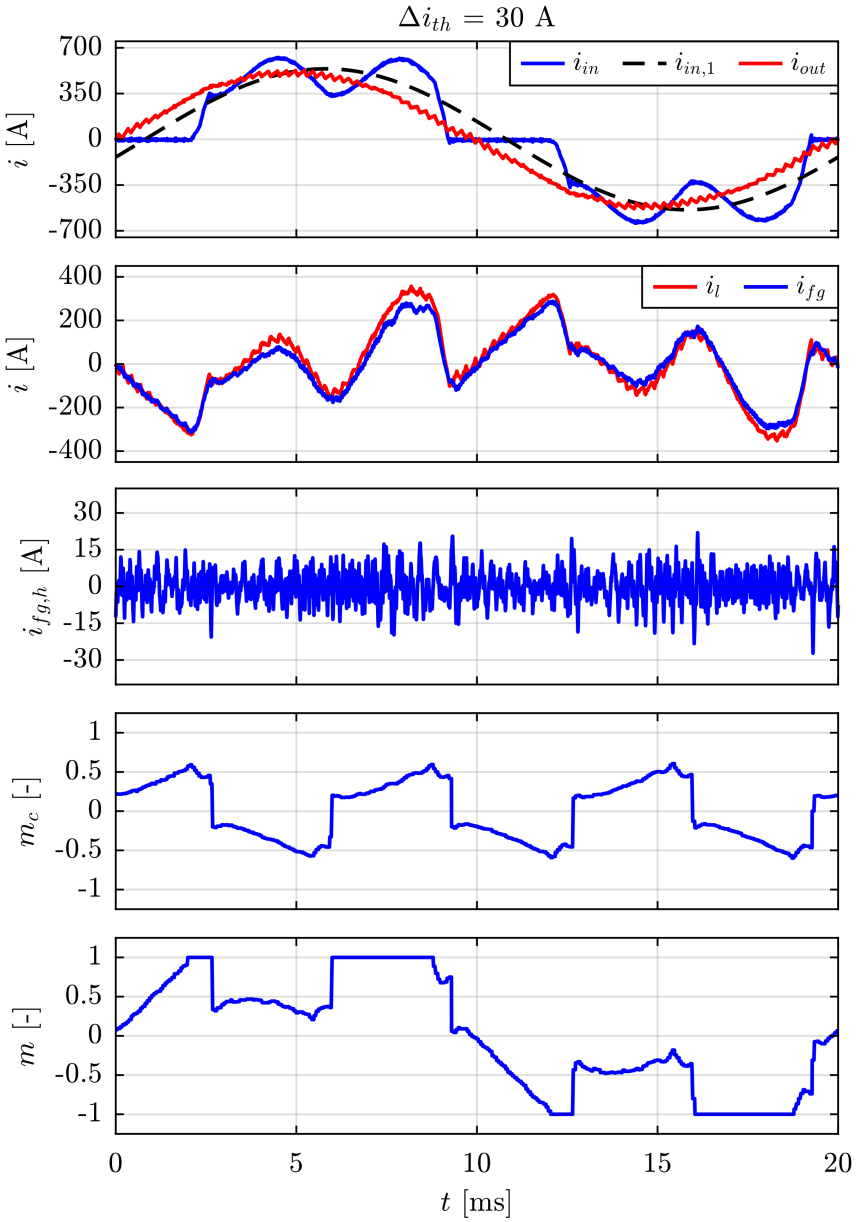


Fig. 6.18 Test 1: system steady-state operation while the CUT is providing full-power (P_{CUT} = 260 kW). The APF is implementing APF-GDPWM with f_{sw} = 16 kHz in the case of hysteresis selector enabled with Δi_{th} = 30 A. From top to bottom: CUT input current i_{in} and its fundamental component $i_{in,1}$, CUT output current i_{out}, current absorbed by the regenerative system i_l, current injected by the APF at the PCC i_{fg}, residual APF current ripple injected at the PCC $i_{fg,h}$, zero sequence modulation index m_c and phase modulation index m [129].

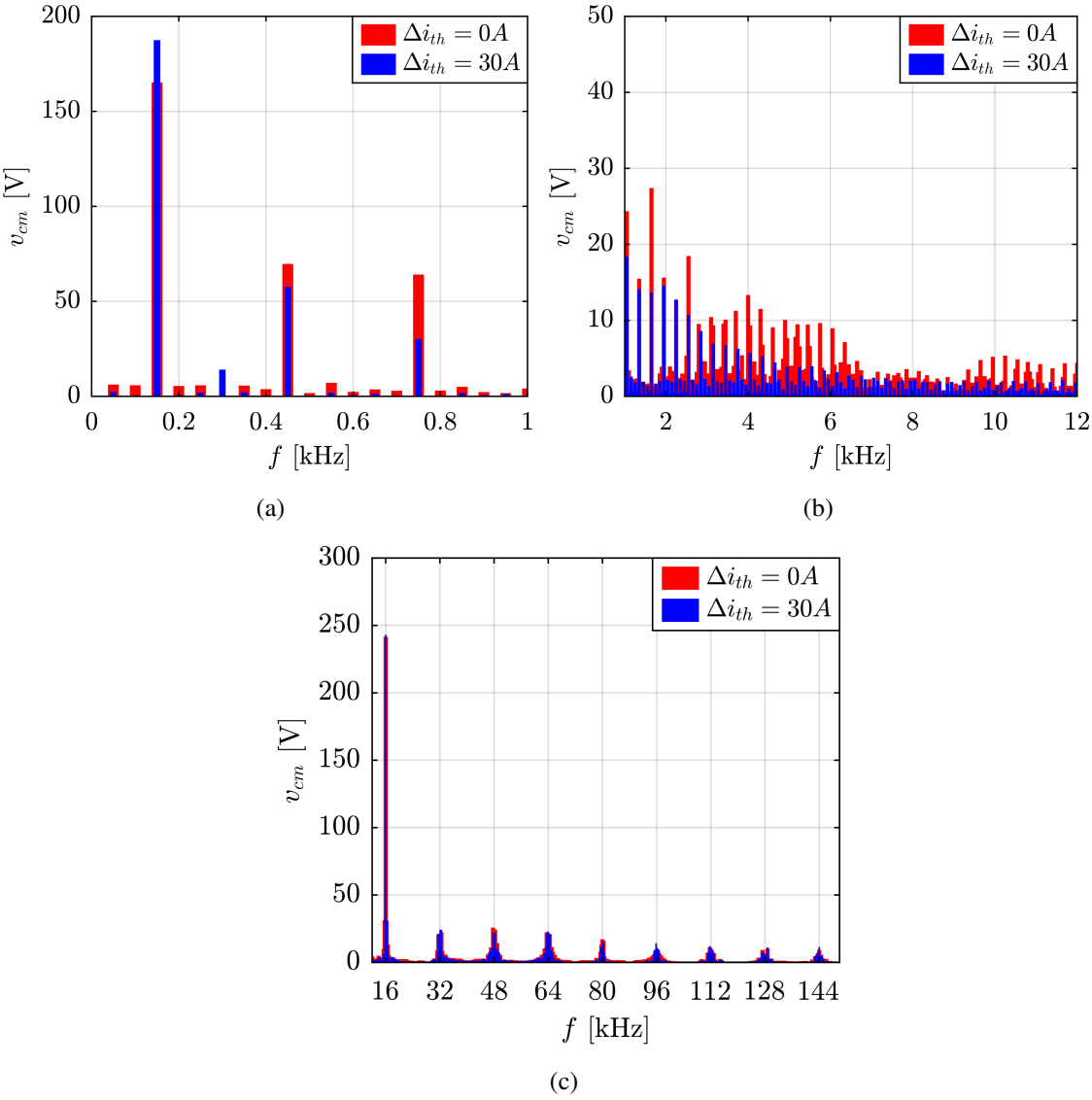


Fig. 6.19 Test 1: system steady-state operation while the CUT is providing full-power (P_{CUT} =260 kW). CM voltage v_{cm} harmonic spectrum in the low frequency (a), mid frequency (b) and high frequency (c) ranges [129].

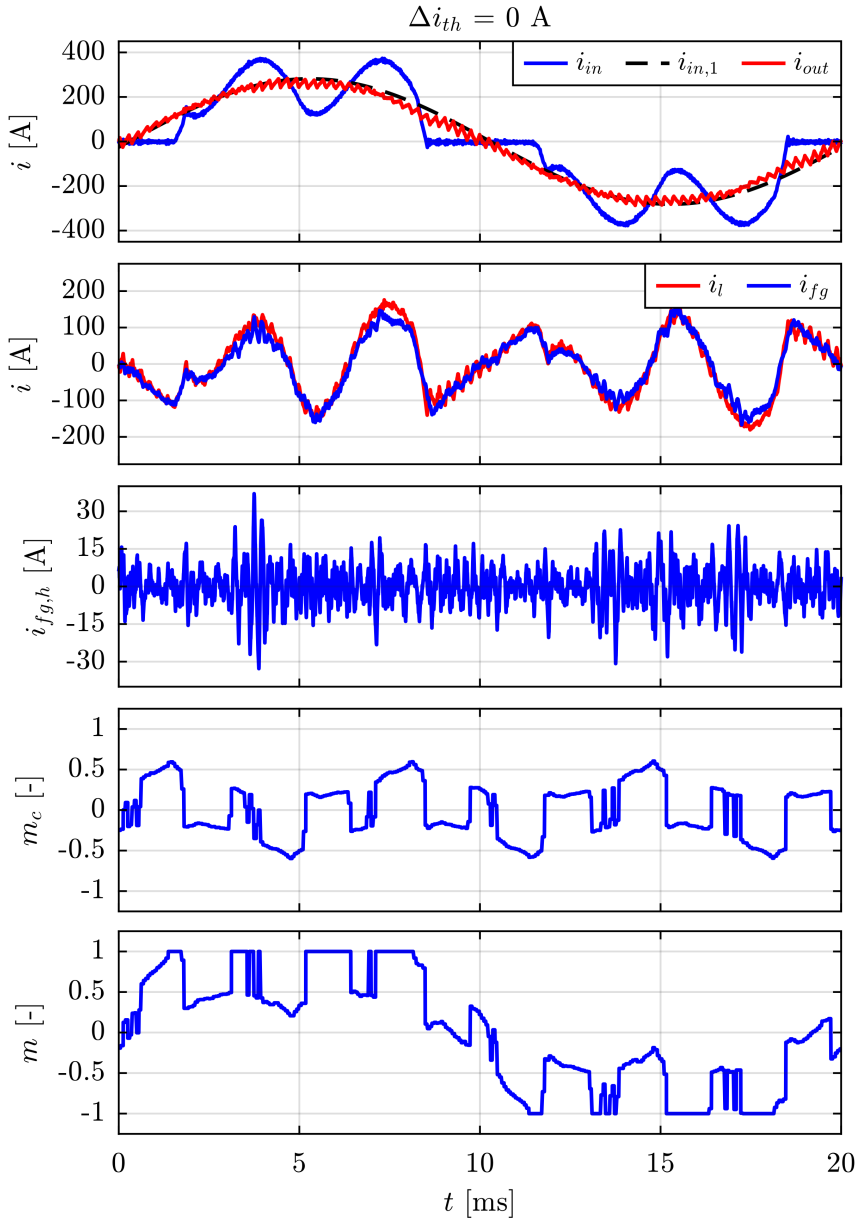


Fig. 6.20 Test 2: system steady-state operation while the CUT is providing half-power (P_{CUT} = 135 kW). The APF is implementing APF-GDPWM with f_{sw} = 16 kHz in the case of hysteresis selector disabled. From top to bottom: CUT input current i_{in} and its fundamental component $i_{in,1}$, CUT output current i_{out}, current absorbed by the regenerative system i_l, current injected by the APF at the PCC i_{fg}, residual APF current ripple injected at the PCC $i_{fg,h}$, zero-sequence modulation index m_c and phase modulation index m.

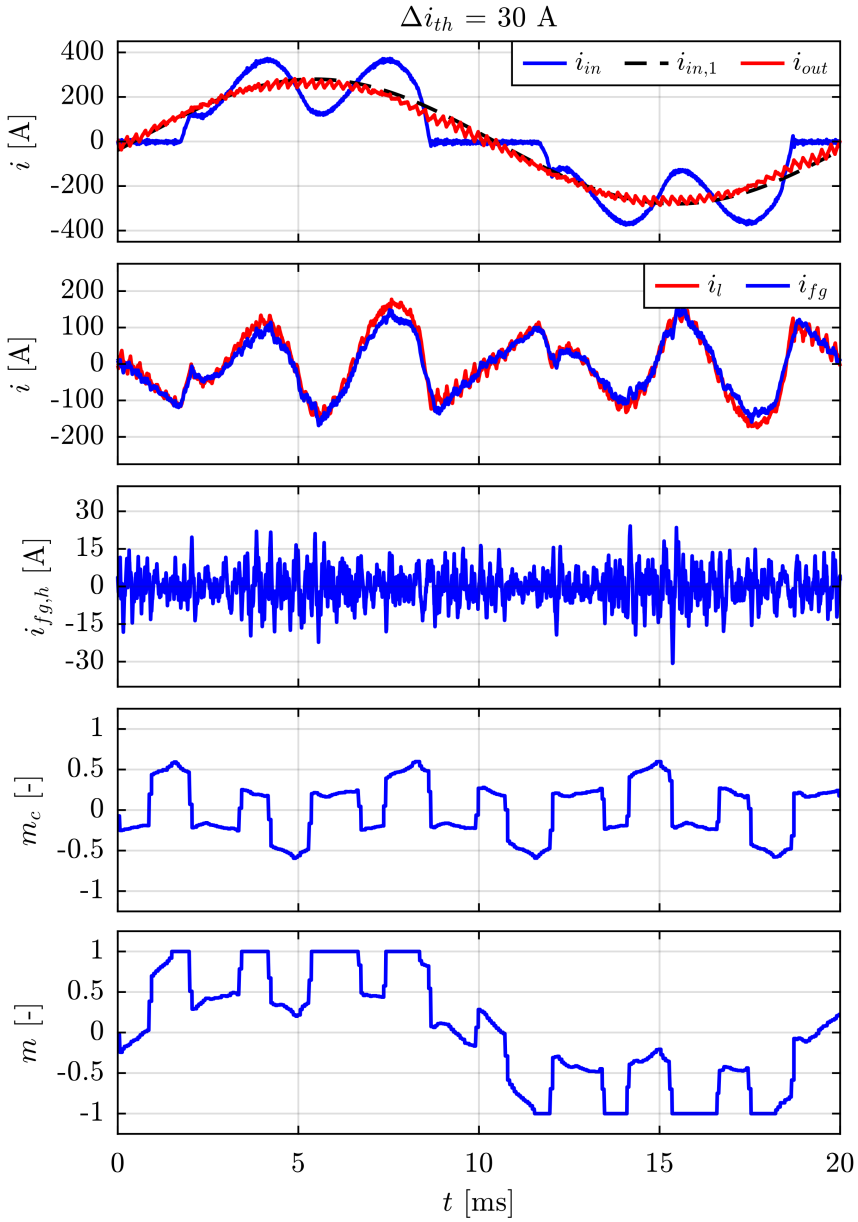


Fig. 6.21 Test 2: system steady-state operation while the CUT is providing half-power (P_{CUT} = 135 kW). The APF is implementing APF-GDPWM with f_{sw} = 16 kHz in the case of hysteresis selector enabled with Δi_{th} = 30 A. From top to bottom: CUT input current i_{in} and its fundamental component $i_{in,1}$, CUT output current i_{out}, current absorbed by the regenerative system i_l, current injected by the APF at the PCC i_{fg}, residual APF current ripple injected at the PCC $i_{fg,h}$, zero sequence modulation index m_c and phase modulation index m.

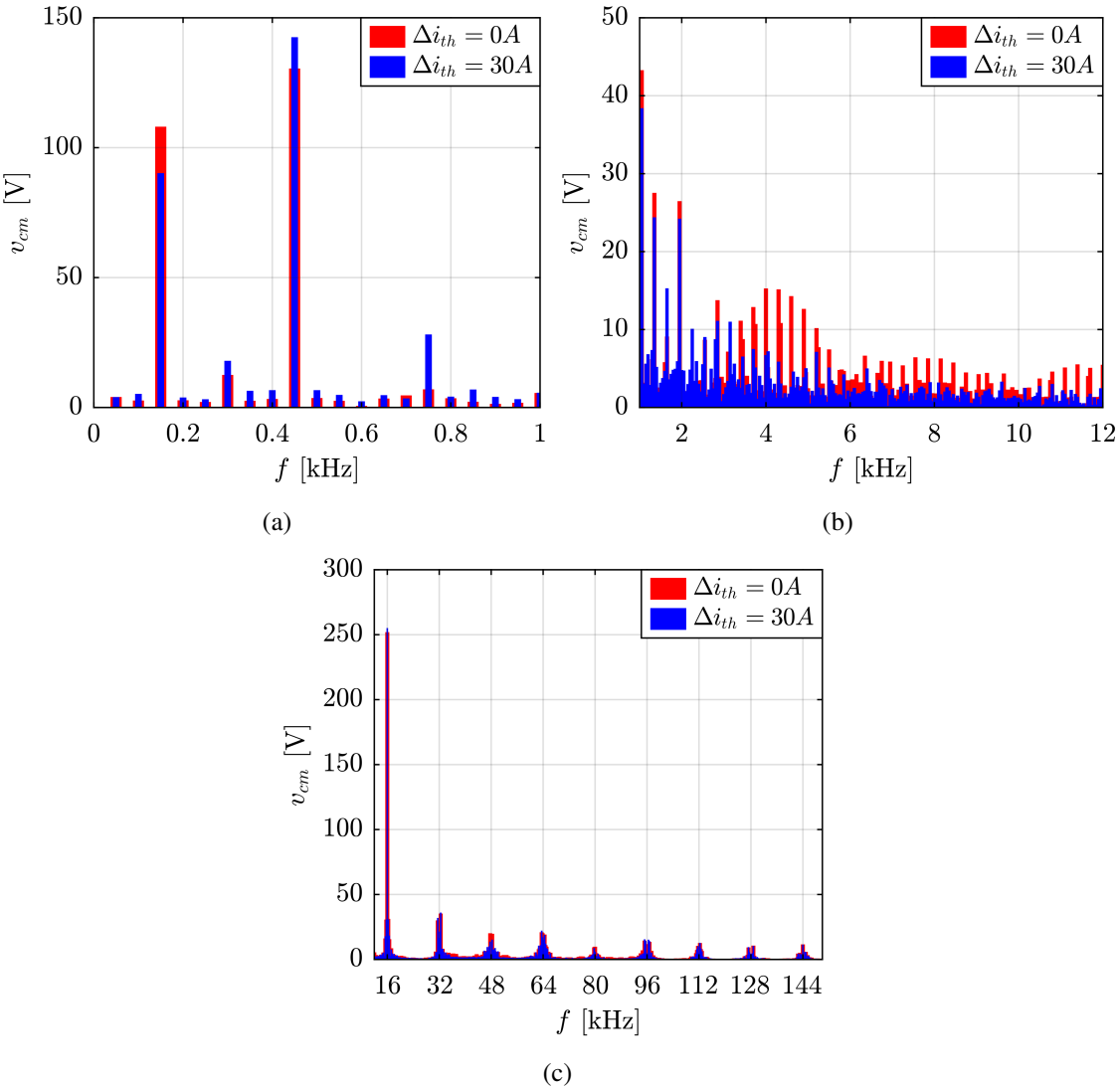


Fig. 6.22 Test 2: system steady-state operation while the CUT is providing half-power (P_{CUT} =135 kW). CM voltage v_{cm} harmonic spectrum in the low frequency (a), mid frequency (b) and high frequency (c) ranges.

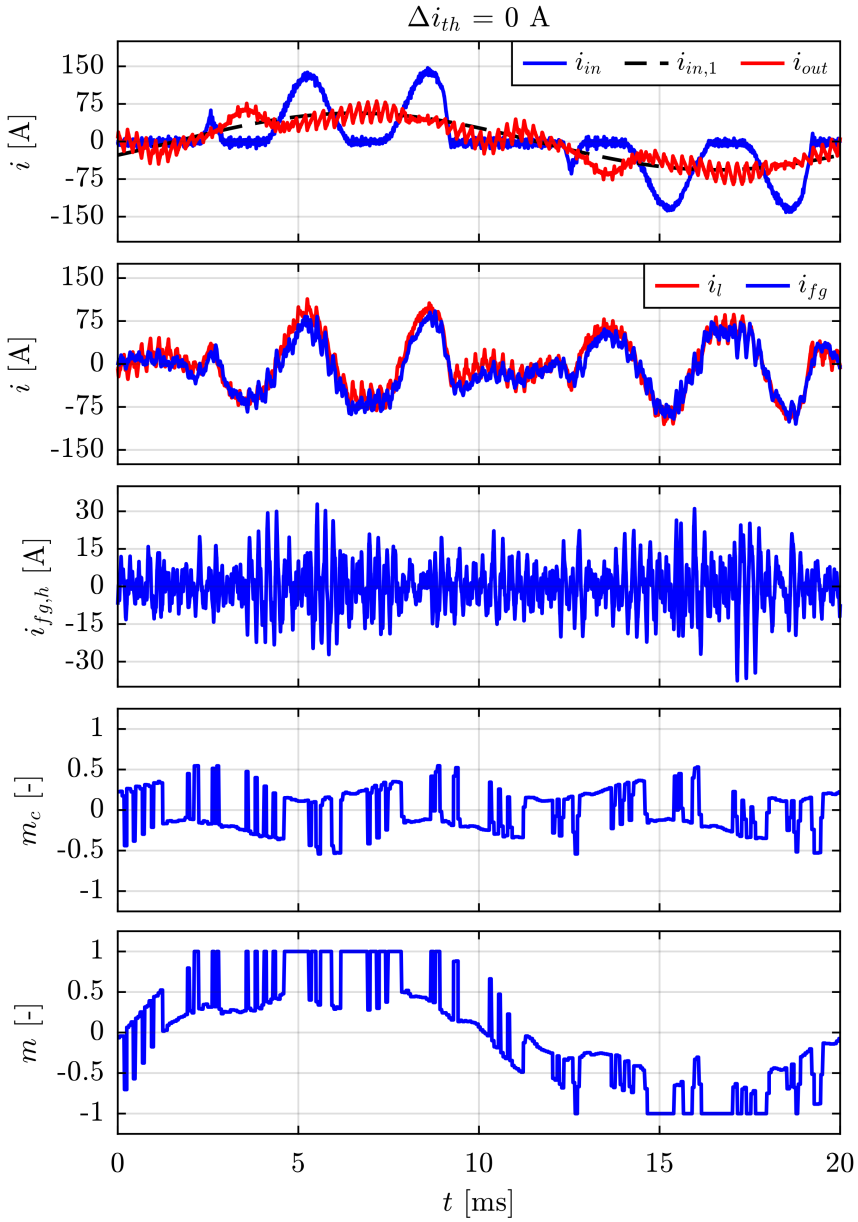


Fig. 6.23 Test 3: system steady-state operation while the CUT is providing one-tenth-power (P_{CUT} =28 kW). The APF is implementing APF-GDPWM with f_{sw} = 16 kHz in the case of hysteresis selector disabled. From top to bottom: CUT input current i_{in} and its fundamental component $i_{in,1}$, CUT output current i_{out}, current absorbed by the regenerative system i_l, current injected by the APF at the PCC i_{fg}, residual APF current ripple injected at the PCC $i_{fg,h}$, zero sequence modulation index m_c and phase modulation index m [129].

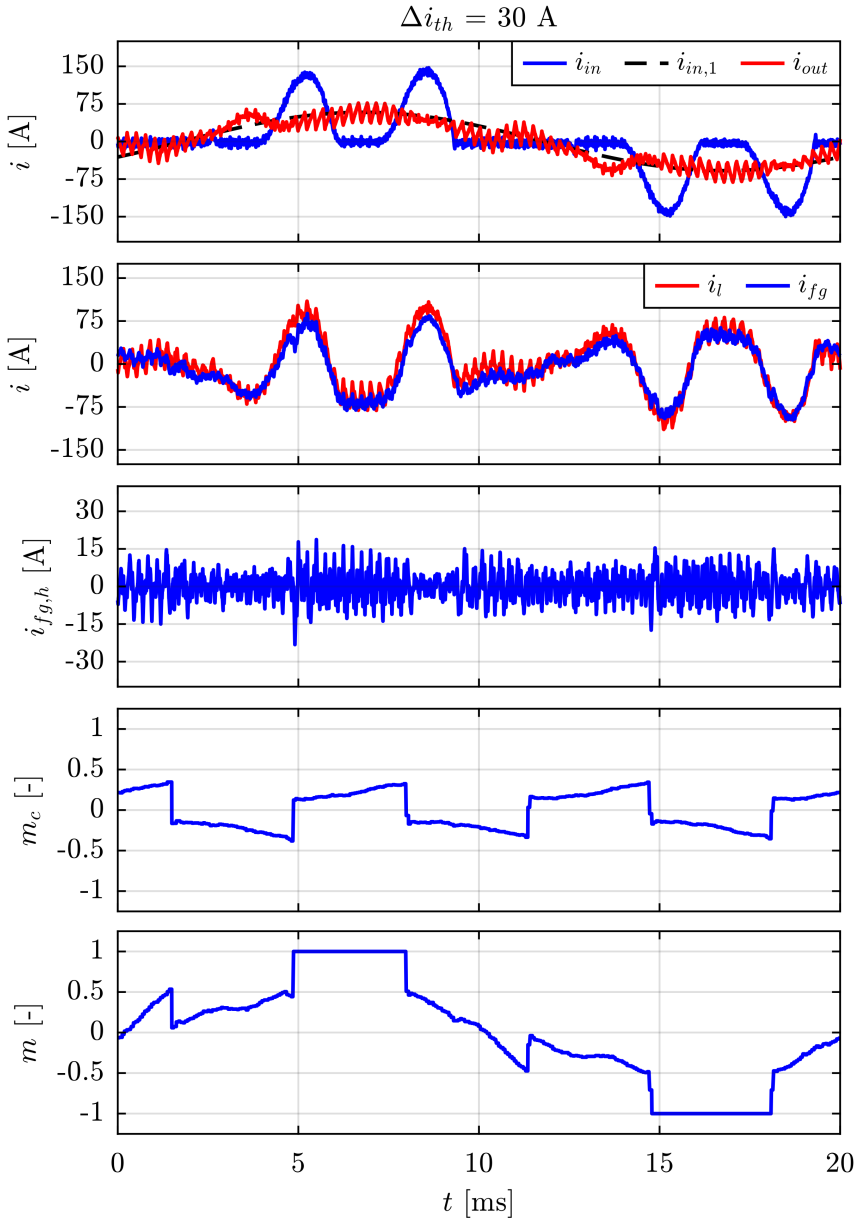


Fig. 6.24 Test 3: system steady-state operation while the CUT is providing one-tenth-power (P_{CUT} =28 kW). The APF is implementing APF-GDPWM with f_{sw} = 16 kHz in the case of hysteresis selector enabled with Δi_{th} = 30 A. From top to bottom: CUT input current i_{in} and its fundamental component $i_{in,1}$, CUT output current i_{out}, current absorbed by the regenerative system i_l, current injected by the APF at the PCC i_{fg}, residual APF current ripple injected at the PCC $i_{fg,h}$, zero-sequence modulation index m_c and phase modulation index m [129].

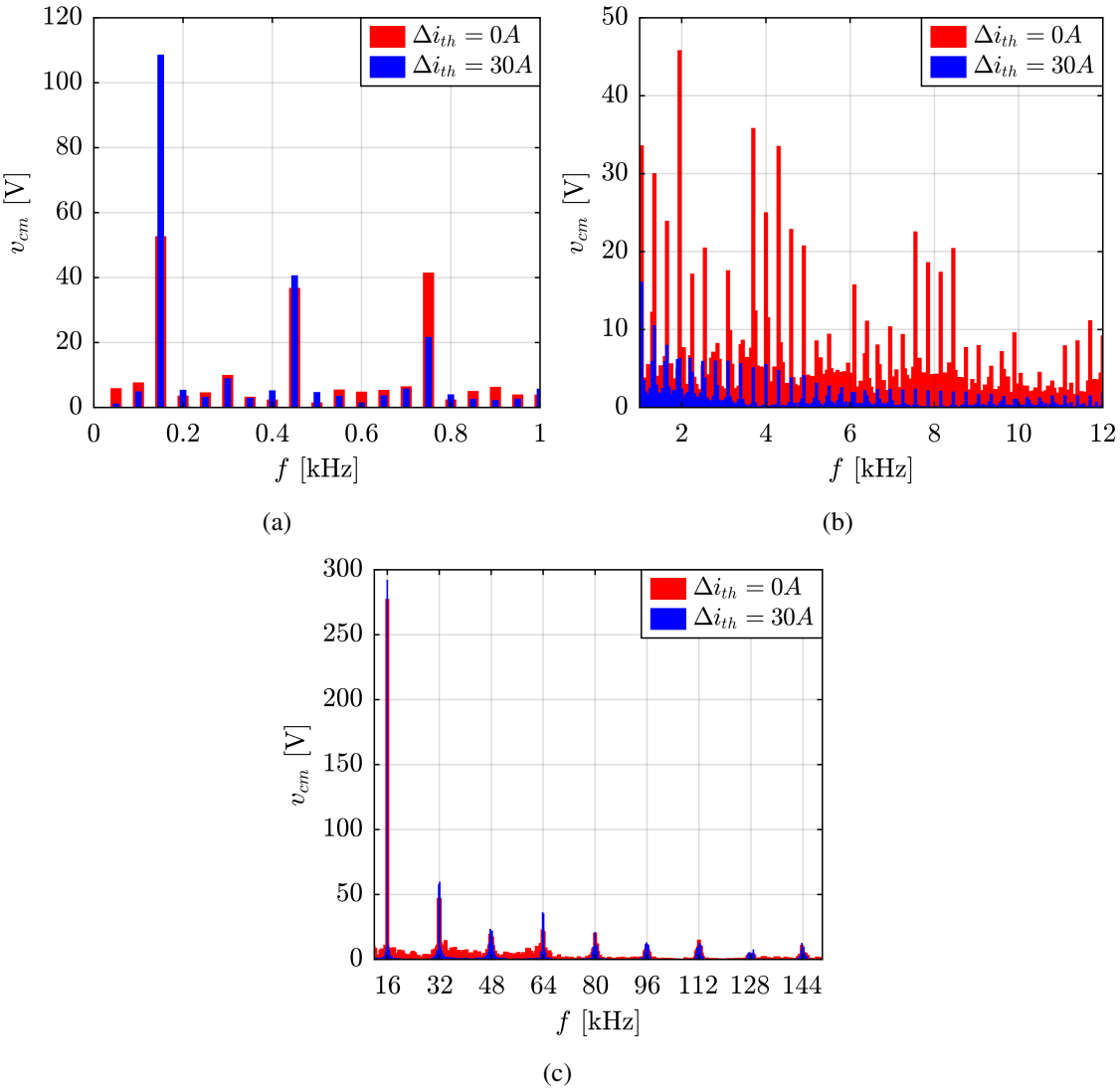


Fig. 6.25 Test 3: system steady-state operation while the CUT is providing one-tenth-power (P_{CUT} =28 kW). CM voltage v_{cm} harmonic spectrum in the low frequency (a), mid frequency (b) and high frequency (c) ranges [129].

Chapter 7

Design Procedure for Differential-Mode LCL Filters in APFs

This chapter proposes a step-by-step procedure for designing the grid-interfacing DM LCL filter of an APF. This chapter is organized as follows:

- The introductory section highlights the role of the DM LCL filter in attenuating high-frequency current ripple in grid-tied inverters. Furthermore, a literature review of DM LCL filter design procedures, both for AFEs and APFs, is provided. It is thus demonstrated that the design procedures developed for AFEs are overly restrictive when applied to APFs, while procedures specifically developed for APFs tend to oversize the DM LCL filter, with negative implications for its cost and volume. This justifies the need for a new design procedure for the DM LCL filter in APF applications;
- Preliminary considerations on the DM LCL filter are discussed to establish the relationships necessary for the design phase;
- The proposed procedure is thus presented, providing a detailed description of the filter parameters calculations and the subsequent validation checks, which verify both proper filtering performance and the filter non-interference with the APF low-frequency harmonic control;
- Two design examples are presented for a two-level APF: in one case employing SVPWM with f_{sw} = 8 kHz and in the other using APF-GDPWM with f_{sw} = 16 kHz;

- Experimental tests are carried out to compare the performance of an APF implementing APF-GDPWM and SVPWM, while interchanging the grid-interfacing DM LCL filters designed through the proposed procedure;
- The final section presents the conclusions and emphasizes the main contributions of the work.

The contributions discussed in this chapter were published in [129].

7.1 Research Context & Motivation

A proper design of the DM grid-interfacing filter is required for every grid-connected power converters to ensure the compliance with current harmonic restrictions at the PCC [13]. The filter role is to attenuate the high-frequency current harmonics caused by inverter switching, which are strictly linked to the implemented modulation technique and the resulting flux ripple λ_h, as demonstrated in Chapter 6. As reported in the literature, the LCL filter represents the most widely adopted topology for power applications exceeding a few kilowatts [39], [147]. In comparison with a conventional L filter and for an equivalent total inductance, the LCL structure can achieve up to three times greater attenuation at high frequencies [147], [148], [149], thus offering a more compact and economically efficient solution.

Given the critical role of the DM LCL filter, numerous design methodologies have been proposed in the literature for grid-connected inverters [39], [147], [148], [149], [150] and, more specifically, for APFs [113], [114], [115], [116]. However, the design criteria established for inverters and rectifiers prove overly stringent when applied to APFs, particularly with respect to resonant frequency constraints [115]. In particular, design procedures for APFs emphasize the proper placement of the resonance frequency to guarantee both proper compensation of low-order harmonics via APF control and effective suppression of switching-induced ripple components.

The methods presented in [113], [115] and [116] do not account for the fact that the APF switching ripple should be evaluated on the total current drawn by the system at the PCC (i_g in Fig. 5.1), which depends on both the APF and the non-linear load currents. Instead, the above-mentioned design procedures constrain the ripple relative to the APF compensation current (i_{fg}), resulting in filter oversizing with significant implications for

cost and volume. The design procedure proposed in [114] appropriately sizes the APF LCL filter based on the line current at the PCC. However, it does not provide detailed guidelines for selecting the specific values of the inductances and capacitance.

Motivated by the limitations of existing solutions in the literature, this chapter presents a straightforward step-by-step procedure for designing the DM LCL filter of an APF. The results of the design procedure depend on both:

- The operating condition of the APF, i.e., the chosen PWM technique, the modulation index M, the switching frequency f_{sw} and the highest harmonic component to be compensated h;
- The characteristics of the non-linear load, i.e., the rated power P_l, the fundamental component of the load current $i_{l,1}$ and the load current total harmonic distortion THD_i.

7.2 Preliminary Considerations

The high-frequency single-phase equivalent circuit of the DM LCL filter connecting the APF to the grid is depicted in Fig. 7.1. During the preliminary design stages, the damping resistance R_f is neglected. The grid impedance is modeled as a grid inductance L_g, which can be considered as an additional inductor in series with the LCL filter, enhancing its high-frequency attenuation. However, its value is typically unknown beforehand, since it depends on the APF installation location and can vary considerably during operation [76]. Therefore, to adopt a conservative design approach, L_g is neglected in the proposed procedure. The system transfer functions employed for the filter design are listed below:

$$Y_f(s) = \frac{i_f(s)}{v_h(s)} = \frac{1}{sL_f} \cdot \frac{s^2 + \omega_f^2}{s^2 + \omega_0^2} \tag{7.1}$$

$$Y_{fg}(s) = \frac{i_{fg}(s)}{v_h(s)} = \frac{1}{s(L_f + L_{fg})} \cdot \frac{\omega_0^2}{s^2 + \omega_0^2} \tag{7.2}$$

$$\omega_f^2 = \frac{1}{C_f L_{fg}} \tag{7.3}$$

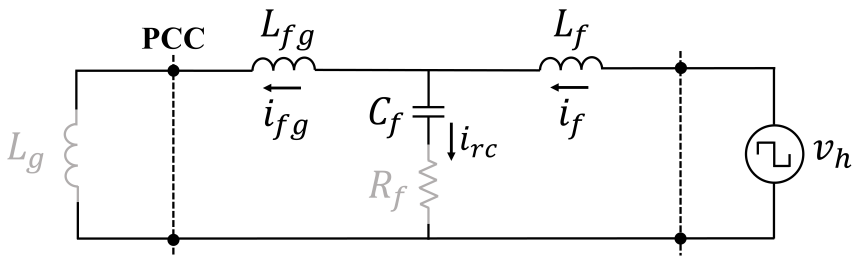


Fig. 7.1 High-frequency single-phase equivalent circuit of the LCL filter interfacing the APF to the grid. The grid inductance L_g and the damping resistance R_f are neglected and are thus shown in grey [129].

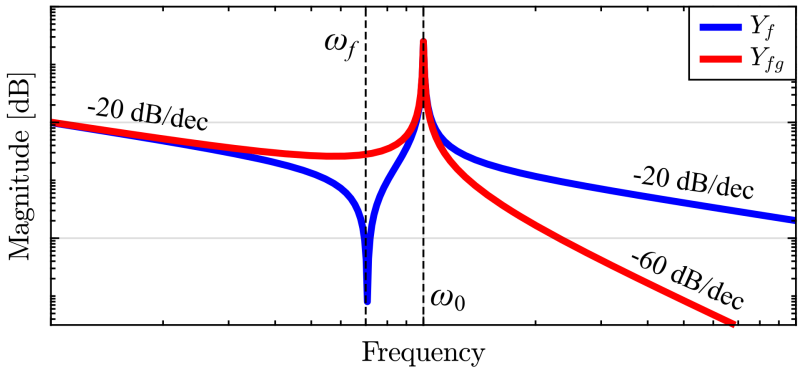


Fig. 7.2 Qualitative representation in the logarithmic scale of the magnitude of the admittances $Y_f(s)$ and $Y_{fg}(s)$ in case of negligible damping resistance R_f. The resonance frequency ω_0 and anti-resonance frequency ω_f are reported in the graph with the attenuation characteristics of the LCL filter [129].

$$\omega_0^2 = \frac{L_f + L_{fg}}{C_f L_f L_{fg}} \tag{7.4}$$

where the admittances Y_f and Y_{fg} relate, respectively, the APF-side (i_f) and grid-side (i_{fg}) currents to the ripple voltage (v_h), with their qualitative trends illustrated in Fig. 7.2; ω_0 and ω_f denote the system resonance and anti-resonance frequencies, respectively, which depend on the APF-side inductance L_f, grid-side inductance L_{fg}, and capacitance C_f. To improve scalability and applicability, the procedure is expressed in per-unit, with the base values defined as follows:

$$Z_b = \frac{V_b^2}{S_b} \tag{7.5}$$

$$L_b = \frac{Z_b}{\omega_b} \tag{7.6}$$

$$C_b = \frac{1}{\omega_b \cdot Z_b} \tag{7.7}$$

where ω_b, V_b and S_b are the grid base frequency, phase-to-phase base voltage and power, respectively.

7.3 Proposed Design Procedure

The grid is considered to operate at its nominal voltage and frequency (i.e., $\omega_g = e_g = 1$ pu), while the non-linear load is assumed to run at full-power (i.e., $P_l = 1$ pu). The design procedure involves the following computations, to be executed sequentially as listed:

- **APF-Side Inductance L_f:** The parameter is selected to minimize the current stress on the semiconductor devices, thus limiting the peak current in accordance with the rating current of the power switches. Consequently, the maximum peak-to-peak current ripple $i_{f,h,pp\ max}$ is constrained as follows:

  $$i_{f,h,pp\ max} = k_{L_f} \cdot I_{l,1} \tag{7.8}$$

  where $I_{l,1}$ denotes the load peak fundamental current and k_{L_f} is an attenuation factor, recommended to lie within the range of 20–30 %.

  As in (6.13), $i_{f,h,pp\ max}$ is influenced by both L_f and $\lambda_{h,pp\ max}$, with the latter depending on the modulation index M and the chosen PWM technique, as depicted in Fig. 6.11. Accordingly, the following per-unit expression for the inductance L_f can be obtained by combining (6.17), (6.18), (7.6), and (7.8):

  $$L_f = \frac{2\pi}{3} \cdot \frac{\lambda_{h,pp\ max}}{\omega_{sw} \cdot M \cdot k_{L_f}} \tag{7.9}$$

- **Capacitance C_f:** When the APF is connected to the grid but remains disabled, the reactive power generated by C_f (Q_c) must not degrade the power factor at the PCC beyond an acceptable threshold. Consequently, the following constraint is imposed:

$$Q_{c,max\ OFF} = k_{C_{f,OFF}} \cdot P_l = k_{C_{f,OFF}} \tag{7.10}$$

where $Q_{c,max\ OFF}$ denotes the maximum allowable reactive power generated by C_f when the APF is in the idle state and $k_{C_{f,OFF}}$ is a percentage coefficient suggested within the range of 3–5 %, that relates $Q_{c,max\ OFF}$ to the load active power P_l.

During normal operation, the APF can compensate for Q_c through a feedforward control action. Nevertheless, the corresponding power effort must remain limited, as the majority of the APF rated power S_{apf} should be allocated to line current compensation. Assuming that the APF rated current I_{apf} equals the load distorted current $I_{l,d} = I_{l,1} \cdot THD_i$, a second constraint on Q_c can thus be defined:

$$Q_{c,max\ ON} = k_{C_{f,ON}} \cdot S_{apf} = k_{C_{f,ON}} \cdot THD_i \tag{7.11}$$

where $Q_{c,max\ ON}$ denotes the maximum admissible value of Q_c that can be compensated in feedforward mode by the APF and $k_{C_{f,ON}}$ is a percentage factor suggested in the range of 3–5 % relating $Q_{c,max\ ON}$ to S_{apf}.

Since, in per-unit terms, $C_f \simeq Q_c$, an expression for the computation of C_f can be derived by combining (7.10)–(7.11):

$$C_f = \min\left(k_{C_{f,OFF}}, k_{C_{f,ON}} \cdot THD_i\right) \tag{7.12}$$

In practice, $k_{C_{f,OFF}}$ and $k_{C_{f,ON}}$ are typically set to identical values. Consequently, the most restrictive condition between (7.10) and (7.11) depends solely on the load input THD_i.

- **Grid-Side Inductance L_{fg}:** Once L_f and C_f have been determined, the value of L_{fg} can be calculated following the approach in [39], by combining (7.1)–(7.2) and imposing the desired current ripple attenuation factor $k_{L_{fg}} = \left|i_{fg}(s)/i_f(s)\right|$ at the switching frequency f_{sw}. The resulting per-unit expression is therefore obtained as follows:

$$L_{fg} = \frac{\left(1 + \frac{1}{k_{L_{fg}}}\right) \cdot L_f}{L_f \cdot C_f \cdot \omega_{sw}^2 - 1} \tag{7.13}$$

The attenuation coefficient $k_{L_{fg}}$ is recommended to lie within the range of 10–20 %, with its specific value depending on the adopted PWM strategy. As illustrated in Fig. 6.9, different PWM techniques exhibit distinct HDF values and, consequently, different RMS current ripple $I_{fg,h}$. For an equivalent impact on the THD_i measured at the PCC, a modulation technique characterized by a higher HDF requires a lower value of $k_{L_{fg}}$. For example, since $HDF \propto I_{fg,h}^2$, the attenuation factors corresponding to the APF-GDPWM and SVPWM can be related as follows:

$$k_{L_{fg,APF-GDPWM}} = k_{L_{fg,SVPWM}} \cdot \sqrt{\frac{HDF_{SVPWM}}{HDF_{APF-GDPWM}}} \tag{7.14}$$

- **Damping Resistance R_f:** The inclusion of a damping resistor R_f in the LCL filter is necessary to mitigate current oscillations at the resonance frequency, which arise from the zero impedance condition at ω_0. Typically, the value of R_f is chosen to be proportional to the capacitive reactance, as suggested in [148], [149], according to the following relation:

$$R_f = \frac{1}{3\omega_0 C_f} \tag{7.15}$$

The suppression of resonant oscillations can be achieved either through the physical insertion of a damping resistor or by integrating into the APF current control one of the active damping algorithms proposed in the literature [114], [151], [152], [153], which emulate the required resistive behavior by means of a virtual resistance. With the active damping approach, the use of a physical resistor is avoided, resulting in a notable reduction of overall filter losses. However, a passive damping solution is employed in this work to prevent the APF current control from being directly involved in the filter design, thus simplifying the analysis.

Once the filter inductive (L_f and L_{fg}), capacitive (C_f) and resistive (R_f) components have been determined, the following constraints are verified to prevent resonant behavior, ensure the proper low-frequency current compensation performed by the APF control, minimize the impact on power line consumption and guarantee compliance with regulatory limits on harmonic distortion at the PCC:

- **Resonance Frequency ω_0:** The upper limit for ω_0 reported in the literature [39], [113], [114], [115], [116], [147], [148], [149], [150] is set to one-half of ω_{sw} to prevent undesired amplification of switching harmonics:

$$\omega_0 \leq \frac{\omega_{sw}}{2} \tag{7.16}$$

  If (7.16) is not satisfied, ω_0 can be reduced by increasing L_f, C_f, or L_{fg}, as indicated by (7.4);

- **Anti-Resonance Frequency ω_f:** The APF harmonic compensation performance can be compromised if ω_f is sufficiently low to interact with the highest-order harmonic that the APF is required to mitigate. To prevent limitations in current control, the following constraint is imposed:

$$\omega_f \geq 2h \cdot \omega_g \tag{7.17}$$

  If the constraint in (7.17) is violated, C_f or L_{fg} must be reduced in accordance with (7.3);

- **Damping Resistors Losses P_d:** LCL filter losses must be limited to reduce their impact on overall power line consumption. Specifically, P_d should not exceed a set proportion $k_{P_d,l}$ of the load rated power P_l. At the same time, P_d must remain within limits that prevent excessive stress on the APF cooling system (heatsink and fans), meaning it should also stay below a defined fraction $k_{P_d,apf}$ of the APF nominal power S_{apf}. Accordingly, the following constraint is applied:

$$P_d \leq \min\left(k_{P_d,l}, k_{P_d,apf} \cdot THD_i\right) \tag{7.18}$$

  where $P_d = 3R_f I_{rc}$, with I_{rc} denoting the RMS current flowing through the capacitor C_f.

  A recommended value for both $k_{P_d,l}$ and $k_{P_d,apf}$ is 1 %. If condition (7.18) is not satisfied, R_f must be reduced by increasing either ω_0 or C_f, in accordance with (7.15). Alternatively, I_{rc} can be limited by increasing L_f, thus improving the high-frequency current filtering provided by the converter-side inductor.

- **Current Ripple $I_{fg,h}$:** The residual current ripple from the APF injected at the PCC should not significantly affect the THD_i of the overall grid current (i_g in

Fig. 5.1). The LCL filter must provide sufficient high-frequency attenuation to ensure compliance with harmonic distortion standards [13], which set a maximum limit of $THD_i \leq 5$ % for weak grids ($SCR < 20$). Since the APF installation location is not predetermined and the SCR is therefore unknown a priori, $I_{fg,h}$ is required to satisfy the worst-case scenario with an additional 50 % margin, accounting for partial low-frequency current compensation performed by the APF control, as well as unmodeled effects and component tolerances:

$$I_{fg,h} \leq 2.5\% \tag{7.19}$$

If the constraint in (7.19) is not met, L_f, C_f, or L_{fg} must be increased to enhance the filter high-frequency attenuation.

7.4 Design Examples

The procedure described above is applied to design the LCL filter for a two-level APF, considering the implementation of SVPWM with f_{sw} = 8 kHz (Filter 1) and APF-GDPWM with f_{sw} = 16 kHz (Filter 2), respectively. Table 7.1 reports the system base values, the operating characteristics of both the APF and the non-linear load and the indices used for designing the LCL filters. Once the modulation index is set (i.e., $M = 0.9$), the corresponding values of HDF and $\lambda_{h,pp\ max,pu}$ for the design stage can be determined from Fig. 6.9 and Fig. 6.11, respectively, according to the selected modulation technique.

Table 7.2 lists the calculated parameters (L_f, C_f, L_{fg}, and R_f) for both Filter 1 and Filter 2, along with the switching frequency f_{sw}, the selected modulation technique and the corresponding PWM waveform quality indices HDF and $\lambda_{h,pp\ max}$. The table also reports the resulting values of ω_0, ω_f, P_d, and $I_{fg,h}$, which comply with the respective constraints in (7.16), (7.17), (7.18) and (7.19).

While ω_f and ω_0 are calculated using (7.3)–(7.4), P_d and $I_{fg,h}$ are determined through a straightforward MATLAB simulation of the system. Figure 7.3 presents the simulated waveforms of i_{rc} (from which P_d is derived), $i_{f,h}$, and $i_{fg,h}$.

The design procedure resulted in the prototyping of L_f and L_{fg} using toroidal cores made of powder-type magnetic material and wound with Litz wire. The same technology

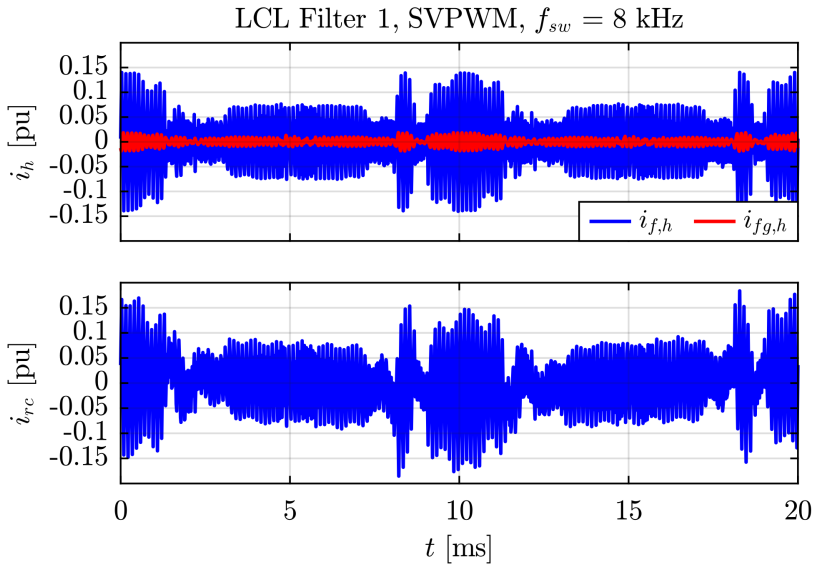
Table 7.1 System main data and coefficients for the LCL filter design [129].

Base Values		**Non-Linear Load**		**Active Power Filter**		**LCL Filter Design Factors**	
S_b	260 kVA	P_l	1.0 pu	S_{apf}	0.33 pu	k_{L_f}	25 %
V_b	400 V_{rms}	$I_{l,1}$	1.0 pu	M	0.9	$k_{C_{f,OFF}}$	4 %
ω_b	314 rad/s	THD_i	33 %	h	25	$k_{C_{f,ON}}$	4 %
Z_b	0.62 Ω					$k_{L_{fg,SVPWM}}$	15 %
L_b	1.96 mH					$k_{L_{fg,APF\text{-}GDPWM}}$	11 %
C_b	5.17 mF					$k_{P_{d,l}}$	1 %
						$k_{P_{d,apf}}$	1 %

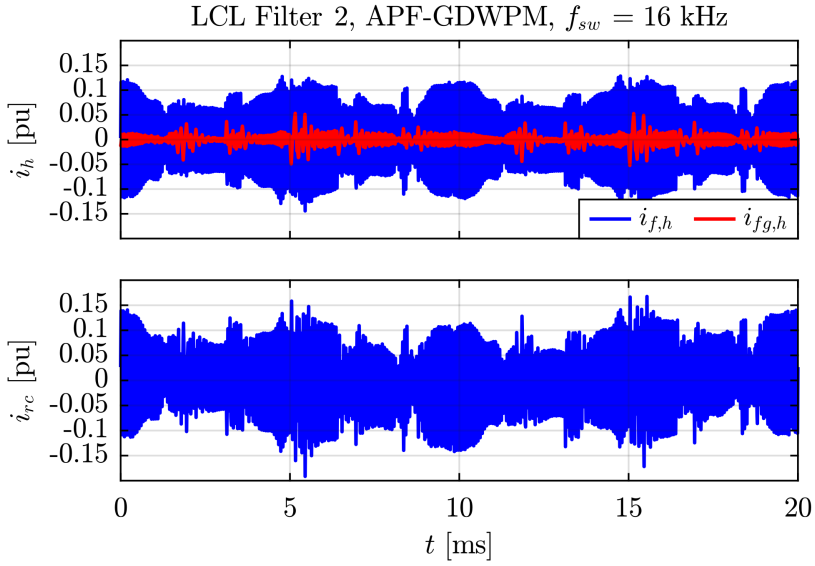
Table 7.2 LCL filter design results [129].

Parameter	**Filter 1**	**Filter 2**	**Constraint**
Modulation	SVPWM	APF-GDPWM	-
f_{sw} [kHz]	8	16	-
$\lambda_{h,pp,max}$ [pu]	0.78	0.88	-
HDF [-]	0.26	0.45	-
L_f [µH]	**89**	**50**	-
C_f [µF]	**68**	**68**	-
L_{fg} [µH]	**48**	**15**	-
R_f [mΩ]	**225**	**136**	-
ω_0 [rad/s]	21745	-	≤ 25133
	-	36007	≤ 50266
ω_f [rad/s]	17552	31694	≥ 15708
P_d [%]	0.21	0.15	≤ 0.33
$I_{fg,h}$ [%]	1.00	1.54	≤ 2.5

was employed for the inductors in both Filter 1 and Filter 2. Photographs of the realized L_f and L_{fg} inductors are shown in Fig. 7.4 and Fig. 7.5, respectively.



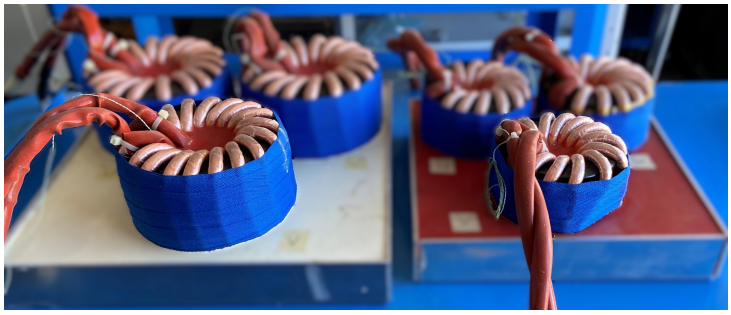
(a)



(b)

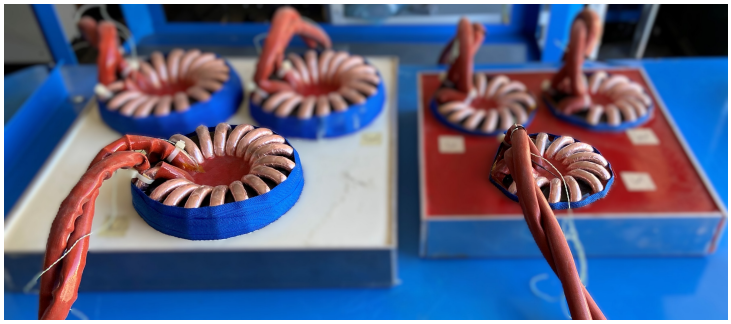
Fig. 7.3 Simulation results: current ripple in the APF-side inductor L_f ($i_{f,h}$) and grid-side inductor $L_{f,g}$ ($i_{fg,h}$) and capacitor current (i_{rc}) obtained respectively with LCL Filter 1, SVPWM, f_{sw} = 8 kHz (a) and LCL Filter 2, APF-GDPWM, f_{sw} = 16 kHz (b) [129].

As the required capacitance C_f and current i_{rc} are expected to be similar for Filter 1 and Filter 2, the same PCB-mounted film capacitors were employed for the capacitor branch in both prototypes. A picture of the capacitive element is shown in Fig. 7.6.



(a) (b)

Fig. 7.4 View of the APF-side inductor L_f of Filter 1 (a) and 2 (b). The inductors are encapsulated in thermally conductive resin. The volume and weight of each inductor are respectively 2.39 l and 9.6 kg for Filter 1 and 1.30 l and 5.8 kg for Filter 2 [129].



(a) (b)

Fig. 7.5 View of the APF-side inductor L_{fg} of Filter 1 (a) and 2 (b). The inductors are encapsulated in thermally conductive resin. The volume and weight of each inductor are respectively 1.59 l and 6.5 kg for Filter 1 and 0.74 l and 2.6 kg for Filter 2 [129].

The designed LCL filters have been assembled, and for both, the actual admittance $Y_f(s)$ was measured using a Hioki IM3536 LCR meter. A comparison between the expected and experimentally measured admittances is presented in Fig. 7.7. Despite minor differences in resonance and anti-resonance frequencies and in damping caused by component tolerances, the measured admittance curves closely follow the ideal ones for $\omega \leq h\omega_g$ and $\omega \geq \omega_{sw}$, thus ensuring the intended filter behaviour within the control frequency range and the required high-frequency attenuation.

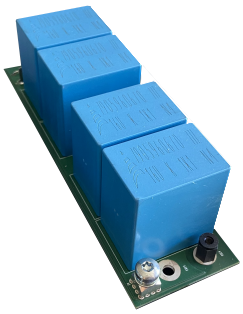


Fig. 7.6 View of the capacitor board used both in Filter 1 and 2 [129].

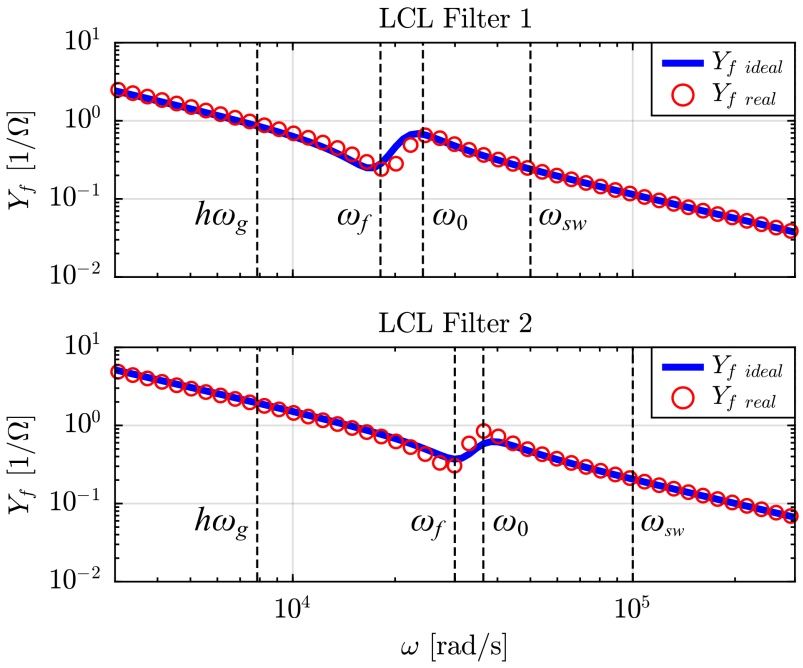


Fig. 7.7 Expected (i.e., ideal) and measured (i.e., real) curves of Y_f for LCL Filter 1 and 2. The ideal curves are obtained from (7.1) [129].

7.5 Experimental Validation

The system setup employed for the experimental validation in Chapter 6, consisting of a 260 kVA regenerative system with installed in parallel a TRL 9 industrial 2-level APF (Fig. 6.13), is reused to carry out the performance comparison tests between the APF-GDPWM and the SVPWM. Moreover, the APF can be alternatively connected to the grid through LCL Filter 1 or 2, both designed according to the proposed procedure, with their specifications listed in Table 7.2. The implemented APF control strategy is the algorithm

presented in Chapter 5, while the DC-link voltage is controlled to maintain $M = 0.9$ and the non-linear load current compensation up to 25^{th} harmonic order is performed.

Power measurements were performed using the HBM Genesis data recorder connected between the LCL filter and the PCC (Figs. 6.13 and 6.14). The tests were conducted with the APF operating under three different configurations, while the regenerative system delivered full-power (P_{CUT} = 260 kW). In *Case 1* (Fig. 7.8), the APF operates using SVPWM at f_{sw} = 8 kHz and it is connected to the grid via LCL Filter 1. In *Case 2* (Fig. 7.9), LCL Filter 1 is retained, while the APF employs APF-GDPWM at f_{sw} = 16 kHz. In *Case 3* (Fig. 7.10), the APF uses APF-GDPWM at f_{sw} = 16 kHz, while it is interfaced to the grid through LCL Filter 2. The tests results are summarized in Table 7.3.

By comparing *Case 1* and *Case 2*, the power devices losses theory presented in Chapter 6 is experimentally confirmed. Indeed, it is outlined that APF-GDPWM, compared to SVPWM, enables a doubling of the switching frequency from 8 kHz to 16 kHz without increasing total losses. Notably, without modifying the existing hardware (i.e., power switches and LCL filter), the measured losses for the converter operating at f_{sw} = 8 kHz and using SVPWM are slightly higher than those measured with the converter operating at f_{sw} = 16 kHz and using APF-GDPWM (0.94 % vs 0.83 % of P_{CUT}). An overall reduction in converter losses is achieved, despite the regenerative system being an inductive non-linear load (THD_i = 34.3 %) and the switching losses reduction being less pronounced in this case, as discussed in Chapter 6. This is because the use of APF-GDPWM also reduces the capacitor current i_{rc}, resulting in lower damping resistor losses: 0.22 % for SVPWM at f_{sw} = 8 kHz, compared with 0.10 % for APF-GDPWM at f_{sw} = 16 kHz. LCL filter losses were not considered in the theoretical analysis of Chapter 6. Their reduction further confirms the effectiveness of APF-GDPWM. Moreover, the doubling of the switching frequency in *Case 2* reduces the current ripple $i_{fg,h}$ injected into the grid by the APF from 1.63 % to 1.33 % of $i_{in,1}$.

The comparison between *Case 1* and *Case 3* indicates that employing APF-GDPWM with a doubled switching frequency allows for a more compact filter design, reducing the installed inductance, the volume and the weight, while achieving similar performance regarding the APF current ripple $i_{fg,h}$, total converter losses P_{loss} and damping resistor losses P_d. In particular, LCL Filter 2, relative to LCL Filter 1, achieves a 53 % reduction in total inductance (137 vs. 65 µH), a single-phase L_f inductor with 46 % smaller volume (2.39 vs. 1.30 l) and 40 % lighter weight (9.6 vs. 5.8 kg) and a single-phase L_{fg} inductor with 54 % reduced volume (1.59 vs. 0.74 l) and 60 % lower weight (6.5 vs. 2.6 kg). The

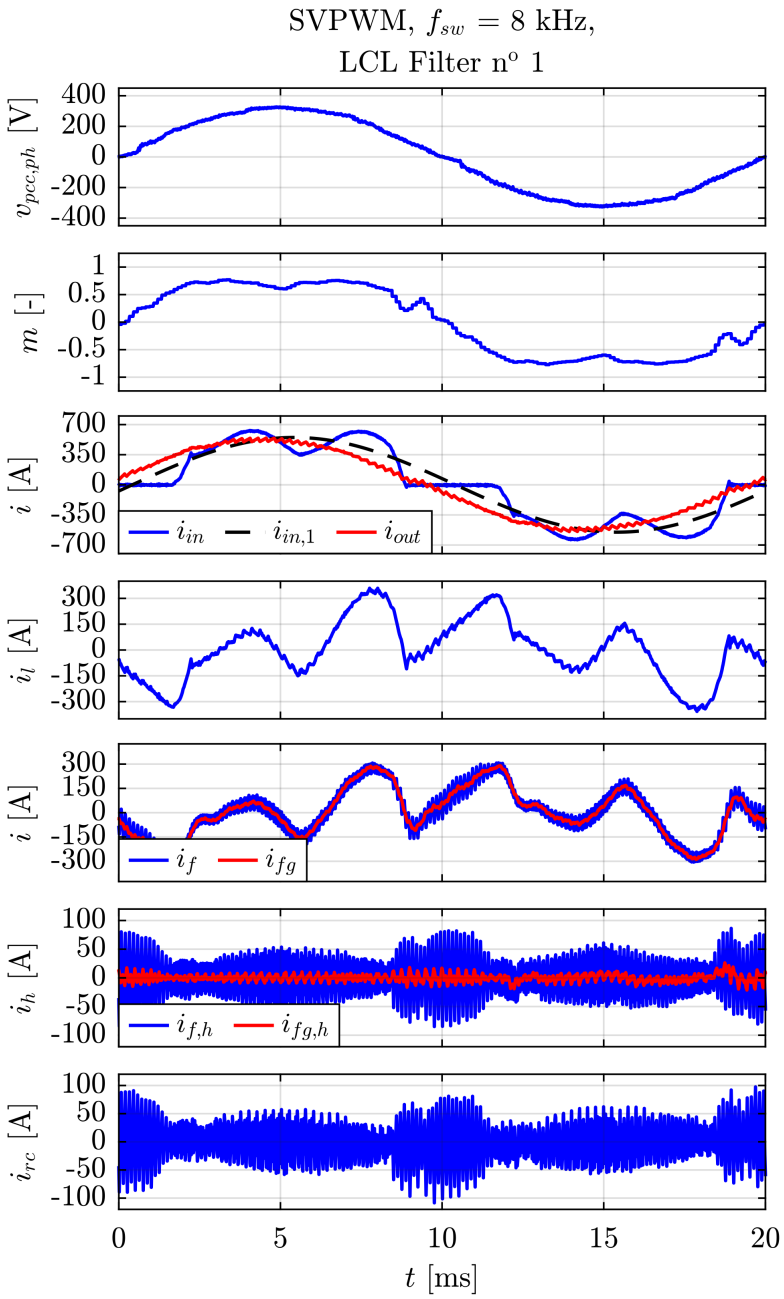


Fig. 7.8 *Case 1*: APF steady state operation in case of SVPWM at f_{sw} = 8 kHz and installation of LCL Filter 1. From top to bottom: phase PCC voltage $v_{pcc,ph}$, phase modulation index m, CUT input current i_{in} and its fundamental component $i_{in,1}$, CUT output current i_{out}, current absorbed by the regenerative system i_l, inverter-side APF current i_f, current injected by the APF at the PCC i_{fg}, high frequency current ripple $i_{f,h}$ and $i_{fg,h}$, capacitor current i_{rc} [129].

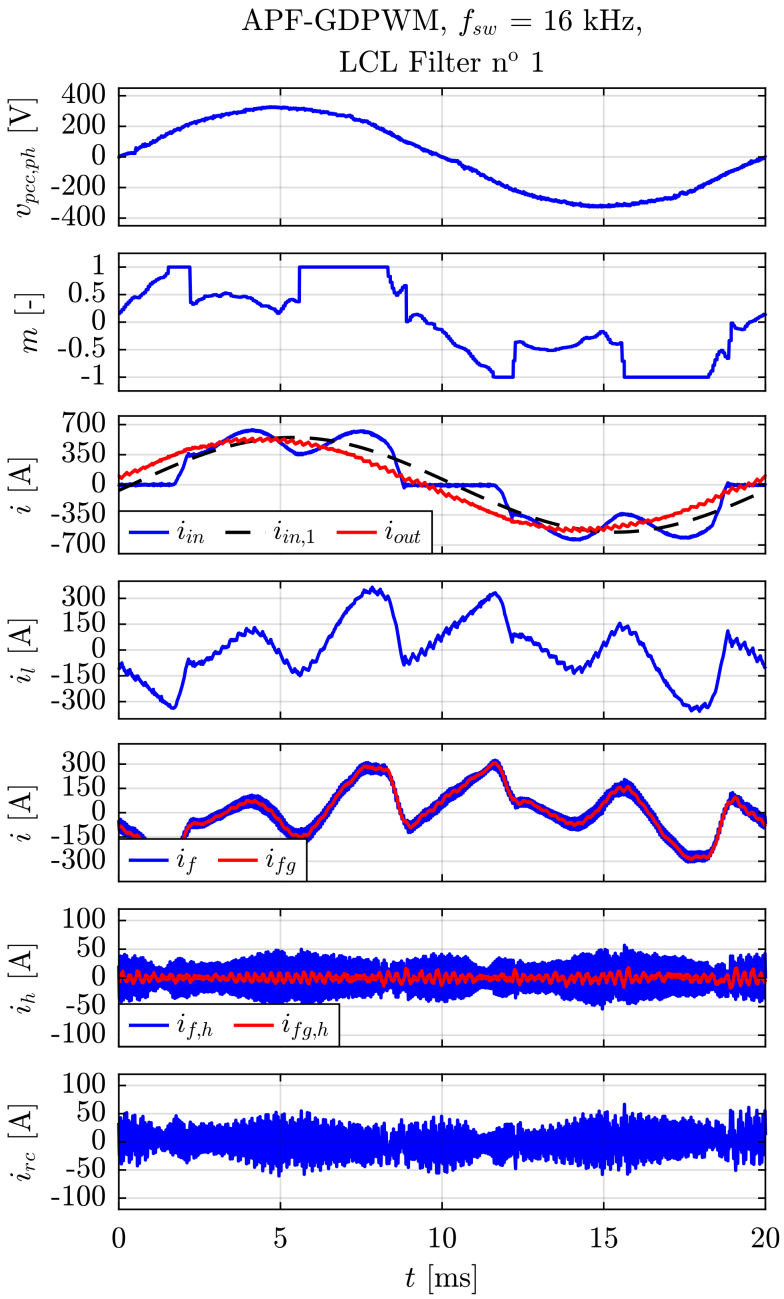


Fig. 7.9 *Case 2*: APF steady state operation in case of APF-GDPWM at f_{sw} = 16 kHz and installation of LCL Filter 1. From top to bottom: phase PCC voltage $v_{pcc,ph}$, phase modulation index m, CUT input current i_{in} and its fundamental component $i_{in,1}$, CUT output current i_{out}, current absorbed by the regenerative system i_l, inverter-side APF current i_f, current injected by the APF at the PCC i_{fg}, high frequency current ripple $i_{f,h}$ and $i_{fg,h}$, capacitor current i_{rc} [129].

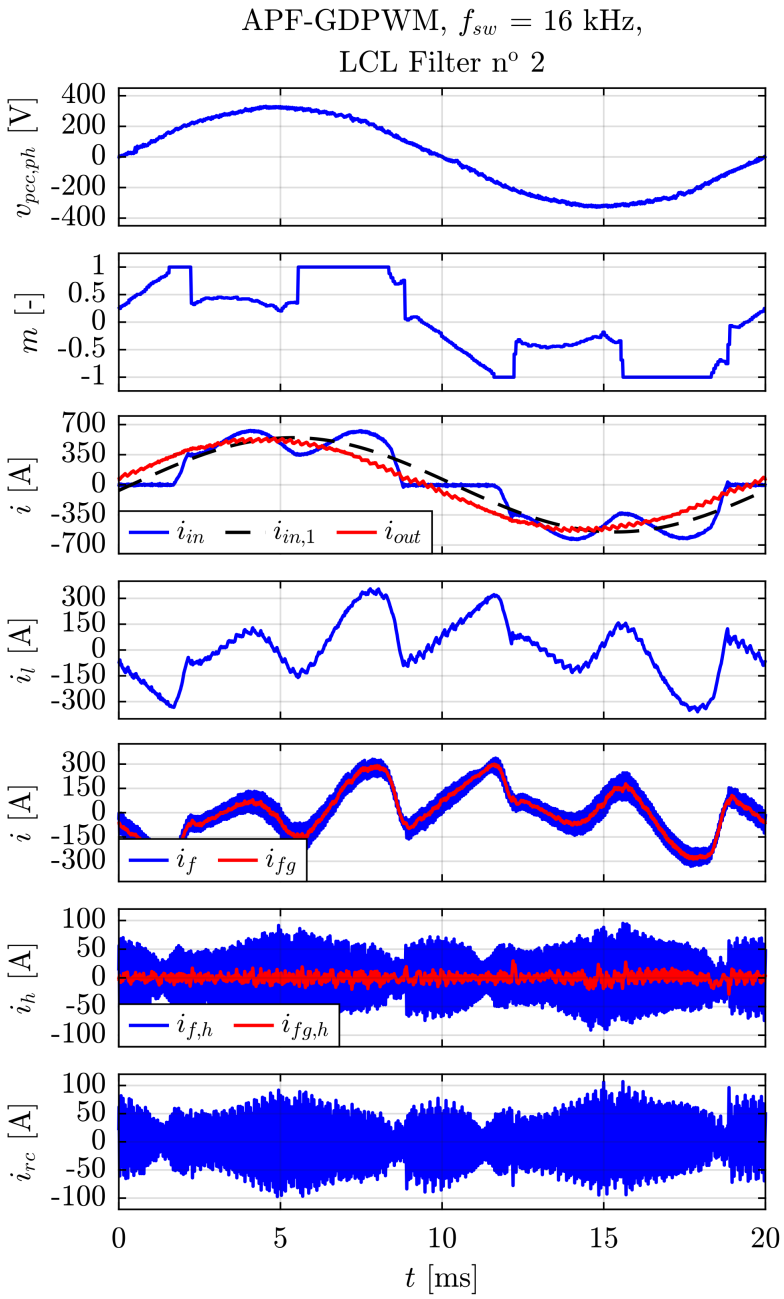


Fig. 7.10 *Case 3*: APF steady state operation in case of APF-GDPWM at f_{sw} = 16 kHz and installation of LCL Filter 2. From top to bottom: phase PCC voltage $v_{pcc,ph}$, phase modulation index m, CUT input current i_{in} and its fundamental component $i_{in,1}$, CUT output current i_{out}, current absorbed by the regenerative system i_l, inverter-side APF current i_f, current injected by the APF at the PCC i_{fg}, high frequency current ripple $i_{f,h}$ and $i_{fg,h}$, capacitor current i_{rc} [129].

Table 7.3 Experimental results with SVPWM vs APF-GDWPM [129].

Quantity	**Unit**	**Case 1**	**Case 2**	**Case 3**
LCL Filter	-	1	1	2
Modulation	-	SVPWM	APF-GDPWM	APF-GDPWM
f_{sw}	kHz	8	16	16
$I_{fg,h}$	%	1.63	1.33	1.86
P_d*	%	0.22	0.10	0.16
P_{loss}	%	0.94	0.83	1.07

* P_d is not directly measured, but estimated by considering the damping resistance R_f and the capacitor current i_{rc}, while neglecting the skin effect.

obtained values of $i_{fg,h}$ and P_d comply with the constraints specified in (7.18)–(7.19) for both *Case 1* ($i_{fg,h}$ = 1.63 %, P_d = 0.22 %) and *Case 3* ($i_{fg,h}$ = 1.86 %, P_d = 0.16 %). Meanwhile, the overall APF power losses P_{loss} amount to approximately 1 % of P_{CUT} for both cases (0.94 % in *Case 1* and 1.07 % in *Case 3*), ensuring minimal impact of the APF on the system total power consumption at the PCC.

7.6 Conclusion

This chapter proposes a step-by-step design methodology for the DM LCL filter used to interface an APF to the grid. The design procedure aims to achieve a filter configuration that minimizes the installed inductance and capacitance, thus reducing the cost, weight and volume of the application, while still meeting the harmonic distortion requirements imposed by standards, avoiding interference with the low-frequency harmonic compensation performed by the APF control and limiting power losses. The design procedure considers both the characteristics of the non-linear load, including the system rated power and the line current total harmonic distortion, as well as the operating conditions of the APF, such as the chosen modulation technique, the switching frequency and the modulation index.

The experimental results were obtained by interchanging the designed LCL filters used to interface the TRL 9 two-level industrial APF with the grid and by applying either SVPWM or APF-GDPWM, while the APF compensates for the harmonic distortion injected by a 260 kVA regenerative testing system for industrial AC–AC power converters.

The test results indicate that, compared to SVPWM, APF-GDPWM allows more effective utilization of the existing hardware (i.e., power switches, cooling system and DM LCL filter) by allowing the switching frequency to be doubled from 8 kHz to 16 kHz, thus resulting in reduced current ripple and lower power losses. Furthermore, the increased control bandwidth improves dynamic performance and enables compensation of higher-order harmonics. Alternatively, implementing APF-GDPWM with the doubled switching frequency permits the use of a more compact and cost-effective DM LCL filter, achieving a 46 % reduction in volume and 40 % in weight for the converter-side inductor L_f and a 54 % reduction in volume and 60 % in weight for the grid-side inductor L_{fg}, while preserving the APF compensation performance and efficiency achieved with SVPWM.

Concluding, a two-level APF implementing APF-GDPWM can represent a cost-effective alternative compared to more expensive solutions, such as three-level inverters using standard SVPWM.

Chapter 8

Conclusion and Future Works

8.1 Conclusion

Both VSMs algorithms and APFs represent a valid solution to provide the full or partial spectrum of grid ancillary services, which are normally in charge to SGs. These applications facilitate the penetration of grid-tied power converters, particularly inverters used for grid-interfacing RESs and high-power loads in the case of VSMs, as well as non-linear loads such as diode or thyristor front-end rectifiers in the case of APFs.

This PhD thesis proposes innovative control strategies for both VSMs and APFs aimed at enabling the proper provision of grid ancillary services, with particular attention to limiting component stress, mitigating premature aging phenomena, reducing converter losses and ensuring compliance with grid-tied power converters standards. Nevertheless, hardware design guidelines are provided with the purpose of developing solutions suitable for the proposed control strategies, while reducing converter volume, weight and cost.

The dissertation is divided into two main parts: one addressing control algorithms for VSM applications and the other focusing on control aspects and hardware design considerations for APFs.

Virtual Synchronous Machines

The principal contributions related to VSMs are summarized as follows:

- **Power Coupling in VSMs:** This phenomenon can induce reactive power injection during active power support and vice versa, leading to unnecessary current stress on power devices and the propagation of power fluctuations from the inverter AC-side to the DC-stage, potentially shortening the lifespan of DC-connected batteries. To address this issue, a feedforward-based solution is proposed and integrated into the VSM model, ensuring complete active–reactive power decoupling while the VSM provides grid support. This topic has been thoroughly examined in Chapter 3 of this PhD thesis and the results obtained have led to the publication of [C4] and [J3];

- **Grid Impedance Estimation Through VSM-Driven Inverters:** Accurate knowledge of grid impedance is essential for properly tuning the VSM control blocks and inverter current controllers. Since existing estimation methods are mainly designed for grid-following converters and have limitations when applied to VSM applications, this thesis proposes in Chapter 4 a dedicated VSM-based grid impedance estimator. The estimator can be integrated into any VSM model, inherently rejects measurement noise common in industrial environments and is fully tunable with respect to estimation time and achieved accuracy. The designed estimator has been registered as a national patent [P1] and has resulted in the publications [C1], [C2] and [J2].

Active Power Filters

The main achievements pertaining to APF applications are summarized as follows:

- **Dedicated DPWM Technique for APFs:** The designed APF-GDPWM algorithm, presented in Chapter 6 of this thesis, is robust against power line noise acquired by APF line current sensors, making it particularly suitable for industrial environments where voltage and current disturbances are common. Compared to conventional SVPWM, the proposed DPWM method allows more efficient use of existing hardware by reducing the devices losses and enables the doubling of the switching frequency, thus decreasing high-frequency current ripple injected into the grid. The APF-GDPWM algorithm is currently implemented in TRL 9 industrial APFs installed at the Prima Electro S.p.A. facility and used to cancel the harmonic distortion generated by regenerative systems during the end-of-line testing of AC–AC industrial inverters. Moreover, the design of this APF-dedicated DPWM solution has led to the publication of [C3] and [J1];

- **Design Procedure for the DM LCL Filter of APFs:** Unlike LCL filter design methodologies in the literature, the design approach proposed in Chapter 7 of this thesis accounts for both the APF operating conditions and the characteristics of the compensated non-linear load, ensuring filter non-interference with the low-frequency harmonic compensation performed by the APF control, limited filter losses and compliance with harmonic distortion standards at the PCC, while minimizing filter size, weight and cost. The work carried out in this research area has resulted in contributions published in [J1].

In conclusion, this PhD thesis advances the state of the art in VSM and APF technologies, providing theoretical contributions and experimentally validated solutions that foster the proliferation of grid-tied power converters, thus paving the way toward a more converter-dominated and stable power system.

8.2 Future Works

The main avenues for future research emerging from this thesis are as follows:

(1) Control of DC-DC Converters in Ultra-Fast DC Chargers for Grid Support

In the discussion on VSMs (Chapters 2, 3, and 4) the DC source to which the VSM-driven inverter is connected was considered ideal and DC power supplies were used during the experimental tests. By idealizing the DC-stage, the analysis could focus exclusively on the inverter control. However, in applications such as ultra-fast DC chargers, the EV batteries are connected to the AFE DC-side through an isolated DC–DC converter, whose control strategy can significantly affect the dynamics of providing grid ancillary services. Consequently, future research could focus on the development of coordinated control solutions of the entire ultra-fast DC charging system, comprising both the AFE and the isolated DC-DC converter, to guarantee proper and timely provision of grid support.

(2) Integration of VSM Algorithms into APFs

In this thesis, VSM algorithms and APF applications have been addressed as distinct topics. Nevertheless, APFs are fundamentally grid-tied inverters and, as such, can be configured

to emulate the behavior of SGs through the implementation of a VSM control algorithm within their control unit. Since APFs are not supplied by an independent DC energy source, VSM-embedded APFs can provide, in addition to the harmonic compensation, the grid ancillary services related to reactive power injection, such as voltage regulation and fault current injection during grid faults. Moreover, the energy stored in the DC-link capacitors can be partially employed to assist the grid with inertial support by varying the DC voltage level. The topic of APFs integrated with VSM algorithms is scarcely addressed in the literature. Consequently, this represents a promising area for future research.

Appendix A

Power Devices Losses in APFs

This section describes the calculation of both conduction and switching losses in the power devices of a two-level three-phase APF.

A.1 Conduction Losses

The mean conduction losses of a generic power switch (e.g., IGBT, MOSFET, etc.) over one switching period can be expressed as follows [133]:

$$p_c = (R_{on} \cdot i_{cell,x} + V_{th}) \cdot i_{cell,x} \cdot d \tag{A.1}$$

where $i_{cell,x}$ denotes the current flowing through the positive ($x = pos$) or negative ($x = neg$) unidirectional switching cell containing the power switch (see Fig. A.1) and d represents the duty cycle.

The current $i_{cell,x}$ is assumed to remain constant over a switching period, whereas the duty cycle d is defined as:

$$d = \frac{v^* + v^*_{cm}}{V_{dc}} + \frac{1}{2} \tag{A.2}$$

where v^* denotes the leg reference voltage, while the zero-sequence voltage v^*_{cm} depends on the implemented PWM strategy.

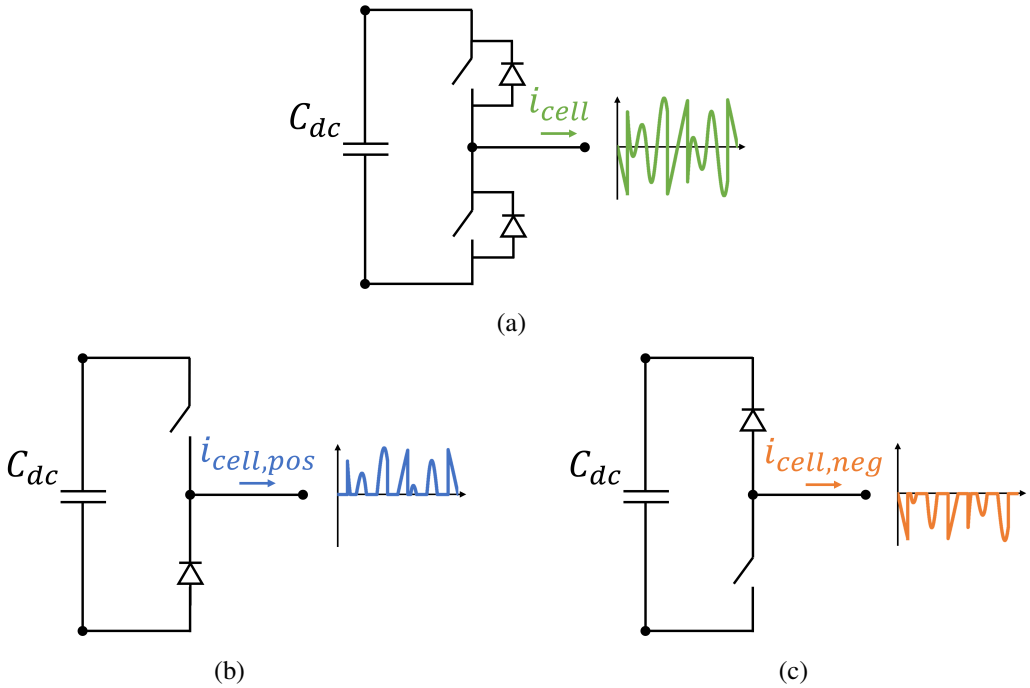


Fig. A.1 The inverter leg of a two-level three-phase APF (a) is a bidirectional switching cell, which can be subdivided into two unidirectional cells. Each cell consists of a power switch (e.g., IGBT or MOSFET) with the related freewheeling diode. The unidirectional cells conduct respectively positive $i_{cell,pos}$ (b) and negative $i_{cell,neg}$ (c) currents. Instantaneously, the APF output current is $i_{cell} = i_{cell,pos} + i_{cell,neg}$ [129].

The average conduction losses over one fundamental period are therefore obtained by combining (A.1)–(A.2) and carrying out the following integration:

$$P_c = \frac{1}{2\pi}\int_0^{2\pi} p_c(\theta)\,d\theta \; = A + B + C \tag{A.3}$$

$$A = \frac{1}{2\pi}\int_0^{2\pi} \frac{R_{on}\cdot i_{cell,x}(\theta)^2 \cdot v^*(\theta)}{V_{dc}} + \frac{V_{th}\cdot i_{cell,x}(\theta)\cdot v^*(\theta)}{V_{dc}}\,d\theta \tag{A.4}$$

$$B = \frac{1}{2\pi}\int_0^{2\pi} \frac{R_{on}\cdot i_{cell,x}(\theta)^2 \cdot v^*_{cm}(\theta)}{V_{dc}} + \frac{V_{th}\cdot i_{cell,x}(\theta)\cdot v^*_{cm}(\theta)}{V_{dc}}\,d\theta \tag{A.5}$$

$$C = \frac{1}{2\pi} \int_0^{2\pi} \frac{R_{on} \cdot i_{cell,x}(\theta)^2}{2} + \frac{V_{th} \cdot i_{cell,x}(\theta)}{2} \, d\theta \tag{A.6}$$

Term A in (A.4) depends on the relationship between $i_{cell,x}$ and v^*. It represents the component associated with the provision of active power (P_{apf}) by the APF. Since an APF primarily injects reactive (Q_{apf}) and distortion (D_{apf}) powers to compensate for the non-linear load current, while drawing only a small amount of P_{apf} to cover its internal losses, term A can be considered negligible.

Term B in (A.5) is associated with the interaction between $i_{cell,x}$ and v^*_{cm}. As demonstrated in [133] for the case where the output current contains only the fundamental component, the zero-sequence voltage does not affect the conduction losses. This conclusion remains valid even when multiple harmonic components are present. Therefore, the value of B is zero.

As a result, (A.3) depends solely on term C in (A.6), which can be expressed in detail as follows:

$$C = \frac{R_{on}}{2} \cdot \frac{1}{2\pi} \int_0^{2\pi} i_{cell,x}(\theta)^2 \, d\theta + \frac{V_{th}}{2} \cdot \frac{1}{2\pi} \int_0^{2\pi} i_{cell,x}(\theta) \, d\theta$$

$$P_c = C = \frac{R_{on}}{2} \cdot I^2_{cell,x,rms} + \frac{V_{th}}{2} \cdot I_{cell,x,m} \tag{A.7}$$

A.2 Switching Losses

Assuming a linear relationship between the switching energy loss and the switched current [133], the mean switching losses of a generic power switch over one switching period can be expressed as follows:

$$p_{sw} = \frac{E_{sw}}{V_{dc,n} \cdot I_n} \cdot f_{sw} \cdot V_{dc} \cdot i_{cell,x,sw} \tag{A.8}$$

where $i_{cell,x,sw}$ denotes the unidirectional cell switched current.

The current $i_{cell,x,sw}$ is zero when the inverter leg is clamped to either the positive or negative DC rail. Otherwise, it is equal to $i_{cell,x}$ [132]:

$$i_{cell,x,sw} = \begin{cases} 0, & d = 0 \vee d = 1 \\ i_{cell,x} & 0 < d < 1 \end{cases} \tag{A.9}$$

For a CPWM, the switching current $i_{cell,x,sw}$ is identical to $i_{cell,x}$ at all times. Consequently, the mean switching losses over one fundamental period for a standard CPWM can be expressed as:

$$P_{sw,CPWM} = \frac{1}{2\pi} \int_0^{2\pi} p_{sw,CPWM}(\theta)\, d\theta$$

$$P_{sw,CPWM} = \frac{E_{sw}}{V_{dc,n} \cdot I_n} \cdot f_{sw} \cdot V_{dc} \cdot \frac{1}{2\pi} \int_0^{2\pi} i_{cell,x}(\theta)\, d\theta$$

$$P_{sw,CPWM} = \frac{E_{sw}}{V_{dc,n} \cdot I_n} \cdot f_{sw} \cdot V_{dc} \cdot I_{cell,x,m} \tag{A.10}$$

By definition, the switching loss factor quantifies the ratio between the switching losses associated with a specific PWM technique, such as APF-GDPWM, and those of a standard CPWM (6.4). Accordingly, a generalized expression for the switching losses under any modulation technique can be obtained by combining (6.4) with (A.10):

$$P_{sw} = \frac{E_{sw}}{V_{dc,n} \cdot I_n} \cdot f_{sw} \cdot V_{dc} \cdot k_{sw} \cdot I_{cell,x,m} \tag{A.11}$$

The computation of P_c and P_{sw} has been performed for the power switch (i.e., IGBT or MOSFET). However, an equivalent analysis for the freewheeling diode would yield the same expressions as in (A.7) and (A.11).

List of Acronyms & Symbols

List of Acronyms

AFE	Active Front-End
APF	Active Power Filter
CM	Common-Mode
CO_2	Carbon Dioxide
CPWM	Continuous Pulse-Width Modulation
CSP	Concentrated Solar Power
CUT	Converter Under Test
DM	Differential-Mode
DPWM	Discontinuous Pulse-Width Modulation
EV	Electric Vehicle
FFT	Fast Fourier Transform
GDPWM	Generalized Discontinuous Pulse-Width Modulation
HDF	Harmonic Distortion Factor
HPF	High-Pass Filter
MPPT	Maximum Power Point Tracking
NPC	Neutral Point Clamped

PCC Point of Common Coupling

PI Proportional-Integral Regulator

PLL Phase Locked-Loop

P-SSI Proportional-Sinusoidal Signal Integrator Regulator

PV Photovoltaic

PWM Pulse-Width Modulator

RES Renewable Energy Source

RLS Recursive Least Squares

ROCOF Rate of Change of Frequency

SCR Short-Circuit Ratio

SG Synchronous Generator

SVPWM Space Vector Pulse-Width Modulation

SSI Sinusoidal Signal Integrator

THD Total Harmonic Distortion

THD_i Current Total Harmonic Distortion

TSO Transmission System Operator

VSC Virtual Synchronous Compensator

VSG Virtual Synchronous Generator

VSM Virtual Synchronous Machine

List of Symbols

b_p	Active Droop Coefficient
b_q	Reactive Droop Coefficient
C_b	Base Capacitance
C_{dc}	DC-Link Capacitance
C_f	Filter Capacitance
C_r	Resonant Load Capacitance
d	Duty Cycle
D_{apf}	APF Distortion Power
e_g	Equivalent Thevenin Grid Voltage
$\tilde{e}_g$	Estimated Equivalent Thevenin Grid Voltage
E_{sw}	Power Device Total Switching Energy Loss
f_b	Grid Base Frequency
$f_{cut-off\ est}$	Grid Impedance Estimator Cut-Off Frequency
f_r	Virtual Frequency
f_s	Sampling Frequency
f_{sw}	Switching Frequency
h	Harmonic Order
H	Inertia Constant
HDF^{η}	HDF Under Equal Efficiency
i^*	APF Current Reference
i_{apf}	APF output current
I_{apf}	APF Rated current

$i_{cell,x}$	Inverter Unidirectional Switching Cell Current
i_{cell}	Inverter Bidirectional Switching Cell Current
$i_{cm\ comp}$	Hysteresis Selector CM Computation Current
i_{dc}	Inverter DC-Side Current
i_f	Current in Inverter-Side Inductor
$i_{f,h}$	Current Ripple in Inverter-Side Inductor
i_{fg}	Current in Grid-Side Inductor
$i_{fg,h}$	Current Ripple in Grid-Side Inductor
i_g	Grid Current
i_i	Inverter Output Current
$\hat{I}_i$	Inverter Output Current Peak
i_i^*	Inverter Current Reference
i_{in}	CUT Input Current
i_{inj}	Inverter Injected Current
i_{inj}^*	Inverter Injected Current Reference
i_l	Load Current
I_n	Nominal Current
i_{out}	CUT Output Current
i_{rc}	Current in Capacitor Branch
i_{set}	Current Regulator Reference
i_v	Virtual Current
i_x	Phase x APF Current Reference
i_y	Phase y APF Current Reference

j	Imaginary Unit
k	Sampling Period
k_1	First-Harmonic P-SSI Integral Gain
k_6	Sixth-Harmonic SSI Integral Gain
k_{12}	Twelfth-Harmonic SSI Integral Gain
k_{18}	Eighteenth-Harmonic SSI Integral Gain
k_{24}	Twenty-Fourth-Harmonic SSI Integral Gain
k_{C_f}	Filter Capacitance Attenuation Factor
k_{est}	Integral Estimator Gain
k_f	APF Form Factor
k_{L_f}	Inverter-Side Inductance Attenuation Factor
$k_{L_{fg}}$	Grid-Side Inductance Attenuation Factor
k_p	First-Harmonic P-SSI Proportional Gain
k_{P_d}	Damping Resistor Losses Attenuation Factor
k_{sw}	Switching Loss Factor
L_b	Base Inductance
L_{eq}	Equivalent DM Filter Inductance
L_f	Inverter-Side Inductance
L_{fg}	Grid-Side Inductance
L_g	Grid Inductance
L'_g	Raw Grid Inductance
$\tilde{L}'_g$	Estimated Raw Grid Inductance
$L_{g\ eq}$	Equivalent Series Grid Inductance

$\tilde{L}_{g\ eq}$	Estimated Grid Inductance
$\tilde{L}_{g\ eq\ th}$	Theoretical Estimated Grid Inductance
L_r	Resonant Load Inductance
L_{test}	Series External Inductance
L_{tot}	Total Line Inductance
L_v	Virtual Inductance
m	Phase Instantaneous Modulation Index
M	Modulation Index
m_c	Zero-Sequence Instantaneous Modulation Index
M_{max}	Maximum Modulation Index in Linearity Range
P^*	Active Power Reference
P_{apf}	APF Active Power
p_c	Power Device Conduction Losses Over a Swtiching Period
P_c	Power Device Conduction Losses Over a Fundamental Period
P_{CUT}	CUT Output Power
P_d	Damping Resistor Losses
P_d^*	Frequency Droop Active Power Reference
P_i	Inverter Output Active Power
P_l	Load Rated Power
P_{loss}	Total Converter Losses
P_{set}	Active Power Setpoint
p_{sw}	Power Device Switching Losses Over a Swtiching Period
P_{sw}	Power Device Switching Losses Over a Fundamental Period

P_v	Virtual Active Power
P_v^*	Virtual Active Power Reference
q^*	Inverter Switches Commands
Q^*	Reactive Power Reference
Q_{apf}	APF Reactive Power
q_b	Grid Disconnection Command
Q_c	Reactive Power Generated by Filter Capacitor
Q_d^*	Voltage Droop Reactive Power Reference
q_{dec}	P-Q Decoupling External Command
Q_i	Inverter Output Reactive Power
q_{L_g}	Grid Inductance Estimation Command
$q_{L_{gext}}$	Grid Inductance Estimation External Command
q_{R_g}	Grid Resistance Estimation Command
$q_{R_{gext}}$	Grid Resistance Estimation External Command
Q_{set}	Reactive Power Setpoint
Q_v	Virtual Rective Power
Q_v^*	Virtual Rective Power Reference
q_{VSM}	VSM Enabling Signal
R_f	Damping Resistance
R_g	Grid Resistance
$\tilde{R}_g$	Estimated Grid Resistance
$\tilde{R}_{g\ th}$	Theoretical Estimated Grid Resistance
R_g'	Raw Grid Resistance

$\tilde{R}'_g$	Estimated Raw Grid Resistance
R_{on}	Power Device On-State Resistance
R_r	Resonant Load Resistance
R_{test}	Series External Resistance
R_{tot}	Total Line Resistance
R_v	Virtual Resistance
s	Laplace Operator
S_{apf}	APF Rated Power
S_b	Base Power
S_i	Inverter Output Apparent Power
S_n	Nominal Power
t	Time
T_s	Sampling Period
$T_{v,j}$	Power Device Junction Temperature
v^*	Inverter Voltage Reference
V_b	Base Voltage
v_c	Grid Voltage Across Filter Capacitor Branch
$\tilde{v}_c$	Estimated Grid Voltage
v_c^*	Grid Voltage Reference
$\hat{V}_c$	Grid Voltage Amplitude
$\hat{V}_c^*$	Grid Voltage Amplitude Reference
v_{cm}	Inverter CM Output Voltage
v_{cm}^*	Zero-Sequence Voltage

V_{dc}	DC-Link Voltage
$V_{dc,n}$	Nominal DC-Link Voltage
$V_{g,e}$	Power Device Gate-Emitter Voltage
v_h	Inverter Output Ripple Voltage
v_{pcc}	PCC Voltage
$v_{pcc,filt}$	Filtered PCC Voltage
V_{th}	Power Device Threshold Voltage
v_x	Phase x APF Voltage Reference
v_y	Phase y APF Voltage Reference
X/R	Ratio of Grid Reactance to Resistance
Y_f	DM Filter Inverter-Side Admittance
Y_{fg}	DM Filter Grid-Side Admittance
Z_b	Base Impedance
γ	Phase Shift between Virtual Current and Electromotive Force
Γ	Error Evalation Variable
Γ_{th}	Error Evalation Threshold
δ	Load Angle
$\tilde{\delta}$	Estimated Load Angle
Δ	Small Signal Variation
Δi_{fault}	Injected Fault Current
Δi_{th}	Hysteresis Selector Current Threshold
$\Delta i_{v,d,err}$	Virtual Reactive Current Error
$\Delta P_{inertial}$	Inertial Active Power

$\Delta Q_{v,err}$	Virtual Reactive Power Error
ΔV_{dip}	Voltage Dip Amplitude
ΔZ_{e_g}	Grid Parameter Estimation Error due to Grid Voltage Deviation
ΔZ_{ω}	Grid Parameter Estimation Error due to Grid Frequency Deviation
$\Delta\lambda_{L_g}$	Additive Excitation Flux for Grid Inductance Estimation
$\Delta\lambda_{R_g}$	Additive Excitation Flux for Grid Resistance Estimation
$\Delta\lambda_{Z_g}$	Additive Excitation Flux for Grid Impedance Estimation
$\Delta\omega_{Z_g}$	Additive Virtual Rotor Freuqency for Grid Impedance Estimation
ϵ_{L_g}	Relative Grid Inductance Estimation Error
ϵ_{R_g}	Relative Grid Resistance Estimation Error
ζ	Damping Factor
θ	Grid & Virtual Rotor Position
λ_b	APF Base Flux
λ_e	Excitation Flux
λ_e^0	Excitation Flux Integral Term
$\lambda_{e,dec}$	Excitation Flux Feedforward Term
λ_h	APF Flux Ripple
λ_h^η	APF Flux Ripple Under Equal Efficiency
τ_e	Excitation Time Constant
τ_{est}	Estimation Time Constant
$\tau_{est,real}$	Real Estimation Time Constant
ω	Grid & Virtual Rotor Frequency
ω^*	Grid & Virtual Rotor Frequency Reference

ω^0	Grid & Virtual Rotor Frequency Integral Term
ω_0	DM LCL Filter Resonance Frequency
ω_b	Grid Base Frequency
ω_{dec}	Grid & Virtual Rotor Frequency Feedforward Term
ω_f	DM LCL Filter Anti-Resonance Frequency
ω_g	Grid Frequency
ω_{sw}	Switching Frequency

References

[1] World Energy Outlook 2024. Technical report, IEA, Paris, October 2024. Licence: CC BY 4.0 (report); CC BY NC SA 4.0 (Annex A).

[2] James Manwell, Jon Mcgowan, and A Rogers. *Wind Energy Explained: Theory, Design and Application, Second Edition*, volume 30. 03 2006.

[3] Remus Teodorescu, Marco Liserre, and Pedro Rodriguez. *Grid Converter Structures for Wind Turbine Systems*, pages 123–143. 2007.

[4] Robert Foster, Majid Ghassemi, and Alma Cota. *Solar Energy: Renewable Energy and the Environment*. 08 2009.

[5] Remus Teodorescu, Marco Liserre, and Pedro Rodriguez. *Photovoltaic Inverter Structures*, pages 5–29. 2007.

[6] T. Esram and P. L. Chapman. Comparison of Photovoltaic Array Maximum Power Point Tracking Techniques. *IEEE Transactions on Energy Conversion*, 22(2):439–449, 2007.

[7] Global EV Outlook 2025. Technical report, May 2025.

[8] Srdjan Srdic and Srdjan Lukic. Toward Extreme Fast Charging: Challenges and Opportunities in Directly Connecting to Medium-Voltage Line. *IEEE Electrification Magazine*, 7(1):22–31, 2019.

[9] Suwaiba Mateen, Mohmmad Amir, Ahteshamul Haque, and Farhad Ilahi Bakhsh. Ultra-Fast Charging of Electric Vehicles: A Review of Power Electronics Converter, Grid Stability and Optimal Battery Consideration in Multi-Energy Systems. *Sustainable Energy, Grids and Networks*, 35:101112, 2023.

[10] Hao Tu, Hao Feng, Srdjan Srdic, and Srdjan Lukic. Extreme Fast Charging of Electric Vehicles: A Technology Overview. *IEEE Transactions on Transportation Electrification*, 5(4):861–878, 2019.

[11] Prabha Kundur. *Power System Stability and Control.* McGraw-Hill Education, January 1994. ISBN: 978-0-07-035958-1.

[12] Australian Energy Market Operator (AEMO). Power System Requirements, jul 2020.

[13] IEEE Standard for Harmonic Control in Electric Power Systems. *IEEE Std 519-2022 (Revision of IEEE Std 519-2014)*, pages 1–31, 2022.

[14] IEA. Unlocking the Potential of Distributed Energy Resources. Technical report, IEA, May 2022.

[15] High Penetration of Power Electronic Interfaced Power Sources and the Potential Contribution of Grid Forming Converters. Technical report, ENTSO-E, Brussels, January 2020.

[16] Grid-Forming Capabilities: Towards System Level Integration. ENTSO-E, Brussels, March 2021.

[17] Shaik Nyamathulla and C. Dhanamjayulu. A Review of Battery Energy Storage Systems and Advanced Battery Management System for Different Applications: Challenges and Recommendations. *Journal of Energy Storage*, 86:111179, 2024.

[18] Batteries and Secure Energy Transitions. Technical report, IEA, Paris, October 2024. Licence: CC BY 4.0 (report); CC BY NC SA 4.0 (Annex A).

[19] Metin Kesler, Mithat C. Kisacikoglu, and Leon M. Tolbert. Vehicle-to-Grid Reactive Power Operation Using Plug-In Electric Vehicle Bidirectional Offboard Charger. *IEEE Transactions on Industrial Electronics*, 61(12):6778–6784, 2014.

[20] Jingyang Fang, Hongchang Li, Yi Tang, and Frede Blaabjerg. On the Inertia of Future More-Electronics Power Systems. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 7(4):2130–2146, 2019.

[21] Matthew T. Lawder, Bharatkumar Suthar, Paul W. C. Northrop, Sumitava De, C. Michael Hoff, Olivia Leitermann, Mariesa L. Crow, Shriram Santhanagopalan, and Venkat R. Subramanian. Battery Energy Storage System (BESS) and Battery Management System (BMS) for Grid-Scale Applications. *Proceedings of the IEEE*, 102(6):1014–1030, 2014.

[22] World Energy Issues Monitor. Technical report, WEC, London, April 2024.

[23] 28 April 2025 Blackout. Technical report, ENTSO-E, Brussels, 2025.

[24] Terna. Pilot Project Fast Reserve, 2020.

[25] Fingrid. Fast Frequency Reserve, 2020.

[26] Sid-Ali Amamra and James Marco. Vehicle-to-Grid Aggregator to Support Power Grid and Reduce Electric Vehicle Charging Cost. *IEEE Access*, 7:178528–178538, 2019.

[27] Konstantinos Oureilidis, Kyriaki-Nefeli Malamaki, Konstantinos Gallos, Achilleas Tsitsimelis, Christos Dikaiakos, Spyros Gkavanoudis, Milos Cvetkovic, Juan Manuel Mauricio, Jose Maria Maza Ortega, Jose Luis Martinez Ramos, George Papaioannou, and Charis Demoulias. Ancillary Services Market Design in Distribution Networks: Review and Identification of Barriers. *Energies*, 13(4), 2020.

[28] Jon Are Suul, Salvatore D'Arco, and Giuseppe Guidi. Virtual Synchronous Machine-Based Control of a Single-Phase Bi-Directional Battery Charger for Providing Vehicle-to-Grid Services. *IEEE Transactions on Industry Applications*, 52(4):3234–3244, 2016.

[29] Xiangwu Yan, Jiajia Li, Bo Zhang, Zhonghao Jia, Yang Tian, Hui Zeng, and Zhipeng Lv. Virtual Synchronous Motor Based-Control of a Three-Phase Electric Vehicle Off-Board Charger for Providing Fast-Charging Service. *Applied Sciences*, 8(6), 2018.

[30] Jhonatan D. Paucara, José Carlos U. Peña, and Damian Sal y Rosas. HESS Management for Virtual Inertia, Frequency and Voltage Support through Off-Board EV Bidirectional Chargers. *IEEE Open Journal of the Industrial Electronics Society*, pages 1–10, 2024.

[31] Fabio Mandrile, Davide Cittanti, Vincenzo Mallemaci, and Radu Bojoi. Electric Vehicle Ultra-Fast Battery Chargers: A Boost for Power System Stability? *World Electric Vehicle Journal*, 12(1), 2021.

[32] IEEE Recommended Practice for Use and Functions of Virtual Synchronous Machines. *IEEE Std 2988-2024*, pages 1–52, 2025.

[33] Vincenzo Mallemaci, Fabio Mandrile, Sandro Rubino, Andrea Mazza, Enrico Carpaneto, and Radu Bojoi. A Comprehensive Comparison of Virtual Synchronous Generators with Focus on Virtual Inertia and Frequency Regulation. *Electric Power Systems Research*, 201:107516, 2021.

[34] Myada Shadoul, Razzaqul Ahshan, Rashid S. AlAbri, Abdullah Al-Badi, Mohammed Albadi, and Mohsin Jamil. A Comprehensive Review on a Virtual-Synchronous Generator: Topologies, Control Orders and Techniques, Energy Storages, and Applications. *Energies*, 15(22), 2022.

[35] W.M. Grady, M.J. Samotyj, and A.H. Noyola. Survey of Active Power Line Conditioning Methodologies. *IEEE Transactions on Power Delivery*, 5(3):1536–1542, 1990.

[36] H. Akagi. New Trends in Active Filters for Power Conditioning. *IEEE Transactions on Industry Applications*, 32(6):1312–1322, 1996.

[37] B. Singh, K. Al-Haddad, and A. Chandra. A New Control Approach to Three-Phase Active Filter for Harmonics and Reactive Power Compensation. *IEEE Transactions on Power Systems*, 13(1):133–138, 1998.

[38] Dayi Li, Tingkang Wang, Wenhao Pan, Xinzhi Ding, and Jie Gong. A Comprehensive Review of Improving Power Quality Using Active Power Filters. *Electric Power Systems Research*, 199:107389, 2021.

[39] M. Liserre, F. Blaabjerg, and S. Hansen. Design and control of an LCL-filter-based three-phase active rectifier. *IEEE Transactions on Industry Applications*, 41(5):1281–1291, 2005.

[40] Vincenzo Mallemaci, Fabio Mandrile, Alessia Camboni, Enrico Carpaneto, and Radu Bojoi. Grid-Following Virtual Synchronous Machines: A valid solution fulfilling the Newest Grid Codes Regarding the Reactive Grid Support During Faults. In *2024 IEEE 22nd Mediterranean Electrotechnical Conference (MELECON)*, pages 1169–1174, 2024.

[41] Hans-Peter Beck and Ralf Hesse. Virtual Synchronous Machine. In *Proc. 9th Int. Conf. Elect. Power Qual. Utilisation*, pages 1–6, 2007.

[42] Yong Chen, Ralf Hesse, Dirk Turschner, and Hans-Peter Beck. Dynamic Properties of the Virtual Synchronous Machine (VISMA). *Renewable Energies and Power Quality Journal*, 9(1):755–759, 2011.

[43] Weiyi Zhang, Andrés Tarraso, Joan Rocabert, Alvaro Luna, J. Ignacio Candela, and Pedro Rodriguez. Frequency Support Properties of the Synchronous Power Control for Grid-Connected Converters. *IEEE Transactions on Industry Applications*, 55(5):5178–5189, 2019.

[44] M.P.N van Wesenbeeck, S.W.H. de Haan, P. Varela, and K. Visscher. Grid Tied Converter with Virtual Kinetic Storage. In *2009 IEEE Bucharest PowerTech*, pages 1–7, 2009.

[45] Yuko Hirase, Kazushige Sugimoto, Kenichi Sakimoto, and Toshifumi Ise. Analysis of Resonance in Microgrids and Effects of System Frequency Stabilization Using a Virtual Synchronous Generator. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 4(4):1287–1298, 2016.

[46] Fabio Mandrile, Enrico Carpaneto, and Radu Bojoi. Grid-Feeding Inverter with Simplified Virtual Synchronous Compensator Providing Grid Services and Grid Support. *IEEE Trans. Ind. Appl.*, 57(1):559–569, January 2021.

[47] Zeev Kustanovich, Shivprasad Shivratri, Hang Yin, Florian Reissner, and George Weiss. Synchronverters With Fast Current Loops. *IEEE Transactions on Industrial Electronics*, 70(11):11357–11367, 2023.

[48] Qing-Chang Zhong and George Weiss. Synchronverters: Inverters That Mimic Synchronous Generators. *IEEE Transactions on Industrial Electronics*, 58(4):1259–1267, 2011.

[49] K. Sakimoto, Y. Miura, and T. Ise. Stabilization of a Power System with a Distributed Generator by a Virtual Synchronous Generator Function. In *8th International Conference on Power Electronics - ECCE Asia*, pages 1498–1505, 2011.

[50] Yong Chen, Ralf Hesse, Dirk Turschner, and Hans-Peter Beck. Comparison of Methods for Implementing Virtual Synchronous Machine on Inverters. *Renewable Energies and Power Quality Journal*, 10(6):734–739, 2012.

[51] Salvatore D'Arco, Jon Are Suul, and Olav B. Fosso. Control System Tuning and Stability Analysis of Virtual Synchronous Machines. In *2013 IEEE Energy Conversion Congress and Exposition*, pages 2664–2671, 2013.

[52] Mohammad Ebrahimi, S. Ali Khajehoddin, and Masoud Karimi-Ghartemani. An Improved Damping Method for Virtual Synchronous Machines. *IEEE Transactions on Sustainable Energy*, 10(3):1491–1500, 2019.

[53] Fabio Mandrile, Vincenzo Mallemaci, Enrico Carpaneto, and Radu Bojoi. Lead-Lag Filter-Based Damping of Virtual Synchronous Machines. *IEEE Transactions on Industry Applications*, 59(6):6900–6913, 2023.

[54] Salvatore D'Arco, Jon Are Suul, and Olav B. Fosso. A Virtual Synchronous Machine Implementation for Distributed Control of Power Converters in SmartGrids. *Electric Power Syst. Res.*, 122:180–197, 2015.

[55] Fabio Mandrile, Enrico Carpaneto, Eric Armando, and Radu Bojoi. Simple Tuning Method of Virtual Synchronous Generators Reactive Control. In *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 2779–2785, 2020.

[56] Vincenzo Mallemaci, Fabio Mandrile, Enrico Carpaneto, and Radu Bojoi. Simplified Virtual Synchronous Compensator with Grid–Forming Capability. *IEEE Transactions on Industry Applications*, 59(5):6203–6219, 2023.

[57] Alessandro Roveri, Vincenzo Mallemaci, Fabio Mandrile, and Radu Bojoi. Power Decoupling Methods for Grid Support Provided by Ultra-Fast Bidirectional Chargers. *IEEE Open Journal of Industry Applications*, 6:107–119, 2025.

[58] Alessandro Roveri, Vincenzo Mallemaci, Fabio Mandrile, and Radu Bojoi. Power Decoupling Method for Grid Inertial Support Provided by Ultra-Fast Bidirectional Chargers. In *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 6544–6546, 2023.

[59] Mingxuan Li, Yue Wang, Weihao Hu, Sirui Shu, Peng Yu, Zhenyuan Zhang, and Frede Blaabjerg. Unified Modeling and Analysis of Dynamic Power Coupling for Grid-Forming Converters. *IEEE Transactions on Power Electronics*, 37(2):2321–2337, 2022.

[60] Kotub Uddin, Andrew D. Moore, Anup Barai, and James Marco. The Effects of High Frequency Current Ripple on Electric Vehicle Battery Performance. *Applied Energy*, 178:142–154, 2016.

[61] J.M. Guerrero, Luis Garcia de Vicuna, J. Matas, M. Castilla, and J. Miret. Output Impedance Design of Parallel-Cconnected UPS Inverters with Wireless Load-Sharing Control. *IEEE Transactions on Industrial Electronics*, 52(4):1126–1135, 2005.

[62] Hisham Mahmood, Dennis Michaelson, and Jin Jiang. Accurate Reactive Power Sharing in an Islanded Microgrid Using Adaptive Virtual Impedances. *IEEE Transactions on Power Electronics*, 30(3):1605–1617, 2015.

[63] Tiliang Wen, Donghai Zhu, Xudong Zou, Bingchen Jiang, Li Peng, and Yong Kang. Power Coupling Mechanism Analysis and Improved Decoupling Control for Virtual Synchronous Generator. *IEEE Transactions on Power Electronics*, 36(3):3028–3041, 2021.

[64] Joan Rocabert, Alvaro Luna, Frede Blaabjerg, and Pedro Rodríguez. Control of Power Converters in AC Microgrids. *IEEE Transactions on Power Electronics*, 27(11):4734–4749, 2012.

[65] Teng Wu, Zeng Liu, Jinjun Liu, Shike Wang, and Zhiyuan You. A Unified Virtual Power Decoupling Method for Droop-Controlled Parallel Inverters in Microgrids. *IEEE Transactions on Power Electronics*, 31(8):5587–5603, 2016.

[66] Xiangwu Yan and Ye Zhang. Power Coupling Analysis of Inverters Based on Relative Gain Method and Decoupling Control Based on Feedforward Compensation. In *International Conference on Renewable Power Generation (RPG 2015)*, pages 1–5, 2015.

[67] Mingxuan Li, Yue Wang, Ningyi Xu, Wenti Wang, Yonghui Liu, Hao Wang, and Yao Weizheng. A Power Decoupling Control Strategy for Droop Controlled Inverters and Virtual Synchronous Generators. In *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, pages 1713–1719, 2016.

[68] Tiliang Wen, Xudong Zou, Xiang Guo, Donghai Zhu, Li Peng, and Xuefeng Wang. Feedforward Compensation Control for Virtual Synchronous Generator to Improve Power Decoupling Capability. In *2019 14th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, pages 2528–2533, 2019.

[69] Shuan Dong and Yu Christine Chen. Reducing Transient Active- and Reactive-Power Coupling in Virtual Synchronous Generators. In *2019 IEEE 28th International Symposium on Industrial Electronics (ISIE)*, pages 1090–1095, 2019.

[70] Bin Li, Lin Zhou, Xirui Yu, Chen Zheng, and Jinhong Liu. Improved Power Decoupling Control Strategy Based on Virtual Synchronous Generator. *IET Power Electronics*, 10(4):462–470, 2017.

[71] Mingxuan Li, Yue Wang, Yonghui Liu, Ningyi Xu, Sirui Shu, and Wanjun Lei. Enhanced Power Decoupling Strategy for Virtual Synchronous Generator. *IEEE Access*, 8:73601–73613, 2020.

[72] Salvatore D'Arco and Jon Are Suul. Phase Angle Feed-Forward Control for Improving the Power Reference Tracking of Virtual Synchronous Machines. *IEEE Transactions on Industry Applications*, 60(1):851–864, 2024.

[73] Andong Liu, Jun Liu, and Qiong Wu. Improvement of VSG Transient Performance Based on Power Feedforward Decoupling Control. *IET Generation, Transmission & Distribution*, 16(20):4080–4095, 2022.

[74] Ningbo Dong, Mengfei Li, Xiaofei Chang, Wei Zhang, Huan Yang, and Rongxiang Zhao. Robust Power Decoupling Based on Feedforward Decoupling and Extended State Observers for Virtual Synchronous Generator in Weak Grid. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 11(1):576–587, 2023.

[75] Alessandro Roveri, Vincenzo Mallemaci, Fabio Mandrile, and Radu Bojoi. Enhanced Virtual Synchronous Machine With Online Grid Impedance Estimation. *IEEE Open Journal of Industry Applications*, 6:427–444, 2025.

[76] Mathieu Kervyn De Meerendre, Eduardo Prieto-Araujo, Khaled H. Ahmed, Oriol Gomis-Bellmunt, Lie Xu, and Agustí Egea-Àlvarez. Review of Local Network Impedance Estimation Techniques. *IEEE Access*, 8:213647–213661, 2020.

[77] V. Mallemaci. Next Generation Grid-Tied Inverters with Virtual Synchronous Machine Features for Grid Services and Grid Support, 2024.

[78] Alessandro Roveri, Vincenzo Mallemaci, Fabio Mandrile, and Radu Bojoi. A Virtual Synchronous Machine Based Algorithm for Online Grid Impedance Estimation. In *2024 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 740–747, 2024.

[79] Alessandro Roveri, Federico Campanelli, Fabio Mandrile, and Radu Bojoi. Improved Virtual Synchronous Machine with Grid Impedance Estimator for Islanding Detection. In *PCIM Conference 2026; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2026, *Accepted for Publication*.

[80] Mauricio Cespedes and Jian Sun. Adaptive Control of Grid-Connected Inverters Based on Online Grid Impedance Measurements. *IEEE Transactions on Sustainable Energy*, 5(2):516–523, 2014.

[81] F. Reißner and G. Weiss. Robust and Adaptive tuning of PI Current Controllers for Grid Forming Inverters. *IEEE Open Journal of the Industrial Electronics Society*, pages 1–14, 2024.

[82] Abdelhady Ghanem, Mohamed Rashed, Mark Sumner, M. A. El-sayes, and I. I. I. Mansy. Grid Impedance Estimation for Islanding Detection and Adaptive Control of Converters. In *8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, pages 1–6, 2016.

[83] Nils Hoffmann and Friedrich Wilhelm Fuchs. Minimal Invasive Equivalent Grid Impedance Estimation in Inductive–Resistive Power Networks Using Extended Kalman Filter. *IEEE Transactions on Power Electronics*, 29(2):631–641, 2014.

[84] Shihan Liu, Yanjun Li, Ji Xiang, and Feifan Ji. Islanding Detection Method Based on System Identification. *IET Power Electronics*, 9(10):2095–2102, 2016.

[85] L. Asiminoaei, R. Teodorescu, F. Blaabjerg, and U. Borup. Implementation and Test of an Online Embedded Grid Impedance Estimation Technique for PV Inverters. *IEEE Transactions on Industrial Electronics*, 52(4):1136–1144, 2005.

[86] Denis Keuton Alves, Ricardo L. A. Ribeiro, Flavio Bezerra Costa, and Thiago Oliveira Alves Rocha. Real-Time Wavelet-Based Grid Impedance Estimation Method. *IEEE Transactions on Industrial Electronics*, 66(10):8263–8265, 2019.

[87] Mihai Ciobotaru, Remus Teodorescu, and Frede Blaabjerg. On-Line Grid Impedance Estimation Based on Harmonic Injection for Grid-Connected PV Inverter. In *2007 IEEE International Symposium on Industrial Electronics*, pages 2437–2442, 2007.

[88] Yanqi Cheng, Weimin Wu, Yong Yang, Eftichios Koutroulis, Henry Shu-Hung Chung, Marco Liserre, and Frede Blaabjerg. Zero-Sequence Voltage Injection-Based Grid Impedance Estimation Method for Three-Phase Four-Wire DC/AC Grid-Connected Inverter. *IEEE Transactions on Industrial Electronics*, 71(7):7273–7279, 2024.

[89] Arpan Malkhandi, Nilanjan Senroy, and Sukumar Mishra. A Dynamic Model of Impedance for Online Thevenin's Equivalent Estimation. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 69(1):194–198, 2022.

[90] Mauricio Céspedes and Jian Sun. Online Grid Impedance Identification for Adaptive Control of Grid-Connected Inverters. In *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 914–921, 2012.

[91] Nabil Mohammed and Mihai Ciobotaru. Fast and Accurate Grid Impedance Estimation Approach for Stability Analysis of Grid-Connected Inverters. *Electric Power Systems Research*, 207:107831, 2022.

[92] Pablo Garcia, Mark Sumner, Angel Navarro-Rodríguez, Juan M. Guerrero, and Jorge García. Observer-Based Pulsed Signal Injection for Grid Impedance Estimation in Three-Phase Systems. *IEEE Transactions on Industrial Electronics*, 65(10):7888–7899, 2018.

[93] Tomi Roinila, Matti Vilkko, and Jian Sun. Online Grid Impedance Measurement Using Discrete-Interval Binary Sequence Injection. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2(4):985–993, 2014.

[94] Roni Luhtala, Tomi Roinila, and Tuomas Messo. Implementation of Real-Time Impedance-Based Stability Assessment of Grid-Connected Systems Using MIMO-Identification Techniques. *IEEE Transactions on Industry Applications*, 54(5):5054–5063, 2018.

[95] Tomi Roinila and Tuomas Messo. Online Grid-Impedance Measurement Using Ternary-Sequence Injection. *IEEE Transactions on Industry Applications*, 54(5):5097–5103, 2018.

[96] Giovanni Marini, Alessandro Lidozzi, Marco di Benedetto, and Luca Solero. White Noise Based Synchronous Active DC and AC Impedance Estimation From Front-End Inverters. *IEEE Transactions on Energy Conversion*, 39(2):930–940, 2024.

[97] Marco Liserre, Frede Blaabjerg, and Remus Teodorescu. Grid Impedance Estimation via Excitation of LCL - Filter Resonance. *IEEE Transactions on Industry Applications*, 43(5):1401–1407, 2007.

[98] Adrian V. Timbus, Pedro Rodriguez, Remus Teodorescu, and Mihai Ciobotaru. Line Impedance Estimation Using Active and Reactive Power Variations. In *2007 IEEE Power Electronics Specialists Conference*, pages 1273–1279, 2007.

[99] Mihai Ciobotaru, Remus Teodorescu, Pedro Rodriguez, Adrian Timbus, and Frede Blaabjerg. Online Grid Impedance Estimation for Single-Phase Grid-Connected Systems Using PQ Variations. In *2007 IEEE Power Electronics Specialists Conference*, pages 2306–2312, 2007.

[100] Haoxin Yang and Yi Tang. A Noninvasive Grid Impedance Estimation Method With Phase-Lock Loops. *IEEE Transactions on Power Electronics*, 39(8):9059–9065, 2024.

[101] Je-Hee Cho, Ki-Young Choi, Yong-Wook Kim, and Rae-Young Kim. A Novel P-Q Variations Method Using a Decoupled Injection of Reference Currents for a Precise Estimation of Grid Impedance. In *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 5059–5064, 2014.

[102] Nabil Mohammed, Tamas Kerekes, and Mihai Ciobotaru. An Online Event-Based Grid Impedance Estimation Technique Using Grid-Connected Inverters. *IEEE Transactions on Power Electronics*, 36(5):6106–6117, 2021.

[103] Jingyang Fang, Han Deng, and Stefan M. Goetz. Grid Impedance Estimation Through Grid-Forming Power Converters. *IEEE Transactions on Power Electronics*, 36(2):2094–2104, 2021.

[104] Jianwen Sun, Jingrong Yu, Juncheng Qiu, and Yishuo Wang. Transient-Responses-Based Grid Impedance Estimation for Grid-Forming Converters. In *2022 4th International Conference on Electrical Engineering and Control Technologies (CEECT)*, pages 741–745, 2022.

[105] Jingrong Yu, Wenjing Liu, Jianwen Sun, Fu Zhang, and Yuxiang Yang. An improved grid impedance estimator for grid-forming converters in consideration of controller dynamics. *International Journal of Electrical Power & Energy Systems*, 154:109424, 2023.

[106] Nabil Mohammed, Mohammad Hasan Ravanji, Weihua Zhou, and Behrooz Bahrani. Online Grid Impedance Estimation-Based Adaptive Control of Virtual Synchronous Generators Considering Strong and Weak Grid Conditions. *IEEE Transactions on Sustainable Energy*, 14(1):673–687, 2023.

[107] Florian Reißner and George Weiss. Grid Impedance Measurement for Inverters with Current Controllers and Virtual Impedances. In *2024 22nd International Conference on Intelligent Systems Applications to Power Systems (ISAP)*, pages 1–6, 2024.

[108] Andres Tarraso, Jose Ignacio Candela, Joan Rocabert, and Pedro Rodríguez. Selective Harmonic Compensation in SPC Grid-Forming Converters for Improving Power Quality in Weak Grid. *IEEE Transactions on Power Delivery*, pages 1–11, 2024.

[109] Sohail Ahmad Ali, Sheikh Izzal Azid, Shyamal Shivneel Chand, and Maurizio Cirrincione. Online RLS Impedance Estimation - Based Adaptive Control of Virtual Synchronous Generators in Grid Forming Inverters. In *2023 International Aegean Conference on Electrical Machines and Power Electronics (ACEMP) & 2023*

International Conference on Optimization of Electrical and Electronic Equipment (OPTIM), pages 1–8, 2023.

[110] Santiago Cobreces, Emilio J. Bueno, Daniel Pizarro, Francisco J. Rodriguez, and Francisco Huerta. Grid impedance monitoring system for distributed power generation electronic interfaces. *IEEE Transactions on Instrumentation and Measurement*, 58(9):3112–3121, 2009.

[111] IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces. *IEEE Std 1547-2018 (Revision of IEEE Std 1547-2003)*, pages 1–138, 2018.

[112] IEEE Standard Conformance Test Procedures for Equipment Interconnecting Distributed Energy Resources with Electric Power Systems and Associated Interfaces. *IEEE Std 1547.1-2020*, pages 1–282, 2020.

[113] M. Tavakoli Bina and E. Pashajavid. An Efficient Procedure to Design Passive LCL-Filters for Active Power Filters. *Electric Power Systems Research*, 79(4):606–614, 2009.

[114] Yi Tang, Poh Chiang Loh, Peng Wang, Fook Hoong Choo, Feng Gao, and Frede Blaabjerg. Generalized Design of High Performance Shunt Active Power Filter With Output LCL Filter. *IEEE Transactions on Industrial Electronics*, 59(3):1443–1452, 2012.

[115] Qian Liu, Li Peng, Yong Kang, Shiying Tang, Deliang Wu, and Yu Qi. A Novel Design and Optimization Method of an LCL Filter for a Shunt Active Power Filter. *IEEE Transactions on Industrial Electronics*, 61(8):4000–4010, 2014.

[116] Lin Zhou, Zhiwen Liu, Yanchao Ji, Daoyuan Ma, Jianze Wang, and Lingda Li. A Improved Parameter Design Method of LCL APF Interface Filter. In *2020 IEEE International Conference on Artificial Intelligence and Computer Applications (ICAICA)*, pages 948–952, 2020.

[117] H. Akagi, H. Hasegawa, and T. Doumoto. Design and Performance of a Passive EMI Filter for Use with a Voltage-Source PWM Inverter Having Sinusoidal Output Voltage and Zero Common-Mode Voltage. *IEEE Transactions on Power Electronics*, 19(4):1069–1076, 2004.

[118] Srinivas Gulur, Vishnu Mahadeva Iyer, and Subhashish Bhattacharya. A CM Filter Configuration for Grid-Tied Voltage Source Converters. *IEEE Transactions on Industrial Electronics*, 67(10):8100–8111, 2020.

[119] Marcelo Lobo Heldwein, Luca Dalessandro, and Johann W. Kolar. The Three-Phase Common-Mode Inductor: Modeling and Design Issues. *IEEE Transactions on Industrial Electronics*, 58(8):3264–3274, 2011.

[120] Oscar Lopez, Francisco D. Freijedo, Alejandro G. Yepes, Pablo Fernandez-Comesana, Jano Malvar, Remus Teodorescu, and Jesus Doval-Gandoy. Eliminating Ground Current in a Transformerless Photovoltaic Application. *IEEE Transactions on Energy Conversion*, 25(1):140–147, 2010.

[121] Marcelo C. Cavalcanti, Kleber C. de Oliveira, Alexandre M. de Farias, Francisco A. S. Neves, Gustavo M. S. Azevedo, and Felipe C. Camboim. Modulation Techniques to Eliminate Leakage Currents in Transformerless Three-Phase Photovoltaic Systems. *IEEE Transactions on Industrial Electronics*, 57(4):1360–1368, 2010.

[122] Emre Un and Ahmet M. Hava. A Near-State PWM Method With Reduced Switching Losses and Reduced Common-Mode Voltage for Three-Phase Voltage Source Inverters. *IEEE Transactions on Industry Applications*, 45(2):782–793, 2009.

[123] R.I. Bojoi, G. Griva, V. Bostan, M. Guerriero, F. Farina, and F. Profumo. Current Control Strategy for Power Conditioners Using Sinusoidal Signal Integrators in Synchronous Reference Frame. *IEEE Transactions on Power Electronics*, 20(6):1402–1412, 2005.

[124] *Grid Synchronization in Single-Phase Power Converters*, chapter 4, pages 43–91. John Wiley & Sons, Ltd, 2011.

[125] Ke Ma, Shihao Xia, Yuhao Qi, Xu Cai, Yubo Song, and Frede Blaabjerg. Power-Electronics-Based Mission Profile Emulation and Test for Electric Machine Drive System—Concepts, Features, and Challenges. *IEEE Transactions on Power Electronics*, 37(7):8526–8542, 2022.

[126] R. Bojoi, E. Armando, S.G. Rosu, S. Vaschetto, and P. Soccio. Virtual Load with Common Mode Active Filtering for Power Hardware-in-the-Loop Testing of Power Electronic Converters. In *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, pages 1875–1881, 2014.

[127] P. Sandholdt, E. Ritchie, J.K. Pedersen, and R.E. Betz. A Dynamometer Performing Dynamical Emulation of Loads with Nonlinear Friction. In *Proceedings of IEEE International Symposium on Industrial Electronics*, volume 2, pages 873–878 vol.2, 1996.

[128] Till Boller and Ralph M. Kennel. Virtual Machine — A Hardware in the Loop Test for Drive Inverters. In *2009 13th European Conference on Power Electronics and Applications*, pages 1–5, 2009.

[129] Alessandro Roveri, Vincenzo Mallemaci, Fabio Mandrile, and Radu Bojoi. Design Guidelines for Active Power Filters Operating in Disturbed Industrial Environments. *IEEE Open Journal of Industry Applications*, 7:216–237, 2026.

[130] Alessandro Roveri, Fabio Mandrile, Vincenzo Mallemaci, and Radu Bojoi. Discontinuous PWM Modulation for Active Power Filters Operating in Disturbed Environments. In *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 6429–6436, 2023.

[131] Cristian Lascu, Lucian Asiminoaei, Ion Boldea, and Frede Blaabjerg. High Performance Current Controller for Selective Harmonic Compensation in Active Power Filters. *IEEE Transactions on Power Electronics*, 22(5):1826–1835, 2007.

[132] A.M. Hava, R.J. Kerkman, and T.A. Lipo. A high-performance generalized discontinuous PWM algorithm. *IEEE Transactions on Industry Applications*, 34(5):1059–1071, 1998.

[133] J.W. Kolar, H. Ertl, and F.C. Zach. Influence of the Modulation Method on the Conduction and Switching Losses of a PWM Converter System. *IEEE Transactions on Industry Applications*, 27(6):1063–1075, 1991.

[134] The Dung Nguyen, Julien Hobraiche, Nicolas Patin, Guy Friedrich, and Jean-Paul Vilain. A Direct Digital Technique Implementation of General Discontinuous Pulse Width Modulation Strategy. *IEEE Transactions on Industrial Electronics*, 58(9):4445–4454, 2011.

[135] Junhyuk Lee, Myeong-Won Kim, and Jung-Wook Park. Carrier Selection Strategy of Generalized Discontinuous PWM Method for Current Reduction in DC-Link Capacitors of VSI. *IEEE Transactions on Power Electronics*, 37(9):10428–10442, 2022.

[136] Baris Ciftci and Ahmet M. Hava. Performance Evaluation and Selection of PWM Switching and Control Methods for Grid Connected Modular Multilevel Converters. In *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 3622–3629, 2015.

[137] Hanwei Xu, Lie Xu, Kui Wang, Zedong Zheng, and Yongdong Li. Switching Losses Reduction of Grid-tied Inverters With Variable Switching Frequency Discontinuous PWM. In *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 1567–1573, 2019.

[138] Zeljko Jankovic, Puneeth Murthy, Lixiang Wei, and Adel Nasiri. Dynamic Discontinuous PWM for Grid-tied Inverter Applications. In *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 5032–5039, 2020.

[139] Petros Karamanakos, Mehrdad Nahalparvari, and Tobias Geyer. Fixed Switching Frequency Direct Model Predictive Control With Continuous and Discontinuous Modulation for Grid-Tied Converters With LCL Filters. *IEEE Transactions on Control Systems Technology*, 29(4):1503–1518, 2021.

[140] Lucian Asiminoaei, Pedro Rodriguez, and Frede Blaabjerg. Application of Discontinuous PWMModulation in Active Power Filters. *IEEE Transactions on Power Electronics*, 23(4):1692–1706, 2008.

[141] A.W. Kelley and W.F. Yadusky. Rectifier for Minimum Line-Current Harmonics and Maximum Power Factor. *IEEE Transactions on Power Electronics*, 7(2):332–341, 1992.

[142] Predrag Pejovic and Johann W. Kolar. Exact Analysis of Three-Phase Rectifiers With Constant Voltage Loads. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 55(8):743–747, 2008.

[143] Mitsubishi Electric. CM450DX-24T1/CM450DXP-24T1 Datasheet, January 2025.

[144] A.M. Hava, R.J. Kerkman, and T.A. Lipo. Simple Analytical and Graphical Methods for Carrier-Based PWM-VSI Drives. *IEEE Transactions on Power Electronics*, 14(1):49–61, 1999.

[145] Sandro Rubino. Advanced Electric Drives: Modeling, Design, and Implementation - Part I. University Lecture – PhD Program in Electrical, Electronics and Communications Engineering, Politecnico di Torino, 2025.

[146] Sandro Rubino. Advanced Electric Drives: Modeling, Design, and Implementation - Part II. University Lecture – PhD Program in Electrical, Electronics and Communications Engineering, Politecnico di Torino, 2025.

[147] Remus Narcis Beres, Xiongfei Wang, Marco Liserre, Frede Blaabjerg, and Claus Leth Bak. A Review of Passive Power Filters for Three-Phase Grid-Connected Voltage-Source Converters. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 4(1):54–69, 2016.

[148] Sampath Jayalath and Moin Hanif. Generalized LCL-Filter Design Algorithm for Grid-Connected Voltage-Source Inverter. *IEEE Transactions on Industrial Electronics*, 64(3):1905–1915, 2017.

[149] Davide Cittanti, Fabio Mandrile, Matteo Gregorio, and Radu Bojoi. Design Space Optimization of a Three-Phase LCL Filter for Electric Vehicle Ultra-Fast Battery Charging. *Energies*, 14(5), 2021.

[150] Emre Kantar and Ahmet M. Hava. Optimal Design of Grid-Connected Voltage-Source Converters Considering Cost and Operating Factors. *IEEE Transactions on Industrial Electronics*, 63(9):5336–5347, 2016.

[151] Jörg Dannehl, Friedrich Wilhelm Fuchs, Steffan Hansen, and Paul Bach Thøgersen. Investigation of Active Damping Approaches for PI-Based Current Control of Grid-Connected Pulse Width Modulation Converters With LCL Filters. *IEEE Transactions on Industry Applications*, 46(4):1509–1517, 2010.

[152] Rafael Peña-Alzola, Marco Liserre, Frede Blaabjerg, Martin Ordonez, and Yongheng Yang. LCL-Filter Design for Robust Active Damping in Grid-Connected Converters. *IEEE Transactions on Industrial Informatics*, 10(4):2192–2203, 2014.

[153] Alessia Camboni, Alessandro Roveri, Fabio Mandrile, and Radu Bojoi. Simple Active Damping Solution for Industrial Grid-Tied Inverters Using LCL Filters. In *2025 IEEE Energy Conversion Conference Congress and Exposition (ECCE)*, pages 1–7, 2025.

List of Figures

List of Tables