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12 October 2024

A 6-to-38Gb/s Capture-Range Bang-Bang Clock and Data Recovery Circuit with Deliberate-Current-Mismatch Frequency Detection and Interpolation-Based Multi-Phase Clock Generation

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Abstract

This paper reports a bang-bang clock and data recovery circuit (BBCDR) with an ultra-wide capture range. The circuit exhibits automatic frequency capture and phase locking over a wide 6-to-38Gb/s range without using a frequency detector, allowed by a recently proposed deliberate-current-mismatch technique. Moreover, we accurately obtain an eight-phase clock through analog interpolation of quadrature signals over the whole wide frequency range, by introducing a tunable capacitor array before an inverter-based phase interpolator. A 65-nm prototype of the developed BBCDR occupies an area of 0.07mm^2 and attains a bit error rate of less than 10^{-12} under a continuously variable input frequency, with a total power consumption of 24.6 mW for a 32-Gb/s non-return-zero input, thus leading to 0.769-pJ/bit energy efficiency.

Index Terms

Bang-Bang clock and data recovery (BBCDR), wide capture range, phase interpolator (PI), frequency detector (FD), switched-capacitor (SC) array, hybrid control circuit (HCC), current mismatch, ring oscillator (RO), R-2R digital-to-analog converter (DAC).

I. Introduction

The exponential growth in data transmission over the last decades is driving a swift evolution in wireline receivers [1-2] with serializer-deserializer (SerDes) systems experiencing a continuously increasing performance demand.

In this scenario, multi tens-of-gigabits-per-second SerDes are necessary to accommodate the increasing data traffic quest in a limited number of channels. Moreover, flexible wireline communication systems require a wide capture range [3] to meet the different imperatives of a variety of standards and applications. Meeting both high-speed and wide-capture-range requirements simultaneously without compromising reliability and power consumption is extremely challenging and an area of intense research recently.

To cover the input data format from a few gigabits per second to tens of gigabits per second, the "analog" receiver necessitates a clock and data recovery (CDR) circuit with a very wide frequency capture capability [4]. Previous work [5] employs a low-noise crystal as a reference clock, which increases the overall cost and the design complexity. Reference-less CDR mainly targets applications that are not feasible to use an external crystal [6]. However, the reference-less CDR must extract the frequency and phase information from the incoming data, which makes it hard to achieve wide-range frequency-acquisition ability. The state-of-the-art CDRs use a separate frequency detector (FD) [7-13] and dual-loop structure [14-19] to extend the capture range, thus increasing the design complexity and hardware cost. Another evolution has opted for an analog-to-digital converter (ADC)-based scheme, and a great amount of signal processing in the digital domain [20-24], which leads to a large power consumption and loop latency. Even if some solutions have been proposed in [25-31], they either require complex loop topologies [25,31] and large power consumption [26-28] or result in a limited capture range [29-30]. To tackle these issues, we have developed a deliberate-current-mismatch frequency acquisition technique in [32-35] that is applied in a single-loop CDR without an external reference and separate FD. In this paper, we further enhanced the technique presented in [32]-[35] to a wider frequency acquisition range to satisfy multi-standard applications. Considering that the frequency capture range in the [32]-[35] technique was limited by the clock generation concept, we propose

an interpolation-based multi-phase clock generation to achieve a wider frequency acquisition range as well as a group of band preset signals for fast frequency acquisition at a high data rate. The proposed wide-capture-range CDR enables fast acquisition speed with low hardware cost, low power consumption, and high energy efficiency.

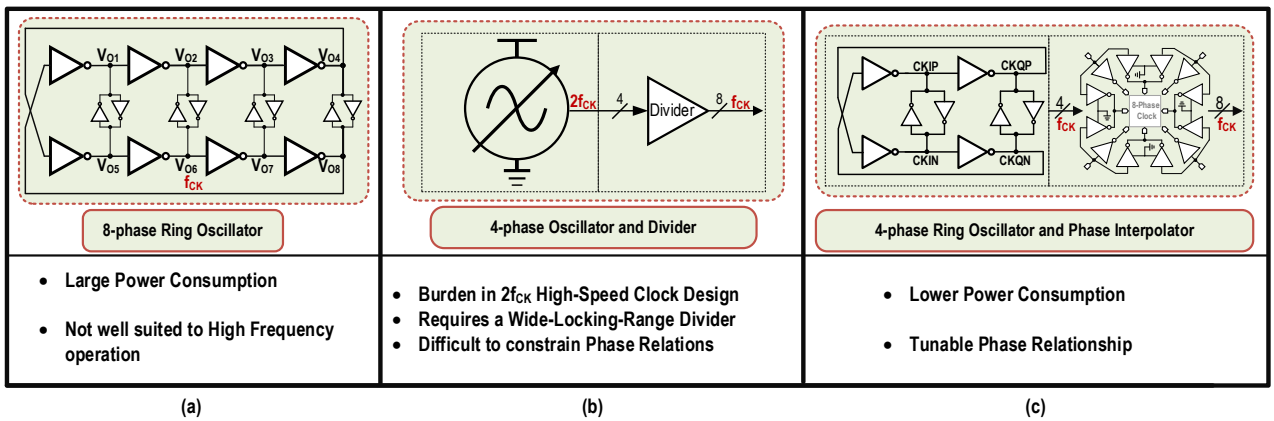


Fig. 1. Commonly-used eight-phase clock generation schemes: (a) eight-phase ring oscillator (b) the divider follows the four-phase oscillator and (c) the phase interpolator follows the four-phase ring oscillator.

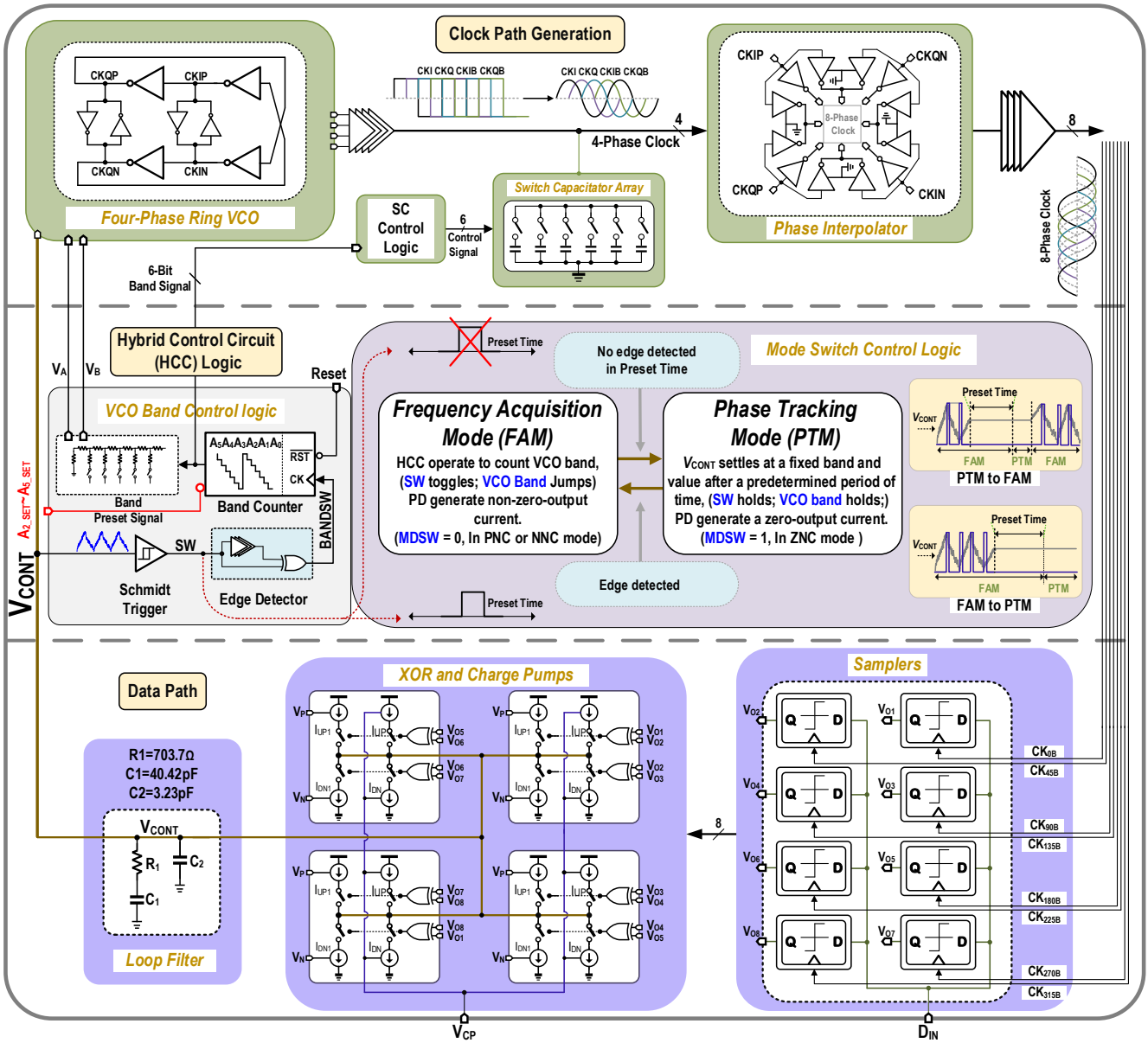
To relieve the constraints on clock generation, wide-range CDR designs commonly use half-rate and quarter-rate schemes. These structures can effectively reduce the requested oscillator frequency to a half or a quarter, relieving the design pressure on clock generation. However, this scheme requires multi-phase clock signals. Furthermore, in a bang-bang clock and data recovery (BBCDR) with a 2x oversampling ratio, as proposed in [13], the clock phase needs to double for the phase detection function [34-36].

Fig. 1 illustrates multi-phase clock generation used in different clock generation schemes. Fig. 1(a) exhibits eight inverter-based cells to build an eight-phase voltage-controlled ring oscillator (RO). This scheme commonly uses a current-starved RO to realize a wide frequency output, resulting in large power consumption, which negatively impacts the CDR energy efficiency. In addition, the eight-phase RO has intrinsic frequency limitations that render it unsuitable to operate at a very high-frequency f_{CK}. As an alternative, a four-phase oscillator generates a quadrature clock signal at a double frequency $2f_{CK}$ [37], starting from an eight-phase clock obtained with a frequency divider [Fig. 1(b)]. However, such a clock

generation scheme also has several drawbacks: first, it requires an oscillator operating at a frequency $2f_{CK}$, much higher than the target clock frequency f_{CK}. Additionally, it also needs a frequency divider with a wide frequency range, which increases the design complexity. Finally, with the divider operating in an open loop, it does not precisely constrain the phase relationship of the generated clock signals. An alternative solution consists in adopting a current-starved RO used to generate a quadrature clock and then obtaining an eight-phase clock signal by interpolation, as in Fig. 1(c) [38]. Compared to Fig. 1(a), the adoption of a four-phase RO greatly reduces power consumption, leading to better energy efficiency. Besides, when compared with the scheme in Fig. 1(b), both the four-phase RO and eight-phase clocks are at the same frequency f_{CK}, which avoids the burden of a very high-frequency oscillator.

In this paper, we present an ultra-wide-capture-range BBCDR structure covering a 6-to-38Gb/s input data rate with minimal hardware cost and low power consumption. The proposed BBCDR incorporates a quarter-rate scheme and a bang-bang phase detector (BBPD), which entails an eight-phase clock signal. Aiming to eliminate the problems of the multi-phase clocks in Figs.1(a) and (b), we adopt the scheme in Fig. 1(c) in the proposed BBCDR and an analog, a flexible, low-cost inverter-based PI with its intrinsic frequency range limitations originally overcome by the configurable switched capacitor (SC) array on the output of the clock buffers driving the succeeding PI.

The remaining paper has the following organization: Section II details the top architecture of the proposed BBCDR. Then, Section III discloses the circuit implementation of the BBCDR, while Section IV validates the effectiveness of the proposed scheme based on measurements of a 65-nm CMOS prototype. Finally, Section V provides the summary and conclusions.



SW	Schmitt trigger output; SW=0,loop in PNC mode; SW=1,loop in NNC mode;	**MDSW**	Mode switch signal; MDSW=0, FAM mode; MDSW=1,PTM mode;	**FAM**	Frequency acquisition mode	**PTM**	Phase tracking mode
Reset	Global reset signal	**BANDSW**	Edge output, band switch signal	**PNC**	Positive net current	**NNC**	Negative net current

Fig. 2. The top architecture of the proposed BBCDR.

II. Top Architecture of The Proposed BBCDR

Fig. 2 outlines the top architecture of the proposed BBCDR. It consists of three main blocks: the multi-phase clock generation block, the hybrid control circuit (HCC) logic, and the data path, whose structure and operation we describe in detail next.

A. Multi-Phase Clock Generation

We employ a four-phase RO in the proposed BBCDR to enable a wide clock-frequency range at low power consumption, deriving an eight-phase clock from its quadrature outputs by an inverter-based PI module. Due to the wide range of the RO output, the four-phase clock is nearly sinusoidal at high frequencies, while it is closer to a square wave with steep transitions at low frequencies. Such waveforms, however, are not suitable for the inverter-based PI, which relies on smooth, nearly sinusoidal phase inputs. Aiming to enable inverter-based PI over a wide frequency range, we introduce a digitally-controlled switched capacitor (SC) array, automatically tuned by the BBCDR controller to offer a different capacitive load to the clock buffers at different frequencies, to ensure that the PI has an approximately sinusoidal clock signal as input over the whole frequency range. To keep the SC array from affecting the RO frequency, we use a pair of differential buffers to isolate the RO and SC loads.

B. Quarter-Rate Data Path

Fig. 2 shows the data path in the BBCDR loop in the lower part. Eight double-tail flip-flops (DT FF) perform data retiming. DT FF are preferred over other topologies for their higher robustness. Moreover, the transistor sizes in the regeneration phase of the FF are increased to support high-speed data transmission. The circuit feeds the retimed data into the XOR gates and the charge pump (CP) blocks: the XOR gates compare the data signals sampled by adjacent phase clocks and perform phase detection of the 8-phase BBPD, while the CP module [39], operating as a trans-conductor, converts the phase difference between the discriminated clock and data into a current pulse.

The output current of the CP block charges or discharges the second-order loop filter (LF), in such a way that a real-time current pulse signal carries the information about the phase difference between the clock and data, which adjusts the VCO control voltage (V_{CONT}) dynamically through the loop filter to control the VCO in close-loop.

C. Hybrid Control Circuit (HCC)

The hybrid control circuit (HCC) mainly comprises a hybrid logic module, and is in charge of the generation of the band control signals for automatic band switching and continuous frequency acquisition. For this purpose, the HCC block consists of two parts: the first part is the VCO band control logic, including a binary counter (band counter), whose content corresponds to the VCO band, and a comparator with hysteresis driven by the V_{CONT} signal from the data path, whose output transitions drive the clock of the band counter. The band counter can be also preset by the external signals (A_{2_SET}~A_{5_SET}), for fast frequency locking. The second part is the mode switch control logic, which is in charge to control the alternate selection between negative and positive SP in the CP. The HCC block interacts with both the data and the clock path, thus controlling the global mode switching and frequency acquisition.

D. Deliberate-Current-Mismatch-based FD-less Technique

The proposed BBCDR is based on a deliberate-current-mismatch-based FD-less technique proposed in our previous paper [32-35] to achieve frequency capture at low hardware cost and low power consumption. Besides, we insert a non-zero SP to retrofit the symmetric PD curve, so that the PD generates a non-zero net output within a cycle slip [40]. For this aim, we insert an additional CP branch (indicated as the SP CP hereafter) controlled by the bias voltages V_{P} and V_{N} (Fig. 3), in parallel with the main CP circuit. Depending on the bias voltages V_{P} and V_{N}, digitally selected, we can operate the circuit in three modes: the positive-net-current (PNC) mode, when only the upper SP CP branch is on, the negative-net-current (NNC) mode, when

only the lower SP CP branch is on, and the zero-net-current output (ZNC) mode, in which both the branches of the SP CP are off. The PNC and NNC non-zero output modes activated during the frequency acquisition mode (FAM) allow FD-less frequency capture ability. By contrast, the ZNC mode activated after frequency locking and with the loop in the phase tracking mode (PTM), achieves a better jitter performance by operating the PD as a normal PD with a ZNC.

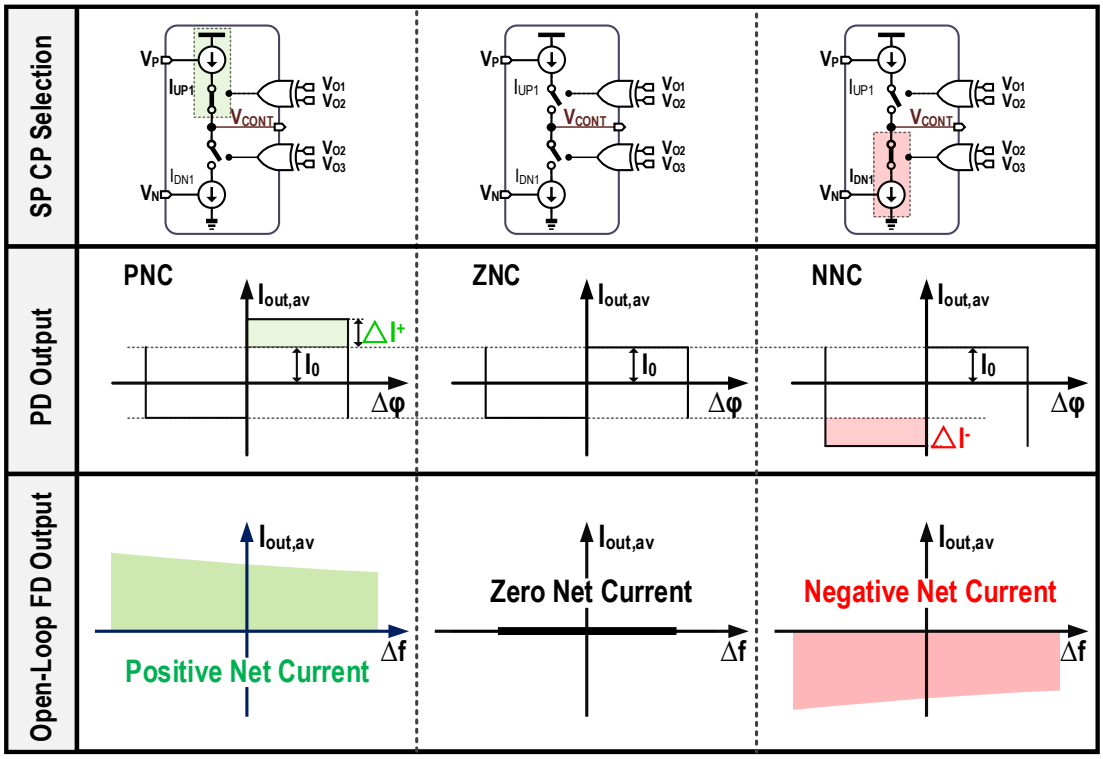


Fig. 3. Block diagram of the proposed SP-selected CP along with open-loop PD and FD curves

III. Circuit Implementation

A. Voltage-Controlled Ring Oscillator

The proposed BBCDR includes a current-starved RO that provides a quadrature clock signal, with a wide frequency tuning range. The entire four-phase oscillator consists of two identical cells, with the schematic shown in the right part of Fig. 4(a). By varying the gate voltages V_A and V_B of the bias transistors, we can control the frequency of the current-starved RO, determined by the current flowing through its branches. In the proposed cell, there are two bias transistors in each current path, such that the current flowing through

the upper and lower branches will change at the same time while changing the control voltage. This topology is suitable to obtain four-phase clock signals over a very wide tuning range as shown in Fig. 4(c). V_A and V_B are in charge of the coarse tuning in the proposed RO for band switching while V_{CONT} controls the fine-tuning after the selection of a certain band. To simplify the simulation setting, we set the sum of the bias voltages V_A and V_B as 1 V. The result shows that the operating frequency of RO varies from 1 GHz to 14 GHz. Fig. 4(d) plots the post-layout simulation results of the phase noise (PN) profile.

Within a cell, the drain terminals of the bias transistors controlled by the same voltage V_A (V_B) in different branches are tied together to control their current precisely. We can combine all the PMOS controlled by V_A and NMOS controlled by V_B. To have a symmetrical layout, we assign to each branch a pair of bias transistors of the same size.

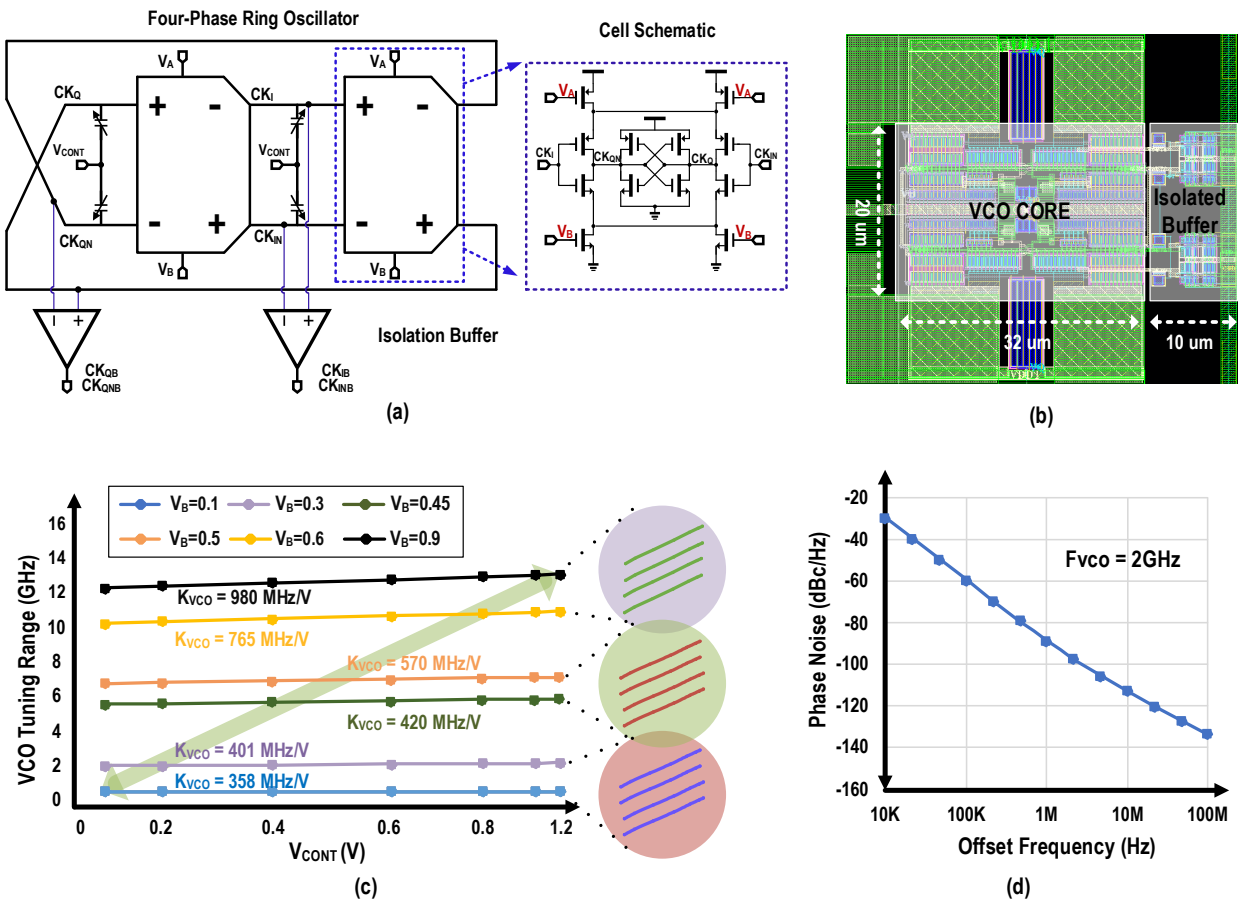
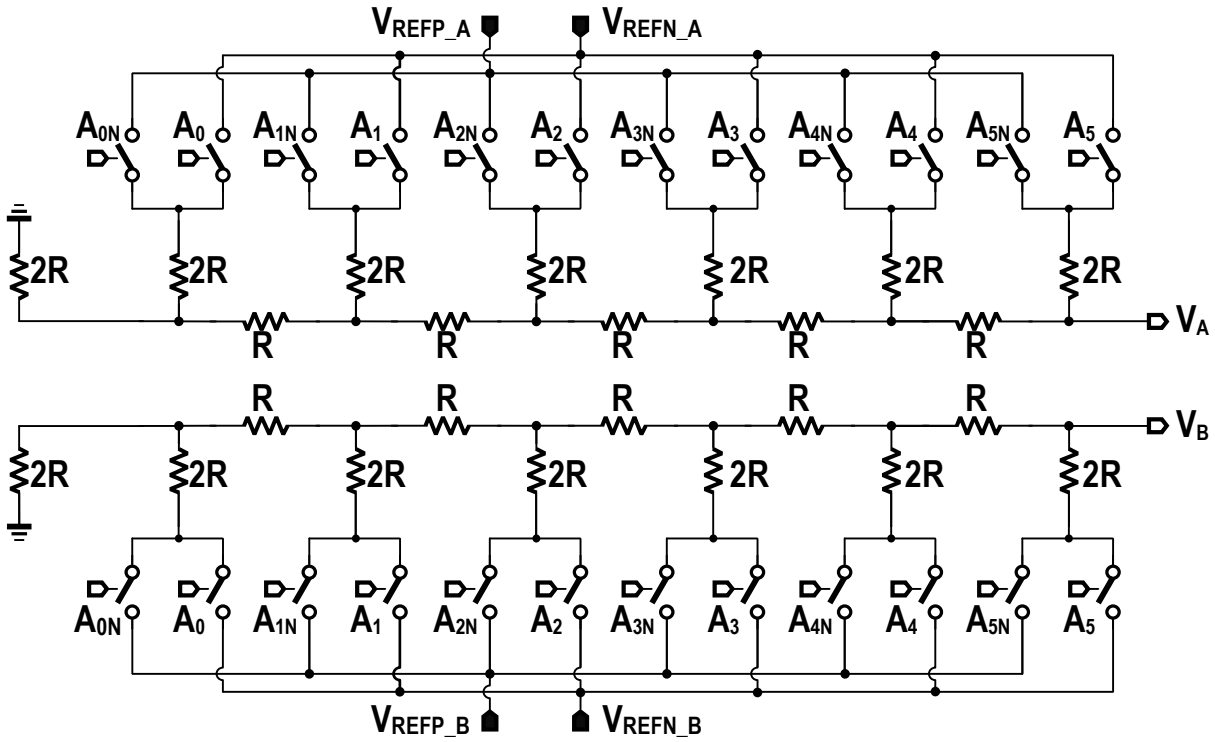
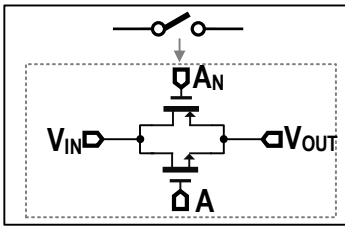


Fig. 4. (a) Schematic of the four-phase voltage-controlled RO and (b) its layout, (c) tuning range under different biases, and (d) simulated PN.

As mentioned in Section II, the insertion of an SC array at the RO output buffers smoothens the quadrature clock at low frequency, as required for proper phase interpolation. To decouple the SC array from the RO, i.e. to prevent the SC array from affecting the operation of the RO and its frequency, we use a differential buffer. Fig. 4(b) shows the complete layout of the RO. To ensure proportionality, the layout is strictly centrally symmetrical. The length of the VCO core is about 32 μm, and its width is 20 μm. We place the isolated buffer on the right side and its size is close to 10x20 μm^2. This placement is beneficial to keep the overall symmetry and reduce the distance mismatch between the four phases of the clock. The RO provides a wide frequency range to support the loop and also enables a wide-capture-range CDR design.



(a)



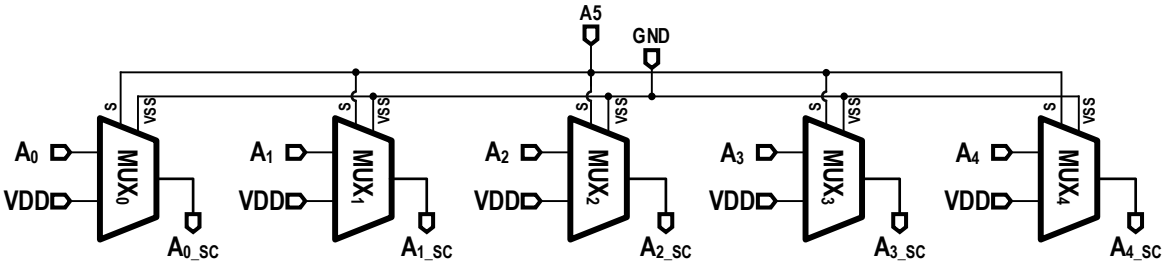
PMOS	8μm / 0.06μm	R	857Ω
NMOS	4μm / 0.06μm		

(b)

Fig. 5. (a) Schematic and (b) design size of the 6-bit R-2R DAC.

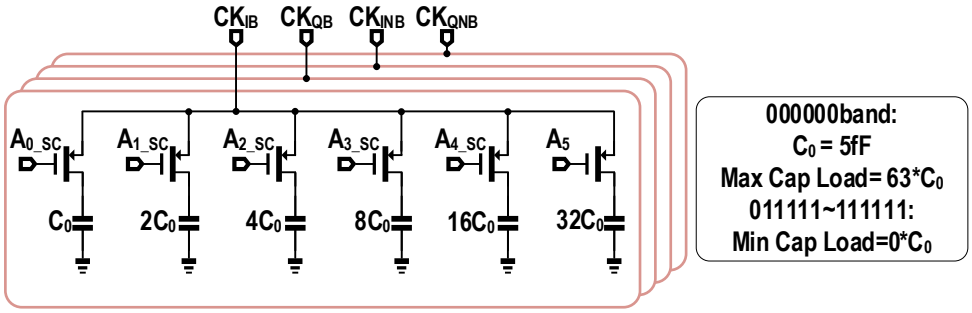
B. 6-bit R-2R Digital-to-Analog Converter (DAC)

We introduce a 6-bit R-2R digital-to-analog converter (DAC) in our BBCDR to generate the bias voltages V_A and V_B of the RO, as well as to perform coarse frequency tuning. The DAC consists of resistors and switches controlled by the band selection signals A_1~A_5, [Fig. 5(a)], with the design sizes from Fig. 5(b). Two pairs of reference voltages V_{REFP_A}~V_{REFN_A} and V_{REFP_B}~V_{REFN_B} define the DAC output range. Depending on the binary value encoded in the A_1~A_5 signals, the connection of the resistors will change, respectively, thus changing V_A and V_B.



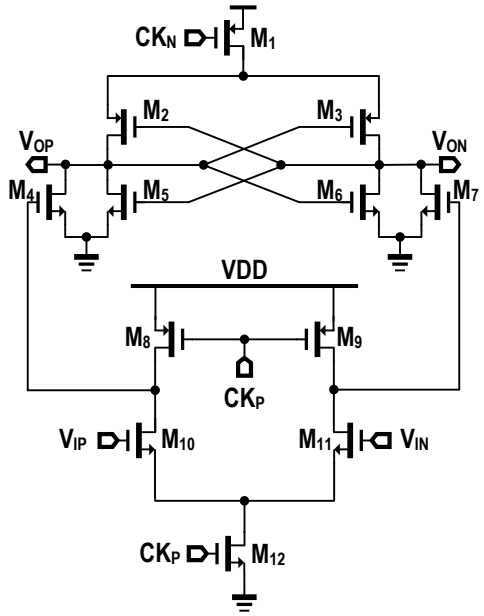
Truth Table					
A_5	A_{0_SC}	A_{1_SC}	A_{2_SC}	A_{3_SC}	A_{4_SC}
0	A_0	A_1	A_2	A_3	A_4
1	VDD				

(a)



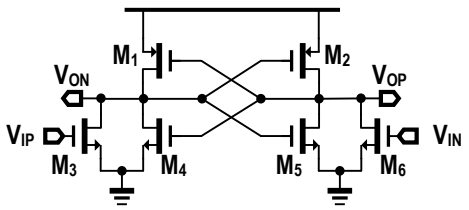
(b)

Fig. 6. Block diagram of (a) the control logic and (b) the SC array.



M_1	8.4μm / 0.06μm
M_2,M_3	3μm / 0.06μm
M_5,M_6	1μm / 0.06μm
M_4,M_7	3.2μm / 0.06μm
M_8,M_9	2.4μm / 0.06μm
M_{10},M_{11}	1.2μm / 0.06μm
M_{12}	4μm / 0.06μm

(a)



M_1,M_2	2μm / 0.06μm
M_3,M_6	3.2μm / 0.06μm
M_4,M_5	0.6μm / 0.06μm

(b)

Fig. 7. Schematic of (a) the two-stage double-tail FF and (b) the RS latch.

C. SC Array and Its Control Logic

Since the PI requires near sinewave signals with smooth transitions for proper operation, whereas the RO output signal is like a square wave in the low-frequency range, the SC array, acting as a variable load, placed at the output of the RO clock buffers smoothens their output. Considering that the VCO output is naturally a sine wave in the higher frequency range, we should configure a small load capacitor (or no capacitor at all) at high frequency to avoid excessive signal attenuation, whereas a larger load capacitor is necessary at low frequency. Fig. 6(a) displays the control logic and the corresponding truth table of the SC array [Fig. 6(b)]. The generated signal changes the load capacitance of the clock by controlling the PMOS-based switches.

When the most significant bit A_5 is 0, the total load capacitance decreases as the VCO band, decided by the binary value A_0~A_4, rises. The maximum load capacitance is $63C_0$ (315fF), and is applied in the lowest frequency band. Once the most significant bit A_5 is 1, we set all control signal outputs to VDD to turn off the PMOS switches, with the load capacitance completely cut off. The value of C_0 (5fF) is determined by post-layout simulation ensures good phase interpolation over the wide frequency range. Since C_{load} takes its maximum value at the lowest band (band0), in which the VCO operates at a relatively low frequency, the additional capacitance results in a minor increase in power consumption. Based on post-layout simulation results, the VCO operates at 2.41 GHz in band0 with 0.5V V_{CONT}, and the total power consumption of the VCO and isolation buffer increases from 5.7mW to 6.16mW with the maximum SC load.

D. DT FF

The data path samples the input over eight uniformly-spaced phases, resulting in a 2x oversampling ratio under a quarter rate operation. Based on Alexander's topology, the modified BBPD employs eight flip-flops to strobe the input data. To retime the input and offer a clear demultiplexed output also at high frequency, we employ a DT FF in the proposed CDR. The schematic of the two-stage DT FF is shown in Fig.7(a). The two-stage structure has less stacking and can therefore operate at a lower supply voltage. The double tail enables both a large current in the latching stage (wide M_1) for fast latching, independently of the common mode voltage of the input, as well as a small current in the input stage (small M_{12}) [41]. Fig.7(b) depicts an RS latch used to convert the DT FF output into an NRZ data format.

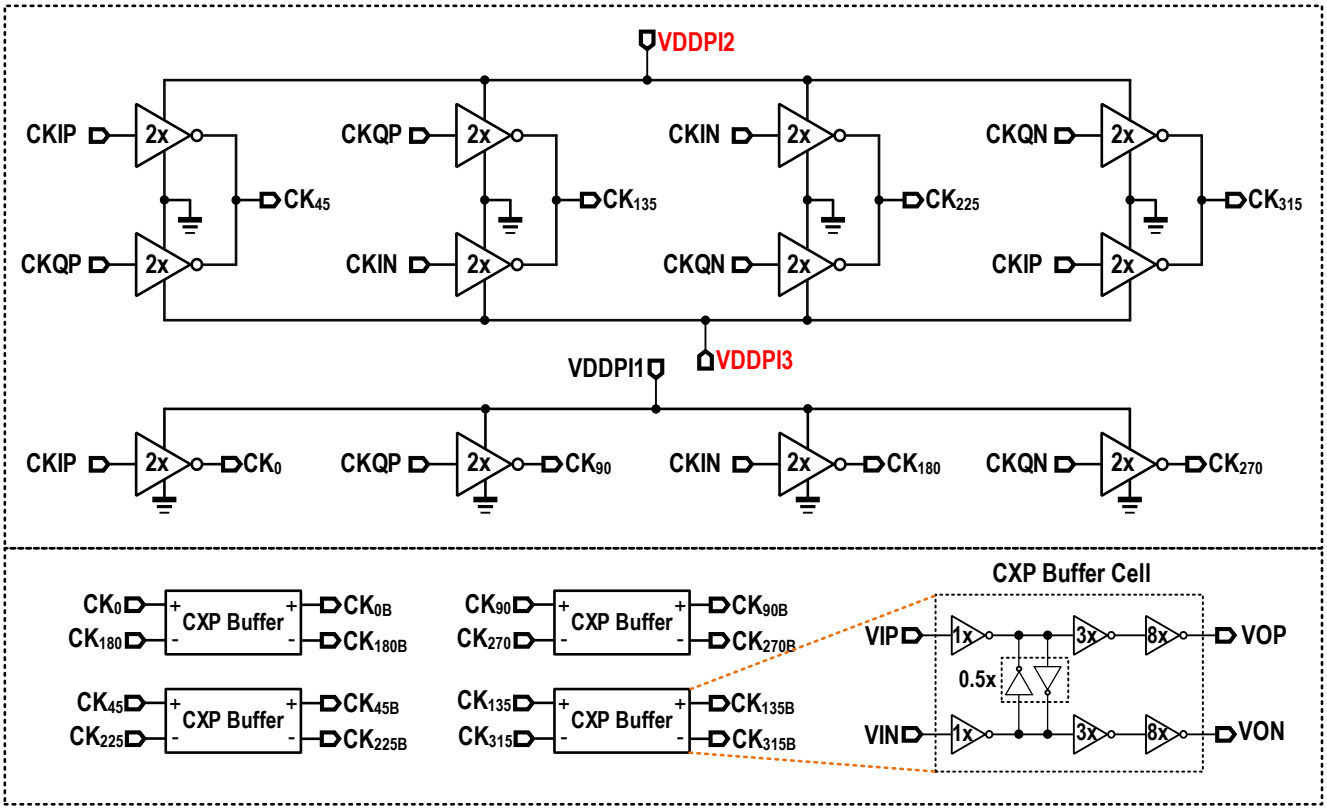


Fig. 8. Developed inverter-based PI for the clock generation.

E. PI

To perform high-resolution phase generation we employed an analog, inverter-based PI based on previous works [42-53] in the proposed BBCDR. Despite its intrinsic phase capture range limitation, this topology is preferable to digital PIs [45-47] for its intrinsic simplicity, adjustable output phase, and low power.

To ensure the monotonicity and linearity of the PI, we should carefully design the gain K_{PI} to be constant [48]. Moreover, the analog PI requires a reset logic to limit the control voltage within the range. It follows that the PI has an intrinsic phase capture range limitation and cannot provide 0° to 360° phase rotation [48].

We choose this open-loop PI structure instead of a close-loop PI-based DLL [44] with the consideration that the external tunning of supply voltage is suitable to cover the phase error caused by PVT variation. Since we found that a small change in the supply voltage will result in a sufficiently large phase variation to cover the phase tuning requirement, this PI will not result in a large variation in output signal amplitude while

tuning the phase.). Moreover, since the PI we introduced in this paper is only used to generate a multi-phase clock signal, the accuracy of the locking process is entirely managed by the BBPD. An accurate digital-controlled PI would have not brought any significant advantage in terms of accuracy in our design, while it would have unnecessarily increased the locking time, since digital-controlled PIs show a tradeoff between accuracy and the number of locking cycles [44]. On the other hand, the analog structure we chose enables continuous fine-grained tuning without increasing the locking time.

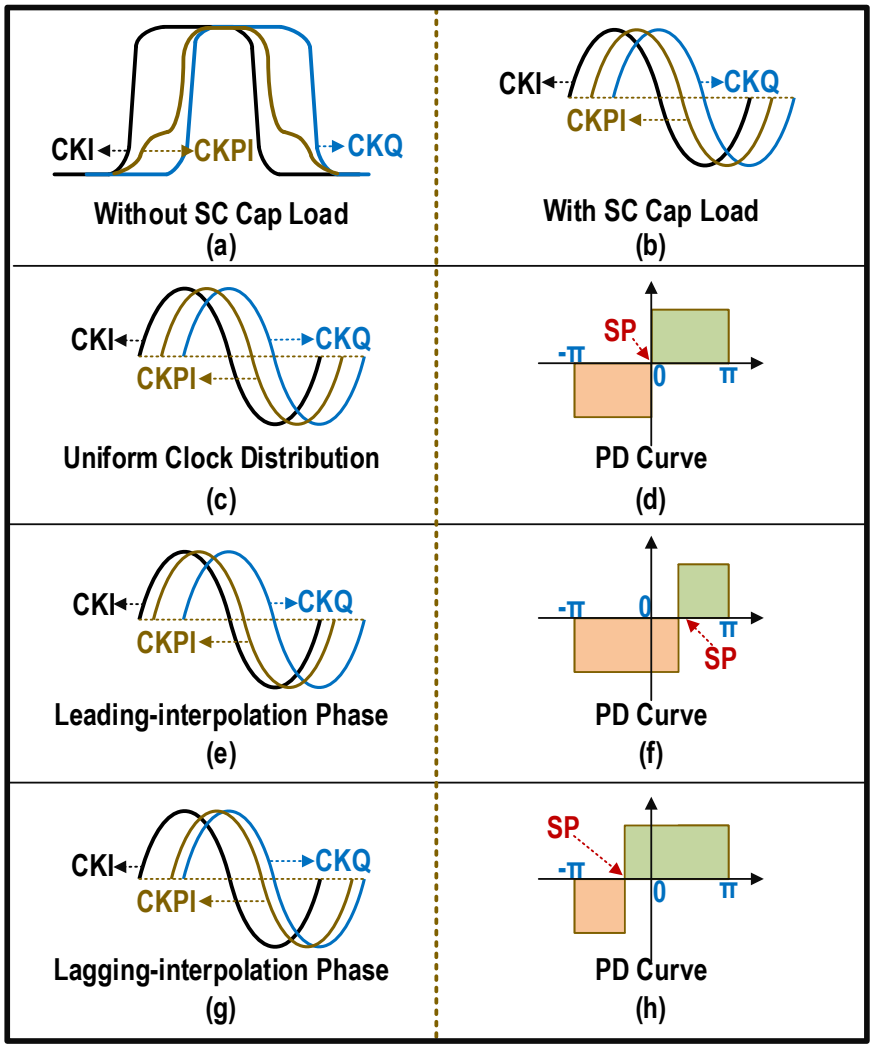


Fig. 9. Effects of the phase skew on the PD curve (waveforms in (a)-(b) are based on simulation results).

The upper part of Fig. 8 shows the structure of the employed PI, with its core followed by four differential buffers to drive the generated clock signals. The same figure also shows the schematic of the drivers. Cells operated at the *VDDPI1* supply voltage generate the quadrature signals CK_0, CK_{90}, CK_{180} and CK_{270}, with the interpolated clock generated by equal-weighted-quadrature signals. *VDDPI2* controls the percentage of the phase-leading signal and *VDDPI3* is the percentage of the signal with a phase lagging of 90 degrees. The change in the two supply voltages *VDDPI* can slightly change the weight of the input signal, thus changing the phase generated by interpolation. For example, when CK_{IP} and CK_{QP} generate CK_{45}, with *VDDPI2*=1.05V and *VDDPI3*=1V, the generated CK_{45} will be closer to CK_0. On the contrary, with *VDDPI2*=1V and *VDDPI3*=1.05V, the generated CK_{45} will lag and is closer to CK_{90}.

While the SC array is used to smoothen steep clocks (Fig. 9(a)) into sinusoidal waves (Fig. 9(b)) for better phase generation, the interpolated clock phase shows a slight non-ideal deviation over the entire tuning range due to the wide output range of the clock. This clock phase deviation affects the PD curve (Fig. 9), resulting in a shift of the SP point over the *x*-axis. When interpolating a uniformly distributed clock [Fig. 9(c)], we obtain a symmetrically distributed PD curve [Fig. 9(d)], and the clock phase in itself does not give any contribution to the SP, since the net PD output over a duty cycle is 0. When the interpolated clock is leading [Fig. 9(e)], it expands the interval in which the CP current is negative (Fig. 9(f)), and the PD gets a negative net current for one duty cycle, which is equivalent to having a positive SP point in the *x*-axis [19]. On the contrary, when the interpolated clock is lagging [Fig. 9(g)], it expands the positive current interval (Fig. 9(h)), and PD results in a positive net current over a duty cycle, which is equivalent to having a negative SP point. We can observe that, during the FAM, the alternately switched upper and lower extra CP branches introduce a change in the SP by translating the PD curve along the *y*-axis, as previously outlined in Section II-D, while the non-uniform distribution of the clock described above is equivalent to a translation along the *x*-axis. In the frequency capture phase, the effects of two SP point shifts, due to the deliberately inserted current mismatch, relate to the clock phase - superimposed to shape the PD curve, among which the deliberately inserted SP through the SP CP plays a dominant role. Moreover, fine-tuning the *VDDPI* can eliminate the SP

shift caused by the interpolated clock phase.

The robustness of the PI is verified by simulation under PVT variation in Fig. 10. The PI shows a large phase deviation and differential non-linearity (DNL) at low frequency without phase tuning, and better linearity at high frequency. The nonideal clock phase worsen the PD curve asymmetry. Although the negative output region is heavily compressed with a -0.6 DNL clock as shown in Fig. 11(a), we must emphasize that the large PI nonlinearity will not affect the PD output polarity with appropriate SPCP bias (Fig. 11(a)). Although the lagging phase error compresses the negative output region of the PD curve, a large VNN bias will guarantee the PD has a negative output in a cycle slip under NNC mode. The CDR can also achieve a robustness frequency acquisition and band searching without precise PI tuning, as observed in the measurement results reported in Fig. 21 in Section IV of this paper.

The phase non-linearity, however, results in a large PD mismatch, which worsens the jitter performance in the phase locked state. The open-loop PI enables artificially external tuning to optimize the jitter performance, which ensures the PI has a high linearity output signal under PVT variations over the entire operating range. The loop has a symmetrical PD curve under ideal clock phase in Fig. 11(b), results in a better frequency tracking and phase locking.

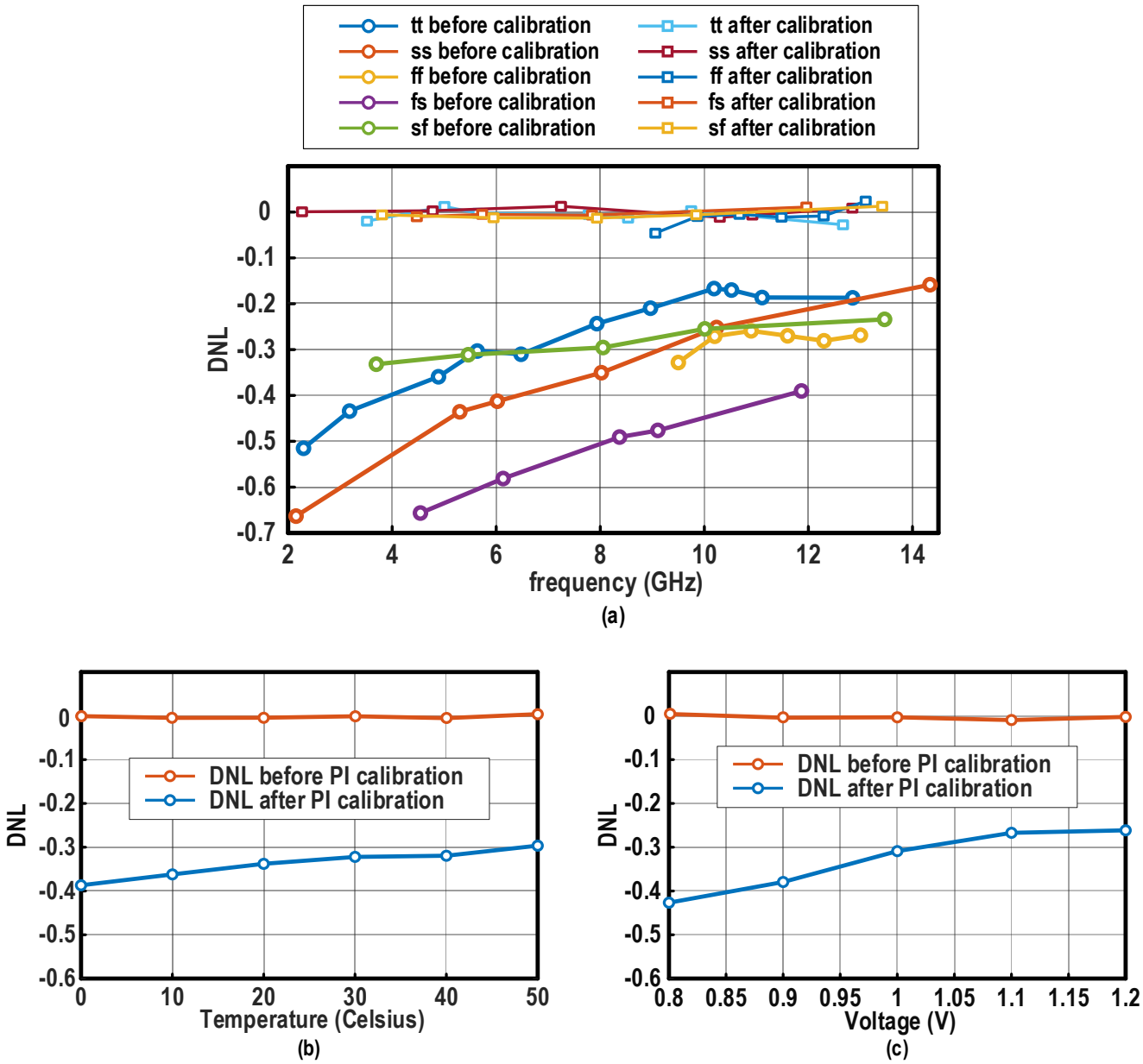


Fig. 10 (a) The simulation DNL of PI with and without PI phase tuning under different corners and (b) temperature and (c) voltage variation.

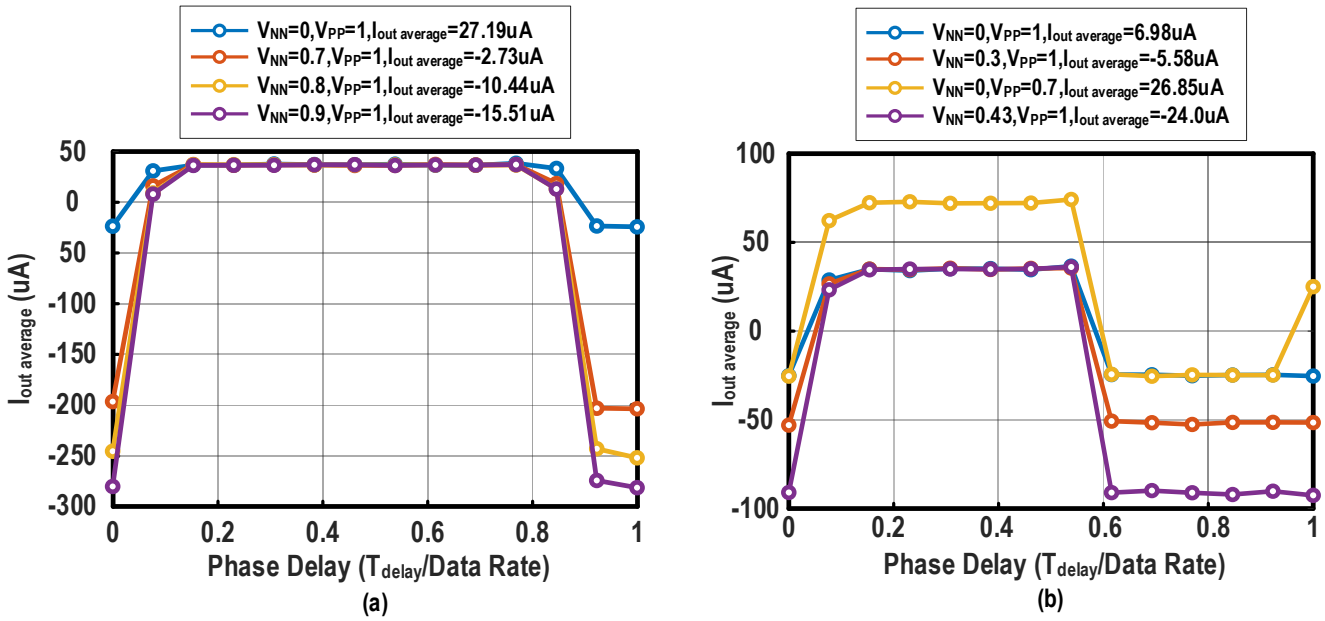


Fig. 11 The PD curve under different SPCP biases with (a)-0.6 DNL clock phase (b) ideal clock phase

F. Details of our HCC

The HCC introduced in Fig. 12 combines VCO hopping control logic and mode switching control logic. In the VCO hopping control logic, the hysteresis comparator (i.e., Schmitt trigger) is employed to control the range of V_{CONT} with its schematic disclosed in Fig. 13. Whenever V_{CONT} reaches the upper or lower threshold voltage (V_{S+} and V_{S-}) of the Schmitt trigger, it will produce an edge signal on ***SW***, converted by an edge detector into a pulse signal ***BANDSW*** and fed to the 6-bit binary counter to realize RO band selection. On the other hand, we specifically introduce a set of signals A_{2_SET}~A_{5_SET} to externally control the VCO band.

In the same HCC block, the mode switch control logic is in charge to control the loop toggling between FAM and the PTM, by selecting the SP point shift. When ***MDSW*** is 0, it assigns PD to FAM, with the deliberate current mismatch inserted for FD-less frequency acquisition. Otherwise, When V_{CONT} is within the preset V_{REF} range (V_{REF-}~V_{REF+}) and the VCO does not jump to a different band within a fixed preset time (obtained by a 2-bit counter driven by a current-starved oscillator), a DFF maintains the high-level mode switching signal ***MDSW***, as presented in Fig. 12. Then, the BBCDR completed the frequency locking with success and it will switch into PTM with a zero net current output. Due to the SP selection mechanism, the

proposed BBCDR can realize both continuous frequency acquisition and automatic band switching.

The function of the reference VREF- and VREF+ is to set a reasonable range of VCONT. It makes sure that the control voltage of VCO will not be in an extreme value like 1V or 0V. Once VCONT is out of VREF range, CDR will be forced to FAM mode to continue searching for frequency lock, thus VRFE also acts as a fail-safe mechanism in the loop operation. The value of VREF is set to be close to the threshold of the Schmitt trigger.

Although the CDR handles high-speed input data, the HCC operates at a low frequency and the input signal of the counter is a rail-to-rail pulse of several hundred megahertz. Therefore, the HCC block has strong robustness to ensure successful locking.

A 6-bit ripple counter included in the HCC block controls the RO band switching as shown in Fig. 14. We specially design the 3rd to the 6th DFFs of the ripple counter as externally set to allow presetting of the VCO band. Fig. 17 and Fig. 20 illustrate the detailed operation process, with some intermediate processes omitted for fast locking, respectively.

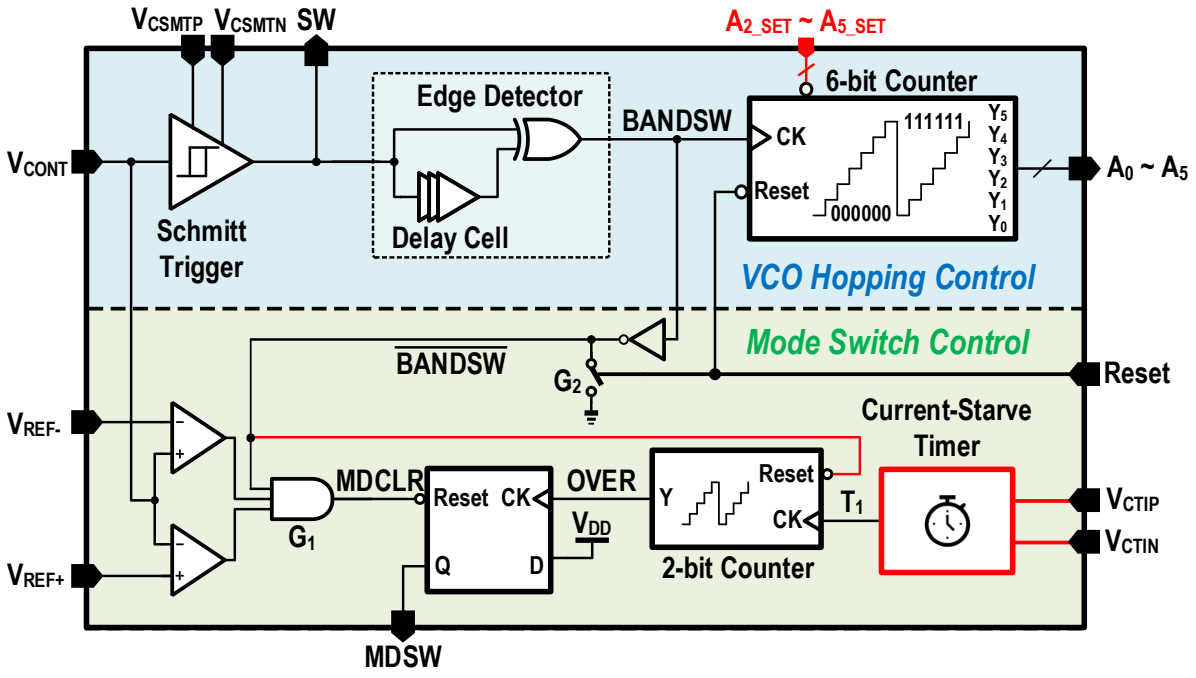
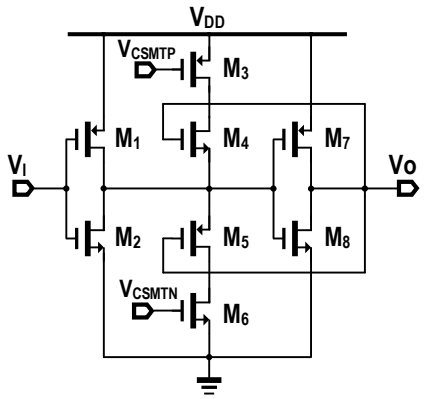


Fig. 12. Block diagram of our presented HCC



M_1	1.2μm / 0.06μm	M_5	0.6μm / 0.06μm
M_2	0.53μm / 0.06μm	M_6	2μm / 0.06μm
M_3	4μm / 0.06μm	M_7	1.7μm / 0.06μm
M_4	1.4μm / 0.06μm	M_8	0.85μm / 0.06μm

Fig. 13. Schematic and detailed size of the Schmitt trigger

We employ the current starved timer to generate the preset time interval (Fig. 2), i.e. the time interval following a V_{CONT} transition after which the circuit assumes the completion of frequency locking, unless it observes another V_{CONT} transition before. Fig. 15 depicts the schematic of the current starved timer. We add an inverter-based buffer to increase the driving capability of the output signal. The gate of the PMOS devices in the upper branches and of the NMOS in the lower branches connect, respectively, to the control voltages $V_{CTIMERP}$ and $V_{CTIMERN}$, which allow current tuning, thus adjusting the preset time, over a wide range.

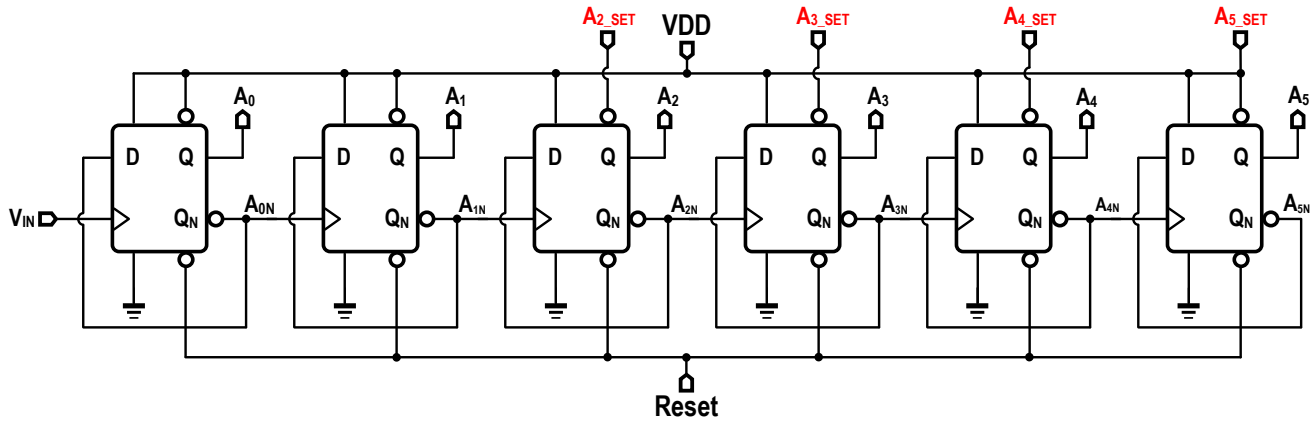
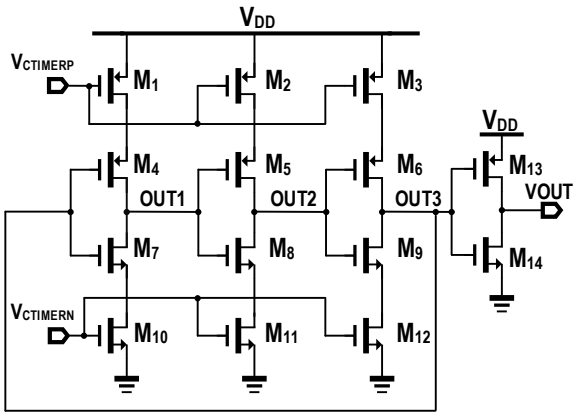


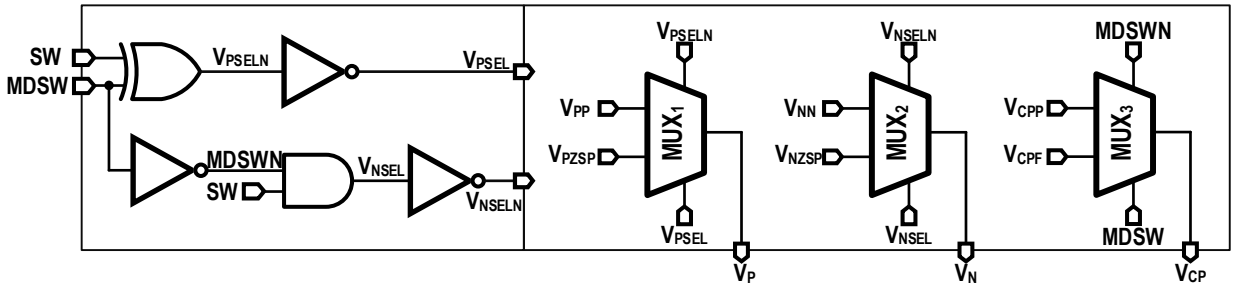
Fig. 14. Block diagram of the bit signal counter with band preset function



M_1-M_6	0.9μm / 0.06μm
M_7-M_{12}	0.45μm / 0.06μm
M_{13}	1.8μm / 0.06μm
M_{14}	0.9μm / 0.06μm

Fig. 15. Schematic and detailed size of the current-starved RO-based timer

To ensure the consistency of V_{CONT} during the entire frequency acquisition, the asymmetrical PD needs to generate a non-zero output current with opposite polarity in adjacent bands. Fig. 16 [34-35] shows the logic of the specific FAM mode control intended to select the polarity of PD net currents over a cycle slip, with the operating mechanism detailed as follows: (1) When the loop is in FAM and ***SW*** signal is 0, MUX_1 selects V_{PP} for V_P to open the extra upper CP current path while MUX_2 selects V_N=V_{NZSP}=0 to turn off the lower extra CP path. The loop results in an asymmetrical PD curve with a positive net current and the charging of the capacitor in the LF enables V_{CONT} to continue to increase. (2) When V_{CONT} rises to the high threshold voltage V_{S+} of the Schmitt trigger, ***SW*** results in 1. In return, the selection of V_{NN} opens the lower current path and the selection of V_{PZSP}=1 closes the upper current path; The loop thus results in a negative output, and V_{CONT} decreases due to the discharge of the LF. (3) ***MDSW*** is 0 due to the dynamic variation of V_{CONT} during the entire frequency acquisition, and we choose a larger bias voltage V_{CPF} for V_{CP} to release a faster frequency hunting; When the ***MDSW*** goes high after frequency locking, both additional CP paths become off and the selection of a smaller bias V_{CPP} leads to better jitter performance.



Truth Table							
Mode	MDSW	SW	V_{PSEL}	V_{NSEL}	V_P	V_N	V_{CP}
FAM	0	0	1	0	V_{PP}	V_{NZSP}	V_{CPF}
	0	1	0	1	V_{PZSP}	V_{NN}	V_{CPF}
PTM	1	0	0	0	V_{PZSP}	V_{NZSP}	V_{CPP}
	1	1	0	0	V_{PZSP}	V_{NZSP}	V_{CPP}

Fig. 16. Implementation and truth table for the SP point selection.

Fig. 17 illustrates better the operation of the HCC, which offers the transient waveforms of the HCC internal node. With the loop initially locked at band3 and a ***Reset*** signal activated at t_0 the circuit releases the FAM and the CDR loses the lock. Regardless of V_{CONT}, the VCO remains settled at band0 with the global ***Reset*** signal asserted. Nonetheless, even with the ***Reset*** signal maintained, the Schmitt trigger follows V_{CONT} to generate the ***SW*** signal. Simultaneously, the edge detector detects the edge of ***SW*** and generates a pulse ***BANDSW*** signal. At t_1, the circuit disables ***Reset***, and the counter begins to increase at each pulse of the input ***BANDSW*** signal. After a continuous search time T_a, the BBCDR achieves frequency locking at t_2. When the timer overflows at t_3, the circuit releases PTM for better jitter performance [54-57].

In Fig. 17(b), with the ***Reset*** maintained, we can observe the same transient waveforms from Fig. 17(a) when the A_{2_SET} is active. It can also perceive that the RO jumps from band0 to band4 instantaneously, thus reducing the total time of frequency locking at band9 to T_b. In Fig. 17(c), we show the case when the circuit maintains A_{3_SET} as a further demonstration: now, with the RO set to band8 immediately with the activation of A_{3_SET}, we can further reduce the frequency locking time T_c.

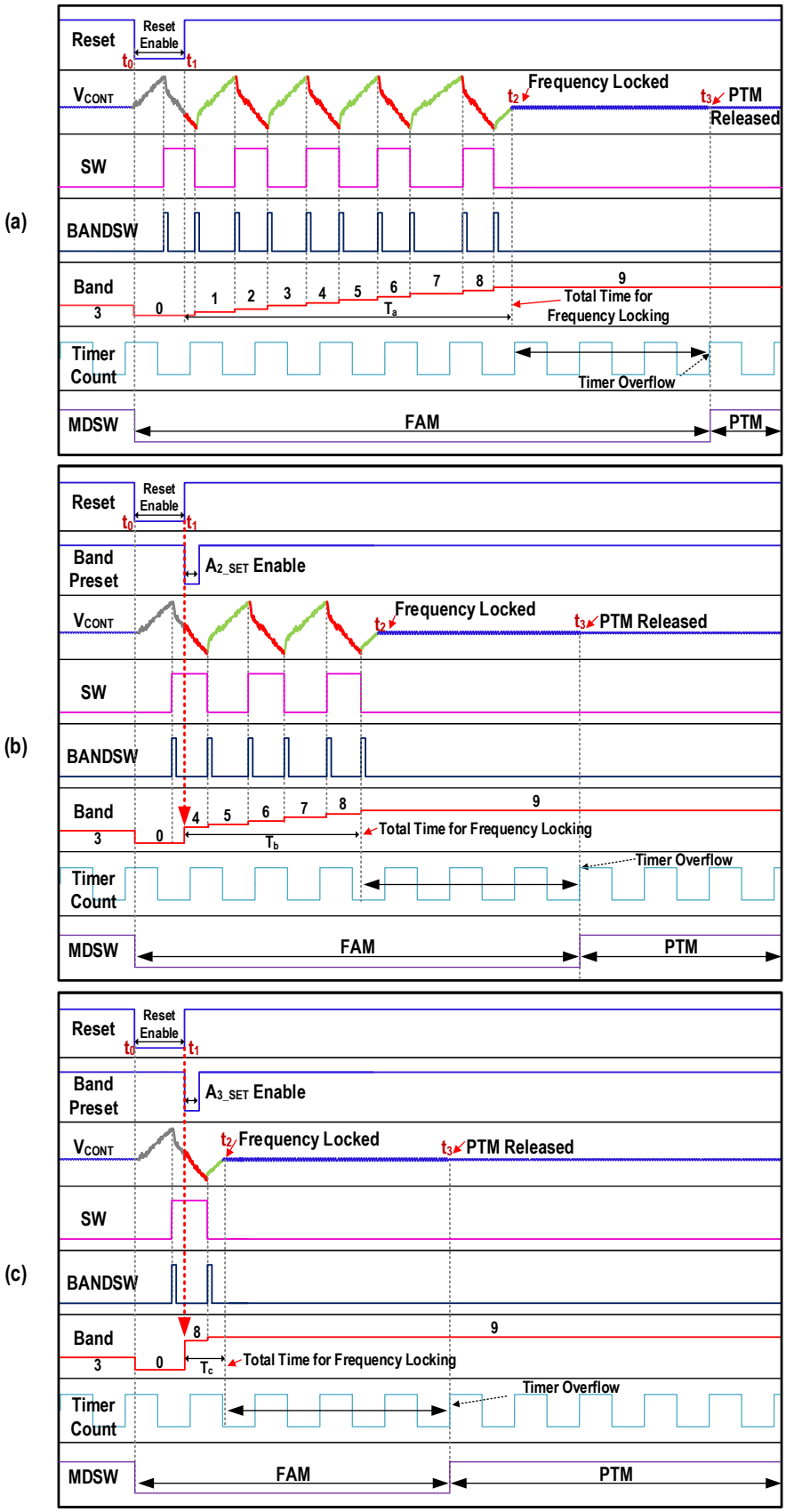
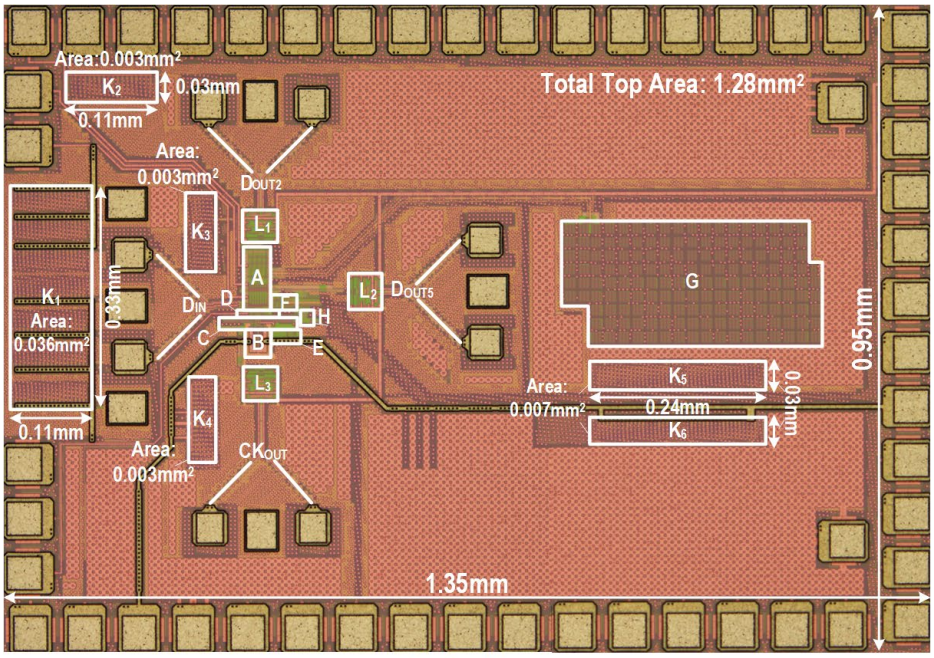


Fig. 17. Critical transient waveforms of our HCC with band preset signal enabled.

IV. Measurement Results

Fig. 18 depicts the top layout of the proposed BBCDR fabricated in a 65-nm CMOS. The active area of the prototype is 0.07mm^2 and the LF occupies 91% of the data path. The total area of the PD, CP, and XOR modules enabling data retiming, phase detection, and frequency acquisition are just 0.0026 mm^2, i.e., 3.7% of the total core area. The multi-phase clock generation occupies 0.0031mm^2 in total, which corresponds to 4.4% of the total active area. The RO and isolation buffer area is 0.0011mm^2, the SC array occupies 0.0011 mm^2, and the RDAC is 0.0007 mm^2. The power breakdown is shown in the lower part. The prototype consumes 24.61 mW with 32 Gb/s input and result in an energy efficiency of 0.769 pJ/bit.



Area Breakdown

Main Circuits		Area	Main Circuits		Area	Auxiliary Circuits			
A	PD + CP + XOR	0.0026	E	RDAC	0.0007	L_1	D_{OUT2} Output Buffer	K	Decoupling Capacitor
B	RO + VCO Buffer	0.0011	F	HCC	0.0005	L_2	D_{OUT5} Output Buffer		
C	SC Array	0.0011	G	LF	0.064	L_3	Clock Output Buffer		
D	PI + PI Buffer	0.0002				H	V_{CONT} Output Buffer		
Total Core Area: 0.07mm²									

Power Breakdown

Sub-Blocks	Power	Proportion	Sub-Blocks	Power	Proportion
VCO	10.37	42.1%	XOR	1.01	4.1%
CP	1.13	4.6%	PD	4.41	18.0%
PI	1.50	6.1%	HCC	0.47	1.9%
PI Buffer	5.72	23.2%	Energy Efficiency = 0.769 pJ/bit @ 32Gb/s		
Total Power Consumption: 24.61mW					

Fig. 18. Chip micrograph with area breakdown.

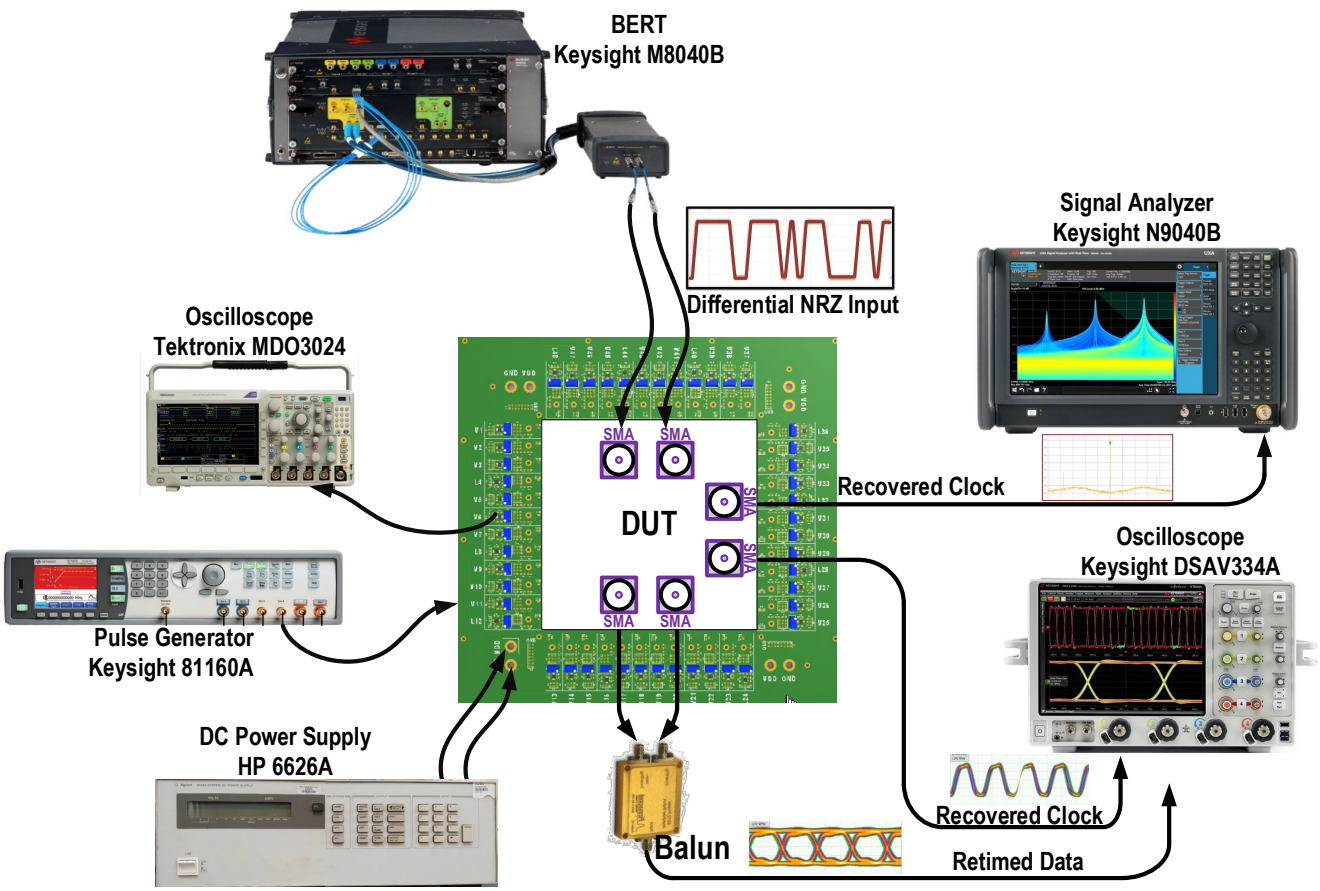


Fig. 19. Experimental setup for the BBCDR testing.

Fig. 19 shows the setup employed for the testing of the BBCDR (device under test, DUT) [58]. The channel loss mainly comes from the high-speed connector and the PCB trace before the DUT. In our design, we chose a short connector and we carefully designed the PCB traces on a Rogers substrate, as demanded to minmize high-speed path loss. In such conditions, our prototype achieves robust operation over a wide capture range without an embedded equalizer.

We use an HP6626A DC power supply to power up multiple pins of the chip through an LDO on the power supply PCB. We also use the Keysight bit error ratio tester (BERT), i.e., M8040B, for NRZ data generation. The circuit transmits the single-ended NRZ data stream through the remote port of the BERT. We transfer the output clock signal obtained from the DUT to the signal analyzer Keysight N9040B for real-time spectrum and phase noise analysis, to observe the difference between the spectrum of the unlocked clock and the locked clock. In addition, we deliver the clock and data to the oscilloscope to assess the eye diagram of the recovered

clock and data. We can also use the oscilloscope to measure the bath curve and BER in the presence of the jitter injection, as well as metrics such as peak-to-peak jitter in the time domain. Baluns convert the differential recovered clock and data signals to single-ended signals for better testing. The oscilloscope Tektronix MDO3024 allows the testing of low-frequency logic signals (e.g. ***SW***, V_{CONT}, ***MDSW*** previously reported in Fig. 17) from the HCC. These logic control signals facilitate the understanding and verification of the internal operation of the circuit. The memory depth of the oscilloscope is sufficient to capture the complete waveforms of all the HCC signals in a single locking process, as shown in Fig. 20 (b) and Fig. 21. With the help of these waveforms, we can completely verify the fully automatic searching process of the VCO band from high to low, and the operation of the loop switching from FAM to PTM after frequency locking. Moreover, we can easily read out with the instrument scale the time required for these operations.

Fig. 20(a) illustrates an idealized timing diagram for comparison and better understanding. Fig. 20(b) plots some acquired waveforms of the low-frequency logical signals from the HCC block to illustrate the settling process. In this example, the location of the target frequency of the NRZ input signal is in band32, with the settling process illustrated for different band preset signal configurations. (1) In case 1, we disable all the band preset signals. After releasing the global ***Reset*** signal, the BBCDR loses lock, and the circuit forces it to band 000000. Since there is no active band preset signal, the loop searches from the lowest band and finally locks at the target frequency after 32 hops. In this case, the BBCDR requires 14.25 μs for frequency acquisition in total. (2) In case 2, we assume the A_{2_SET} signal is enabled after the release of the ***Reset*** signal, in such a way that the loop loses lock after the ***Reset*** signal. After 10 ns the A_{2_SET} activation causes bit2 to set to 1, with the VCO forced to jump from band0 to band4. Since no sudden current injection or leakage occurs in the CP, the V_{CONT} will remain unchanged at band4. The loop then continues to charge or discharge the LF capacitor for frequency capture, toggling between NNC and PNC modes. Fig. 20(b) highlights with a green box the search time saved from band1 to band3 by this operation. (3) In case3, we trigger A_{3_SET} after the release of the ***Reset*** signal, and the loop experiences a band hopping in 10 ns after the time ***Reset*** signal fails and before the enabling of A_{3_SET} signal. Therefore, the bit control signal arrives, with band1 swept by

the RO and the A_{3_SET} signal enables the RO to jump from band1 to band9. We save search time from band2 to band8, with the total lock time of the loop reduced from 14.02 μs in case2 to 11.24 μs in case3. (4) In case4, there is the release of the A_{4_SET} signal and the loop jumps directly from band0 to band16, reducing the lock time to 6.42 μs. (5) Case5, finally releases the A_{5_SET}, with the VCO quickly set to band32 (100000), which is exactly the location of the target. After a short time, with the target hunted, the loop reaches frequency locking in only 0.39 microseconds. This set of test data illustrates that we can partially ignore the search process in the frequency capture using bit preset signals, which demonstrates the possibility of designing a fully automated, wide-range, fast-locking BBCDR.

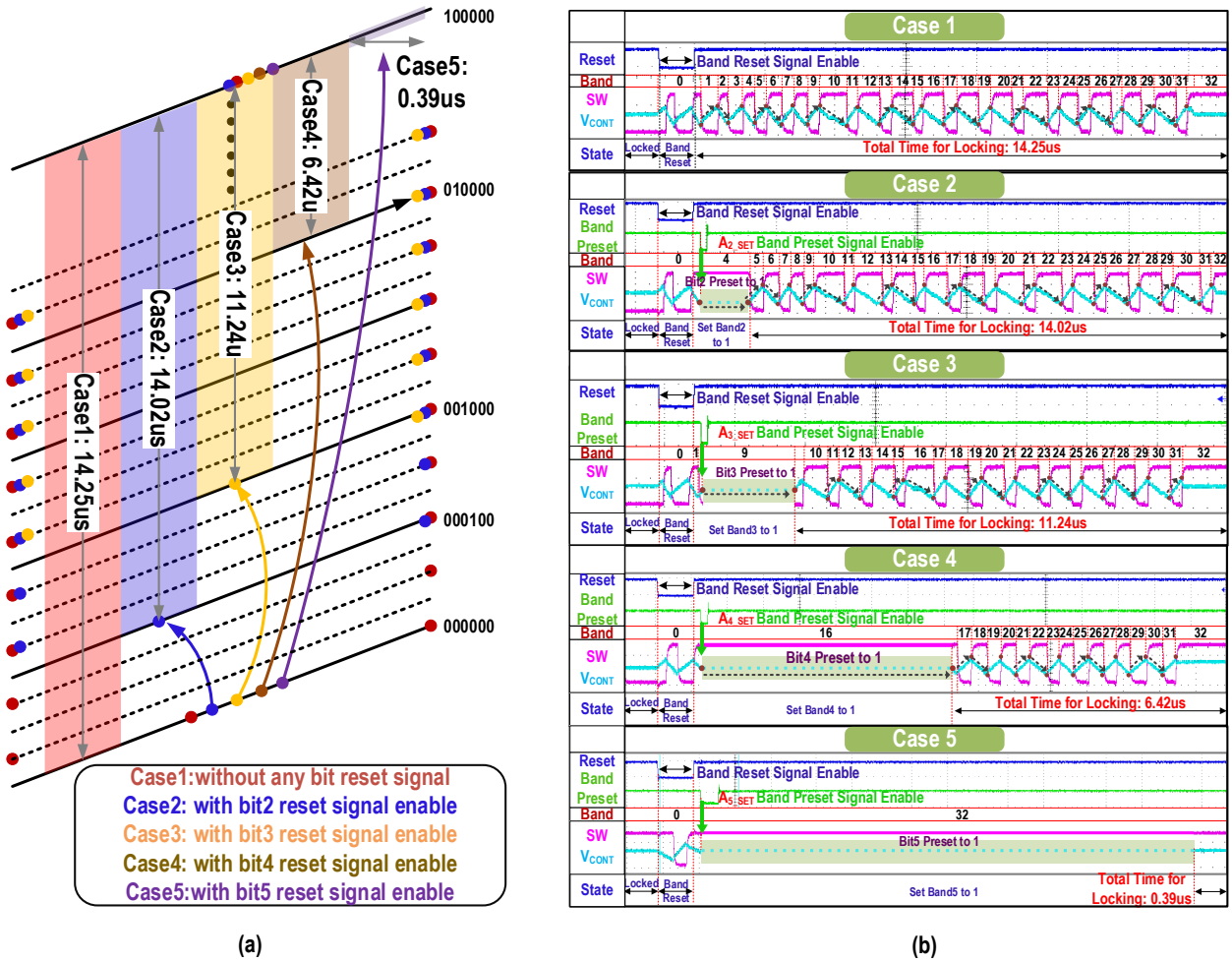


Fig. 20. (a) Illustration of different band-jumping cases and (b) measured dynamic settling process with band preset signal enabled.

It is worth observing that the preset signals do not impair the operation of the loop during the FAM period, as explained below: (1) The V_{CONT} does not change abruptly when the VCO band changes by the preset signal A_{2_SET}~A_{5_SET}, since we only release the control signal of the counter and the CP does not generate a sudden current to charge/discharge the LF. It follows that V_{CONT} is continuous during this process. (2) After a sudden change in the VCO band, the loop remains in FAM and it continues searching for the target under the PNC or the NNC modes.

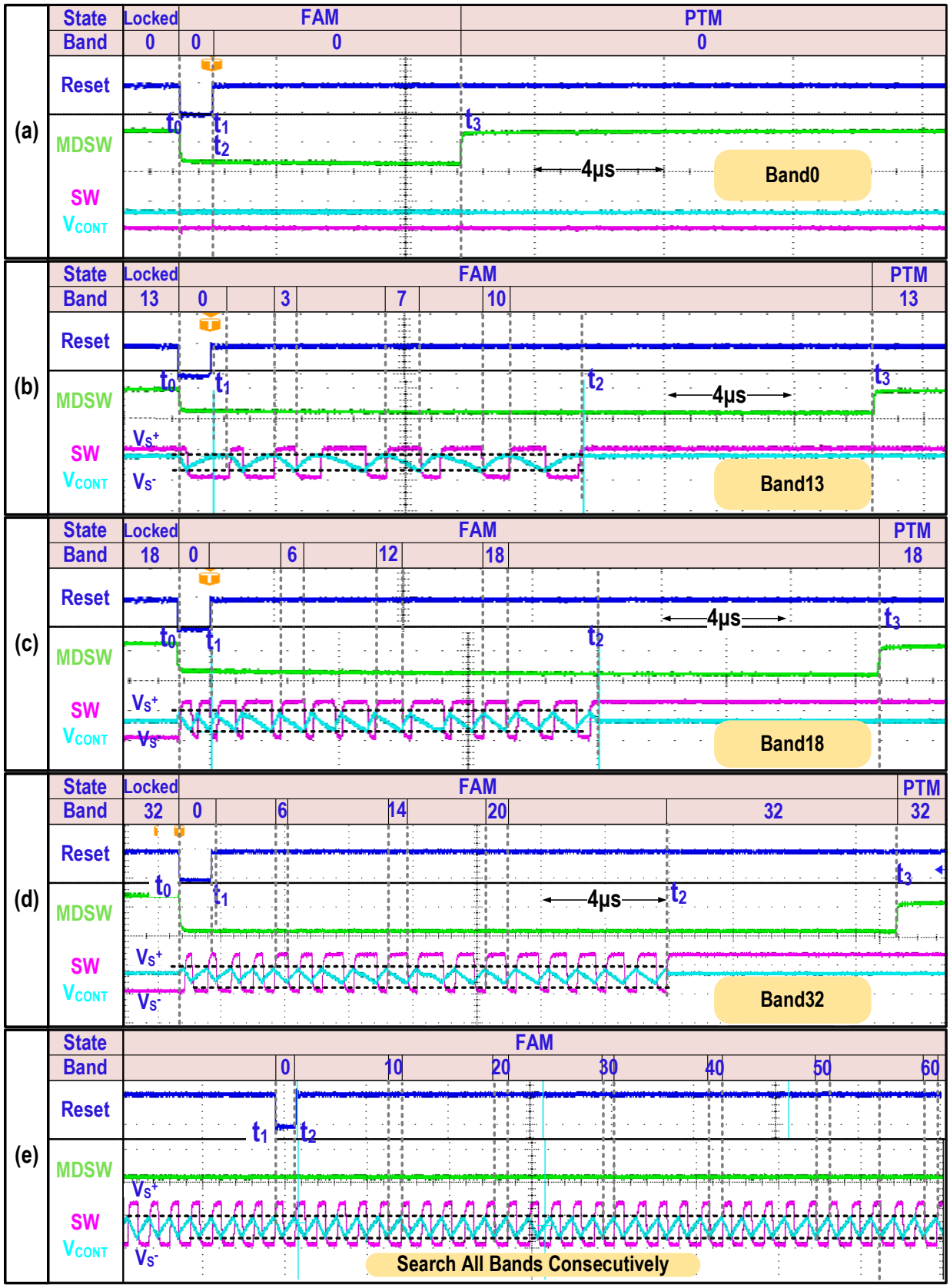


Fig. 21. Measured dynamic settling process with band preset signal disabled.

Fig. 21 displays the correct setting of the BBCDR over a wide frequency range after the ***Reset*** signal, where case (a) locks in band 0 immediately at the reset instant with a 6-Gb/s data rate while case (d) settles at 38 Gb/s after a journey through 32 bands. We can describe a detailed process as follows: Initially, let us consider the BBCDR locked in PTM. The BBCDR receives a new target NRZ data with the global ***Reset*** signal released at t_0, thus resetting the VCO to band 0 (where band 0 is the lowest band and band 63 is the highest). Even though V_{CONT} jumps up and down between t_0 and t_1, the VCO settles itself at band0 due to the active ***Reset*** signal. At t_1, the ***Reset*** signal goes high and the BBCDR enters the FAM. Since a BBPD with a selected SP point generates a non-zero net current to charge and discharge the LF, V_{CONT} wanders up and down between the upper and lower threshold of the Schmitt trigger ($V_{\mathrm{S+}}$ and $V_{\mathrm{S-}}$) to search for the target frequency and the BBCDR switches between PNC and NNC in neighbor bands alternately. In this way, we obtain a continuous automatic frequency capture. After several band hops, the circuit hunts the correct band and the BBCDR locks at t_2 in FAM. When the internal timer of the HCC overflows at t_3, ***MDSW*** goes high and PTM takes over, like this we can further suppress the ripple on V_{CONT} reaching better jitter performance by operating the CP with zero net current over a period. Finally, if the input data is out of the capture range of the BBCDR, such as exceeding the highest capture frequency or the lowest capture frequency, the loop will continuously search all the 64 bands, and then starts from the lowest band0 to the next loop. Fig. 21(e) shows the relevant test result.

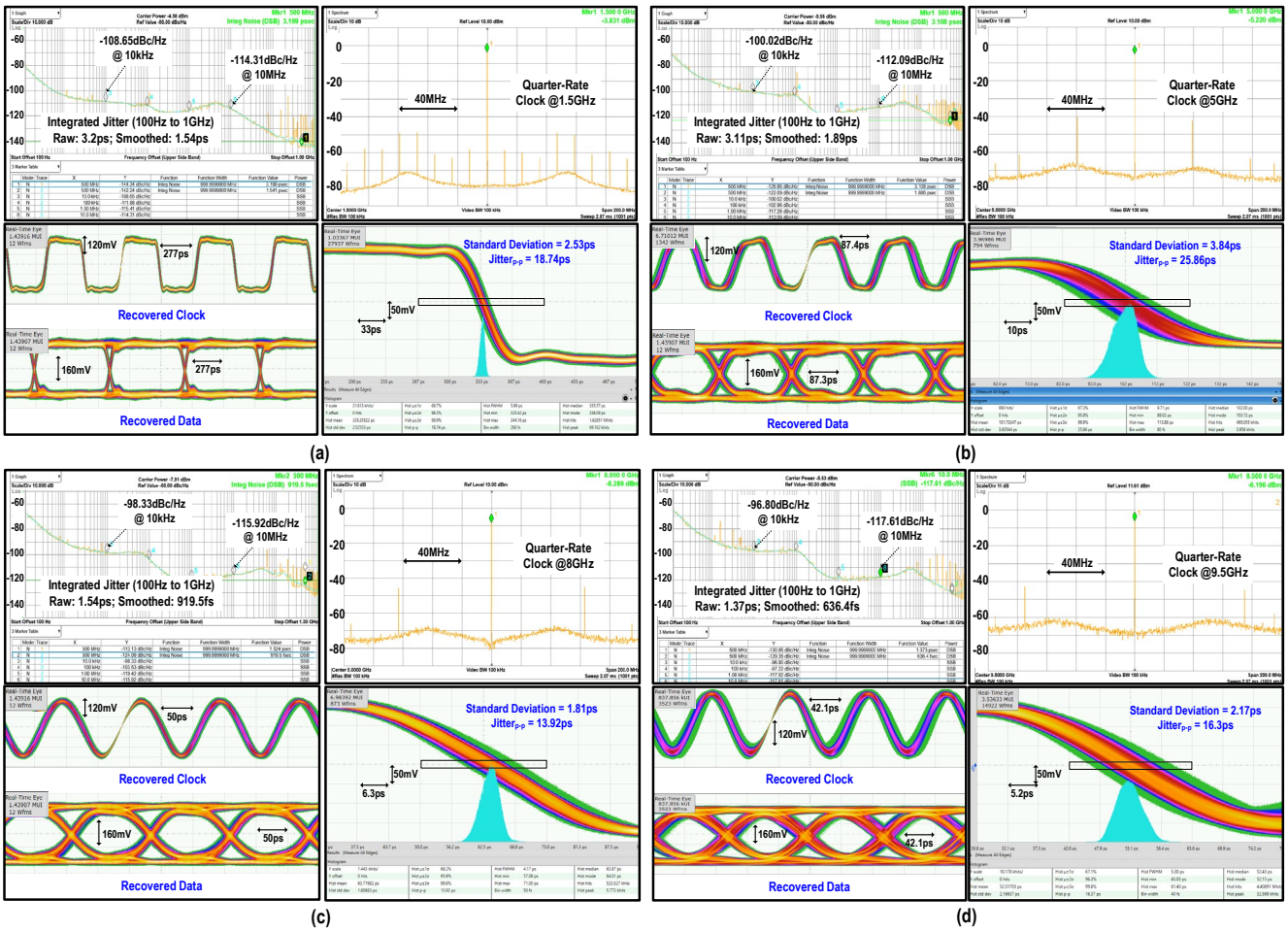


Fig. 22. Measured PN curve, spectrum, eye diagram and jitter histogram at (a) 6 Gb/s, (b) 20 Gb/s, (3) 32 Gb/s and (d) 38 Gb/s.

Figs. 22(a)-(d) shows the test results of the recovered clock and data under different locking conditions in response to a pseudo-random binary sequence (PRBS) of length 2^7-1. We report in detail, the PN, the spectrum, a 4-unit interval (UI) eye diagram, and the jitter histogram at four different data rates, namely: 6 Gb/s, 20 Gb/s, 32 Gb/s, and 38 Gb/s. In Fig. 22(a), the circuit recovers a 1.5-GHz clock with 6-Gb/s data input, and the raw and smoothed integral jitters are 3.2 ps and 1.54 ps, respectively. For the jitter histogram in the time domain, the standard deviation of the jitter is 2.53 ps while the peak-to-peak jitter (jitter$_{P-P}$) is 18.74 ps. At low frequency, the retimed data and clock eye diagram are steeper and closer to a square wave. Fig. 22(b) shows the corresponding recovered clock and data at 20-Gb/s input. The raw and smoothed integral

jitters of the clock are 3.11 ps and 1.89 ps, respectively, which is close to Fig. 22(a). The recovered clock histogram has a standard deviation of 3.84 ps and a peak-to-peak jitter of 25.86 ps. Figs. 20(c) and (d) show the test results at 32-Gb/s and 38-Gb/s input, respectively. When the recovery clock is 8 GHz, the raw and smoothed integral jitters reduce to 1.54 ps and 919.5 fs, respectively. At the recovery clock of 9.5 GHz, the Raw and smoothed integral jitter values further decrease to 1.37 ps and 636.4 fs. The reason for the jitter variation is that both K_{VCO} and K_{PD} are changing with frequency, thus the loop parameters are not constant over a wide operating range. We can tackle this problem in future work by designing a tunable LF. In addition, at high frequencies, the clock and data waveforms are closer to a sinusoidal waveform.

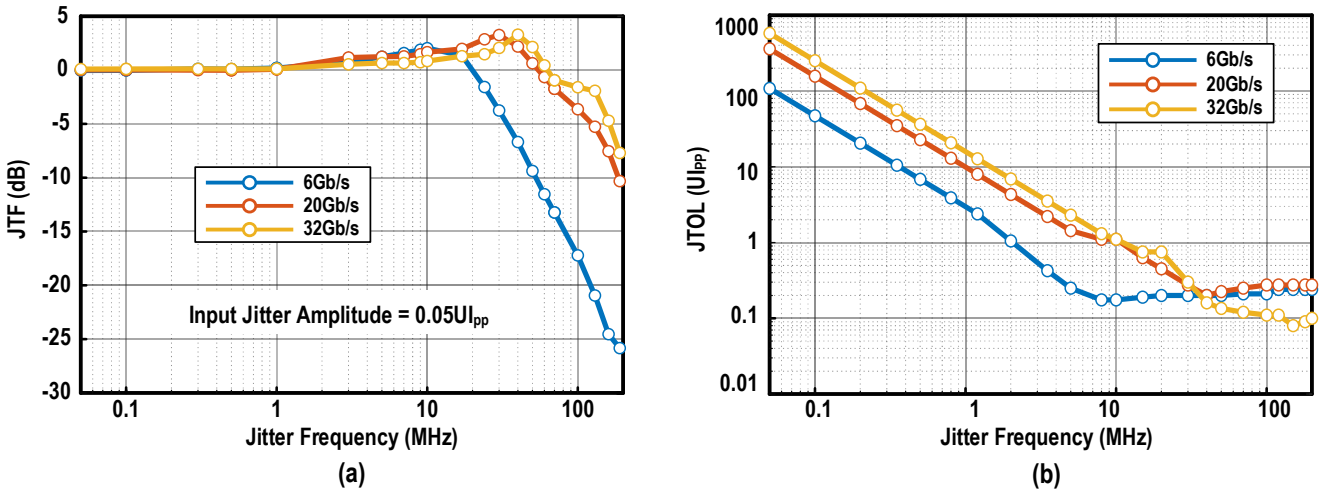


Fig. 23. Measured: (a) JTF and (b) JTOL under different data rates.

TABLE I. Performance Summary and Comparison with the State-of-the-Art.

		This Work		ESSCIRC'18 [52]	SSC-L'20 [53]	JSSC'21 [22]	JSSC'17 [28]	JSSC'20 [54]	JSSC'22 [33]	JSSC'22 [34]
Key Technologies		**Single-Loop Quarter-Rate BBPD**		Half-Rate CFD+DC-FD	Single-Loop Half-Rate Linear PD	Single-Loop Half-Rate BBPD	Single-Loop Half-Rate Baud-Rate PD	Single-Loop Half-Rate Extended BBPD	Single-Loop Full-Rate BBPD	Single-Loop Half-Rate BBPD
Oversampling Ratio		**2x**		2x	N/A	4x	1x	2.5x	3x	2x
Need FD?		**No**		Yes	No	Yes	Yes	Yes	No	No
Data Sampling Clock?		**No**		Yes	Yes	No	No	No	No	No
Data Rate (Gb/s)		**6 to 38**		4 to 10	6.4 to 11	4 to 20	22.5 to 32	6.5 to 12.5	23.4 to 29.1	47.6 to 58.8
Absolute Capture Range (Gb/s)		**32**		6	4.6	16	9.5	6	5.7	11.2
Acquisition Speed((Gb/s)/μs)		**3.19**		0.26	0.29	1.6	0.001	2	8.2	9.81
Output RMS Jitter (ps)		**1.81* / 0.919** @8GHz**		1.05 @5GHz	1.66 @4GHz	1.95 @10GHz	2.6 @12.5GHz	1.15 @5.9GHz	0.487@14GHz	0.416@13GHz
JTOL (UI_{PP}) @ Jitter Frequency	D_{IN} (NRZ)	**0.275 @100MHz**	**0.275 @200MHz**	N/A	0.14 @100MHz	0.42 @100MHz	0.2 @100MHz	0.34 @200MHz	N/A	0.45 @100MHz
	D_{IN} (PAM-4)	**N/A**	**N/A**	N/A	N/A	N/A	N/A	N/A	0.4 @200MHz	0.1 @100MHz
Power Consumption (mW)		**24.6 @32Gb/s**		33 @10Gb/s	N/A	37.3 @20Gb/s	87.61 @32Gb/s	21.13 @10Gb/s	19.16	11 to 13.1
Energy Efficiency (pJ/bit)		**0.769**		3.3	2.7	1.87	2.74	2.11	0.68	0.22 to 0.25
Supply Voltage (V)		**1**		1	1	1.2	0.9	1	1.2 / 0.6	1 / 0.6
Core Area (mm^2)		**0.07**		0.48	0.11	0.045	0.138	0.031	0.0285	0.056
CMOS Technology (nm)		**65**		28	28	65	28	28	28	28

* Obtained from oscilloscope with 0.456ps_{rms} trigger signal; **Obtained from integrated phase noise from 100Hz to 1GHz.

Fig. 23 plots the measured jitter tolerance (JTOL) and the jitter transfer function (JTF) [59-60] of the proposed reference-less BBCDR under locked conditions at three different data rates, i.e. 6 Gb/s, 20 Gb/s, and 32 Gb/s. We test all the JTF curves under a 0.05-UI_{PP} jitter injection performed by the Keysight M8040A BERT. As analyzed before, the loop achieves better jitter performance in PTM with the extra CP path disabled by the HCC control logic and the loop operates with a zero-net-current. At 6-Gb/s PRBS input, the recovery clock operates at 1.5 GHz, with a bandwidth of 25 MHz. The loop bandwidths at 20 Gb/s and 32 Gb/s expand to about 60 MHz and 70 MHz, respectively, due to the variations in K_{VCO} at different frequencies, as discussed above. Under jitter injection by the BERT M8040A, Fig. 23(b) shows the measured JTOL curves. We reach the JTOL at 100 MHz at 0.2 UI_{PP}, 0.29 UI_{PP}, and 0.12 UI_{PP} when inputting 6-Gb/s, 20-Gb/s, and 32-Gb/s PRBS patterns, respectively, which demonstrate the robustness of the proposed BBCDR.

Benchmarking with previous state-of-the-art in Table I, the proposed BBCDR covers the widest input data rate from 6 Gb/s to 38 Gb/s, indicating an absolute capture range of 32 Gb/s. Employing the current-mismatch-based SP selection mechanism, the proposed prototype achieves an acquisition speed of 3.19 (Gb/s)/μs and an energy efficiency of 0.769 pJ/bit.

V. CONCLUSIONS

This paper presented a wide-capture-range quarter-rate BBCDR without both external reference and separate FD. Employing the deliberate-current-mismatch technique and a wideband PI-based multi-phase clock generation scheme, the BBCDR covered NRZ input signals ranging from 6 Gb/s to 38 Gb/s automatically. Under the control of the HCC block, the loop obtained a fast and robust frequency acquisition in a single loop. Fabricated in 65-nm CMOS, the proposed prototype occupied an area of 0.07 mm^2 and scored a 0.769-pJ/bit energy efficiency at 32 Gb/s.

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