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Small-Signal Circuit Model for Synchronous Buck DC/DC Converter featuring ZVS at Low-Side

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***Abstract*—In this paper we provide an improved small-signal equivalent circuit model of a synchronous Buck converter which operates in Continuous Conduction Mode (CCM) and includes an alternative Zero Voltage Switching (ZVS) mechanism for the low-side power MOSFET that rely on the MOSFETs output capacitance. The addressed analysis improves the state of the art in DC/DC small-signal modeling as it is capable to predict unexpected effects on the dynamical system response such as the dependency on input voltage introduced by parasitics. Therefore, a complete design tool which permits to evaluate the impact of the MOSFETs output capacitance and the ZVS network on the converter dynamics is proposed. The derived equivalent circuit model which includes an additional feedforward path and a feedback loop is analyzed and the main open-loop transfer functions (control-to-output, line-to-output, output impedance) are analytically assessed. A verification has been carried out through SIMPLIS circuital simulations, corroborating the validity of the whole evaluation process.**

I. Introduction

Synchronous Buck converters have become widely popular in practical applications [1], [2] due to the looming need to improve the overall power converters efficiency. Employing an half-bridge MOSFET switches to regulate a controlled output voltage a simultaneous conduction condition of the power MOSFETs must be avoided, therefore their control is synchronized. Typically, for a Buck converter which operates in CCM (as the one depicted in Fig. 1(a)) the employed power MOSFETs are complementary turned ON and OFF with a break-before-make control approach, where both the High Side (HS) and Low-Side (LS) switches are turned OFF for a dead-time interval.

With the aim of further minimizing the overall power losses, switching-losses contributions must be carefully reduced. To achieve this scope, a commonly used technique is based on the exploitation of *soft-switching* [3] [4] [5], which allows to recover a non-negligible amount of energy that otherwise would be lost during the switching transitions of the semiconductor devices. Concerning a power MOSFET, its stored energy can be lost when the device is turned on. Therefore, it is preferable to operates MOSFETs with ZVS throughout their turn-on transitions.

Focusing on the LS MOSFET operation during the dead-time interval $\mathrm{T_D}$ (refer to the solid black lines waveforms in Fig. 1(b)), the current soaked up by the inductor starts to discharge the MOSFETs output capacitance, consequently decreasing the switching node voltage $V_{\mathrm{SW}}(t)$. Whether the switching node voltage reaches the threshold voltage of the body diode $\mathrm{D_B^{LS}}$ (Fig. 1(a)) it becomes forward biased, leading to both diode conduction losses and diode reverse recovery losses. On the other side, the premature LS switching-on completely discharges its output capacitance, leading to a further switching loss contribution.

From this simplified analysis, it is inferrable that the appropriate turning on point must anticipates the body-diode forwarding bias and minimize the waste of energy stored in the output capacitor, turning the LS MOSFET ON when its drain-source voltage is very small. The optimum instant of time can be identified introducing the Zero Crossing Detection (ZCD) comparator portrayed in Fig. 1(a), which triggers the turning on command as soon as the SW node voltage drops below a certain threshold value (as graphically represented in Fig. 1(b)). Nevertheless, the ZCD comparator introduction impacts on the power converter dynamics, altering the Buck transient response and the overall system performance.

The contribution of this paper is precisely to examine the dynamic behaviour alteration of a traditional voltage mode controlled Buck converter when the whole ZVS network is introduced, deriving both an equivalent circuit model and evaluating the main open loop transfer functions (control-to-output, line-to-output and output impedance).The achieved results clearly show how the ZCD introduction translates into the addition of a current feedback loop and a voltage feed-forward into the traditional small-signal model of a Buck converter which operates in CCM, affecting the whole duty cycle perturbation.

The manuscript is hence organized as follows. An overview of the Buck converter behaviour under analysis is reported in Section II, highlighting the impact of the added ZVS network on the small-signal dynamics of the system. A canonical equivalent circuit model which includes the described ZVS mechanism is then proposed in section III and validated through a set of SIMPLIS simulations in section IV, where the main small-signal transfer functions are considered.

II. DC/DC Buck Converter with ZCD

The following analysis is relied on the simplified schematic of the Buck converter shown in Fig. 1(a), empirically evaluating the ZCD block and the MOSFET output capacitance C_{MOS} impact on the converter dynamic performances. The circuital topology taken into account is a voltage-mode controlled Buck converter, which includes a traditional sawtooth-based PWM modulator.

The power stage in Fig. 1(a) comprises the HS and LS power MOSFETs, modeled as a switch $\mathrm{SW_{1,0}}$ and a conduction resistance $\mathrm{R_{on}^{HS,LS}}$ in series, while the capacitive effect is modeled as the capacitance $\mathrm{C_{MOS}}$. The converter output filter includes an inductance L with an equivalent series resistance $\mathrm{ESR_L}$, a capacitance $\mathrm{C_{out}}$ with an equivalent series resistance $\mathrm{ESR_C}$ and the load resistor $\mathrm{R_L}$. An input voltage feed-forwarding is implemented, fixing the sawtooth peak voltage amplitude $\mathrm{V_{pk}} = \mathrm{V_{in}}$. This technique is very common,

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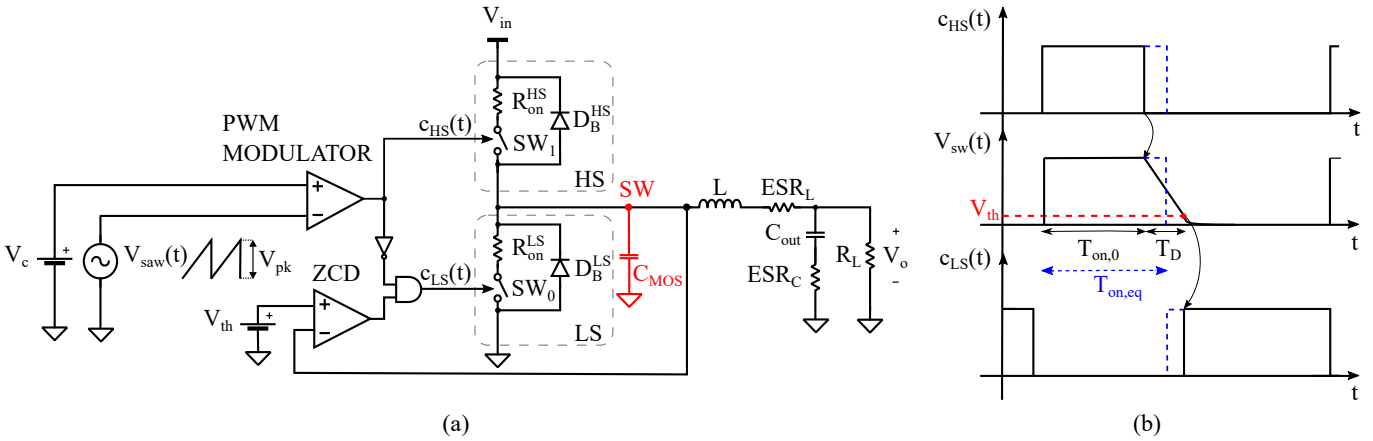

Fig. 1. (a) Schematic of a Buck converter with ZVS Control on the low-side. (b) Dead time of synchronous Buck converter when the ZVS Control on LS MOSFET is present. The SW node voltage decreases linearly when the HS MOSFET is turned OFF, and the LS MOSFET is turned on when $V_{SW} = V_{th}$.

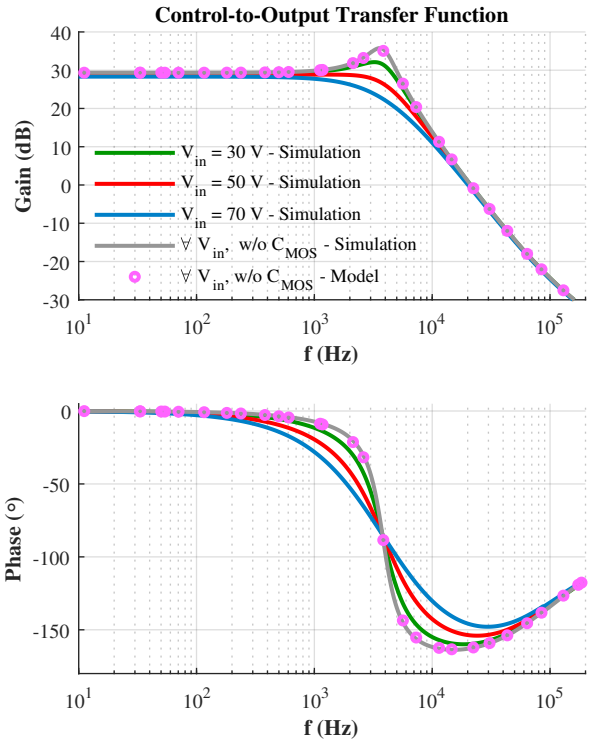

Fig. 2. Control-to-Output Transfer function and V_{in} variation with and without the ZCD loop and C_{MOS} presence

as it provides an output voltage dynamics that is ideally independent from the input voltage value V_{in}.

To easily tackle the study of PWM converters dynamics, averaged linear time-invariant small-signal models [6], [7], [8] turn out to be very useful tools able to approximate the system non-linear switching behaviour with an analytically described equivalent model which allows to estimate the frequency response around a periodic steady-state operating point.
The mathematical model validation is performed with specific circuital simulator designed to handle the small-signal frequency response of switching power systems. In this case, a set of Periodic Operating Point (POP) analyzes followed by AC simulations of the circuit in Fig. 1(a) (accounting the component values listed in Table I) have been performed in SIMPLIS, showing an unexpected V_{in} dependence on the output voltage V_{o} dynamic response with respect to the perturbation of the control voltage V_{c} when the feed-forwarding mechanism is present (i.e., $V_{\text{pk}} = V_{\text{in}}$). The collected results are shown in Fig. 2, where the open-loop control-to-output transfer function is drawn, showing an increasing damping effect for an input voltage sweep $V_{\text{in}} = 30, 50, 70\text{V}$. These simulation results are compared with the ones achieved from a canonical equivalent small-signal representation of the whole Buck converter, operating in CCM. The latter is derived exploiting the high versatility of the traditional small-signal AC model of the switching network in Fig. 1(a), which includes the pair of switches $SW_{1,0}$ and the respective HS and LS MOSFET conduction resistances $R_{\text{on}}^{\text{HS,LS}}$ [9] but it does not account the MOSFET output capacitance C_{MOS}.

III. Small-Signal Circuit Model

The canonical small-signal equivalent circuit [10] in Fig. 3(a) can be obtained, where the switching network is enclosed into the red dashed box while the PWM modulator model is enclosed into the blue dashed box. The symbol $\hat{}$ denotes the small-signal quantities while the steady state part is represented with capital letters. The PWM modulator provides the duty cycle perturbation $\hat{d}_0$ from the control voltage perturbation $\hat{v}_c$, which together with the $\hat{v}_{\text{in}}$ and $\hat{i}_o$ perturbations allows to study the system dynamical performances.

The switching network model includes a controlled current source whose value depends on the steady-state CCM average current in the inductor I_{L} and a controlled voltage source dependant on $e_0 = V_{\text{in}} \cdot R_{\text{on}}^{\text{HS}} I_L + R_{\text{on}}^{\text{LS}} I_L$. The transformer has a turns ratio which changes accordingly to the steady-state duty cycle $D_0 = T_{\text{ON},0}/T_{\text{SW}} = V_{\text{O}}/V_{\text{IN}}$ and an equivalent series resistance $R_{\text{eq}} = R_{\text{on}}^{\text{HS}} D_0 + R_{\text{on}}^{\text{LS}}(1 - D_0)$ is introduced to account the MOSFET conduction resistances. The output filter network is directly connected from the original schematic of Fig. 1(a).

From the circuit in Fig. 3(a) the control-to-output transfer function between $\hat{v}_c(s)$ and $\hat{v}_o(s)$ is hence derived employing a

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TABLE I
BUCK CONVERTER COMPONENT VALUES - SIMPLIS SIMULATIONS

$R_L(\Omega)$	V_{out} (V)	$R_{\text{on}}^{\text{HS}}(\text{m}\Omega)$	$R_{\text{on}}^{\text{LS}}(\text{m}\Omega)$	$L(\mu\text{H})$	$C_{\text{out}}(\mu\text{F})$	$\text{ESR}_L(\text{m}\Omega)$	$\text{ESR}_C(\text{m}\Omega)$	$f_{\text{SW}}(\text{kHz})$	$C_{\text{MOS}}(\text{nF})$
1	3.3	8	6	2.2	800	10	2	500	2

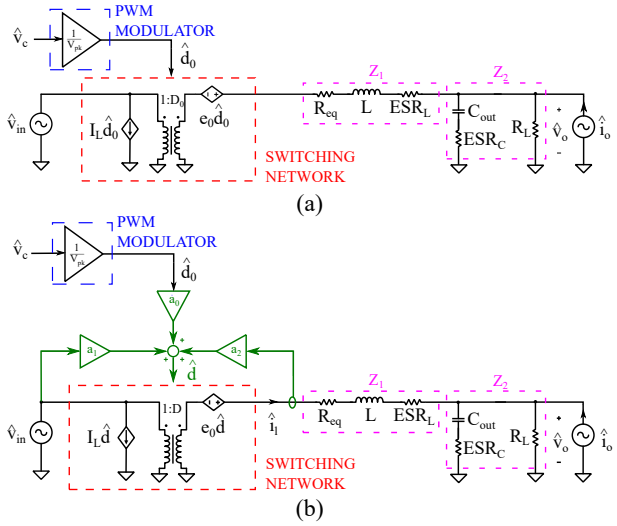

Fig. 3. Small-Signal Model of a Buck Converter. (a): without ZVS; and (b): with ZVS.

TABLE II
OVERALL DUTY CYCLE PARAMETERS

a_0	a_1 (V^{-1})	a_2 (A^{-1})
$\left(1-\frac{C_{\text{MOS}}V_{\text{IN}}(V_{\text{IN}}-V_{\text{O}})}{4LI_{\text{PK}}^2}\right)$	$\frac{C_{\text{MOS}}}{2T_{\text{SW}}I_{\text{PK}}}$	$-\frac{C_{\text{MOS}}V_{\text{IN}}}{2T_{\text{SW}}I_{\text{PK}}^2}$

linear superposition, i.e. imposing $\hat{v}_{\text{in}}(s)$=0 and $\hat{i}_o(s)$=0. This allows to obtain:

$$\frac{\hat{v}_o(s)}{\hat{v}_c(s)} = \frac{e_0}{V_{\text{pk}}} \cdot \frac{Z_2(s)}{Z_2(s)+Z_1(s)} \tag{1}$$

where the impedances $Z_1(s)$ and $Z_2(s)$ enclosed in the purple boxes in Fig. 3(a) can be derived as:

$$\begin{aligned} Z_1(s) &= sL + \text{ESR}_{\text{L}} + \text{R}_{\text{eq}} \\ Z_2(s) &= \left(\frac{1}{sC_{\text{out}}} + \text{ESR}_{\text{C}}\right) \,//\, \text{R}_{\text{L}}. \end{aligned} \tag{2}$$

As shown in Fig. 2, despite the compactness of the circuital model and its easy algebraic maneuverability, it does not include the ZVS mechanism impact on the small-signal model. Note that the capacitance C_{MOS} is not present into the schematic of Fig. 3(a). Plugging it directly in the schematic may be tempting, but it does not provide the correct result. In fact, such approach does not take into account the ZCD loop behaviour (which must be carefully analyzed starting from its operating principle in the time domain portrayed in Fig. 1(b)) and consequently, its impact on the system small-signal model.

Looking at the waveforms in Fig. 1(b), as soon as the HS MOSFET is turned OFF the capacitance C_{MOS} starts to discharge due to the presence of the inductor L, which sinks an amount of current approximately constant and equal to:

$$I_{\text{pk}} = I_l + \frac{1}{2}\frac{V_{\text{in}}-V_{\text{o}}}{L}T_{\text{on},0} \tag{3}$$

where I_l is the average inductor current. The C_{MOS} voltage $\text{V}_{\text{sw}}(\text{t})$ decreases until the ZVS comparator detects a switching node voltage $\text{V}_{\text{sw}} = \text{V}_{\text{th}}$. Assuming without loss of generality that $V_{\text{th}} = 0$, the dead-time T_{d} where both the HS and LS MOSFETs are turned OFF is equal to:

$$T_d = \frac{C_{\text{MOS}}V_{\text{in}}}{I_{\text{pk}}}. \tag{4}$$

The ZVS technique acts as a duty cycle alterations and indeed an equivalent ON time $T_{\text{on,eq}} = T_{\text{on},0} + T_d/2$ can be derived simply rearranging the shape of the $\text{V}_{\text{sw}}(\text{t})$ voltage, as depicted in Fig. 1(b). In particular, the underlying area the $\text{V}_{\text{sw}}(\text{t})$ voltage curve during T_{D} is smeared to obtain a novel square wave. The ON time variation directly reflects on the Buck conversion ratio d as:

$$d = \frac{T_{\text{on,eq}}}{T_{\text{SW}}} = \frac{T_{\text{on},0}+T_d/2}{T_{\text{SW}}}. \tag{5}$$

Perturbing and linearizing the independent parameter d, substituting (3) and (4) in (5) and replacing each quantity with a steady state part plus a time varying small signal contribution, namely:

$$\begin{aligned} d = \hat{d} + D \qquad d_0 = \hat{d}_0 + D_0 \qquad V_{\text{in}} = \hat{v}_{\text{in}} + V_{\text{IN}} \\ I_l = I_L + \hat{i}_l \qquad T_{\text{on},0} = \hat{t}_{\text{on},0} + T_{\text{ON},0}. \end{aligned} \tag{6}$$

The overall duty cycle steady-state and perturbation expressions (respectively, D and $\hat{d}$) are hence derived:

$$\begin{aligned} \hat{d} &= a_0\hat{d}_0 + a_1\hat{v}_{\text{in}} + a_2\hat{i}_l \\ D &= D_0 + \frac{C_{\text{MOS}}V_{\text{in}}}{I_{\text{PK}}}\frac{1}{2T_{\text{SW}}} \end{aligned} \tag{7}$$

where the new parameters introduced are defined in Table II. The extended small-signal equivalent circuit model which embeds the terms in (7) is represented in Fig. 3(b). It correctly introduces the effect of the capacitance C_{MOS} and clearly shows how the ZVS mechanism gives rise to a voltage feed-forward path and an inner current feedback loop, similarly to what described in [11], [12], affecting the system dynamic behaviour.

The input voltage perturbation $\hat{v}_{\text{in}}$, the output current perturbation $\hat{i}_o$ and the control voltage perturbation $\hat{v}_c$ are considered to determine the main open-loop small-signal transfer functions of the extended Buck converter model. Notice that the new circuit model in Fig. 3(b) can be directly derived from the original one in figure Fig. 3(a) simply substituting

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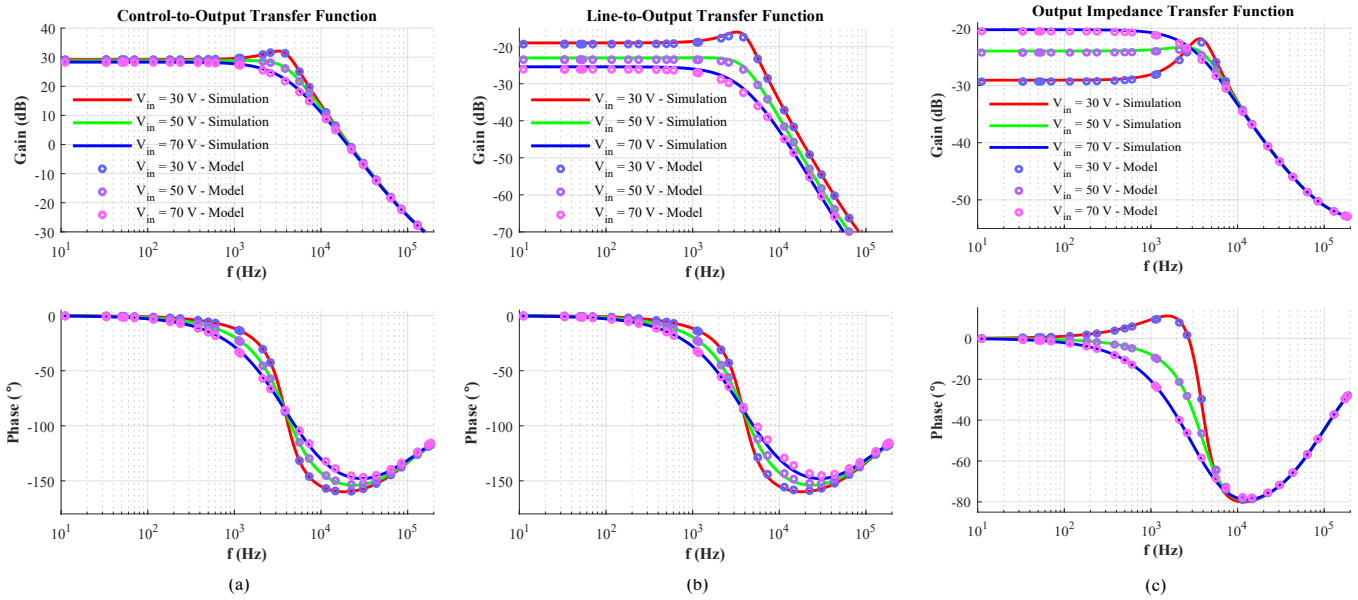

Fig. 4. Comparison between SIMPLIS simulation results and the extended small-signal model derived in IV of the main transfer functions for different V_{in} values. (a) Control-to-output transfer function. (b) Line-to-output transfer function. (c) Output Impedance.

the nominal duty cycle values (d_0 and D_0) with the new ones (d and D), and introducing the green network resulting from (7).

IV. Model Verification

From the extended small-signal model in Fig. 3(b) it is possible to evaluate the dynamic performance of the system, as analytically described from the transfer functions listed in the following.

1) Control-to-Output Transfer Function: For the purpose of determining the control-to-output transfer function, the independent external perturbation sources $\hat{i}_o$ and $\hat{v}_g$ are removed, evaluating the the $\hat{v}_c$ impact on the Buck output voltage $\hat{v}_o$. Following this procedure, the desired transfer function is given by:

$$\frac{\hat{v}_o(s)}{\hat{v}_c(s)} = \frac{a_0 e_0}{V_{\text{pk}}} \frac{Z_2(s)}{Z_2(s) + Z_1(s) + a_2 e_0}. \tag{8}$$

Eq. (8) clearly shows how the $\hat{i}_L$ feedback loop in the overall small-signal model (a_2 in Fig. 3(b)) dampens the control-to-output transfer function. It indeed introduces an equivalent resistance $a_2 e_0$ whose value is V_{in} dependent. The control-to-output transfer function is plotted based on different V_{in} values together with the results offered from the SIMPLIS simulation tool, as shown in Fig. 4(a).

2) Line-to-Output Transfer Function: The open-loop line-to-output transfer function could be derived by nullifying $\hat{i}_o$ and $\hat{v}_c$. Evaluating the transfer function from $\hat{v}_{\text{in}}$ to $\hat{v}_o$:

$$\frac{\hat{v}_o(s)}{\hat{v}_{\text{in}}(s)} = \frac{Z_2(s)(D + a_1 e_0)}{Z_1(s) + Z_2(s) + a_2 e_0}. \tag{9}$$

Both the $\hat{v}_{\text{in}}$ feedforward path and the the $\hat{i}_L$ feedback loop concur in altering the audiosusceptibility of the Buck converter. However, this does not lead to a line transient degradation with respect to the original small-signal model.

The line-to-output transfer function is plotted based on different V_{in} values together with the results offered from the SIMPLIS simulation tool, as shown in Fig. 4(b).

3) Output Impedance: Short-circuiting both the control voltage and the input voltage $\hat{v}_{\text{in}}(s)$ and perturbing with a current source $\hat{i}_o(s)$ the converter output port, the correspondent output voltage perturbation $\hat{v}_o(s)$ can be measured, deriving the open-loop output impedance as:

$$Z_{\text{out}}(s) = \frac{\hat{v}_o(s)}{\hat{i}_o(s)} = Z_2(s) || (Z_1(s) + a_2 e_0). \tag{10}$$

Similarly to what has been discussed for the control-to-output transfer function, the output impedance of the converter became larger and it is also damped due to the $\hat{i}_L$ feedback loop. This consequently modifies the load transient response of the Buck converter.
The output impedance transfer function is plotted based on different V_{in} values together with the results offered from the SIMPLIS simulation tool, as shown in Fig. 4(c).

V. Conclusion

The ZVS mechanism for the LS MOSFET in a synchronous Buck converter has been analytically described and embedded into the traditional equivalent small-signal model of Buck converter operating in CCM. The analysis carried out on the extended small-signal model allowed to predict how the implemented ZVS technique impacts the dynamic performance of the open-loop Buck converter, evaluating the main system transfer functions (i.e., control-to-output, line-to-output and output impedance). Finally, SIMPLIS simulations have been performed to confirm the validity of the derived model, which accurately tracks the system frequency response.

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