

Faults Detection in the Heatsinks Mounted on Power Electronic Transistors

*Original*

Faults Detection in the Heatsinks Mounted on Power Electronic Transistors / Quitadamo, Matteo V.; Piumatti, Davide; SONZA REORDA, Matteo; Fiori, Franco. - In: INTERNATIONAL JOURNAL OF ELECTRICAL AND ELECTRONIC ENGINEERING AND TELECOMMUNICATIONS. - ISSN 2319-2518. - STAMPA. - 9:4(2020), pp. 206-212. [10.18178/ijeetc.9.4.206-212]

*Availability:*

This version is available at: 11583/2789734 since: 2020-02-06T10:37:56Z

*Publisher:*

International Journal of Electrical and Electronic Engineering & Telecommunications

*Published*

DOI:10.18178/ijeetc.9.4.206-212

*Terms of use:*

This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

*Publisher copyright*

(Article begins on next page)

# Faults Detection in the Heatsinks Mounted on Power Electronic Transistors

Matteo V. Quitadamo<sup>1</sup>, Davide Piumatti<sup>2</sup>, Matteo Sonza Reorda<sup>2</sup>, and Franco Fiori<sup>1</sup>

<sup>1</sup>Dip. di Elettronica e Telecomunicazioni (DET) – Politecnico di Torino, Torino, Italy

<sup>2</sup>Dip. di Automatica e Informatica (DAUIN) – Politecnico di Torino, Torino, Italy

Email: {matteo.quitadamo; davide.piumatti; matteo.sonzareorda; franco.fiori}@polito.it

**Abstract**—Nowadays, power electronics is widely used in many applications, e.g., in industrial field, transport field and household appliances used daily. Considering the high temperature reached in power circuits, it is necessary to introduce some heat dissipation systems able to transfer heat to the surrounding environment. The correct mounting of the heatsink or its physical deterioration over time can affect the operation of the system. The overheating may lead to an ageing acceleration of the power devices or to their permanent damage. This greatly influences the reliability and safety of power systems used in safety-critical applications, e.g., for automotive, rail or industrial environments. Hence, it is necessary to introduce some test strategies to identify those heatsinks that do not operate correctly, e.g., because they are not correctly assembled during the production of the Printed Circuit Board (PCB). This paper proposes a methodology to test the assembly of heatsinks on power devices. The proposed approach relies on an in-circuit test method at the end-production on the final PCB. The test is carried out without resorting to thermal measurements. Generally, the thermal measurements cannot be performed by the modern Automatic Test Equipment (ATE). The proposed test methodology was evaluated experimentally on a power MOSFET in TO220 package; the MOSFET considered is used in a half bridge.

**Index Terms**—Power electronics, Heatsink test, Safety-Critical applications, End-manufactory in-circuit test

## I. INTRODUCTION

Power electronics plays a key role in modern technology. It is used in many industrial applications, in the transport and generation of electricity, in the transport systems of goods and people and in many everyday applications. Power electronics is involved in many safety-critical environments such as those industrial, automotive, medical and household ones. In safety-critical systems, a fault can lead to considerable consequences for the health or life of the users. Safety-critical systems require accurate test mechanisms at the end of their manufacturing and in field. All the aspects of critical systems must be tested: the digital control part, the analog part and the power part. Several software and hardware approaches are available to test the digital parts [1]. Other test strategies are also available to test the

analog and power parts [2], [3] and to evaluate the fault coverage [4]–[7] of the test procedures. In contrast to the low power used in digital electronics, in high power applications the temperature can reach very high values [8]. For this reason, it is common to mount on the power devices some heatsinks for quick heat dissipation. Malfunctions of dissipating systems may lead to a dangerous overheating of the power devices. Even the dissipation systems, regardless of its complexity, may thus require testing strategies in order to verify their correct functioning at the end of the production process [9]. Unfortunately, the test of such systems is not always adequately considered and no specific test is carried out. Typically, passive dissipation systems are made of bulky heatsinks equipped with radial metal plates designed for heat dispersion. These systems may not work properly due to their incorrect assembly, their physical breakage or because they are obstructed with dust or dirt.

The aim of this paper is to propose an end-of-manufactory test strategy able to check the correct behavior of the dissipation systems. Currently, the check on the correct assembling of the heatsinks is often performed only in a qualitative way through a simple automatic optical inspection [10]. This test methodology is not sufficient to detect defects in the heatsink assembly phase; the optical inspection only provides a check on the presence of the heatsink on the final PCB. The goal is to propose a methodology able to detect the possible defects affecting the dissipation systems by means of electrical measurements. These defects may be related to the mounting phase of the heatsink during the assembly of the Printed Circuit Board (PCB) [11], [12], or to a damaged heatsink. The use of thermal probes on the heatsink under test is not always effective, because the temperature of the heatsink is not uniform over its surface and it is not always possible to identify a good point for measuring the temperature. Besides that, a lot of Automatic Test Equipment (ATE) are not equipped with thermal probes or other sensors able to monitor the temperature. Some power modules are equipped with thermal sensors suitable to detect the effectiveness of the heatsink. Furthermore, these sensors are rarely placed near all heatsinks present in the system. Usually, on-board sensors are used for monitoring the average temperature of the system. It is common to introduce simple thermal protections, such as those based on Positive or Negative Temperature Coefficient resistors (PTCs or NTCs), which turn off the system in case of

---

Manuscript received October 5, 2019; revised November 2, 2019; accepted November 26, 2019.

Corresponding author: Matteo V. Quitadamo (email: matteo.quitadamo@polito.it)

excessive overheating [13]. Therefore, it is preferable to perform the heatsink test without executing direct thermal measurements, but exploiting voltage and/or current measurement on the Device Under Test (DUT). The modern ATE systems are equipped with several active and passive probes able to perform the electrical measurements with an excellent resolution. Obviously, this is possible only if the ATE is able to access the power devices pins (in other words, if a physical contact of the power device by the ATE probes is possible). In this paper, we propose an analysis of the impact of different assembling defects of the heatsinks on the electrical parameters of the transistor; in particular, the resistance between the drain and source terminals ( $R_{on}$ ) of the MOSFET device is considered [14]. The  $R_{on}$  evaluation is used, in the proposed approach, for testing the heatsink assembly. Such test is performed in-circuit using an ATE. Considering a typical probe equipment of a modern ATE, the proposed methodology does not consider temperature measurements to perform the tests, but it uses only some electrical voltage measurements that can be easily and quickly performed by an ATE. The test is executed on the final PCB at the end of production. The test requires knowing the mathematical relationship between the junction temperature ( $T_j$ ) and the  $R_{on}$  values, and this relationship is obtained experimentally by characterizing the transistor. In particular, the capability of the method to identify small variations of the thermal resistance is checked referring to a simple configuration.

This paper is organized as follows: Section II introduces some concepts concerning the modelling of thermal systems that are normally used to identify the suitable heatsink during the design of the system. In Section II the thermal effects on power devices are discussed. Section III introduces the concepts of thermal faults. The power case study used in this paper is described in Section IV. Section V reports the experimental results on the case study, while Section VI draws some conclusions.

## II. BACKGROUND

This section provides the reader with the required information about the thermal system [15], with particular emphasis on the physical meaning of the thermal quantities used in this paper. The second subsection describes the effects of the temperature on the power devices. Finally, the in-circuit test method developed in this work is described.

### A. Thermal Concept in the Electrical Field

The main concept of the thermal system is briefly introduced. The heat flow propagation in a real device can take place in three different ways: convection, radiation, and conduction [16]. In electronic PCBs, the heat propagation occurs mainly due to the conduction phenomenon; convection and radiation phenomena are normally not considered in the electronic field [16]. Thermal systems are modelled referring to equivalent circuits composed of thermal resistances and thermal capacitances [16], [17]. In physics, the thermal resistance

is defined as the difficulty that heat encounters when going through a solid element of the system [17]. With reference to Fig. 1, that shows a typical heatsink used on a power transistor encapsulated in the TO220 package, it is possible to identify three thermal resistances ( $R_{thjc}$ ,  $R_{thcd}$ ,  $R_{thda}$ ). The thermal resistance  $R_{thjc}$  identifies the difficulty to propagate the heat through the transistor (i.e., from the die to the surface of the transistor package). The value of the  $R_{thjc}$  is provided by the transistor manufacturer. The heat propagation difficulty between two contact surfaces is modelled by  $R_{thcd}$  resistor; the value of  $R_{thcd}$  depends on how the heatsink is mounted on the transistor, as discussed in [18] and [19]. The value of such resistance is mainly determined by the size of the surface contact and by its quality. Finally,  $R_{thda}$  describes the thermal resistance between the heatsink and the air. For the sake of simplicity, in this work, the equivalent thermal resistance from the junction to ambient is considered ( $R_{thja}$ ).

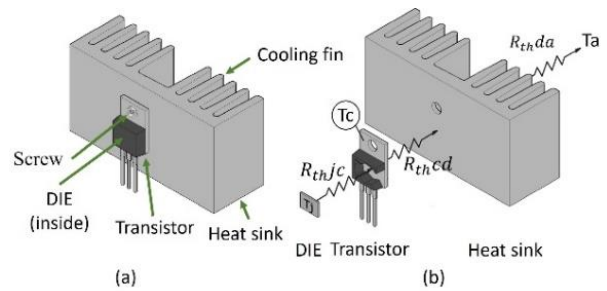


Fig. 1. Model approximation of thermal system: a) Physical system and b) physical system with thermal resistance [20].

The description provided in Fig. 1 is a model approximation, because there are a lot of other factors that influence the system. Fig. 1 assumes that the heat flow is unidirectional from the die to the heatsink, but the heat propagates in every direction. Moreover, the ambient temperature ( $T_a$ ) or other heat sources near to the transistor, influence the system dissipation. For these reasons, the development of a thermal model starting from a simple physical analysis of the system is difficult. In general, as discussed in [21], the  $R_{thja}$  can be estimated by

$$R_{thja} = \frac{T_j - T_a}{P_{dis}} \quad (1)$$

where  $R_{thja}$  identifies the whole thermal resistance of the system,  $T_j$  the junction temperature of the transistor,  $T_a$  the ambient temperature, and finally  $P_{dis}$  is the power dissipated by the transistor.

In addition to thermal resistances, thermal capacitances should be also taken into account. The thermal capacitance of an object describes the amount of heat that the object can store. Such capacitance is defined as the amount of heat to be supplied to a given mass of a material to produce a unit change in its temperature [17]. The thermal capacitance is determined by the mass ( $M$ ) of the object and by its specific heat ( $C$ ):

$$C_{th} = CM \quad (2)$$

The thermal capacitance influences the duration of the thermal transients. When the physical system is in steady-state, i.e. the power dissipated by the transistor is constant, the thermal capacitances do not influence the temperature trend.

**B. Thermal Effects on Power Devices**

The junction temperature significantly impacts the performance and the reliability of the transistors. A high junction temperature accelerates the failure mechanisms and reduces the lifetime of the devices. From an electrical point of view, these failure mechanisms [17] include the gate oxide breakdown, the electromigration, the hot electron effects, and the negative bias temperature instability. The causes of device break are not limited to electrical issues, but also to physical and mechanical ones [17]. The junction temperature fluctuations create, inside of the power devices, some mechanical stresses [17]. The transistor is composed of materials with different thermal coefficients of expansion. The temperature variation causes mechanical stresses between the different materials (silicon, aluminium, iron, plastic, and so on) [17]. The mechanical stresses are the main causes of break of the solder connection of the devices on the board. Other important issues connected to the mechanical stresses are related to the wire bonding connections between the die and the external contacts of the devices. All these aspects reduce the reliability of the device in the long term: this is one of the key aspects for safety systems. Moreover, the junction temperature increase influences many of the functional parameters of the power devices [13], [17], [21]. The drain-source resistance of the MOSFET increases with the junction temperature increase [17], [21], [22]. The conduction loss is almost doubled when the temperature increases from 25 °C to 150 °C [16], [17]. On the other hand, the threshold voltage of a MOSFET decreases with the temperature increase [17], [21]. The reduction in the threshold voltage increases the leakage current of the transistor [17], [21]. All these features of the transistors can be used as Thermal Sensitive Parameters (TSEP) [23]. Such parameters, along with a proper calibration process, allow one to evaluate the junction temperature. In this work the  $R_{on}$  is considered as TSEP.

**C. In-Circuit Test Method**

Modern automatic test equipment (ATE) allow one to perform different tests to be performed at the end of production, and these tests are based on the in-circuit test method. The ATEs are equipped with a given number of needles able of contacting the electrical components on the PCB. These electric needles can be used to apply voltages or to inject/sink currents in the circuit. Moreover, with electric probes, it is possible to perform voltage or current measurements. In general, current measurements are only possible if sense resistors are present in the circuit. During the in-circuit test, the board is not powered and no electrical stimulation is applied to the system, except those supplied by the ATE. Clearly, all precautions concerning the positioning of the guarding probes [11], [12] must be considered. Guarding probes

are able to avoid damage during the in-circuit test, as widely discussed in [11][12]. The test electrical stimuli are applied directly to the transistor. The stimuli would spread through the network damaging the electrical circuits in absence of the guard probes. These guarding probes are useful in the points connected to ground for escaping portions of circuits during in-circuit tests. The current ATEs are equipped with numerous guarding probes used during the in-circuit tests.

**III. PROPOSED APPROACH**

In this paper, a *thermal fault* is defined as an alteration of the dissipation capability of a heatsink, in accord with the thermal resistance concept described in Section II. A thermal fault is an increase of  $R_{thja}$  over the expected value. In other words, there is a further obstacle to the passage of heat from the die to the air due to a thermal fault. Typically, a thermal fault can be caused by incorrect assembling of the heatsink or its physical damage. The proposed approach is based on a characterization of the transistor, and this characterization is performed before the test phase. In particular,  $R_{on}$  of the transistor is characterized considering different  $T_j$ . Afterwards, this characterization is used in the test phase.

**A. Mosfet Temperature Characterization as  $R_{on}$  Function**

The evaluation of the MOSFET temperature performing electrical measurements requires an initial calibration procedure. In particular, a constant current is forced for increase the  $T_j$  temperature; The drain source voltage  $V_{ds}$  is measured during the variation of the  $T_j$ . Such characterization can be divided in two steps, a heating phase and a cooling one. During the heating phase the transistor is in the saturation region, in order to dissipate a lot of power for quickly reach a high temperature (about the maximum  $T_j$  supported by the device). Instead, during the cooling phase the transistor is switched in ohmic region with the purpose of dissipating less power. The temperature of the device is monitored, and synchronously, only during the cooling phase, the  $V_{ds}$  voltage is acquired. Such characterization is performed by means of the circuit in Fig. 2.

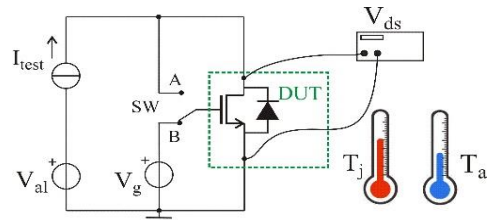


Fig. 2. Circuit for extrapolating the relation between  $T_j$  and  $R_{on}$ .

The switch  $SW$  allows the user to move from the diode configuration of the MOSFET to the ohmic region. The transistor is in saturation region when configured as a diode. The function relating the  $T_j$  to  $R_{on}$  can be extrapolated from the measurements of  $R_{on}$  and the acquired temperature at the same time instants. Such relation is used, in the next step, to evaluate the  $T_j$  and consequently the  $R_{thja}$ . The  $R_{on}$  characterization phase is performed with only the transistor in the on state, and it is

not influenced by the rest of the circuit. Other heat sources that change the temperature of the transistor during the working of the circuit can be detected performing an  $R_{on}$  measurement.

**B. Thermal Faults Detection**

During a test, a wrong assembling of the heatsink can be detected following the steps listed below:

- 1) Knowing the rated dissipated power of the transistor ( $R_{thjs}$ ) and its nominal  $R_{on}$  ( $R_{on,nom}$ ), it is possible to calculate the voltage  $V_{test}$  to apply on transistor. The power considered with such calculation is less than half of the nominal one. This reduces the probability of damaging the device if heatsink is incorrectly mounted.

$$V_{test} = \sqrt{(P_{rat} / 2)^2 R_{on,nom}} \quad (2)$$

The value of  $V_{test}$  does not affect the test, and it is chosen conservatively to avoid damaging the transistor.

- 2) The ATE forces the gate-source voltage ( $V_{gs}$ ) to the nominal high value of the gate driver in order to turn-on the power transistor.
- 3) The voltage  $V_{test}$  is applied to the DUT. During the test, the  $V_{ds}$  voltage and the  $I_d$  current are monitored by the ATE, as shown in Fig. 3.
- 4) When the ratio between the  $V_{ds}$  and  $I_d$  reaches the steady-state (thermal equilibrium), the value of  $R_{on}$  is derived from the last measure of  $V_{ds}$  and of  $I_d$  as  $R_{on} = V_{ds} / I_d$ . The resistance  $R_{on}$  is used to evaluate  $T_j$  by  $R_{on}(T_j)$  characterization.
- 5) The eq. 1 is used to evaluate the  $R_{thja}$ .
- 6) Finally, if the obtained value is larger than the maximum declared, a thermal fault is detected.

Fig. 3 shows the circuit implemented by the ATE to perform the test.

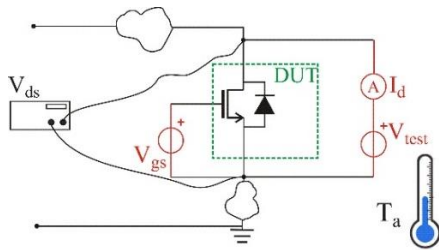


Fig. 3. ATE configuration for testing the heatsink mounting.

**IV. CASE STUDY**

This section describes the circuit used to validate the introduced method. The circuit is an half bridge, i.e., it delivers an output voltage that is lower than the input one. The circuit is shown in Fig. 4.

The converter operates with an input voltage of 48 V and supplies a stable voltage of 12V. The maximum current that can be supplied by the converter is about 4 A. The power transistor considered is available in package TO-220. Its nominal  $R_{on}$  at 25 °C is 600 mΩ. The maximum junction temperature tolerable by the transistor is 150 °C.

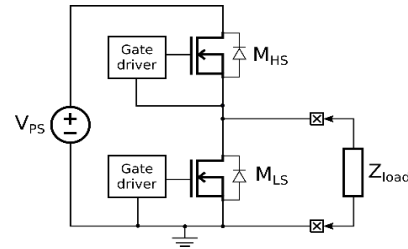


Fig. 4. Half bridge schematic.

**V. EXPERIMENTAL RESULTS**

The proposed methodology has been experimented on one transistor of the case study shown in the previous section. Initially, as discussed in Section III, the power transistor is characterized in order to extract the relationship between the  $T_j$  and the  $R_{on}$ . For the sake of simplicity, since the tab of transistor is directly connected to the drain terminal, it is possible to approximate the junction temperature with the tab temperature during the cooling phase, as discussed in [24]. The Fig. 5 shows the  $T_j$  during the heating and cooling phases, while Fig. 6 shows the  $V_{ds}$  during the cooling phase. This characterization was performed for five different current levels, without and with heatsink. All the experiments highlight that the relationship is significantly not influenced by the power level and by the dissipating conditions, as shown in Fig. 7.

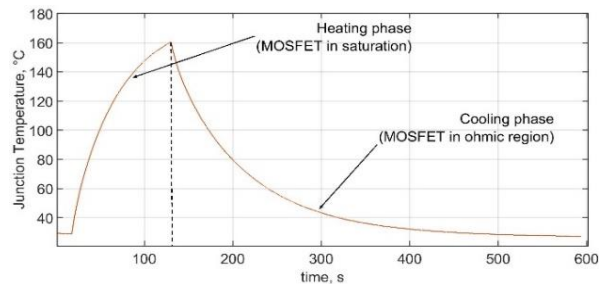


Fig. 5. Junction temperature in the heating and cooling phase during the calibration procedure

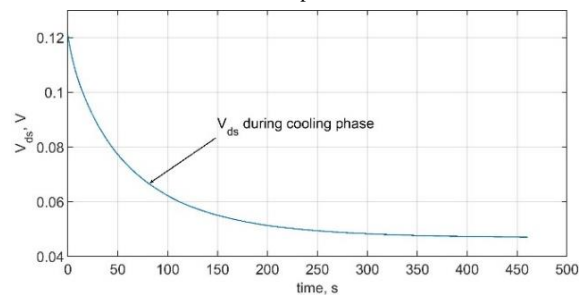


Fig. 6.  $V_{ds}$  in the cooling phase for calibration process.

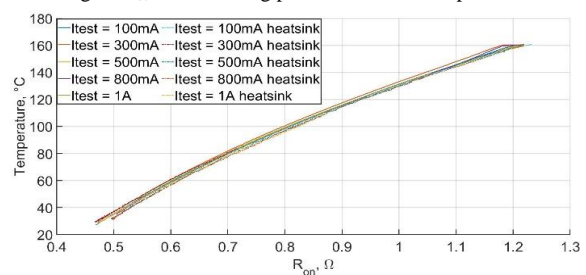


Fig. 7. Junction temperature as function of  $R_{on}$  with several current test and with and without heatsink



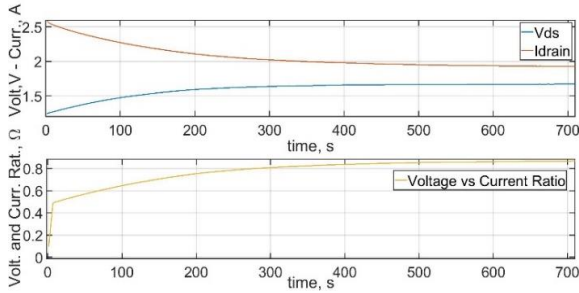


Fig. 8. Vds voltage and Idrain current during the test procedure.

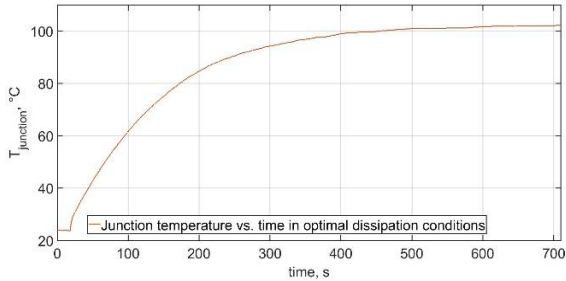


Fig. 9. Junction temperature during the test procedure.

In order to verify the effectiveness of the proposed approach, the DUT was configured for evaluating the thermal resistance in different dissipating conditions. In this analysis, the thermal resistance is evaluated with  $R_{on}$  measurements and with temperature evaluation, in order to compare the obtained results. Firstly, the transistor with an optimal mounting of the heatsink was characterized using four different power level. In such condition, the average value of  $R_{thja}$  measured using the temperature estimated with the thermocouple is 25.22 °C/W (with a standard deviation of  $\pm 2$  °C/W), while the average value evaluated with the proposed approach is 26.17 °C/W (with a standard deviation of  $\pm 1.44$  °C/W). The Fig. 8 shows the behavior of Vds, Idrain and of their ratio with the heatsink correctly assembled; in this chart, the transistor dissipating a power of 1.93W in steady-state. Instead, Fig. 9 shows the behavior of  $T_j$  during the test. It is possible to notice that the steady-state of the voltage and current ratio corresponds to the temperature steady-state, as expected.

Six different fault cases are experimentally considered. In each case a further heat obstacle between the heatsink

and the tab of the MOSFET is voluntarily introduced. All the analyzed cases are reported in Table 1. In particular, the Case 1 refers to a metal washer placed between the tab and the heatsink to reduce the contact surface, while in the Case 2 the metal washer is replaced with a plastic one to reduce the thermal conductivity. In Case 3, the metal screw used to mount the heatsink until this point is replaced with a plastic one. In such case the plastic washer is still between the tab of the MOSFET and the heatsink. In Case 4 the heatsink is again mounted with metal screw but the couple between this one and the bolt is reduced. No obstacles are placed between the heatsink and the tab of the transistor. Finally, Case 5 and Case 6 consider a piece of paper between the heatsink and the tab of the transistor that covers half and all the contact surface respectively. As reported in Table I, all the fault cases show a good matching between  $R_{thja}$  evaluated using the measured temperature and the one estimated with  $R_{on}$ . With the proposed approach, all the considered fault cases are detected. In fact, all the estimated thermal resistances are out of the range of validity provided by the case of optimal mounting. The values reported in Table I were measured in the thermal regime; the system reaches the thermal regime in about 20 minutes.

## VI. CONCLUSION

This paper introduces the concept of thermal fault in heat dissipation systems. An analysis of the thermal effects present on the transistor linked to a device overheating is provided. The overheating of a power device causes a rapid ageing and rapid damage of the transistor. For this reason, it is necessary to perform a test also for heatsinks; in particular, a test on the heatsink assembling is proposed in this paper. An in-circuit test methodology, using electrical measurements, is proposed in this paper. The proposed methodology can be implemented at the end of production by an ATE. The proposed methodology was evaluated on a power device performing accurate results and optimal capability of faults detection.

## CONFLICT OF INTEREST

The authors declare no conflict of interest.

TABLE I: RESULTS OBTAINED FROM THE CONSIDERED CASES

Case	$V_{test}$ (V)	$V_{ds}$ (V)	$I_{ds}$ (A)	$R_{on}$ (mΩ)	$P_{diss}$ (W)	$T_j$ (°C)	$T_j(R_{on})$ (°C)	$T_a$ (°C)	$R_{thja}$ (°C/W)	$R_{thja}(R_{on})$ (°C/W)
Optimal Dissipation	1.86	1.67	1.93	865	3.22	104.8	110.1	23.1	25.34	26.99
	1.09	0.94	1.52	623	1.44	62.9	63.2	23.2	27.55	27.75
	0.634	0.53	1.04	510	0.55	37.6	37.6	23.6	25.35	25.35
	2.59	2.38	2.10	1130	4.99	137.2	147	24.0	22.65	24.61
Case 1	1.16	1.01	1.51	675	1.52	73.8	74.2	23.9	32.69	32.95
	0.635	0.53	1.02	523	0.54	43.6	40.0	24.1	35.87	29.24
	1.81	1.63	1.76	926	2.86	112.2	119.2	24.2	30.75	33.19
	2.62	2.43	1.91	1270	4.64	155.2	160.0	24.3	28.20	29.24
Case 2	1.22	1.08	1.44	750	1.55	88.1	89.1	24.1	41.15	41.78
	1.82	1.66	1.62	1020	2.69	127.9	133.3	25.2	38.19	40.20
Case 3	1.33	1.18	1.46	808	1.72	96.4	99.5	25.3	41.27	43.06
	1.82	1.66	1.62	1020	2.69	127.9	133.3	25.2	38.19	40.20
Case 4	1.27	1.11	1.6	693	1.77	75.8	78.1	25.3	28.43	29.72
Case 5	1.28	1.12	1.62	694	1.82	76.1	79.0	25.0	28.03	29.62
Case 6	1.20	1.06	1.52	695	1.60	77.2	79.5	25.0	32.52	33.95

#### AUTHOR CONTRIBUTIONS

All the authors contribute equally to the implementation of such work, both for bibliographic research, the experimental sessions and for drafting of the paper. All authors had approved the final version.

#### ACKNOWLEDGEMENT

The research was supported by the Power Electronics Innovation Center (PEIC) of Politecnico di Torino.

#### REFERENCES

- [1] U. Backhausen, O. Bailan, P. Bernardi, *et al.*, "Robustness in automotive electronics: An industrial overview of major concerns," in *Proc. IEEE 23rd International Symposium on On-Line Testing and Robust System Design (IOLTS)*, Thessaloniki, 2017, pp. 157-162.
- [2] S. Abdennadher, "Effects of advances in analog, mixed signal and IO circuits on test strategies," in *Proc. 17th Asian Test Symposium*, Sapporo, 2008, pp. 145-145.
- [3] L. Marinelli and R. Small, "Automatic analog circuit test strategist: the application of artificial intelligence to the generation of ATE software," in *Proc. IEEE Automatic Testing Conference, The Systems Readiness Technology Conference, and Automatic Testing in the Next Decade and the 21st Century*, Philadelphia, PA, USA, 1989, pp. 132-137.
- [4] N. B. Hamida and B. Kaminska, "Analog circuit testing based on sensitivity computation and new circuit modeling," in *Proc. IEEE International Test Conference*, Baltimore, MD, USA, 1993, pp. 652-661.
- [5] H. Stratigopoulos and S. Sunter, "Fast monte carlo-based estimation of analog parametric test metrics," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 12, pp. 1977-1990, Dec. 2014.
- [6] S. Sunter. (2018). Analog Fault Simulation Challenges and Solutions. Mentor Graphics. [Online]. Available: [https://semiwiki.com/wp-content/uploads/2017/08/mentorpaper\\_98144.pdf](https://semiwiki.com/wp-content/uploads/2017/08/mentorpaper_98144.pdf)
- [7] D. Piumatti and M. Sonza Reorda, "Assessing test procedure effectiveness for power devices," in *Proc. Conference on Design of Circuits and Integrated Systems (DCIS)*, Lyon, France, 2018, pp. 1-6.
- [8] H. Chen, B. Ji, V. Pickert, and W. Cao, "Real-time temperature estimation for power MOSFETs considering thermal aging effects," *IEEE Trans. on Device and Materials Reliability*, vol. 14, no. 1, pp. 220-228, March 2014.
- [9] A. P. Ferreira, D. Mosse, and J. C. Oh, "Thermal faults modeling using a RC model with an application to web farms," in *Proc. the 19th Euromicro Conference on Real-Time Systems*, Pisa, 2007, pp. 113-124.
- [10] M. L. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*, Springer, 2002.
- [11] C. F. Coombs and H. Holden, *Printed Circuits Handbook*, 7th ed., McGraw-Hill Education, February 2016.
- [12] R. S. Khandpur, *Printed Circuit Boards: Design, Fabrication, Assembly and Testing*, McGraw-Hill, 2006.
- [13] M. H. Rashid, *Power Electronics: Circuits, Devices & Applications*, 4<sup>th</sup> ed., University of Florida, 2018.
- [14] F. Stella, G. Pellegrino, E. Armando, and D. Dapr, "On-line temperature estimation of SiC power MOSFET modules through on-state resistance mapping," in *Proc. IEEE Energy Conversion Congress and Exposition*, Cincinnati, OH, 2017, pp. 5907-5914.
- [15] C. Zhang, M. Mihajlovi, and V. F. Pavlidis, "Adaptive transient leakage-aware linearised model for thermal analysis of 3-D ICs," in *Proc. Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Florence, Italy, 2019, pp. 268-271.
- [16] M. Maerz and P. Nance, "Thermal Modeling of Power-electronic Systems," Fraunhofer Institute for integrated circuits IIS-B, Infineon Technologies AG, *PCIM Europe Mag*, vol. 2, pp. 1-20, Feb. 2000.
- [17] A. Vassighi and M. Sachdev, *Thermal and Power Management of Integrated Circuits*, Springer, 2006, ISBN 978-1-4419-3832-9
- [18] A. Sawle and A. Woodworth. Mounting Guidelines for the Super-247. International Rectifier Application Note AN-997. [Online]. Available: [https://www.fer.unizg.hr/\\_download/repository/ineu\\_sasa/06\\_Hladnjaci/Predavanje-Spoj\\_tr\\_na\\_hladnjak.pdf](https://www.fer.unizg.hr/_download/repository/ineu_sasa/06_Hladnjaci/Predavanje-Spoj_tr_na_hladnjak.pdf)
- [19] P. Dugdale, A. Woodworth, "Mounting Considerations for International Rectifiers Power Semiconductor Packages", International Rectifier Application Note AN-1012, [https://ecee.colorado.edu/~mclurel/IRF\\_Heat\\_Sinks\\_an-1012.pdf](https://ecee.colorado.edu/~mclurel/IRF_Heat_Sinks_an-1012.pdf)
- [20] EngTools.online. (2018). [Online]. Available: <https://www.engtools.online/heatsink.html>
- [21] J. Jose, A. Ravindran, and K. K. Nair, "Study of temperature dependency on MOSFET parameter using MATLAB," *International Research Journal of Engineering and Technology*, vol. 3, no. 7, pp. 1530-1533, July-2016.
- [22] M. Jin, Q. Gao, Y. Wang, and D. Xu, "A temperature-dependent SiC MOSFET modeling method based on MATLAB/Simulink," *IEEE Access*, vol. 6, pp. 4497-4505, Nov. 2017.
- [23] M. H. M. Sathik, J. Pou, S. Prasanth, V. Muthu, R. Simanjorang, and A. K. Gupta, "Comparison of IGBT junction temperature measurement and estimation methods-a review," in *Proc. Asian Conference on Energy, Power and Transportation Electrification (ACEPT)*, Singapore, 2017, pp. 1-8.
- [24] NXP application note AN11261 Using RC Thermal Models. Rev.2. [Online]. Available: <https://assets.nexperia.com/documents/application-note/AN11261.pdf>

Copyright © 2020 by the authors. This is an open access article distributed under the Creative Commons Attribution License (CC BY-NC-ND 4.0), which permits use, distribution and reproduction in any medium, provided that the article is properly cited, the use is non-commercial and no modifications or adaptations are made.



**Matteo Vincenzo Quitadamo** received the M.Sc. degree in electronic engineering from the Politecnico di Torino, Turin, Italy, 2016, where he is currently pursuing his Ph.D. degree. His current research interests include power electronics circuit analysis and design, device modeling, and electromagnetic compatibility.



**Davide Piumatti** received the M.Sc. degree in computer engineering from Politecnico di Torino, Torino, Italy in 2015. Since 2017, he is a Ph.D. student in the Department of Control and Computer Engineering, Politecnico di Torino. His research interests include test of analog, power and digital systems for safety-critical application



**Matteo Sonza Reorda** received the M.Sc. degree in electronics and the Ph.D. degree in computer engineering from Politecnico di Torino, Italy, in 1986 and 1990, respectively, where he is currently a Full Professor with the Department of Control and Computer Engineering. His research interests include test of SoCs and fault tolerant electronic system design.



**Franco Fiori** received the MSc and the Ph.D. degree in Electronic Engineering from the Politecnico di Torino, Italy in 1993 and 1997, respectively. In 1999, he joined the Electronics and Telecom Dpt. of the same University where he is currently an Associate Professor of analog and power electronics. His research interests include the analysis and the design of analog and power electronics as well as electromagnetic compatibility.