

Quality assurance and quality control of the 26 m² SiPM production for the DarkSide-20k dark matter experiment

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Quality assurance and quality control of the 26 m² SiPM production for the DarkSide-20k dark matter experiment

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Abstract DarkSide-20k is a novel liquid argon dark matter detector currently under construction at the Laboratori Nazionali del Gran Sasso (LNGS) of the Istituto Nazionale di Fisica Nucleare (INFN) that will push the sensitivity for Weakly Interacting Massive Particle (WIMP) detection into the neutrino fog. The core of the apparatus is a dual-phase Time Projection Chamber (TPC), filled with 50 tonnes of low radioactivity underground argon (UAr) acting as the WIMP target. NUV-HD-cryo Silicon Photomultipliers (SiPM)s designed by Fondazione Bruno Kessler (FBK) (Trento, Italy) were selected as the photon sensors covering two 10.5 m² Optical Planes, one at each end of the TPC, and a total of 5 m² photosensitive surface for the liquid argon veto detectors. This paper describes the Quality Assurance and Quality Control (QA/QC) plan and procedures accompanying the production of FBK NUV-HD-cryo SiPM wafers manufactured by LFoundry s.r.l. (Avezzano, AQ, Italy). SiPM characteristics are measured at 77 K at the wafer level with a custom-designed probe station. As of March 2025, 1314 of the 1400 production wafers (94% of the total) for DarkSide-20k were tested. The wafer yield is $93.2 \pm 2.5\%$, which exceeds the 80% specification defined in the original DarkSide-20k production plan.

1 Introduction

Silicon Photomultipliers (SiPMs) have emerged as a compelling photosensor solution for detecting single photons in applications ranging from particle physics to medical imaging and beyond [1]. SiPMs consist of an array of tightly packaged Single Photon Avalanche Diodes (SPADs) operated above the breakdown voltage, V_{bd} , so that they generate self sustaining charge avalanches upon absorbing an incident photon [2]. In contrast to the widely used Photo-multiplier Tubes (PMTs), SiPMs are low-voltage powered, insensitive to magnetic field, and have a compact and flat form factor [3]. For these reasons, SiPMs are the adopted solution

in the MEG-II and DUNE experiments [4,5]. In addition, SiPMs have very low residual natural radioactivity, making them especially appealing for low-background experiments such as nEXO and DarkSide-20k [6,7].

DarkSide-20k (DS-20k) is a multi-tonne dark matter detector under construction at the Laboratori Nazionali del Gran Sasso (LNGS) of the Istituto Nazionale di Fisica Nucleare (INFN) that will push the sensitivity for Weakly Interacting Massive Particles (WIMP) detection to the level where solar and atmospheric neutrinos become a significant background. The core of the DS-20k apparatus is a dual-phase Time Projection Chamber (TPC), with a vertical electron drift. The TPC is a 348 cm tall octagonal prism with a 350 cm inner diameter containing the liquid argon (LAr) dark matter target: 50 tonnes of underground argon (UAr) (20 t fiducial volume) [8].

Electron extraction in gas is provided by a stainless steel grid made with 200 μm wires, with a pitch of 3 mm. The gas pocket thickness is expected to be 7 mm. The top and bottom lids of the octagon are made in pure acrylic, and their inner planes are coated with a thin conductive layer of PEDOT:PSS (CleviosTM) and tetraphenyl butadiene (TPB) to shift LAr scintillation light from 128 nm to visible light [9]. The conductive layers allow biasing the inner planes of the two lids, such that they act as cathode and anode. The barrel pieces of the octagon are machined and coated with CleviosTM to define a geometry of conductive rings (field cage) connected by resistors and biased to define a uniform and stable electric drift field of 200 V/cm.

The scintillation light emitted in the TPC is detected by two 10.5 m² optical planes (OP) instrumented with Fondazione Bruno Kessler (FBK) NUV-HD-cryo (near-UV sensitive, high-density, cryogenic compatible) SiPMs located at the top and bottom of the octagonal barrel and used to optically readout the argon scintillation (S1) and electroluminescence (S2) signals in the liquid and gas phase, respectively [10,11].

A stainless steel vessel filled with an additional 36 tonnes of UAr surrounds the TPC. The stainless steel vessel is itself

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immersed in further 650 tonnes of atmospheric liquid argon (AAr), contained within a DUNE-like membrane cryostat. Both argon volumes are outfitted with SiPMs and will serve as the experiment's inner veto (IV) and outer veto (OV) detectors [12].

The inner detector employs the TPC and IV detectors to mitigate the most critical background for dark matter searches, which comes from neutron scattering, while the OV is used to detect and tag external neutrons and muons.

The FBK NUV-HD SiPM technology was introduced in 2016 [13]. The first generation of these devices suffered from a dark count rate (DCR) and afterpulsing probability higher than DS-20k specifications at cryogenic temperatures [7]. A specific process modification was developed by FBK to address the DS-20k requirements [14]. This led to a variant of the FBK NUV-HD technology named FBK NUV-HD-LF (Low Field) that features an almost three-orders of magnitude reduction of the SiPM DCR at 80 K when compared to the standard NUV-HD version, comfortably lower than the DS-20k specification.

Further optimization of this technology allowed for a reduced SiPM afterpulsing probability (NUV-HD-lowAP technology) and quenching resistance, thus optimizing the microcell recharge time constant at cryogenic temperature. These two process adjustments led to the development of a new technology called FBK NUV-HD-cryo, presented in Ref. [15], that not only met but exceeded the DS-20k specifications.

In the final DS-20k photodetector design 24 FBK NUV-HD-cryo SiPMs are aggregated together to form objects known as tiles, with six (three) parallel branches of four (two) SiPMs in series fed into a single transimpedance amplifier (TIA) or a custom designed ASIC amplifier [16, 17], used to instrument the TPC and Veto detectors [18]. The 24 SiPMs are bonded to an Arlon low-radioactive Printed Circuit Board (PCB) [19].

Tiles, in groups of four, are further aggregated in a quadrant: a single analog readout element [20]. Four quadrants are then aggregated into a single object with a total surface area of 400 cm². These devices are called Photo Detector Units (PDUs) and constitute the basic element of the DS-20k photoelectronic system. An example is shown in Fig. 1. In total, 680 PDUs are needed to instrument the two TPC optical planes and the IV and OV detectors (528 TPC, 152 IV and OV), which will make DS-20k the largest SiPM-based cryogenic detector, with more than 260,000 SiPMs.

This paper focuses on the quality assurance and quality control (QA/QC) of the FBK NUV-HD-cryo SiPM production wafers manufactured by LFoundry s.r.l. (Avezzano, AQ, Italy), an Italian semiconductor company with the infrastructure to produce a large number of devices for DS-20k [21].

Wafers manufactured by LFoundry are stored, tested and diced in the Nuova Officina Assergi (NOA) facility, a new

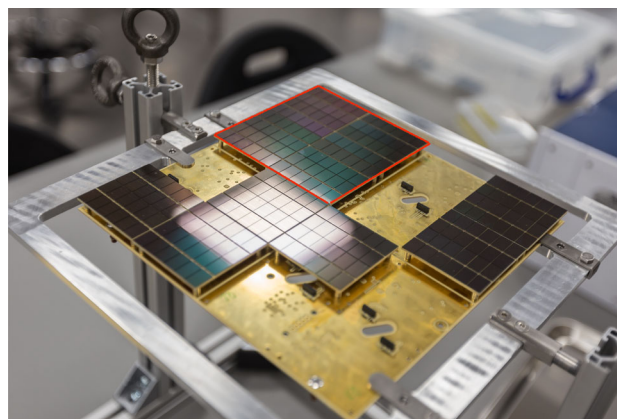


Fig. 1 Tiles prototype partially assembled into a photo detector units (PDU). Each tile consists of 24 FBK NUV-HD-cryo SiPMs with six (three) parallel branches of four (two) SiPMs in series fed into a single transimpedance amplifier (TIA) or a custom designed ASIC amplifier. Tiles, in groups of four, are further aggregated in quadrants. Only one quadrant, shown in red in the figure, is fully populated. Each quadrant is read out as an individual analog readout channel

ISO-6 353 m² clean room packaging facility constructed at INFN LNGS [22–24]. NOA houses state-of-the-art production machines for packaging silicon sensors such as the ones used in DS-20k, and it is currently used for the production of the DS-20k PDUs.

Several SiPM characteristics for each SiPM dice such as breakdown voltage, quenching resistance, leakage current and correlated avalanche noise, are measured with a custom-designed, cryogenic probe station at the wafer level at 77 K. As of March 2025, 1314 of the 1400 production wafers (94% of the SiPM production) were tested. Additionally, 46 extra wafers, considered as engineering pre-production runs, were evaluated. Although identical to those used in the final production, these wafers are termed “engineering” because they were used for prototype tile assembly rather than for fabricating final production-grade tiles. The average wafer yield is $93.2 \pm 2.5\%$, which exceeds the 80% production yield assumed in the original DS-20k production plan.

2 Hardware setup

Figure 2 shows an 8-inch FBK NUV-HD-cryo SiPM production wafers manufactured by LFoundry. Each wafer consists of 268 potentially functional dice, highlighted in yellow in the figure, with a dimension of 11.7×7.9 mm². The wafer in the figure is diced and mounted on a grip-ring, used in the subsequent steps of the DS-20k silicon packaging process flow.

LFoundry produced wafers in 57 batches, known as Lots. Each Lot, containing approximately 25 wafers, is processed together through every foundry stage using automated han-

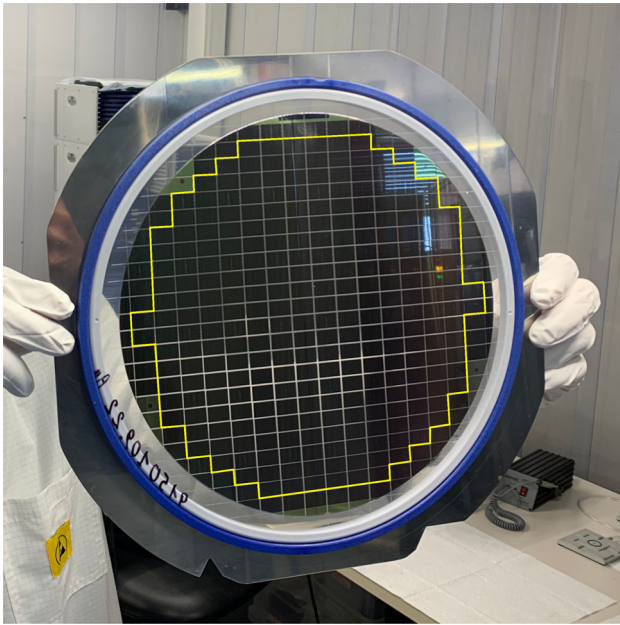


Fig. 2 Production wafer diced and mounted on a grip-ring. The 268 SiPM dice are highlighted in yellow. Due to the overlapping geometry of the probe card and the wafer clamping ring, only 264 of the 268 potentially working SiPMs can be probed at 77 K



Fig. 3 Wafer cassette containing one production Lot (25 wafers). The wafer's gold backside is visible

dling. The most significant variations in wafer performance are expected when comparing different Lots, whereas wafer-to-wafer variations within a single Lot are anticipated to be a minor factor. For batched processes, the differences between wafers are mainly attributable to their positions within the processing equipment. In contrast, for single-process steps, variability arises primarily from tool performance fluctuations over time.¹

¹ An additional component of wafer variability is within-wafer, or site-to-site, variation. This occurs due to process non-uniformities at the wafer scale.

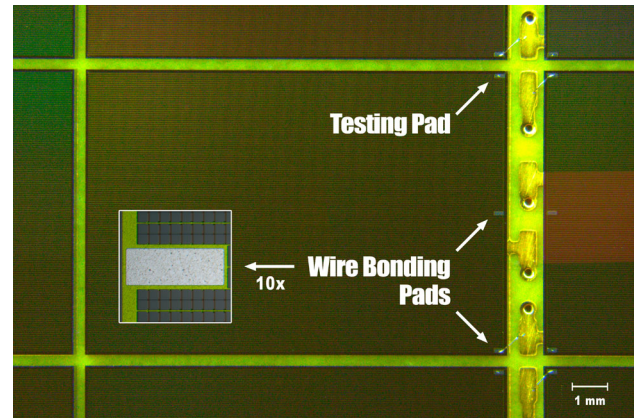


Fig. 4 FBK NUV-HD-cryo SiPM dice bonded to a DS-20k tile. The three aluminum pads are short-circuited together. One of these three pads is used for cryoprobation (top-right), while the other two are used to wire-bond the SiPMs to the corresponding tile PCB. Each dice measures $11.7 \times 7.9 \text{ mm}^2$



Fig. 5 FormFactor PAC200 probe system + S500 Parametric Keithley tester used to characterize the response of the FBK NUV-HD-cryo SiPMs. The entire system is located in a new ISO-6 353 m² clean room packaging facility called the Nuova Officina Assergi (NOA) constructed at the Istituto Nazionale di Fisica Nucleare (INFN) Laboratori Nazionali del Gran Sasso (LNGS)

Figure 3 shows one of the production Lots. Each wafer in the Lot has a gold-coated backside (i.e. silicon substrate) that acts as the SiPM cathode. The SiPM anode contact is made with three bonding pads, connected together, on the frontside of the chips (Fig. 4). One of these three pads is used for cryoprobation (top-right pad in Fig. 4), and the other two are used to wire bond the SiPM to the tile PCB.

A new testing setup (Fig. 5) was built to characterize the SiPM response at the wafer level at 77 K.

It consists of a high precision, semi-automated cryogenic Cascade FormFactor PAC200 probe system (cryoprobe) that cools the wafer to 77 K in a high vacuum environment (10^{-7} mbar) [25]. Wafers are tested with a cantilever, needle-based probe card made by htt group (Munich, Germany) [26] (Fig. 6).

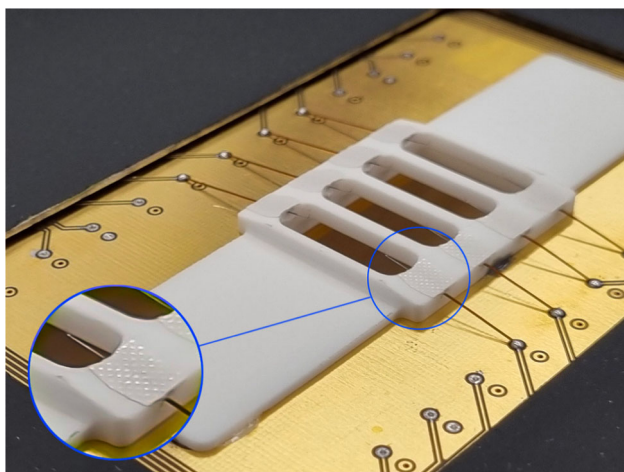


Fig. 6 Htt probe cards designed by FormFactor with 2×4 tungsten needles used for SiPM probing (1 needle per SiPM - shown enlarged in the circle). The white ceramic carrier shown in this photograph connects directly to the needles

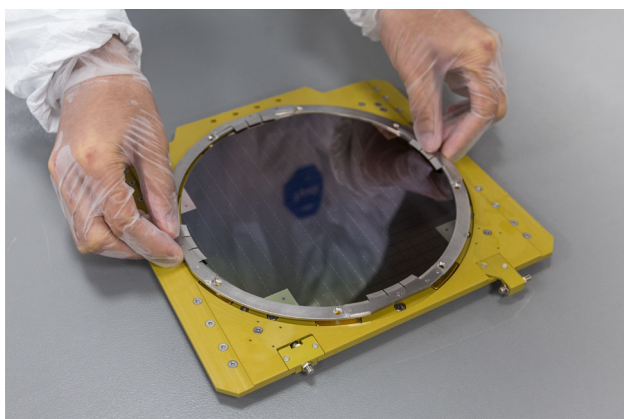


Fig. 7 Production wafer mounted on a gold-plated wafer carrier. The wafer is held in place with a custom-made clamping ring

For the test, wafers are mounted on a gold-plated copper carrier (Fig. 7). Due to mechanical constraints between the probe card and the wafer clamping ring used to hold the wafer in place on the carrier during measurements, 264 out of potentially functional 268 dice in each wafers can be probed with the cryoprobe.²

The wafer carrier is placed in a semi-automatic loader. The loader is evacuated and transports the wafer (in vacuum) into the main chamber via a robot arm. The arm loads the wafer carrier on a gold-plated copper chuck that acts as a common cathode for current–voltage (IV) measurements.

A liquid nitrogen (LN2) cooling coil inside the chuck brings its temperature down to 77 K. The LN2 that flows in the coil is regulated by a needle valve placed on an LN2

transport line that is used to connect the PAC200 probe station to an external LN2 storage Dewar. Two heater resistors maintain the chuck temperature constant to a precision of better than 0.5 K (1σ) at 77 K.

The wafer carrier makes thermal and electrical contact with the chuck through four indium pads. The probe card needles touch down on the wafer surface, contacting the SiPM aluminum pads (1 needle per SiPM). Two probe cards with 24 and 8 needles, respectively, are used to test the wafers and periodically interchanged as part of regular system maintenance. An S500 Parametric tester equipped with Keithley 2612B Source Meters Units (SMU, 1 SMU channel per needle) is used to bias the SiPMs and read their current [27]. The system noise floor (including cables, SMUs, and probe card) is around 10 pA.

The Keithley automated characterization suite (ACS) software program is used in conjunction with the FormFactor PAC200 Velox software to control the cryoprobe automatically, move the chuck from dice to dice, and execute the measurement sequence presented in Sect. 3. A MIDAS-based slow control system [28] is used to monitor the entire procedure and protect the system against human errors (e.g. wrong needle contact heights). Depending on the probe card configuration (i.e. number of needles) and the S500 measurement settings, at least 14 touchdowns are needed to test the accessible wafer surface (264 out of 268 SiPMs). The rate to probe a wafer, including the wafer loading, cooling, measurement, and unloading time, is 0.35 wafers/hour. The cryoprobe is operated 12 h per day, 7 days per week, with an up-time of 85%, which results in a maximum wafer throughput of 25 wafers per week.

3 Experimental details

The forward and reverse bias current–voltage (IV) curves of the testable SiPMs on a wafer (264 out of 268 SiPMs) are collected at 77 K. The cryoprobe vacuum chamber is not completely light-tight: there is a photon-induced rate on the order of a few kHz per SiPM. No external light source is therefore needed to create a measurable current when collecting the reverse bias IV curves. Figure 8 shows IV curves from one production wafer.

To reduce the testing time, SiPMs are measured in parallel. The maximum number of SiPMs that can be measured simultaneously depends on two factors: (i) the probe card configuration (i.e. the number of needles on the card) and, (ii) the parasitic overall series resistance of the measurement system, which includes the cabling and the cryogenic chuck responsible for inducing a voltage drop and therefore lowering the measured current. This drop is negligible for reverse bias IV curves, but it is relevant for forward bias IV curves due

² The 4 SiPMs per wafer not tested with the cryoprobe are not discarded, but instead used to build tiles subsequently tested to ensure compliance with the DS-20k tile specification, presented in a separate work.

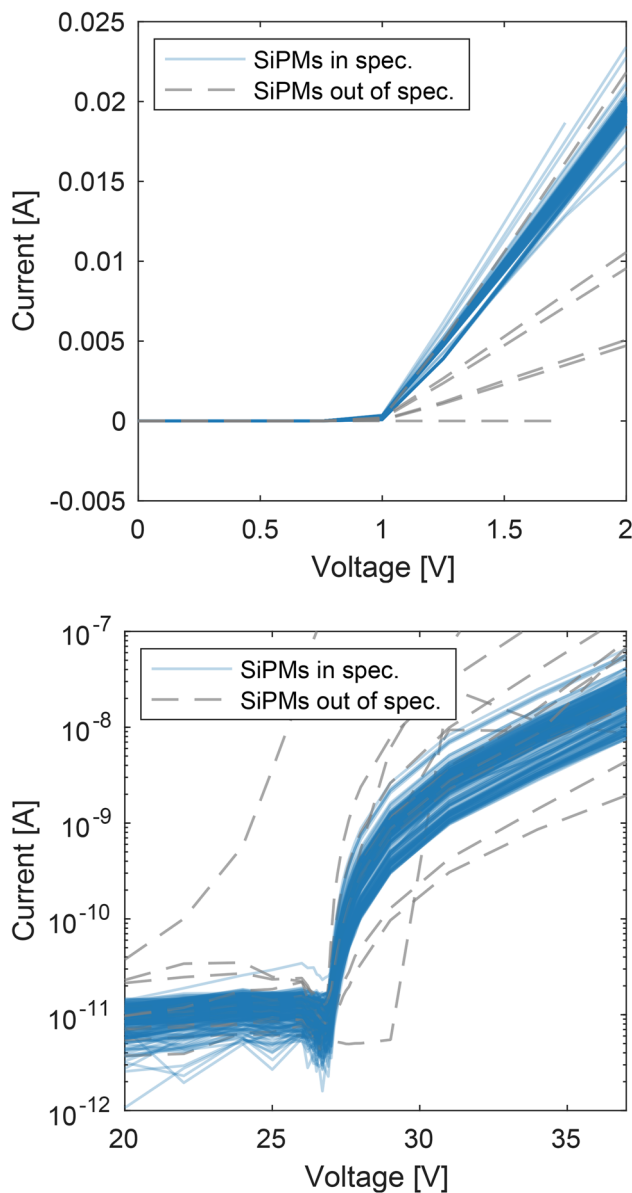


Fig. 8 Forward (top) and reverse (bottom) bias current–voltage (IV) curves for the production Wafer 19 of Lot 9306869. The dashed lines are IV curves that correspond to dice which were discarded based on the selection criteria presented in this work

to the large sourced current (in the order of a few milliAmp), especially when grouping SiPMs, as shown in Fig. 9.³

We also observe a growing instability i.e. larger fluctuation, in the measured current even for reverse bias IV curves, as the number of SiPMs tested in parallel increases, which is

³ The total system resistance is estimated to be 3.7 Ω , of which 2 Ω is due to the resistance between the chuck top surface and its hermetic bottom surface. This value was estimated by the change in slope of the forward bias IV curves when going from a single channel to a four-channel measurement, as shown in Fig. 9. The extrapolated value was also confirmed with a dedicated measurement done on the cryogenic chuck of the PAC200 system.

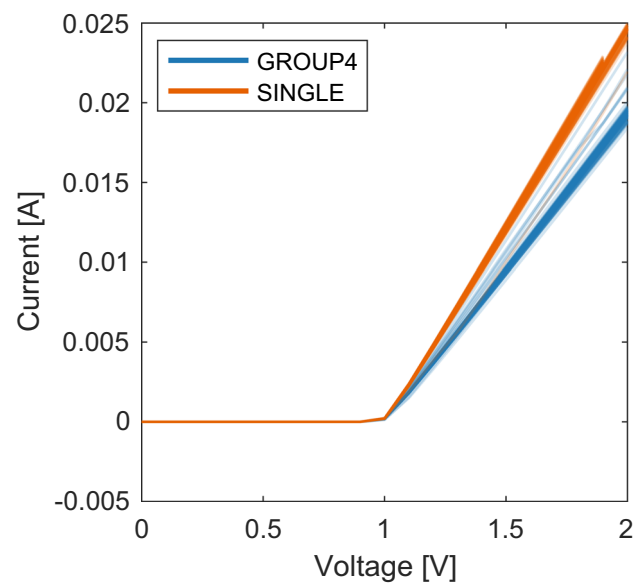


Fig. 9 Forward bias IV curves for one production wafer when simultaneously measuring 4 SiPMs in parallel (GROUP4) versus a single SiPM (SINGLE)

probably due to the common cathode configuration. Overall, we found that grouping 4 (8) SiPMs in parallel for forward (reverse) IV curves represents a good compromise between these effects and the testing throughput.

IV curves in forward bias are measured at constant voltage increments of 0.25 V up to 2 V, which corresponds to a forward current of about 20 mA. IV curves in reverse bias are measured starting from 20 V, several volts below the expected breakdown voltage at 77 K (27.2 V), up to 37 V, which corresponds to roughly 10 V of over voltage, larger than the maximum planned SiPM operating over voltage in the DS-20k detector (7 V). The voltage step is adjusted to be smaller in the range [26.4–27.6] V to obtain a more accurate extrapolation of the breakdown voltage. The step choice is a compromise between accuracy and overall wafer testing time.

A Labview-based application, shown in Fig. 10, was developed to analyze, display, and store the data from the Keithley ACS software (Sect. 2). A PostgreSQL database hosted at INFN-CNAF (Italy) stores the analysis results, tracks the wafers during the entire process flow in NOA, and provides a comprehensive set of criteria for the QA/QC assessment and inventory purposes. The database is also used to keep track of the location and shipping status of wafers, which will be especially important as the detector is assembled.

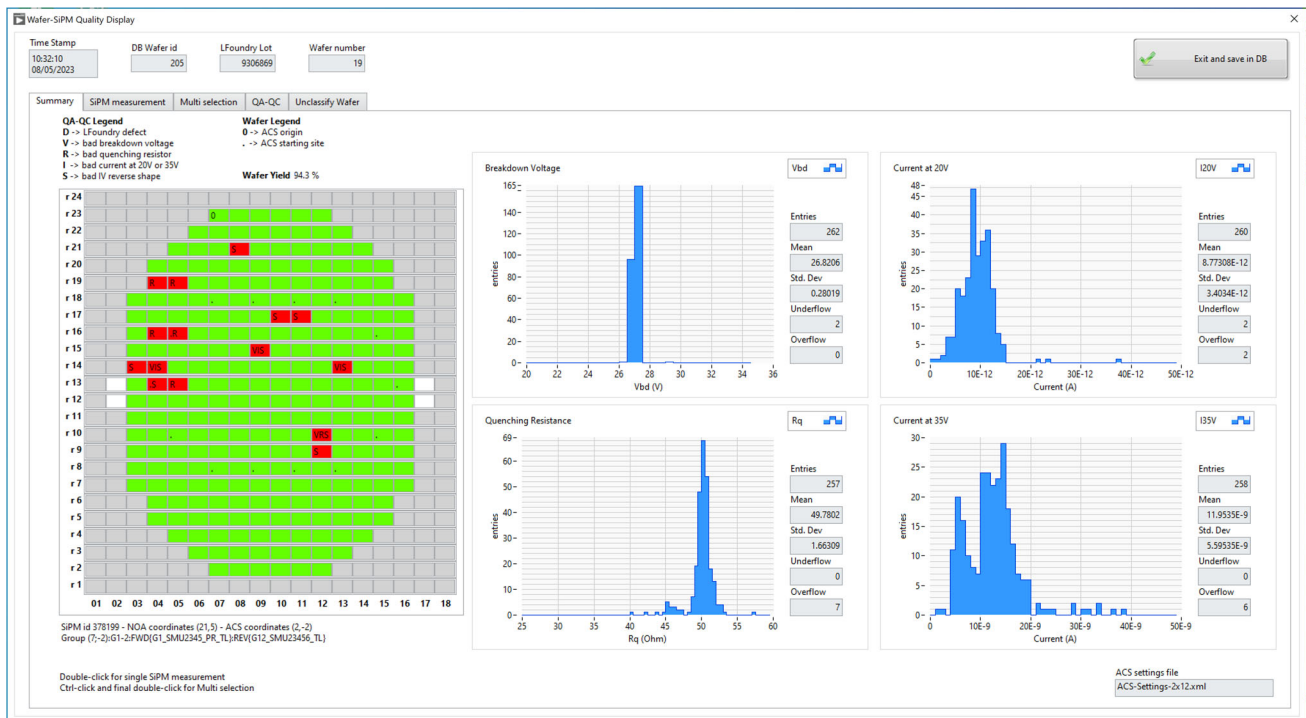


Fig. 10 Main display of the NOA Test Bench SiPM (NOA-TB-SiPM) Labview Application used to analyze the SiPM IV curves measured with the Keithley automated characterization suite (ACS). For each wafer die a reverse and forward bias IV curve is measured at 77 K. Several results are shown to the operator before being stored in the database: (top-left)

breakdown voltage (V_{bd}), (top-right) leakage current below the breakdown voltage (at 20 V) (I_L), (bottom-left) quenching resistor (R_q), and (bottom-right) current at 35 V. Wafer dice coloured in green (red) pass (fail) all (at least one) the wafer-level requirements presented in this work

4 SiPM acceptance criteria

The reverse and forward bias IV curves of each SiPM from all the production wafers are analyzed to ensure compliance with the following DS-20k wafer-level requirements (at 77 K): (i) breakdown voltage $V_{bd} = 27.2 \pm 1.0$ V, (ii) quenching resistor $R_q = 3.35 \pm 1.50$ M Ω , (iii) leakage current below breakdown (at 20 V) $I_L \leq 40$ pA and (iv) Goodness of Fit (GOF) ≤ 20 . The first three requirements are set to obtain an acceptable production yield based on the dispersion of the just introduced parameters measured on pre-production FBK wafers. The goodness of fit parameter is instead based on a χ^2 analysis of the shape of each reverse bias SiPM IV curve and places an upper limit on the SiPM correlated avalanche noise, i.e. crosstalk and afterpulse probability (Sect. 4.4.1). V_{bd} , GOF, and I_L are extracted from the reverse bias IV curve, while R_q is measured from the forward bias IV curve.

4.1 Breakdown voltage distribution

The SiPM breakdown voltage is defined as the voltage at which the first derivative with respect to the voltage of the SiPM current (in log space) is at a maximum [29]. A narrow distribution of this parameter is crucial when grouping

SiPMs in tiles (24 SiPMs, Sect. 1) since a large difference in breakdown voltages would result in a gain and amplitude mismatch when operating tiles at a common bias, reducing the tile single PE resolution [30].⁴

Figure 11 (top) shows the breakdown voltage distribution for all the 359040 tested SiPMs, while Fig. 12 shows the same information grouping SiPMs for their production Lot. At 77 K, the average breakdown voltage is measured to be $\bar{V}_{bd} = 27.19 \pm 0.05$ V.⁵ The dashed lines in the figure represent the DS-20k requirement (27.2 ± 1.0 V). The tested SiPMs comfortably satisfy this requirement.

The variance of the breakdown voltage distribution $\sigma_{V_{bd}}^2$ after exclusion of the out-of-spec data is 0.019 V². This quantity can be decomposed into components:

$$\sigma_{V_{bd}}^2 = \sigma_{V_{bd}/\text{Lot}}^2 + \sigma_{V_{bd}/\text{Wafer}}^2 + \sigma_{V_{bd}/\text{SiPM}}^2, \quad (1)$$

⁴ Within DS-20k, the single photoelectron resolution is defined as the ratio between half of the Gaussian width of the first Photo-electron Equivalent (PE) peak and its centroid.

⁵ In what follows, we will always report summary results using the histogram median and half of its InterQuartile range (IQR/2) so that outliers don't affect the estimators.

where $\sigma_{V_{bd}/Lot}^2$ is the Lot-to-Lot variance, $\sigma_{V_{bd}/Wafer}^2$ is the Wafer-to-Wafer variance of a single Lot, and $\sigma_{V_{bd}/SiPM}^2$ is the SiPM-to-SiPM variance of a single wafer. Each variance contribution has been estimated with a variance component analysis (VCA) [31]. The results are summarized in Table 1. 55.9% of the variance is due to the SiPM-SiPM variability within a wafer. The Lot contribution to the variance is 36.9%, and the remaining 7.3% is due to the Wafer to Wafer variability.

Figure 11 (bottom) shows a visual representation of this analysis using histograms.

We present three histograms: L/W/SiPM, W/SiPM, and SiPM. The L/W/SiPM histogram was obtained by subtracting the median value of the entire distribution from the breakdown voltage of each individual SiPM. Essentially, this represents the whole distribution, shifted to align its median with zero, including all three contributions (Lot, Wafer, SiPM) to the variance. The W/SiPM histogram was created by subtracting the median breakdown voltages within each Lot from the individual SiPM breakdown voltages. This approach removes the Lot-to-Lot contribution to the variance, resulting in each Lot having a median of 0 V. Similarly, the SiPM histogram was produced by subtracting the median breakdown voltages within each Wafer, thus eliminating the Wafer-to-Wafer contribution to the variance. Here the only contribution to the variance is due to the SiPMs themselves.

This representation shows that the breakdown voltage variability drops drastically when the contribution of the Lot is removed. Specifically, moving from L/W/SiPM to W/SiPM, the variance decreases by 36.9% of the total variance, according to Table 1. Furthermore, when the Wafer-to-Wafer variability is removed, i.e., comparing W/SiPM with SiPM, the variance reduction is $1.41 \times 10^{-3} \text{ V}^2$ (7.3% of the total), smaller than the previous case, resulting in a residual variance of $10.8 \times 10^{-3} \text{ V}^2$ that accounts for the 55.9% of the total.

Table 1 Variance component analysis (VCA) of the breakdown voltage (V_{bd}) distribution. VC is the variance component in $\text{V}^2 \times 1000$; % of Tot. is the percentage of each variance component; Cum. VC is the cumulative variance considering the incremental contribution of each component; Cum. Fact. represents the incremental nested factors contributing to the cumulative variance (W and L stand for Wafer and Lot)

Factor	Samples	VC	% of Tot.	Cum. VC	Cum. Fact.
SiPM	359040	10.8	55.9	10.8	SiPM
Wafer	1360	1.41	7.3	12.21	W/SiPM
Lot	58	7.13	36.9	19.34	L/W/SiPM
Total		19.34	100		

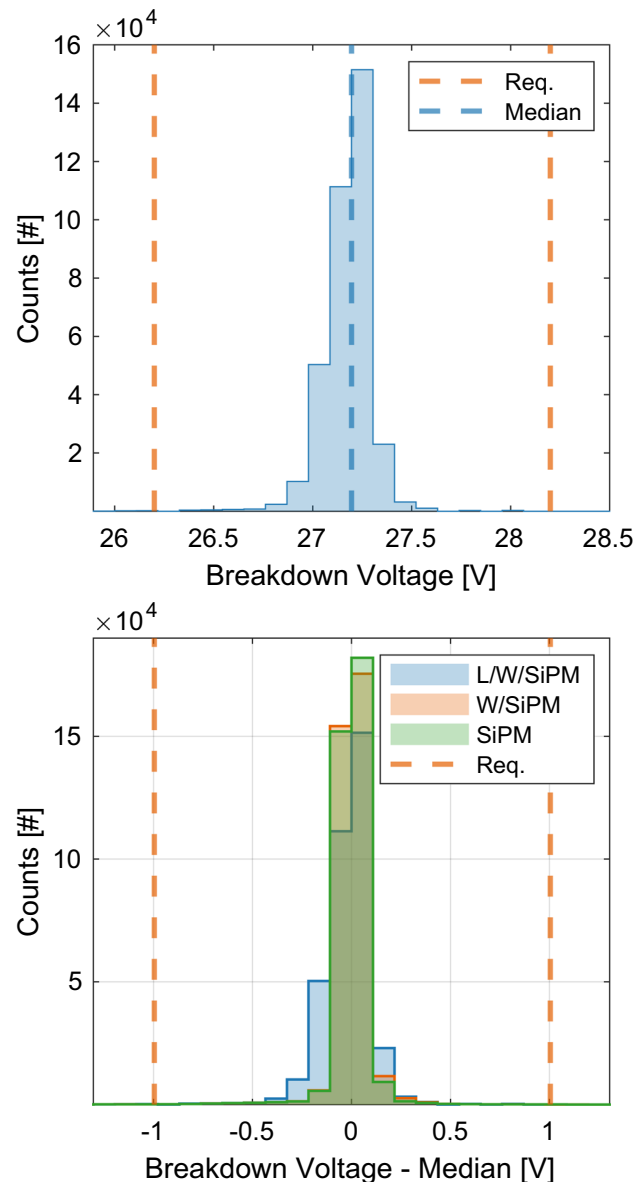


Fig. 11 (Top) breakdown voltage distribution of all the 359040 tested SiPMs. The red dashed lines represent the DS-20k requirements ($27.2 \pm 1.0 \text{ V}$), while the blue line the histogram median. 2698 SiPMs are outside the range of the plot. (Bottom) breakdown voltage variability within single wafers (SiPM), mixing wafers in the same Lot (W/SiPM) and mixing Lots (L/W/SiPM). W and L stand for Wafer and Lot. See text for more details

4.2 Quenching resistor distribution

The SiPM quenching resistor is calculated from the linear part of each forward biased IV curve (Fig. 8) in the regime where the resistance of the SPAD's pn-junction is negligible ($> 1.25 \text{ V}$) [32]. The inverse of the IV curve slope, after correcting for the voltage drop of the measurement system (Sect. 2), is the parallel resistance of all the SiPM SPADs' quenching resistors. A narrow distribution of this parameter

Fig. 12 Box plot of the measured breakdown voltage for the tested Lots (56 production Lots, 2 engineering Lots). The orange line inside each box represents the sample median, while the top and bottom edges are the upper and lower quartiles. Dots represent outliers more than 1.5 interquartile range (IQR) away from the top or bottom of each box. The dashed lines represent the DS-20k requirements (27.2 ± 1.0 V)

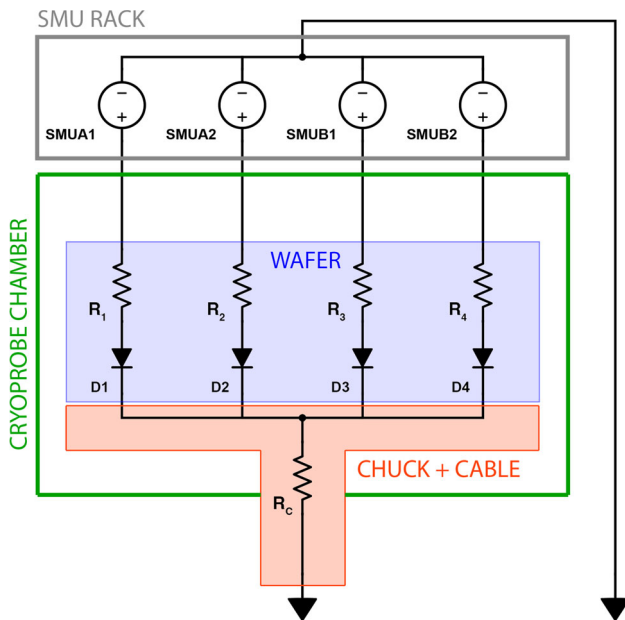
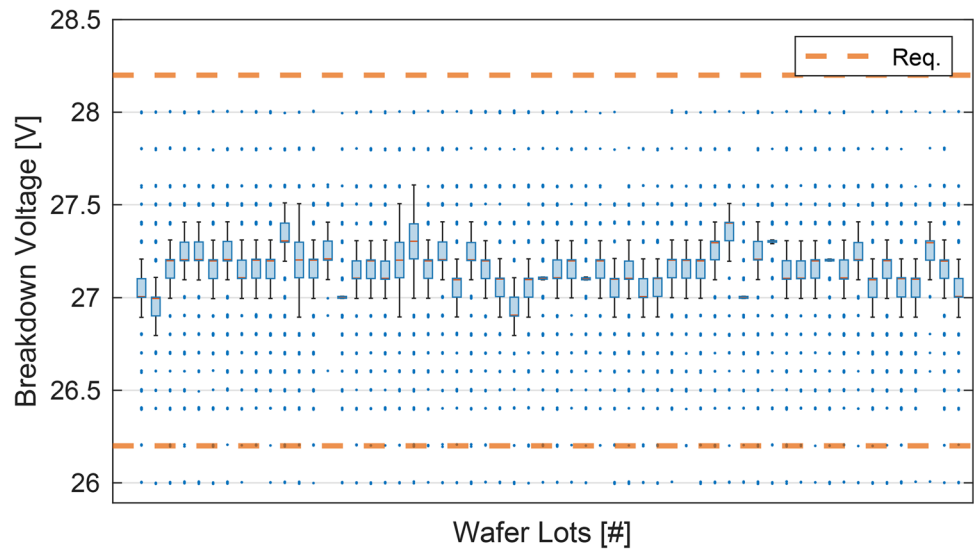


Fig. 13 Schematic of the measurement system for forward bias IV curves. R_c is the series resistance of the cryoprobe+SMUs measurement system, measured to be 3.7Ω . R_i with $i = 1, 2, 3, 4$ are the resistance of the 4 SiPMs measured in parallel

is desirable when grouping SiPMs in tiles since a mismatch in the SiPM quenching resistor would produce a pulse-to-pulse variability of the SiPM pulse shape, depending on the triggered SiPM. If R_c is the series resistance of the measurement system ($R_c = 3.7 \Omega$, Sect. 3), the SiPM SPAD quenching resistor (R_q) can be derived as follows

$$R_q = [R^* - 4R_c] \times N_{\text{cell}} \quad (2)$$

where R^* is the resistance measured using a linear fit to the forward bias IV-curve and $N_{\text{cell}} = 94904$ is the number of SPAD cells in each SiPM. The factor 4 in Eq. 2 accounts for

the fact that SiPMs are measured in parallel groups of 4, as introduced in Sect. 2 and also shown in Fig. 13.

Figure 14 (top) shows the quenching resistor distribution for all 359040 SiPMs tested, while Fig. 15 shows the same information grouping SiPMs for their production Lot. At 77 K, the average quenching resistor is measured to be $\bar{R}_q = 3.34 \pm 0.15 \text{ M}\Omega$. The dashed lines represent the DS-20k requirements ($3.35 \pm 1.50 \text{ M}\Omega$). Table 2 reports the quenching resistor VCA analysis. The production variance ($\sigma_{R_q}^2$) after removing out-of-spec devices is equal to $0.073 (\text{M}\Omega^2)$.

Figure 14 (bottom) shows a visual representation of this analysis, similarly to what was done in Sect. 4.1 for the SiPM breakdown voltage. The variability of the quenching resistor drops drastically when the contribution of the Lot is removed. Specifically, moving from L/W/SiPM to W/SiPM, the variance decreases by $0.045 (\text{M}\Omega)^2$, or 61.8% of the total variance, according to Table 2. Additionally, when the Wafer-to-Wafer variability is removed, i.e., comparing W/SiPM with SiPM, the variance is reduced by $0.009 (\text{M}\Omega)^2$ which is a smaller amount compared to the previous case and corresponding to 11.9% of the total variance. The residual variance (SiPM) is 26.3% of the total.

4.3 Spatial distribution of the breakdown voltage and quenching resistor

In the previous sections, we presented the variability in breakdown voltage and quenching resistance using histograms and VCA analyses. Figure 16 shows the typical spatial distribution of these two parameters on a representative production wafer. The results indicate that both parameters are generally uniform across the wafer, with only a few dice falling outside of specifications. Note that this wafer was selected solely for illustrative purposes; the extremely narrow distributions

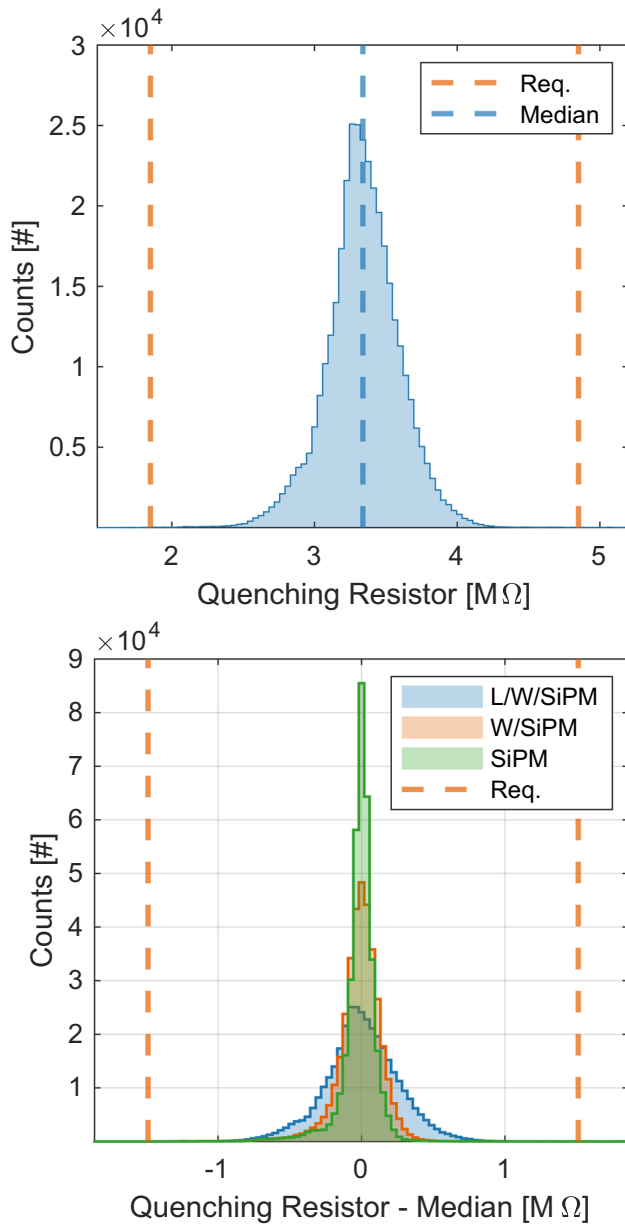


Fig. 14 (Top) quenching resistor distribution of all the 359040 tested SiPMs. The red dashed lines represent the DS-20k requirements (3.35 ± 1.50 MΩ), while the blue line the histogram median. 2517 SiPMs are outside the range of this plot. (Bottom) quenching resistor variability within single wafers (SiPM), mixing wafers in the same Lot (W/SiPM) and mixing Lots (L/W/SiPM). W and L stand for Wafer and Lot. See text for more details

of breakdown voltage and quenching resistance within individual wafers were quantitatively confirmed in the previous sections.

Based on this statistical analysis, the current strategy at the tile assembly stage is to freely combine dice from the same wafer and, when necessary, include dice from wafers within the same Lot. Given the consistent performance of SiPMs across a Lot, it is reasonable to treat the Lot as the

fundamental grouping element for tile assembly rather than the individual wafer.

4.4 Correlated and uncorrelated noise

Dark and correlated avalanche noise are critical SiPM parameters that affect the overall DS-20k detector performance by increasing the number and the fluctuations of detected photons. Fluctuations in the number of detected photo-electrons, for example, may decrease the energy resolution of the detector, as shown in Ref. [33].

Dark noise is a spontaneous charge signal generated by an electron-hole pair formed by thermal or field-enhanced processes [34]. Correlated Avalanche (CA) noise is due to at least two processes: the production of secondary photons in the gain amplification stage during primary avalanches and the trapping and subsequent release of charge carriers produced in avalanches (afterpulsing). Several techniques are used to characterize these two sources of noise while operating the SiPM in pulse counting mode [6, 30, 35]. However, estimating these properties directly from the wafer-level reverse bias IV curves is challenging.

In Sect. 4.4.1, we introduce a new technique that, starting from the shape of the reverse bias IV curve and, regardless of the level of SiPM illumination, ensures that all the production-graded SiPMs: (i) have similar CA noise and (ii) don't present an out-of-spec voltage dependence (e.g. high DCR). The leakage current before the breakdown voltage is also used as a control parameter to identify out-of-spec SiPMs (e.g. shorts). More details are reported in Sect. 4.4.2.

4.4.1 Goodness of fit

To reach the DS-20k design performance, all production-graded SiPMs must have similar correlated noise. The reverse bias SiPM IV curve is sensitive to this quantity. In general, the SiPM current under illumination can be written as [33]

$$I(V, \lambda) = f(V) \times \left[\text{PDE}_\lambda(V) \times \Phi(\lambda) + R_{\text{SiPM}}^{\text{DCR}}(V) \right] \quad (3)$$

where V is the SiPM reverse bias voltage, PDE_λ is the SiPM Photon Detection Efficiency (PDE), and $\Phi(\lambda)$ is the photon flux. $R_{\text{SiPM}}^{\text{DCR}}(V)$ is the SiPM DCR. $f(V)$ is a correction factor that can be written as

$$f(V) \sim q_e \times (1 + \overline{\Lambda}) \times \overline{G}_{1 \text{ PE}}, \quad (4)$$

where $(\overline{G}_{1 \text{ PE}})$ is the SiPM gain for 1 Photo-electron equivalent (PE) charge, $(\overline{\Lambda})$ is the CA noise contribution that arti-

Fig. 15 Box plot of the measured quenching resistor for the tested Lots (56 production Lots, 2 engineering Lots). The line inside each box represents the sample median while the top and bottom edges are the upper and lower quartiles. Dots represent outliers more than 1.5 interquartile range (IQR) away from the top or bottom of each box. The dashed lines represent the DS-20k requirement ($3.35 \pm 1.50 \text{ M}\Omega$)

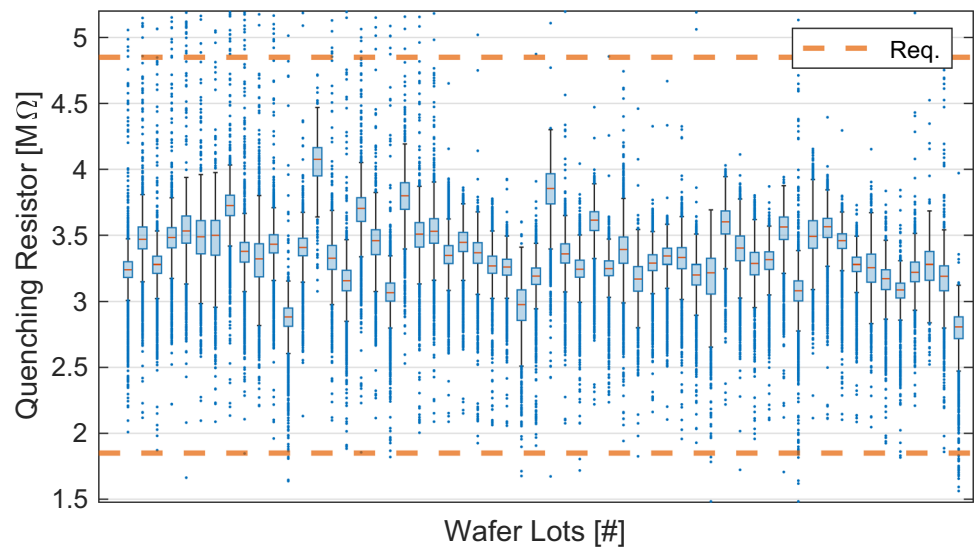


Table 2 Variance component analysis (VCA) of the quenching resistor (R_q) distribution. VC is the variance component in $(\text{M}\Omega)^2$; % of Tot. is the percentage of each variance component; Cum. VC is the cumulative

variance considering the incremental contribution of each component; Cum. Fact. represents the incremental nested factors contributing to the cumulative variance (W and L stand for Wafer and Lot)

Factor	Samples	VC	% of Tot.	Cum. VC	Cum. Fact.
SiPM	359040	0.019	26.3	0.019	SiPM
Wafer	1360	0.009	11.9	0.028	W/SiPM
Lot	58	0.045	61.8	0.073	L/W/SiPM
Total		0.073	100		

cially increases the total current produced by the SiPM and (q_e) is the electron charge [33].⁶

$f(V)$ is a function of the applied bias voltage V but can be considered wavelength-independent because it depends only on the SiPM intrinsic characteristics. This is because the average sensor gain ($\bar{G}_{1 \text{ PE}}$) depends on the SiPM SPAD capacitance while afterpulses and optical crosstalk that contribute to the sensor CAs depend on impurities and cell geometry.

At 77 K, the DCR of these SiPMs is on the order of mHz/mm^2 and makes a negligible contribution to the total current [15]. If we assume that all the SiPMs have identical characteristics e.g. efficiency and correlated noise, and their DCR is negligible compared to the incident photon flux Φ , the ratio point-to-point (i.e. at the same bias voltage) of two SiPMs' IV curves as a function of the applied bias voltage V is a voltage-independent quantity, only proportional to the ratio of the photon fluxes seen by the SiPMs, here called k , as follows

$$\frac{I_1(V, \lambda)}{I_2(V, \lambda)} = \frac{\Phi_1(\lambda)}{\Phi_2(\lambda)} \equiv k. \quad (5)$$

In order to ensure compliance of the wafer level IV curves with Eq. 5, we introduce a parameter called goodness of fit

⁶ The SiPM gain ($\bar{G}_{1 \text{ PE}}$) and the CA noise contribution ($\bar{\Lambda}$) are voltage dependence as shown, for example, in Ref. [30,33]

defined as follows

$$\text{GOF} = \sum_i \frac{(I_i - k\bar{I}_i)^2}{\sigma_i^2(N-1)}, \quad (6)$$

where N is the number of measured points, I_i is the IV curve of any SiPMs in the wafer, and $\bar{I}_i$ is current of a SiPM chosen as to be the reference for the entire DS-20k production, and whose IV curve is named reference-IV. σ_i is instead the uncertainty of the reference IV curve. It is set to be equal to 22% and it was computed accounting for the average point-to-point fluctuation. The sum in Eq. 6 is done over the bias voltage points in the IV curve, starting 0.7 V away from the breakdown voltage of the reference IV-curve ($\bar{I}$) after alignment of the breakdown voltage of the curve I with the one of $\bar{I}$. This was done to avoid the steep IV curve rise, close to the breakdown voltage, where large fluctuations due to baseline noise are present and would affect the GOF computation.

The scaling factor k (Eq. 5) can be calculated analytically by minimizing Eq. 6 as follows

$$k = \frac{\sum_i (\bar{I}_i I_i) / \sigma_i^2}{\sum_i \bar{I}_i^2 / \sigma_i^2}. \quad (7)$$

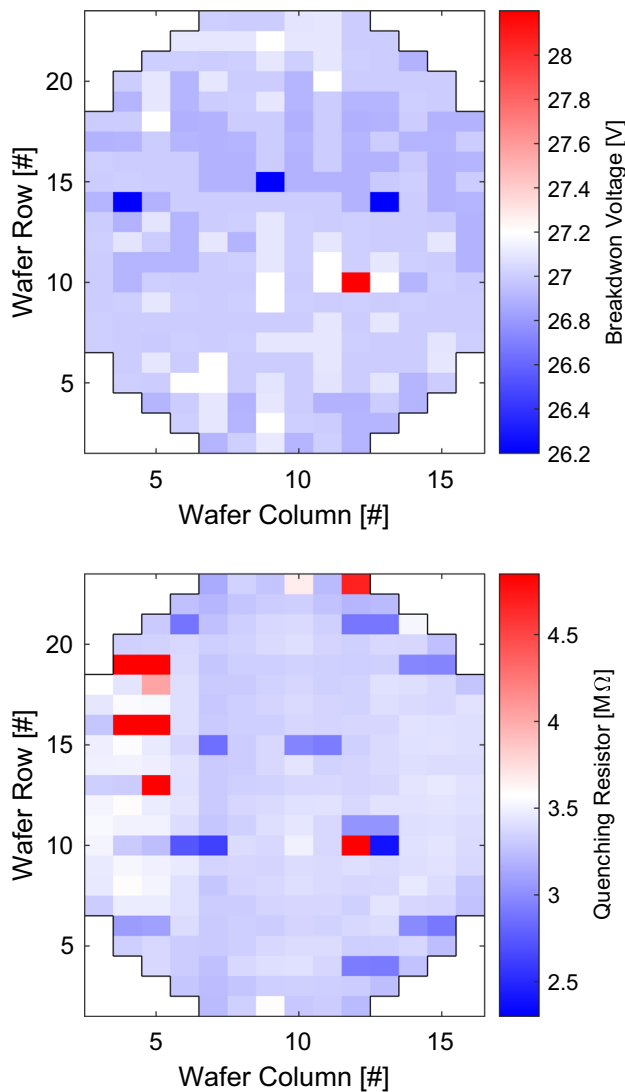


Fig. 16 Spatial distribution of the breakdown voltage (top) and quenching resistor (bottom) for Wafer 19 of Lot 9306869. This wafer is the same whose IV curves are shown in Fig. 8. To keep the scale readable, we associated to the few dice whose breakdown voltage and quenching resistor is outside the range of the figure a value equal to the closest axis range boundary

Figure 17 shows a histogram of the GOF parameter for all the 359040 tested SiPMs.

The average GOF is 1.36 ± 1.49 meaning all SiPMs IV curves are in good agreement with the reference IV curve when scaled with a constant scaling factor. For instance the top panel of Fig. 18 displays the IV curves from the wafers shown in Fig. 8, categorized by their GOF parameter. In contrast, the bottom panel of Fig. 18 presents the same IV curves after scaling using the k -factor calculated from Eq. 7. This scaling compensates for fluctuations due to varying light fluxes beyond the breakdown voltage, resulting in most of the SiPM IV curves matching the reference one within its error margins.

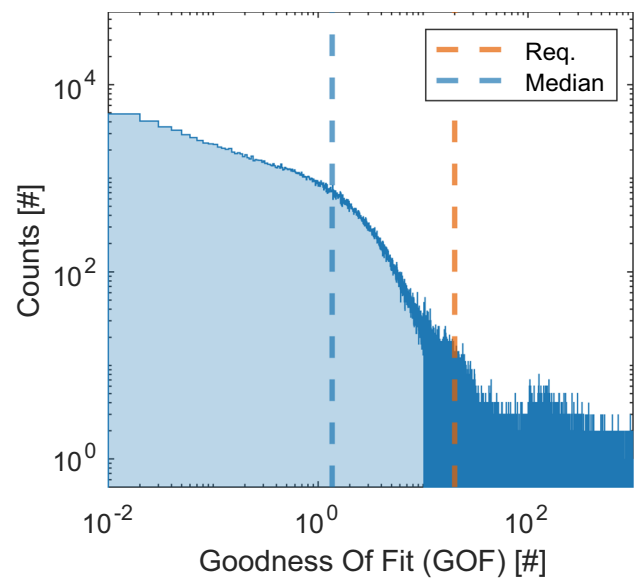


Fig. 17 Goodness of fit (GOF) distribution of all the 359040 SiPMs tested. The dashed line represents the DS-20k requirements ($\text{GOF} \leq 20$), while the blue line the histogram median. 9261 SiPMs are outside the range of the plot

While IV curves with a $\text{GOF} > 20$ deviate noticeably from the reference, there is minimal practical difference among curves with a $\text{GOF} \leq 20$, which is the requirement set for DS-20k production (as illustrated in Fig. 17). The upper limit for the GOF parameter ($\text{GOF} \leq 20$) was established at the 3σ level, meaning that 99.87% of the data satisfy the specification in a one-tailed test; indeed, a theoretical χ^2 distribution with 5 degrees of freedom contains 99.87% of its data below 20.

4.4.2 SiPM leakage current

The cryoprobe vacuum chamber is not light-tight (Sect. 3), which means the SiPM current above the breakdown voltage can not be used as a measurement of the SiPM DCR. However, the current below breakdown (not multiplied contribution) can be used to identify out-of-spec SiPMs.

Below the breakdown voltage, at 77 K, the SiPM current is proportional to the SiPM photon flux. In the absence of gain (Geiger mode multiplication $M=1$) or under the presence of a proportional gain ($M \ll G_{1\text{ PE}}$) the small SPAD capacitance results in a very small current, on the order of a few fA or less, even under kHz of external illumination. This is below the sensitivity of the measurement system.

Figure 19 shows a histogram of the leakage current measured at 20 V, several volts below the average breakdown voltage (Sect. 4.1).

At 77 K, the average leakage current is measured to be $\bar{I}_L = 6.6 \pm 2.2$ pA, which represents the measurement system noise floor (Sect. 2). The vertical line represents the DS-

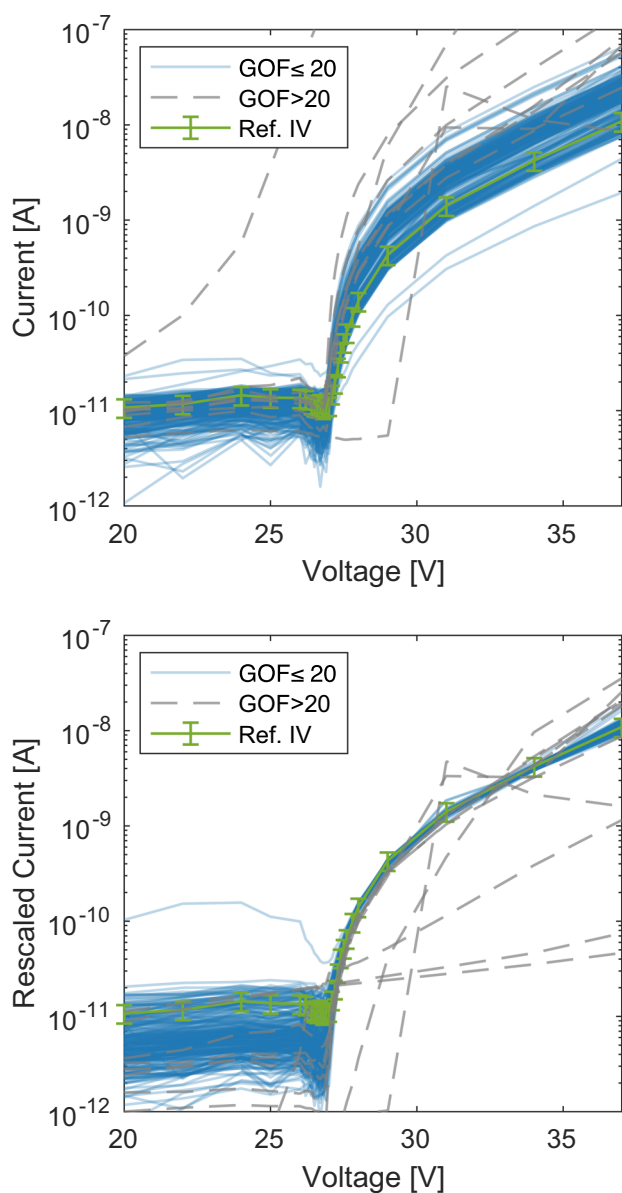


Fig. 18 Reverse bias IV curves for the production Wafer 19 of Lot 9306869 categorized according to their goodness of fit (GOF) parameter (Top). The bottom figures shows the same IVs, always categorized according to their GOF and scaled for the corresponding k -factor, computed as per Eq. 7

20k requirement ($I_L \leq 40$ pA). The upper spec limit for this parameter value was set at the 4σ level: i.e. 99.99% of the data meet the specs.

5 Correlation of the 300 K and 77 K breakdown voltage and quenching resistor data

In Sect. 3, we described the NOA wafer testing workflow, which achieves a throughput of approximately 0.35 wafers

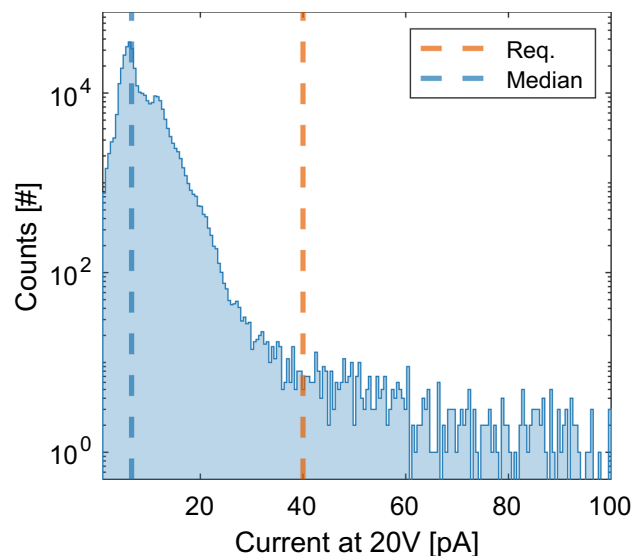


Fig. 19 Leakage Current distribution at 20 V of all the 359040 tested SiPMs. The dashed line represents the DS-20k requirements ($I_L \leq 40$ pA), while the blue line the histogram median. 2403 SiPMs are outside the range of the plot

per hour. The entire wafer testing campaign for DS-20k-now nearly complete-took roughly a year and a half.

Next-generation noble liquid cryogenic experiments, such as Argo and Darwin, plan to have SiPM-based photon-sensitive areas in excess of 100 m^2 [36,37]. Cryogenic wafer-level SiPM QA/QC at this scale will be challenging and will likely require several cryoprobe systems.

In this section, we study the correlation of the dice failure rate at 300 K and 77 K, to understand if room-temperature testing is adequate. Room temperature measurements could likely be performed by the wafer supplier or using measurement systems that are more affordable than the cryogenic prober used for this work.

Figure 20 shows the correlation between the SiPMs breakdown voltage (top) and the quenching resistor (bottom) measured by LFoundry at 300 K and by the cryoprobe system at 77 K. The cryoprobe (Sect. 2) in its actual configuration cannot in fact perform measurements at 300 K due to the mechanical tolerances of the probe card.⁷ Each point in the figure represents a SiPM.

For each production wafer, LFoundry tested the breakdown voltage of 10% of the SiPM dice using a technique similar to the one presented in Sect. 4.1. The quenching resistor was instead inferred by the measurement of the sheet resistance on nine test structures distributed over the wafer, using the Van Der Pauw method, placed on the wafer dicing street.⁸

⁷ The probe card is designed to operate at 77 K. At room temperature, the probe card expands and its needles do not contact the SiPM pads.

⁸ The LFoundry measurements were performed before the deposition of the gold back-metallization (Fig. 3). The large backside resistance at

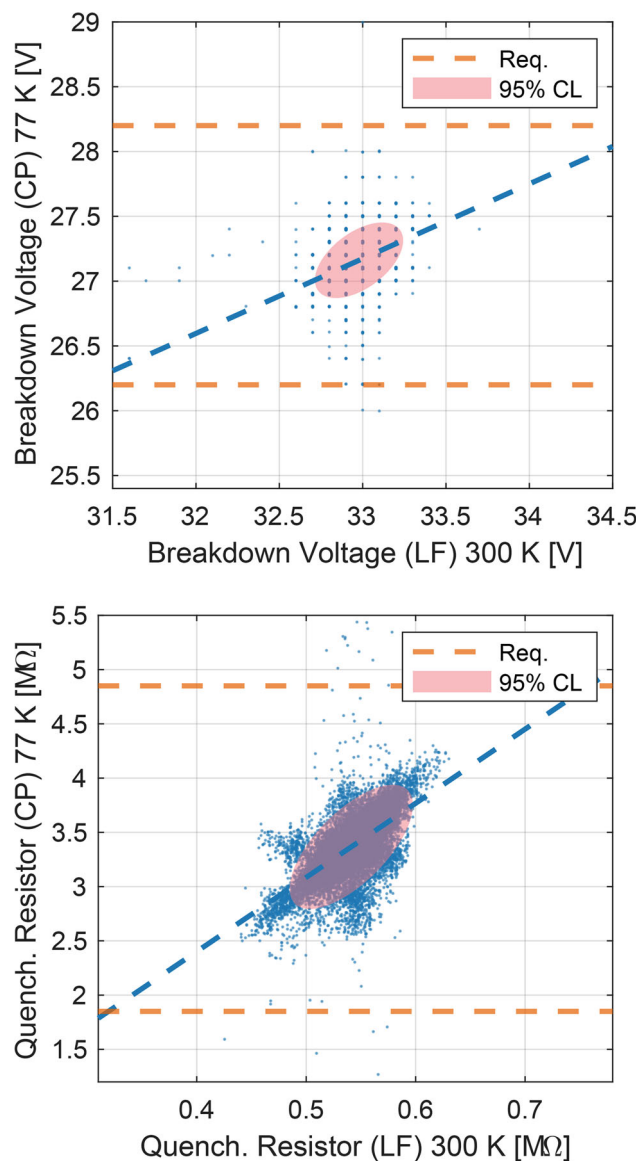


Fig. 20 Correlation of the breakdown voltage (top) and the quenching resistor (bottom) data measured by LFoundry (LF) at 300 K and by the cryoprobe (CP) at 77 K. Each point represents a SiPM. Horizontal orange lines are the SiPMs requirement at 77 K. Horizontal orange lines are the SiPMs requirement at 77 K, while the dashed blue lines are fit to the data. The red circle represents the 95 % confidence level (CL) interval

Overall 44198 and 111316 dice were tested by LFoundry for V_{bd} and R_q , respectively. The horizontal orange lines in Fig. 20 represent the 77 K dice requirements (Sect. 3) and the dashed blue lines are fit to the data. In the same figures, we also reported the 95 % confidence level (CL) interval. Table 3 reports the intersection between the 77 K requirements and

this step of the manufacturing process prevents the usage of the forward bias IV curve, as was shown in Sect. 4.2. The two techniques yield comparable results, as shown in Ref. [38].

Table 3 Breakdown voltage and quenching resistor requirements at 77 K and the extrapolated requirements at 300 K

Quantity	77 [K]	300 [K]
V_{bd} [V]	27.2 ± 1.0	33.1 ± 1.7
R_q [MΩ]	3.35 ± 1.50	0.54 ± 0.22

the data fit line that shows a correlation between the 300 K and the 77 K dataset.

Other than being correlated, the two data sets have similar distributions. This can be seen by comparing the Z-Scored data of the two quantities at both temperatures using QQ-Plots [39], as shown in Fig. 21.

Given a variable $X = V_{bd}, R_q$, the corresponding Z-scored quantity is defined as

$$Z = \frac{X - \bar{X}}{\sigma_X} \quad (8)$$

where $\bar{X}$ and σ_X are the mean and sigma of the corresponding distribution.

Both curves (300 K and 77 K) produce approximately a straight line and almost perfectly overlap, apart from the very edges, confirming they follow the same probability distribution.

The results presented in this section show that based on the measured data more than 99% of the dice that comply at room temperature are also compliant at cryogenic temperature. The low statistics of failing dice however do not allow us to conclude that the room temperature screening is sufficient to identify failing dice at cryogenic temperature. This is a consequence of the high wafer yield and low statistics of failing dice of the LFoundry production. New measurements, with a newly designed probe card that can operate at 300 K, are now being planned to further expand the results presented in this section. These also include the possibility of building a correlation not only based on the SiPMs breakdown voltage and quenching resistor, but also based on the GOF and leakage current parameters that could not be tested using the data presented in this work since LFoundry only performed measurements close to the dice breakdown voltage.

6 Wafer production yield

Figure 22 shows a histogram of the wafer yield for all tested wafers.

The yield has been computed based on the 264 testable dice per wafer. The dashed orange line represents the assumed production yield (80%), computed from pre-production wafers from FBK (Fig. 23).

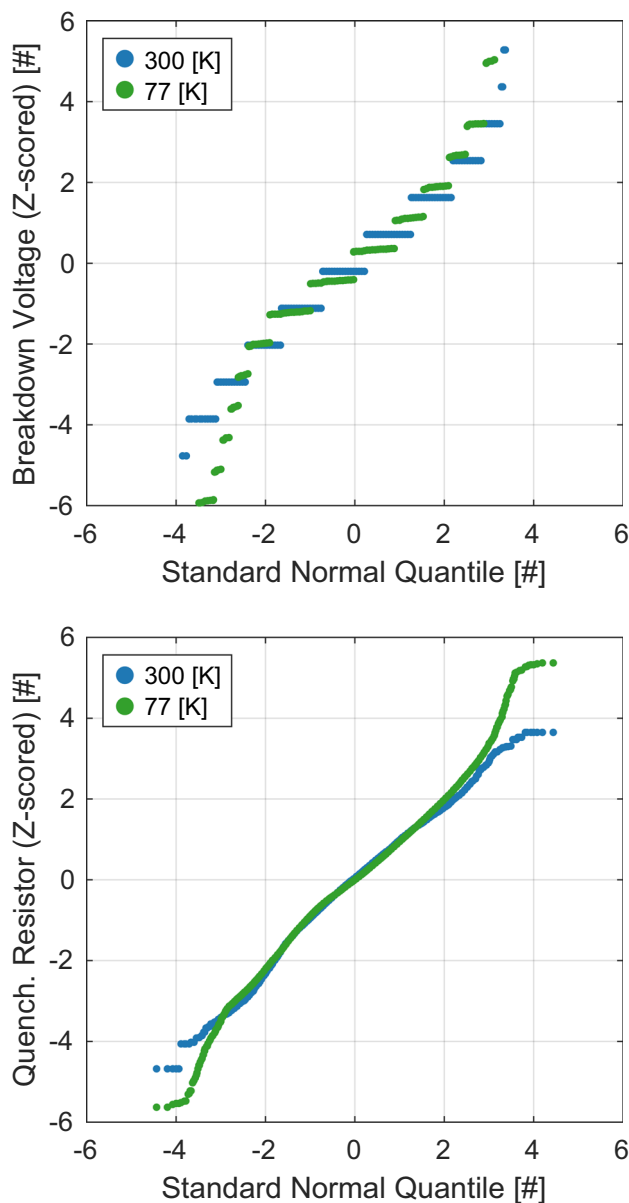


Fig. 21 QQ-Plots of the Z scored breakdown voltage (top) and quenching resistor (bottom) distributions for the 300 K and 77 K data. Both curves (300 K and 77 K) produce approximately a straight line and almost perfectly overlap, apart from the edges, confirming that the two datasets follow the same probability distribution

The tested wafers not only meet but significantly exceed this requirement, with an overall yield of $93.2 \pm 2.5\%$. The Lot-to-Lot yield variation is also mostly negligible, apart for few Lots, as shown in Fig. 24.

This represents a significant improvement if compared with the pre-production results. Indeed, high-volume CMOS foundries typically operate numerous parallelized pieces of equipment in a fully automated manner, which helps reduce non-uniformities and boost yield.

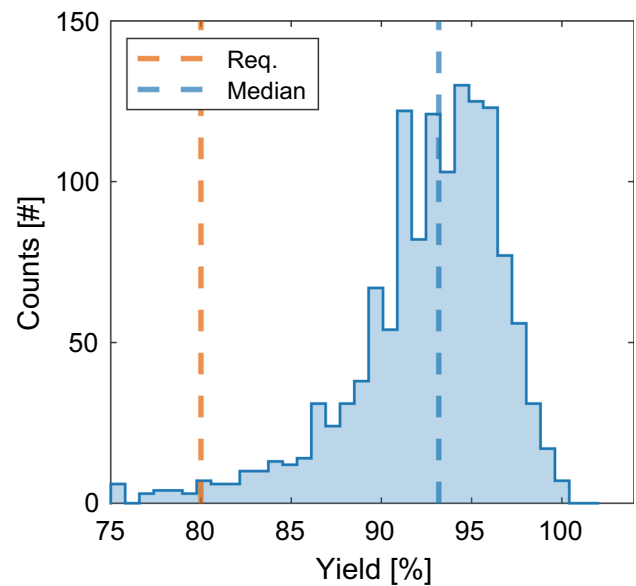


Fig. 22 Histogram of the wafer production yield after applying the screening presented in this work. The two dashed lines represent the histogram median (blue) and the expected production yield (red, 80%), which is based on the yields of pre-production from FBK

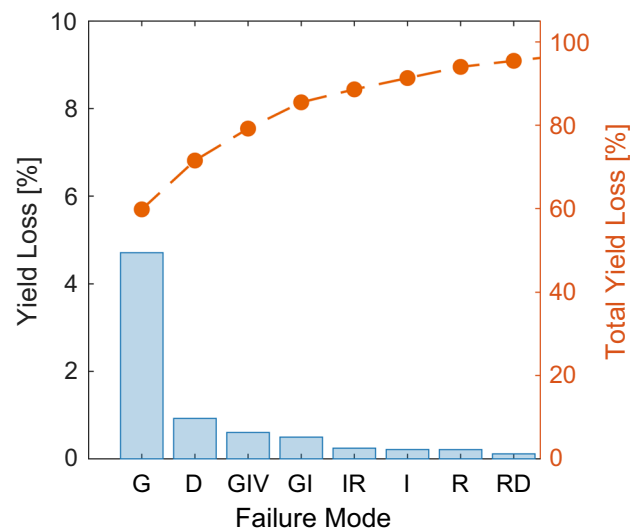


Fig. 23 Pareto plot that shows the source of the wafer yield loss differentiating SiPMs according to their failure loss mechanism: (i) Goodness of fit (G), (ii) leakage current below breakdown (I), (iii) defective pads (D), (iv) quenching resistor (R), (v) breakdown voltage (V) and their combination. To keep the figure readable only the largest source of yield loss are considered, since they overall constitute 95% of screened SiPMs

Figure 23 shows with a Pareto plot the sources of yield loss differentiating SiPMs according to their failure mechanism obtained by singularly applying the previously introduced requirement or by combining them. The largest source of yield loss is the Goodness of fit (G) cut, responsible for screening roughly 5% of the tested SiPMs. The subsequent

Fig. 24 Box plot of the yield for the tested Lots (56 production Lots, 2 engineering Lots). The line inside each box represents the sample median while the top and bottom edges are the upper and lower quartiles. Dots represents wafers in each Lot. The dashed lines represent the DS-20k requirement

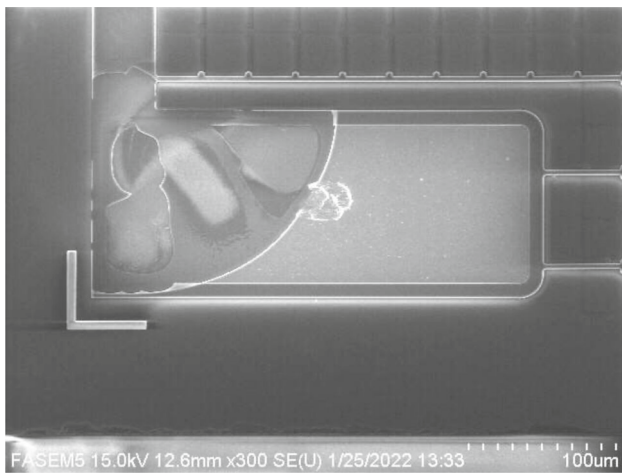
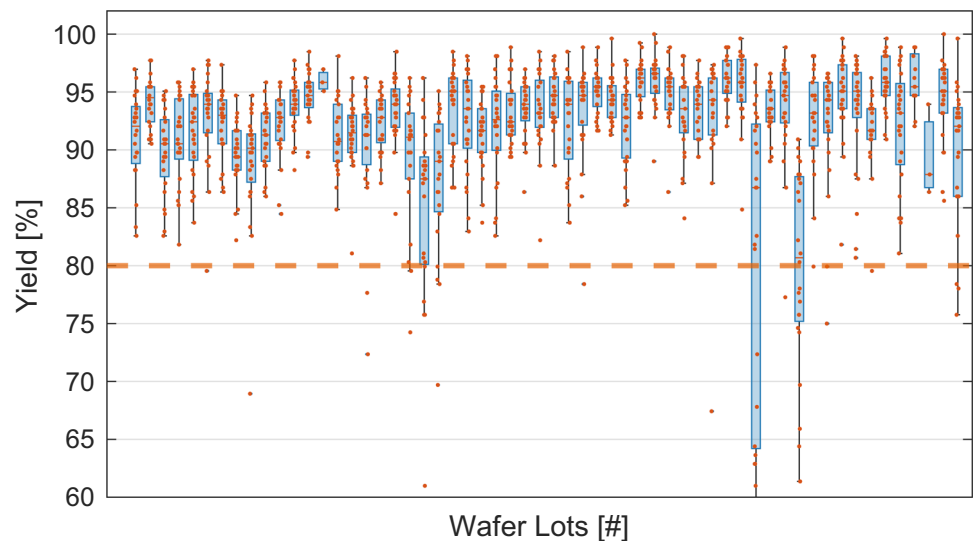


Fig. 25 Scanning electron microscope (SEM) image made by LFoundry of one SiPM pad that was marked as defective. The aluminum pad was etched in an uncontrolled way showing the layers at the bottom of the pad

source of yield loss not yet presented in the previous section of this work, is labeled D in Fig. 23 and it is due to dice classified as out-of-spec at LFoundry's outgoing optical inspection because they have one or more aluminum pads etched in an uncontrolled way during processing. An example of a defective failure is shown in Fig. 25.

Note that these dice do not necessarily fail the characterization tests reported in previous sections of this work. Still, they may be problematic for other steps in the photosensor process flow (e.g. wire bonding). Rather than risk failures of entire tiles due to unforeseen issues with this defect, these dice are discarded, contributing a yield loss on the order of 1% in the overall wafer production.

Figure 23 also shows other sources of yield losses ordered by their progressively lower efficiency in screening SiPMs. Note that the SiPMs discarded only due to their breakdown voltage or quenching resistor represent a negligible fraction.

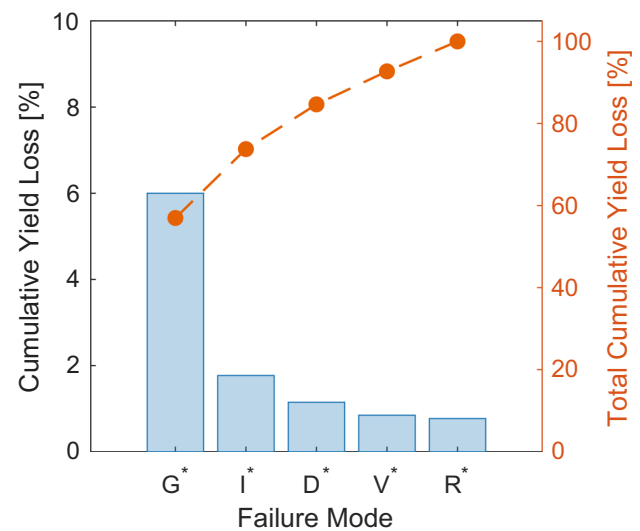


Fig. 26 Pareto plot that shows the cumulative source of the wafer yield loss. Each failure mechanism is treated as an independent quantity. The following yield loss mechanisms have been considered: (i) goodness of fit (G^*), (ii) leakage current below breakdown (I^*), (iii) defective pads (D^*), (iv) quenching resistor (R^*), and (v) breakdown voltage (V^*)

Figure 26 shows again with a Pareto plot the same data of Fig. 23, but each of the failure mechanisms is treated as an independent quantity showing for each of the selection criteria the cumulative yield loss due to each requirement i.e. SiPMs can fail for one or more requirements at the same time.

7 Wafer campaign control plans

The DS-20k wafer testing campaign follows rigorous handling, storage and testing procedures. Wafer Lots are stored for their entire life in the NOA ISO-6 clean room (Sect. 1)

sealed under vacuum anti-static bags. Storage parameters, such as humidity (HM), temperature (T), and radon contamination (RC), are monitored to ensure compliance with the DS-20k exposure specification ($HM < 50\%$, $T < 25^\circ\text{C}$, $RC < 50\text{ Bq/m}^3$).

During wafer handling, only certified tools, such as SPS vacuum pencils, are used to touch the gold back surface of the wafers (Fig. 3), while the wafer front surface is touched only with specifically designed tools e.g. the frame mounter for dicing operation (Fig. 2). The results of the wafer testing campaign are constantly monitored by using statistical process control (SPC) Charts to detect trends or correlations with equipment parts (e.g. probe card needles degradation) and therefore to ensure the reliability of the cryo-probing operation over time. Moreover, process capability indices are used to measure the ability of the cryoprobe process to produce SiPMs within the specification limits.

More generally we monitor, on a weekly basis, three process capability (Cp) indexes linked to the specifications presented in the previous sections of this work: CpL, CpU and Cpk. CpL(U) is a measurement of the cryoprobeing process based on its lower (upper) specification limit LSL(USL). CpL and CpU are defined in Eqs. 9 and 10 as the ratio of two values: (i) the distance between the mean of the measured quantity X and the lower (upper) specification limit LSL (USL), and (ii) the standard deviation of the process ($3\sigma_X$ variation)

$$\text{CpL} = \frac{\bar{X} - \text{LSL}}{3\sigma_X}, \quad (9)$$

$$\text{CpU} = \frac{\text{USL} - \bar{X}}{3\sigma_X}. \quad (10)$$

When upper and lower specifications are both needed to determine the process compliance, as is the case for breakdown voltage and quenching resistor specifications (Sect. 3), the CpL(U) index is substituted by the Cpk, which is defined as the ratio between: (i) the difference between the mean of the measured quantity X and the closest specification limit (USL or LSL), and (ii) the standard deviation of the process ($3\sigma_X$ variation):

$$\text{Cpk} = \min \left[\frac{\text{USL} - \bar{X}}{3\sigma_X}, \frac{\bar{X} - \text{LSL}}{3\sigma_X} \right]. \quad (11)$$

Figures 27 and 28 display the weekly Cpk values for the SiPM breakdown voltage and quenching resistor. The horizontal line at 1.33 represents the industry standard requirement [40], which defines a $4\sigma_X$ difference between the mean of the measured quantity and its upper specification limit.⁹

The figures also show the number of wafers tested each week. This number varies due to periodic maintenance of the cryoprobeing system, which temporarily reduces weekly throughput. It is important to note that the early weeks of operation exhibited artificial variability because only about 20% of the 25 wafers in each Lot were tested before moving on to the next Lot. This strategy was employed to efficiently sample the entire LFoundry wafer production and to assess the expected dominant Lot-to-Lot variability (Sect. 3). Figures 15 and 28 further reveal a correlation with the lot-to-lot variation in the quenching resistor. Additionally, Figs. 27 and 28 occasionally show exceptionally high Cpk values (greater than 5), which are linked to the testing procedure—for instance, during weeks when only a single wafer was tested (such as week 6 or 21). In contrast, single wafers or single Lots tend to exhibit much tighter distributions for breakdown voltage and quenching resistor, as demonstrated in Sects. 4.1 and 4.2. Overall, the process capability indices indicate a stable testing campaign, underscoring the ability of the cryoprobeing process to consistently produce SiPMs within the specified limits.

8 Conclusions

This paper describes measurements performed in support of the DarkSide-20k experiment to characterize the properties of 1400 wafers of FBK NUV-HD-cryo (near-UV sensitive, high-density, cryogenic compatible) SiPMs produced by LFoundry. These wafers will be used to instrument the two 10.5 m^2 DS-20k TPC optical planes and the inner and outer veto detectors. This work focused on the quality control and quality assurance of 1360 wafers (1314 production, 46 engineering), representing 94% of the overall production. The data presented here encompass 56 of the 57 production lots, and include two engineering lots used for preproduction assembly, thereby capturing the Lot-to-Lot variation—the primary source of production variability. We measure an average breakdown voltage at 77 K of $\bar{V}_{\text{bd}} = 27.19 \pm 0.05\text{ V}$, where the central value represents the distribution median and the error half of its interquartile range, that is comfortably within the DS-20k specification ($27.2 \pm 1\text{ V}$). We measure an average quenching resistor value, leakage current below breakdown, and Goodness of Fit (GOF) parameter, all at 77 K, of $\bar{R}_q = 3.34 \pm 0.15\text{ M}\Omega$, $\bar{I}_L = 6.6 \pm 2.2\text{ pA}$, and $\overline{\text{GOF}} = 1.36 \pm 1.49$. These values are consistent with the DS-20k specifications ($I_L \leq 40\text{ pA}$, $R_q = 3.35 \pm 1.50\text{ M}\Omega$, $\text{GOF} \leq 20$). In this work, we also show a correlation between the breakdown voltages and the quenching resistor values at room temperature and 77 K. More than 99% of the dice that are within

(defined as points more than 1.5 IQR above the upper quartile), as detailed in Sect. 4.1.

⁹ Note that the Cpk is computed using the weekly median and standard deviation, with the standard deviation calculated after excluding outliers

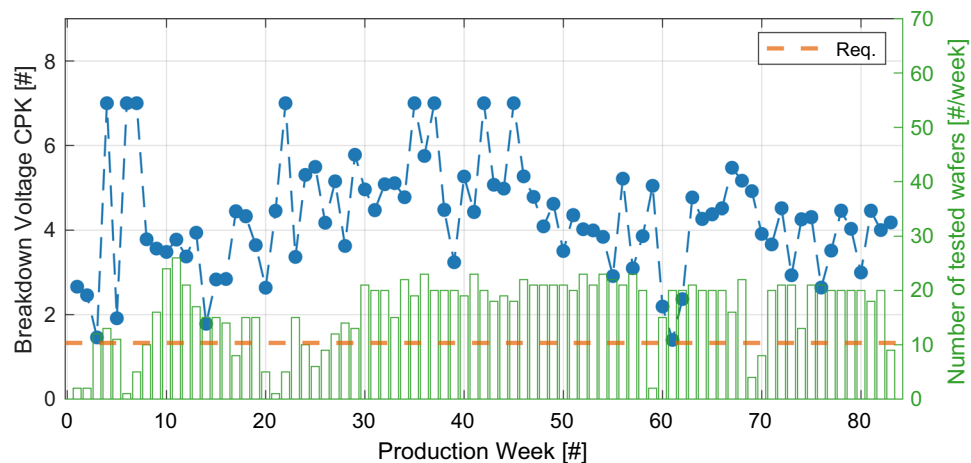


Fig. 27 Weekly based Cpk of the SiPM breakdown voltage (blue dots). The dashed orange line represents the industry standard of 1.33. The green bars are the number of wafers tested in each production week

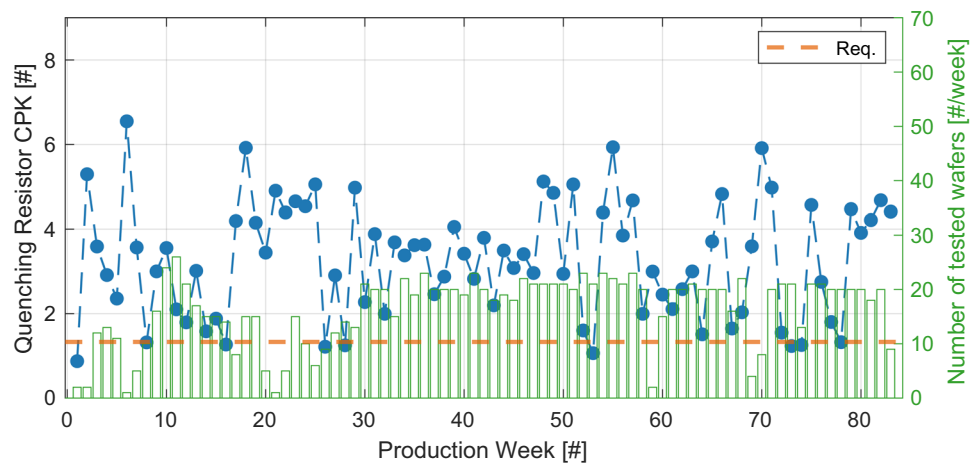


Fig. 28 Weekly Cpk of the SiPM quenching resistor (blue dots). The dashed orange line represents the industry standard of 1.33. The green bars are the number of wafers tested in each production week

specification at room temperature are also compliant at cryogenic temperature. The low statistics of failing dice however do not allow us to conclude that the room temperature screening is sufficient to identify failing dice at cryogenic temperature. This is a consequence of the high wafer yield and low statistics of failing dice of the LFoundry production. Finally, we presented process capability indices that monitor the stability of the cryoprobng operation over time for all the tested wafer-level parameters. The average production wafer yield is $93.2 \pm 2.5\%$, which exceeds the 80% specification defined in the DarkSide-20k production plan. The wafer testing campaign is nearly complete, with fewer than 10% of the wafers remaining to be tested. Following wafer-level testing, tile assembly and PDU assembly are progressing at NOA and in the UK, respectively. A dedicated QA/QC and characterization program is now in place, with the final step being a comprehensive cryogenic test of fully assembled units. These tests are being carried out at various collabora-

tion institutions: the TPC PDUs are tested at INFN Naples, while the veto PDUs are evaluated in Liverpool, Edinburgh, Lancaster, and Warsaw.

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