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(Article begins on next page)

19 April 2024

High Performance Digital Multi-Loop Control of LLC Resonant Converters for EV Fast Charging with LUT-Based Feedforward and Adaptive Gain

Davide Cittanti, Matteo Gregorio, Enrico Vico, Fabio Mandrile, Eric Armando, and Radu Bojoi

***Abstract*—The LLC resonant converter is typically adopted in battery charging applications due to its excellent performance in terms of efficiency, power density and wide input/output voltage regulation. However, this converter is a complex high-order system characterized by a strong non-linear behavior, featuring large variations of the small-signal gain/phase and pole location depending on the operating point. Consequently, these features pose substantial challenges in designing a closed-loop controller and providing constant dynamical performance over a wide operating range. Therefore, this paper proposes a digital multi-loop control strategy for LLC resonant converters ensuring constant closed-loop bandwidth and excellent disturbance rejection performance across the complete converter operating region. The control scheme consists of two cascaded voltage and current loops. To design and tune these controllers, a simplified LLC dual first order small-signal model is proposed. The system non-linear behavior affecting the current control loop is counteracted by a real-time controller gain adaptation process, which ensures constant control bandwidth. In particular, the adaptive gain values are provided by a static switching frequency look-up table (LUT) obtained experimentally. Moreover, the steady state switching frequency value is fed forward at the output of the current loop regulator, providing a further dynamical performance enhancement. The proposed control strategy and controller design procedure are verified both in simulation and experimentally on a 15 kW LLC converter prototype. The results demonstrate the superior reference tracking and disturbance rejection performance of the proposed control strategy with respect to a state-of-the-art solution based on a proportional-integral regulator.**

***Index Terms*—digital control, LLC resonant converter, isolated DC/DC converter, electric vehicle (EV), battery charger**

I. Introduction

THE LLC resonant converter is widely adopted as isolated DC/DC conversion stage in electric vehicle (EV) on-board and off-board chargers (cf. Fig. 1) [1], [2], due to its high achievable efficiency and power density, wide input/output voltage regulation capability with a relatively narrow switching frequency variation, and limited filtering requirements (i.e., due to the converter capacitive output and soft-switching transitions) [3]–[6].

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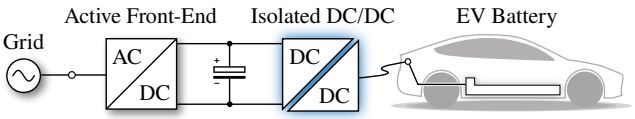

Fig. 1. Schematic overview of an EV off-board DC fast charger.

The tight output current control required in battery charging applications can be extremely challenging, since the multi-resonant nature of the LLC converter causes large system transfer function variations with varying input/output voltage gain and load [7], [8]. In particular, the DC/DC stage of a battery charger is typically subject to an input DC-link voltage ripple with a frequency multiple of the grid frequency (i.e., two or three times, depending on the PFC topology and the DC/DC connection configuration) [9]. The rejection of this voltage ripple requires high output current control bandwidth and consistent control performance across the complete converter operating region, which are both challenging to achieve.

Most low-power LLC converters directly control the voltage across a resistive load, therefore the most widespread control solution is based on an analog closed-loop control of the output voltage, exploiting a voltage-controlled oscillator (VCO) to regulate the switching frequency [10], [11]. However, battery chargers mostly operate in current-controlled (CC) mode, therefore the direct closed-loop control of the converter output current must be provided. Moreover, due to the advent of modern powerful and low-cost digital signal processors (DSPs), industry is increasingly pushing for digital control implementations. The benefits of digital controllers are well known and mainly consist in high degree of reproducibility, strong noise immunity and great flexibility, together with the opportunity of implementing complex control strategies and look-up tables (LUTs) [12]. Nevertheless, the digital implementation is affected by some drawbacks, such as sampling and quantization effects, limited resolution is generating output signals, limited computational speed and zero-order hold (ZOH) effects. In particular, for variable-frequency resonant converter applications, the limited DSP clock resolution may cause limit-cycle oscillations during normal operation [13].

In recent years, several LLC digital control strategies have been published, either implementing a single-loop direct output voltage control [14], [15] (i.e., not applicable to battery charger applications) or a direct output current control with/without an

external voltage loop, depending on the load kind (e.g., resistive, battery, LED) [16]–[21]. The authors in [16] propose a dual-loop control strategy for wide input/output voltage gain battery charging applications, featuring a direct output current control. However, no details on the controller design and/or tuning procedure are provided and no assessment of the dynamical control performance is carried out. A current loop controller design procedure is reported in [17], aiming to stabilize the performance of the outer voltage loop by providing high-enough closed-loop current control bandwidth and thus sufficient dynamical decoupling between the two loops. Nevertheless, also in this case no detailed controller tuning procedure is provided and the control dynamics are assessed focusing on the outer voltage loop, providing no insight on the inner current control loop performance. An effective approach to attenuate the typical input DC-link voltage oscillation of single-phase converters is proposed in [18] and [19], where a resonant controller tuned at the disturbance frequency is placed in parallel to a conventional proportional-integral (PI) or purely integral (I) controller. Both solutions obtain excellent disturbance rejection results, achieving little output current ripple in steady-state conditions. However, the resonant controller does not enhance the control performance outside its tuning frequency, leaving the closed-loop dynamics unaltered with respect to a conventional PI/I controller implementation and thus subject to the large system gain variations. A load feedback linearization approach is adopted in [20] to counteract the system non-linear behavior and provide consistent dynamical performance across the LLC operating range. In particular, first harmonic approximation (FHA) is leveraged to derive a linearization function used inside the output current control loop to compensate the system gain variations. Nevertheless, several system simplifications are made to obtain a practical model for the real-time control implementation and substantial inaccuracy is obtained as a result. This inaccuracy directly translates into an imperfect compensation of the system gain and thus inconsistent closed-loop dynamical performance. No assessment of the current control dynamics is provided in [20], as only the outer voltage loop is experimentally verified. Finally, in [21] a dual-loop voltage-current controller is designed leveraging analytically derived expressions, providing a simple and straightforward controller design procedure. Specifically, the PI regulator of the inner current control loop is tuned at the resonance frequency, identified as the most critical operating point in terms of gain/phase margin. However, the linear PI regulator in [21] cannot counteract the large system gain variations with the operating point, therefore resulting in poor dynamical performance when moving away from resonance. Also in this case, the experimental assessment is only performed for the outer voltage loop, thus providing no insight on the current control loop performance.

Therefore, the goal of this paper is to propose a digital multi-loop control strategy for LLC resonant converters ensuring constant control bandwidth and excellent disturbance rejection across the complete converter operating region. This is mainly achieved with a real-time controller gain adaptation process complemented by a feedforward action, leveraging a static switching frequency LUT obtained by experimental characterization of the converter. Even though this strategy is mainly intended for EV battery charging, it may also be extended to all those applications requiring tight output current and/or voltage control. The main contributions of this work can be summarized in:

- the derivation of a simplified dual first order small-signal model of the LLC resonant converter, enabling straightforward design and tuning of the cascaded dual-loop controllers;
- the proposal of a closed-loop current control strategy providing constant dynamical performance with respect to the operating point (i.e., input/output voltage gain and load variations) and ensuring high disturbance rejection;
- the experimental verification of the closed-loop output current control performance in all operating conditions, assessing reference step response, sinusoidal reference tracking and input DC-link voltage ripple rejection.

In particular, this article extends the work presented in [25] bringing in added value, namely proposing a simplified dual first order small-signal model of the LLC converter, adding a gain adaptation process within the current control loop to ensure constant control bandwidth, and assessing the dynamical performance of the proposed control strategy with a thorough experimental validation.

This paper is structured as follows. In Section II, the LLC small-signal behavior in analyzed and a simplified dual first order model, later exploited for the controller design, is derived. In Section III, the proposed LLC digital multi-loop control strategy is described in detail and a straightforward controller tuning procedure is provided, leveraging analytically derived expressions. The control performance is then validated in Section IV, where the closed-loop small-signal system behavior is verified in simulation environment and the large-signal control dynamics are assessed experimentally on a $15\,\mathrm{kW}$ LLC converter prototype. Finally, Section V summarizes and concludes this work.

II. LLC Small-Signal Model

The full-bridge LLC resonant converter system illustrated in Fig. 2 is considered throughout this work. Nevertheless, all considerations can be extended to the half-bridge LLC topology by simply considering half of the input voltage square-wave amplitude. The system is characterized by four state variables: the resonant inductor current i_r, the resonant capacitor voltage v_c, the transformer magnetizing current i_m and the output capacitor voltage v_o. Since the inverter full-bridge is assumed to be controlled by frequency modulation at $50\,\%$ duty cycle (i.e., no phase-shift control), the only system input variable is the inverter switching frequency f_sw, while the input DC-link voltage V_i, the battery equivalent resistance R_b and the battery open-circuit voltage V_b can be considered as system parameters or disturbances. Due to the high order of the system and the non-linear behavior of both inverter and rectifier stages, the LLC control design is fairly complicated and requires appropriate mathematical models.

Therefore, this section focuses on the LLC resonant converter small-signal behavior. In particular, the well known LLC seventh order model is briefly introduced in Section II-A

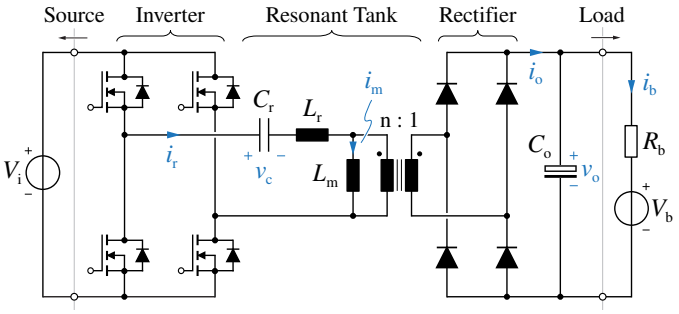

Fig. 2. Schematic of the considered LLC converter system, consisting of an ideal voltage source, a full-bridge inverter, a resonant tank (with integrated n : 1 transformer), a full-wave rectifier, a capacitive filter and a battery load.

and a detailed analysis of the transfer function linking the converter switching frequency to the output current is reported. In Section II-B, a recently developed LLC simplified third order model is summarized and explained, acting as foundation for the following section. Finally, a novel decoupled dual first order small-signal model (i.e., divided in two dynamically independent AC and DC subsystems) is proposed in Section II-C, aiming to provide simple and straightforward plant transfer functions for the design of the current and voltage controllers.

A. Full 7th Order System Model

The most widespread approach to derive an accurate small-signal model of the LLC resonant converter is the extended describing function (EDF) method [14], [19]–[23]. This approach is based on a sinusoidal first harmonic approximation (FHA) of the system state variables and converts the non-linear contributions of the system equations (e.g., modulus and sign functions) into their first harmonic components at the switching frequency (for AC quantities) or into their average values (for DC quantities). Notably, this process results in an increase of the system order, since each AC sinusoidal variable must be expressed by two independent sine and cosine components. The four original system state variables (i_r, v_c, i_m, v_o) thus become seven (i_{rs}, i_{rc}, v_{cs}, v_{cc}, i_{ms}, i_{mc}, v_o), where the subscripts s and c refer to the sine and cosine components, respectively. A seventh order system results:

$$\begin{cases} \dfrac{di_{rs}}{dt} = -\omega_{sw} i_{rc} + \dfrac{1}{L_r}\left(\dfrac{4}{\pi}V_i - v_{cs} - \dfrac{4}{\pi} n v_o \dfrac{i_{rs}-i_{ms}}{i_p}\right) & (1) \\ \dfrac{di_{rc}}{dt} = \omega_{sw} i_{rs} - \dfrac{1}{L_r}\left(v_{cc} + \dfrac{4}{\pi} n v_o \dfrac{i_{rc}-i_{mc}}{i_p}\right) & (2) \\ \dfrac{dv_{cs}}{dt} = -\omega_{sw} v_{cc} + \dfrac{1}{C_r} i_{rs} & (3) \\ \dfrac{dv_{cc}}{dt} = \omega_{sw} v_{cs} + \dfrac{1}{C_r} i_{rc} & (4) \\ \dfrac{di_{ms}}{dt} = -\omega_{sw} i_{mc} + \dfrac{1}{L_m}\dfrac{4}{\pi} n v_o \dfrac{i_{rs}-i_{ms}}{i_p} & (5) \\ \dfrac{di_{mc}}{dt} = \omega_{sw} i_{ms} + \dfrac{1}{L_m}\dfrac{4}{\pi} n v_o \dfrac{i_{rc}-i_{mc}}{i_p} & (6) \\ \dfrac{dv_o}{dt} = \dfrac{1}{C_o}\left(\dfrac{2}{\pi} n i_p - \dfrac{v_o - V_b}{R_b}\right) & (7) \end{cases}$$

where $\omega_{sw} = 2\pi f_{sw}$ and i_p is the amplitude of the transformer primary current

$$i_p = \sqrt{(i_{rs} - i_{ms})^2 + (i_{rc} - i_{mc})^2}. \quad (8)$$

The system state equations (1)–(7) represent the large-signal model of the LLC resonant converter. In particular, (1)–(6) describe the AC subsystem (i.e., the resonant tank dynamics), whereas (7) describes the DC subsystem (i.e., the output filter dynamics). Even though the EDF method linearizes the square-wave operation of the full-bridge inverter through FHA, the approximated output rectifier operation still yields non-linear voltage and current terms, arising from the product of two or more state variables in (1)–(2), (5)–(6). Therefore, to obtain a small-signal model of the system, equations (1)–(7) must be linearized around the converter operating point, leading to the well documented seventh order state-space representation of the LLC converter [14], [19]–[23].

Since the main LLC control design and tuning challenges are related to the current control loop (cf. Section III), a particular focus is dedicated to the switching frequency-to-output current $\tilde{i}_o(s)/\tilde{\omega}_{sw}(s)$ transfer function (i.e., where superscript $\sim$ indicates small-signal quantities). It is worth noting that the sixth order AC subsystem (1)–(6) and the first order DC subsystem (7) are considered to be completely decoupled in the following, since the resonant tank dynamics are typically much faster than the output filter ones [20] and the adopted dual-loop control strategy features a switching frequency feedforward term within the current control loop that directly compensates the output voltage variations (cf. Section III). Therefore, $v_o \approx V_o$ can be considered as a given parameter in (1)–(6), simplifying the current control plant transfer function $\tilde{i}_o(s)/\tilde{\omega}_{sw}(s)$. A qualitative overview of the pole location p_i and transfer function shape in buck mode ($V_o < V_i$), unity-gain mode ($V_o = V_i$) and boost mode ($V_o > V_i$) is reported in Fig. 3(a), (b) and (c), respectively, highlighting the pole movement and the transfer function variation with the output load (i.e., I_o).

Fig. 3(b) represents the LLC small-signal operation at unity-gain, where the inverter switching frequency f_{sw} is equal to the resonance frequency $f_r = 1/2\pi\sqrt{L_r C_r}$. It is observed that the transfer function is characterized by a single dominant pole in the origin of the root locus and both low-frequency gain and phase are unaffected by the load current value, which only modifies the high-frequency behavior of the transfer function. Therefore, being the controller bandwidth typically placed 1–2 decades lower than the resonance frequency f_r, in this region the system practically behaves as a pure integrator.

A similar behavior is observed for boost-mode operation in Fig. 3(c), where $f_{sw} < f_r$. The low-frequency system transfer function features a first order low-pass filter characteristic with a single dominant pole that moves towards the origin of the root locus for decreasing load values (i.e., increasing f_{sw}).

Finally, Fig. 3(a) represents the system operation in buck-mode, where $f_{sw} > f_r$. A very different behavior is observed in this case, as the system transfer function shape and characteristics change significantly with the output load I_o. In particular, in light load conditions the system features a single dominant pole near the origin of the root locus. The

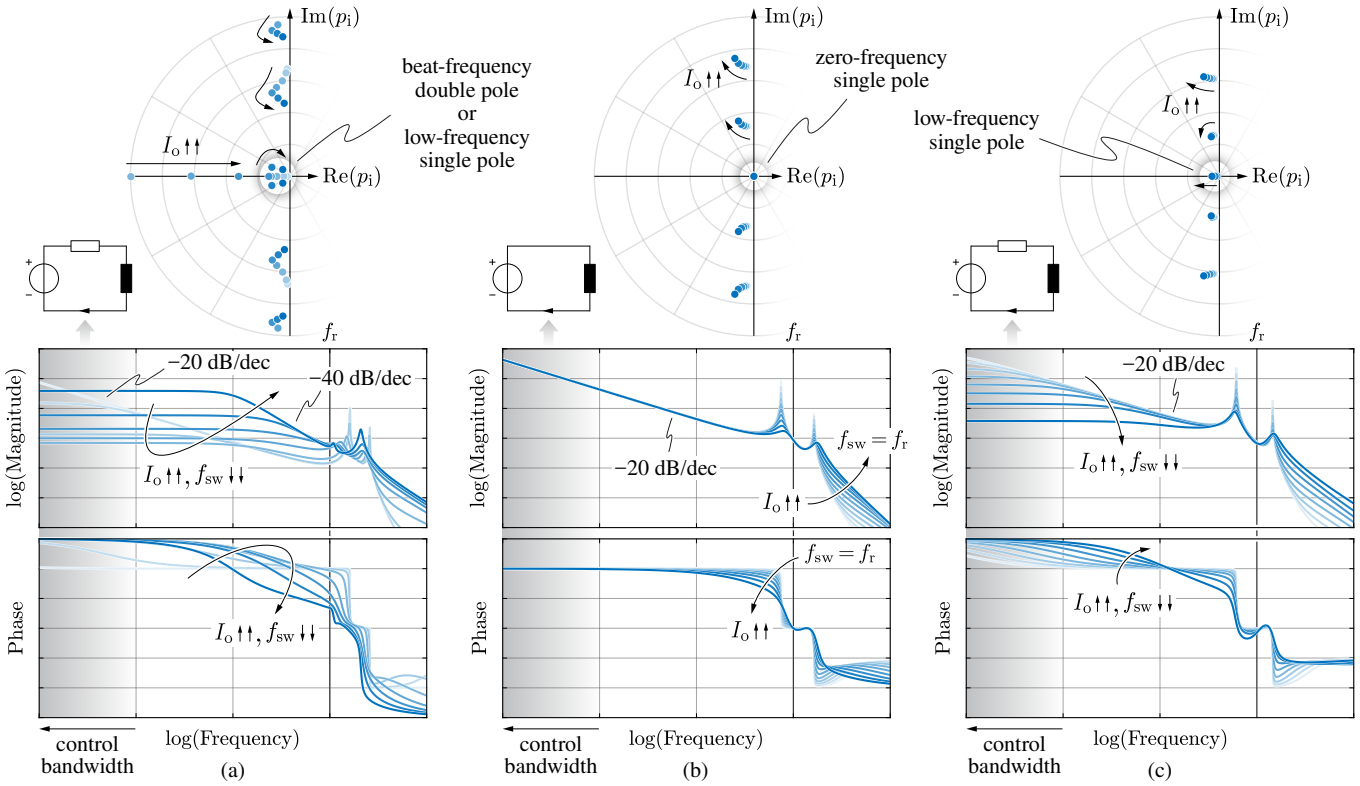

Fig. 3. Qualitative overview of the sixth order AC subsystem transfer function $\tilde{i}_o(s)/\tilde{\omega}_{sw}(s)$ poles, magnitude and phase in (a) buck-mode operation ($V_o < V_i$), (b) unity-gain operation ($V_o = V_i$) and (c) boost-mode operation ($V_o > V_i$). The AC and DC subsystems are assumed to be decoupled (i.e., $v_o \approx V_o$ in (1)–(6)) due to the much faster resonant tank dynamics and due to the adopted dual-loop control strategy, featuring a switching frequency feedforward term within the current control loop that directly compensates the output voltage variations (cf. Section III). The pole and transfer function variations with respect to the output load I_o are indicated and the dominant pole or pole pair is highlighted. The typical region of interest for the controller design is located 1–2 decades below the resonance frequency f_r, where the system approximately behaves as a first-order low-pass filter (i.e., RL circuit) in (a) and (c), or as a pure integrator (i.e., L circuit) in (b).

load increase and the simultaneous reduction of the switching frequency shift the dominant pole location to higher frequencies, up to when this pole encounters another real pole, merging into an imaginary dominant pole pair known as beat-frequency double pole (i.e., $f_b = f_{sw} - f_r$) [22]. Increasing further the system output load, the beat-frequency reduces, the small-signal steady-state gain increases and the imaginary pole pair gets more and more damped. Therefore, when the output load exceeds a specified threshold value dependent on the input/output voltage gain (i.e., referred to as the *V* region in series resonant converters [22]) the double pole splits again and a single dominant pole is obtained. As the beat-frequency double pole typically in no conditions gets near to the control bandwidth region (i.e., either due to the pole splitting when $V_o \approx V_i$, or due to the high pole frequency at maximum load for $V_o < V_i$), the system transfer function may be treated as a first order low-pass filter, similarly to boost-mode operation.

Therefore, even though the AC subsystem can only be fully characterized with a sixth order model, the transfer function analysis highlights the opportunity of representing the main system features with a simplified small-signal model, valid within the frequency region of interest for the controller design.

B. Reduced 3rd Order System Model

A reduced LLC third order small-signal model is derived in [24], adopting the same approach of [22] and [25] developed

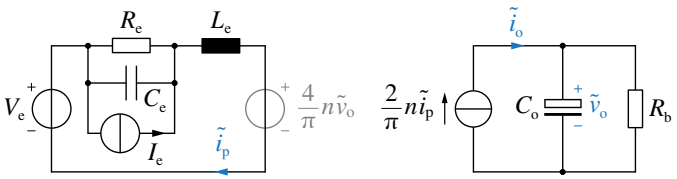

Fig. 4. Reduced third order small-signal equivalent circuit of the considered LLC system assuming a switching frequency perturbation $\tilde{\omega}_{sw}$: (a) AC subsystem, (b) DC subsystem. The voltage source related to $\tilde{v}_o$ is greyed out, as it can be disregarded when the output voltage dynamics are neglected (i.e., $v_o \approx V_o$). The values of V_e, I_e, R_e, L_e and C_e are reported in [24].

for the series resonant converter. The model order reduction is mainly obtained by approximating the resonant capacitor C_r small-signal behavior as the one of an equivalent inductor. This approximation is described in detail in [25] and maintains validity for perturbation frequency values much lower than the converter switching frequency (i.e., $|j\omega| \ll 2\pi f_{sw}$). Treating the resonant capacitor as an equivalent inductor, allows to directly reduce the order of the system by two (i.e., from seven to five), as the newly defined equivalent inductor is in series with L_r. Moreover, by leveraging the superimposition principle and performing substantial circuit manipulations, the considered system is further simplified in [24] and a reduced third order small-signal model is obtained.

This model is represented in equivalent circuit form in Fig. 4, assuming $\tilde{\omega}_{\rm sw}$ as the only system perturbation. The expressions of the circuit component values are reported in [24]. It is observed that AC and DC subsystems are coupled through $\tilde{v}_{\rm o}$ and $\tilde{i}_{\rm p}$, as the dynamics of the two circuits are not assumed to be independent. The passive components within the AC subsystem model different small-signal features, namely:

- $R_{\rm e}$ represents the total resonant tank impedance at the operating switching frequency [26], [27], as it determines the small-signal current value at steady state. Therefore, $R_{\rm e}=0$ at $f_{\rm sw}=f_{\rm r}$ and increases in buck and boost modes [26], [27]. It is worth noting that [24] considers $R_{\rm e}\approx 0$ in boost mode operation due to the typically low resonant tank impedance value, nevertheless this is not valid in general.
- $L_{\rm e}$ represents the integral behavior of the resonant tank and, in resonance and boost modes directly defines the high-frequency dynamical evolution of the small-signal current.
- $C_{\rm e}$ represents the buck mode beat-frequency double pole dynamics, being defined as $C_{\rm e}=1/4\pi^2 L_{\rm e}(f_{\rm sw}-f_{\rm r})^2$ for $f_{\rm sw}>f_{\rm r}$ and $C_{\rm e}=0$ for $f_{\rm sw}\leq f_{\rm r}$. In particular, the pole splitting phenomenon is determined by $R_{\rm e}/\sqrt{L_{\rm e}/C_{\rm e}}>0.5$ and is either achieved for large values of $R_{\rm e}$ (i.e., light-load, $f_{\rm sw}\gg f_{\rm r}$) or for large values of $C_{\rm e}$ (i.e., heavy-load, $f_{\rm sw}\approx f_{\rm r}$) [26], [27].

Unfortunately, the third order model presented in [24] is still unsuited for a straightforward controller design, mainly due to the $L_{\rm e}C_{\rm e}$ resonance, the presence of two sources (i.e., $V_{\rm e}$, $I_{\rm e}$) and the coupling of AC and DC subsystems. Therefore a further model simplification is proposed in the following.

C. Proposed Dual 1st Order System Model

Based on the considerations reported in Section II-A, the small-signal equivalent circuit model of [24] is here simplified further according to the following assumptions:

- the AC and DC subsystem dynamics can be considered decoupled (cf. Section II-A);
- the buck mode beat-frequency double pole dynamics can be disregarded (i.e., $C_{\rm e}\approx 0$), as the imaginary pole pair is typically placed outside the region of interest for the controller design (cf. Fig. 3).

These assumptions allow to represent the LLC small-signal behavior with the two decoupled and dynamically-independent first order systems illustrated in equivalent circuit form in Fig. 5 (i.e., derived in Appendix A). The system state-space equations are thus expressed as:

$$\begin{cases} \dfrac{{\rm d}\tilde{i}_{\rm o}}{{\rm d}t}=\dfrac{1}{L_{\rm eq}}\left(V_{\rm eq}-R_{\rm eq}\tilde{i}_{\rm o}\right) & (9)\\ \dfrac{{\rm d}\tilde{v}_{\rm o}}{{\rm d}t}=\dfrac{1}{C_{\rm o}}\left(\tilde{i}_{\rm o}-\dfrac{\tilde{v}_{\rm o}-V_{\rm b}}{R_{\rm b}}\right) & (10)\end{cases}$$

which define the dynamical evolution of the two control state variables $i_{\rm o}$ and $v_{\rm o}$.

While the physical meaning of the equivalent circuit parameters of the DC subsystem is straightforward, being directly related to the output filter and load, the understanding of the AC subsystem active and passive components requires further insight. Defining the static converter voltage gain M and quality factor Q as

$$M=\frac{nV_{\rm o}}{V_{\rm i}},\qquad Q=\frac{\pi^2}{8}\frac{Z_{\rm r}}{n^2}\frac{I_{\rm o}}{V_{\rm o}}, \tag{11}$$

where $Z_{\rm r}=\sqrt{L_{\rm r}/C_{\rm r}}$ is the characteristic impedance of the resonant tank, it is possible to completely identify a generic converter steady-state operating point in the inductive region (i.e., the stable region) with the sole parameter pair (M,Q).

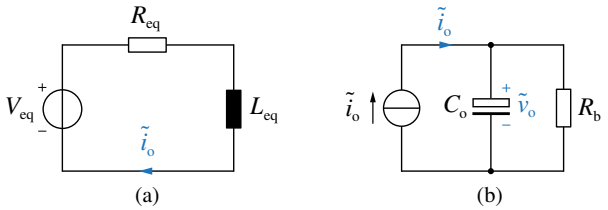

Fig. 5. Proposed dual first order simplified small-signal equivalent circuit of the considered LLC system assuming a switching frequency perturbation $\tilde{\omega}_{\rm sw}$: (a) AC subsystem, (b) DC subsystem.

It is derived from [24] that the equivalent circuit voltage source $V_{\rm eq}$ represents the static output voltage gain variation induced by a small-signal switching frequency perturbation $\tilde{f}_{\rm sw}=\tilde{\omega}_{\rm sw}/2\pi$ and is expressed by

$$V_{\rm eq}=\frac{\partial V_{\rm o}}{\partial f_{\rm sw}}\tilde{f}_{\rm sw}=\frac{V_{\rm i}}{n}\frac{\partial M}{\partial f_{\rm sw}}\tilde{f}_{\rm sw}, \tag{12}$$

It is worth noting that $\partial M/\partial f_{\rm sw}<0$, as an increase of the switching frequency leads to a lower static output voltage. The expression of $V_{\rm eq}$ has been independently confirmed at resonance in [21], [28] and is here extended to all operating conditions.

The physical meaning of $R_{\rm eq}$ remains the same as for $R_{\rm e}$ in [24], [26], [27], i.e., representing the overall static resonant tank impedance and linking the steady-state output current variation to the steady-state output voltage variation as

$$R_{\rm eq}=\frac{\partial V_{\rm o}/\partial f_{\rm sw}}{\partial I_{\rm o}/\partial f_{\rm sw}}=\frac{\pi^2}{8}\frac{Z_{\rm r}}{n^2}\frac{1}{M}\frac{\partial M/\partial f_{\rm sw}}{\partial Q/\partial f_{\rm sw}}. \tag{13}$$

It can be observed from (12) and (13), that the ratio $V_{\rm eq}/R_{\rm eq}$ correctly provides the static small-signal current value $\tilde{f}_{\rm sw}\cdot\partial I_{\rm o}/\partial f_{\rm sw}$.

Finally, $L_{\rm eq}$ is directly obtained by multiplying the expressions of $L_{\rm e}$ found in [24] by $\pi^2/8n^2$ (cf. Appendix A), obtaining

$$L_{\rm eq}=\begin{cases}\dfrac{\pi^2}{8}\dfrac{L_{\rm r}}{n^2}\left[1+\dfrac{f_{\rm r}^2}{f_{\rm sw}^2}+\dfrac{1}{\lambda}\left(1-\dfrac{f_{\rm sw}}{f_{\rm r}}\right)\right] & f_{\rm sw}<f_{\rm r}\\ \dfrac{\pi^2}{4}\dfrac{L_{\rm r}}{n^2} & f_{\rm sw}=f_{\rm r}\\ \dfrac{\pi^2}{8}\dfrac{L_{\rm r}}{n^2}\left(1+\dfrac{f_{\rm r}^2}{f_{\rm sw}^2}\right) & f_{\rm sw}>f_{\rm r}\end{cases} \tag{14}$$

where $\lambda=L_{\rm r}/L_{\rm m}$ is the LLC inductance ratio. It is observed that the expression of the equivalent inductance depends on the LLC operating region (i.e., either buck, boost or resonance modes) and varies with the switching frequency. In particular, in boost mode (i.e., $f_{\rm sw}<f_{\rm r}$) $L_{\rm eq}$ also depends on λ, as the

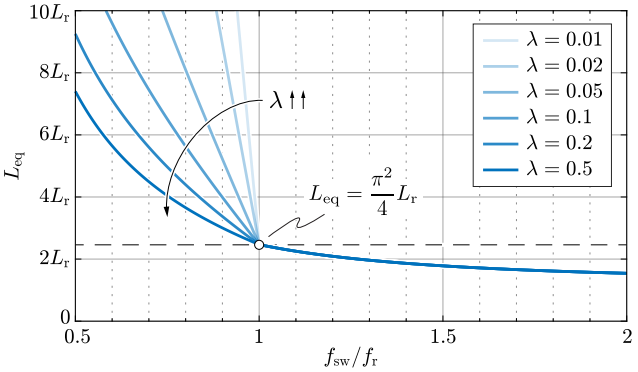

Fig. 6. Small-signal equivalent inductance L_{eq} as function of the normalized switching frequency f_{sw}/f_r and the inductance ratio λ, assuming $n = 1$.

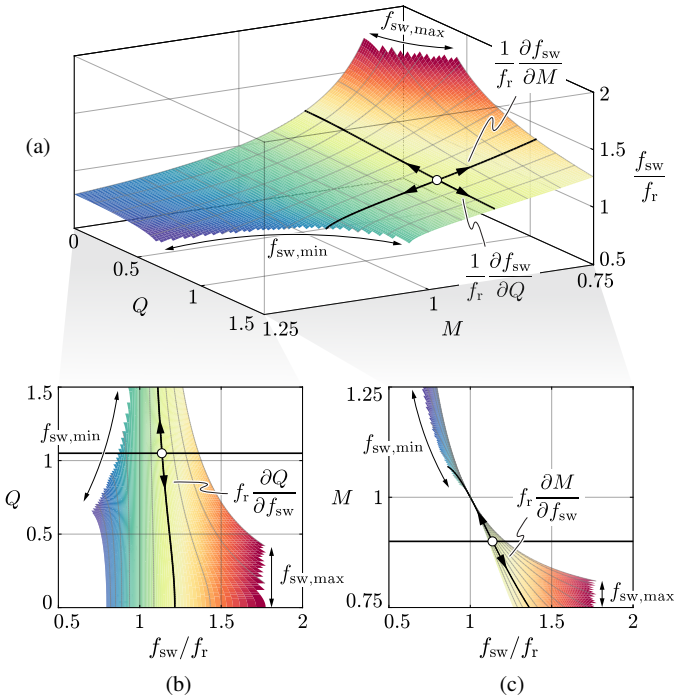

Fig. 7. Normalized static switching frequency f_{sw}/f_r as function of the converter voltage gain M and quality factor Q obtained with first harmonic approximation (FHA) [29], [30]: (a) 3D surface plot $f_{sw}(M, Q)$, (b) 2D contour plot $Q(f_{sw}, M)$, (c) 2D contour plot $M(f_{sw}, Q)$. The system maximum and minimum switching frequency limits $f_{sw,min}$, $f_{sw,max}$ are indicated. The $\circ$ symbol indicates the considered operating point and the values of $\partial Q/\partial f_{sw}$, $\partial M/\partial f_{sw}$ are represented by the slope of the isolines in (b) and (c), respectively.

magnetizing inductance affects the resonant tank operation during the time intervals at the end of each switching period, when $i_r = i_m$ [24]. The L_{eq} variation is illustrated in Fig. 6 as function of the normalized switching frequency f_{sw}/f_r and the inductance ratio λ. Intuitively, a larger value of L_m (i.e., a lower value of λ) translates in a larger value of L_{eq}. It is worth noting that the L_{eq} expression at resonance has been also independently confirmed in [21], [28].

The simplified first order transfer function of the AC subsystem can be therefore directly derived from (9) as

$$\frac{\tilde{i}_o(s)}{\tilde{f}_{sw}(s)} = \frac{1}{\tilde{f}_{sw}} \frac{V_{eq}}{R_{eq} + sL_{eq}}. \tag{15}$$

It can be observed that the small-signal steady-state gain

$$\left.\frac{\tilde{i}_o(s)}{\tilde{f}_{sw}(s)}\right|_{s\to 0} = \frac{1}{\tilde{f}_{sw}} \frac{V_{eq}}{R_{eq}} = \frac{8}{\pi^2} \frac{n^2}{Z_r} V_o \frac{\partial Q}{\partial f_{sw}} \tag{16}$$

is proportional to $\partial Q/\partial f_{sw}$, while the dynamic (i.e., high-frequency) small-signal gain

$$\left.\frac{\tilde{i}_o(s)}{\tilde{f}_{sw}(s)}\right|_{s\to \infty} = \frac{1}{\tilde{f}_{sw}} \frac{V_{eq}}{sL_{eq}} = \frac{V_i/n}{sL_{eq}} \frac{\partial M}{\partial f_{sw}} \tag{17}$$

is proportional to $\partial M/\partial f_{sw}$. The static values of M and Q can be expressed as functions of the switching frequency by leveraging the first harmonic approximation (FHA) [29], [30], as

$$M = \frac{1}{\sqrt{\left(1 + \lambda - \lambda \frac{f_r^2}{f_{sw}^2}\right)^2 + Q^2 \left(\frac{f_{sw}}{f_r} - \frac{f_r}{f_{sw}}\right)^2}} \tag{18}$$

and

$$Q = \frac{\sqrt{\frac{1}{M^2} - \left(1 + \lambda - \lambda \frac{f_r^2}{f_{sw}^2}\right)^2}}{\left|\frac{f_{sw}}{f_r} - \frac{f_r}{f_{sw}}\right|}. \tag{19}$$

Deriving expressions (18) and (19) with respect to the switching frequency f_{sw}, the desired derivative values are obtained as

$$\frac{\partial M}{\partial f_{sw}} = -\frac{1}{f_{sw}} \frac{2\lambda \frac{f_r^2}{f_{sw}^2}\left(1 + \lambda - \lambda \frac{f_r^2}{f_{sw}^2}\right) + Q^2\left(\frac{f_{sw}^2}{f_r^2} - \frac{f_r^2}{f_{sw}^2}\right)}{\left[\sqrt{\left(1 + \lambda - \lambda \frac{f_r^2}{f_{sw}^2}\right)^2 + Q^2\left(\frac{f_{sw}}{f_r} - \frac{f_r}{f_{sw}}\right)^2}\right]^3} \tag{20}$$

and

$$\frac{\partial Q}{\partial f_{sw}} = -\frac{1}{f_{sw}} \frac{2\lambda \frac{f_r^2}{f_{sw}^2}\left(1 + \lambda - \lambda \frac{f_r^2}{f_{sw}^2}\right) + Q^2\left(\frac{f_{sw}^2}{f_r^2} - \frac{f_r^2}{f_{sw}^2}\right)}{Q\left(\frac{f_{sw}}{f_r} - \frac{f_r}{f_{sw}}\right)^2}. \tag{21}$$

The static value of $f_{sw}(M, Q)$ can be found numerically and is illustrated in Fig. 7, considering the LLC circuit parameters reported in Section IV. In particular, Fig. 7(b) and (c) highlight the strong system non-linearity, translating into large variations of both $\partial M/\partial f_{sw}$ and $\partial Q/\partial f_{sw}$ depending on the operating point. These variations in turn modify the small-signal system transfer function according to (16) and (17), translating into a first order system with variable gain and moving pole and posing substantial control challenges.

The availability of the M and Q derivative expressions (20), (21) allows to evaluate numerically V_{eq} and R_{eq} depending on the system operating point. Therefore, the magnitude and phase trends of the simplified transfer function $\tilde{i}_o(s)/\tilde{f}_{sw}(s)$

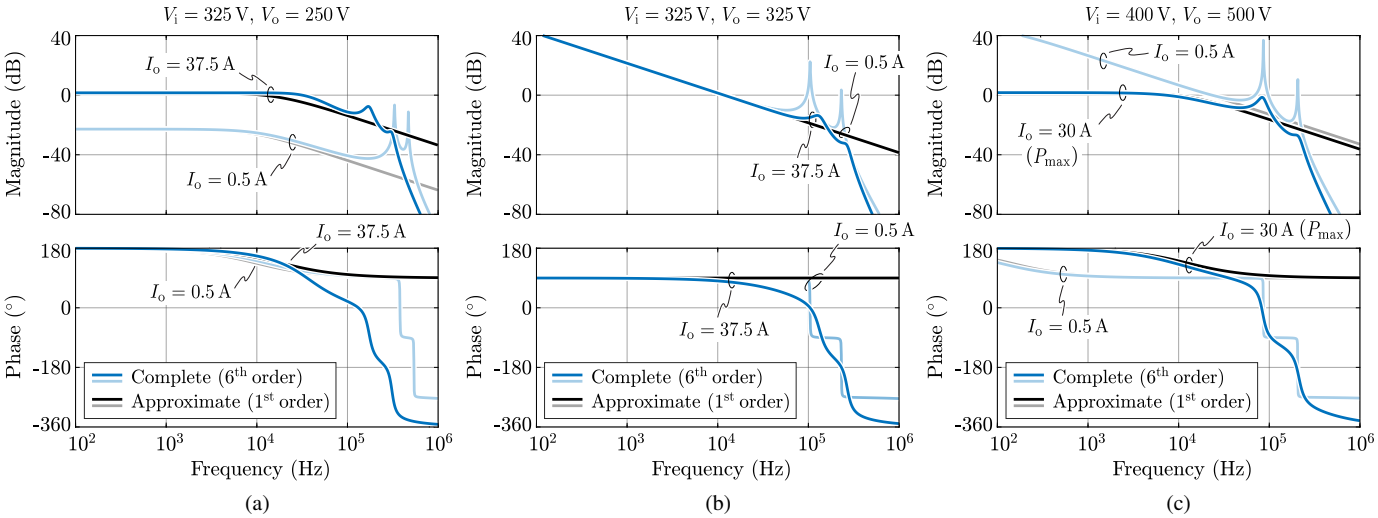

Fig. 8. Switching frequency-to-output current transfer function $\tilde{i}_\mathrm{o}(s)/\tilde{f}_\mathrm{sw}(s)$ comparison between the full sixth order small-signal model and the proposed simplified first order small-signal model of the LLC converter AC subsystem: (a) buck mode operation ($M \approx 0.77$), (b) resonance/unity-gain mode operation ($M = 1$) and (c) boost mode operation ($M = 1.25$). The system parameters and limits reported in Section IV are considered. The small-signal transfer functions are shown in both minimum and maximum load conditions.

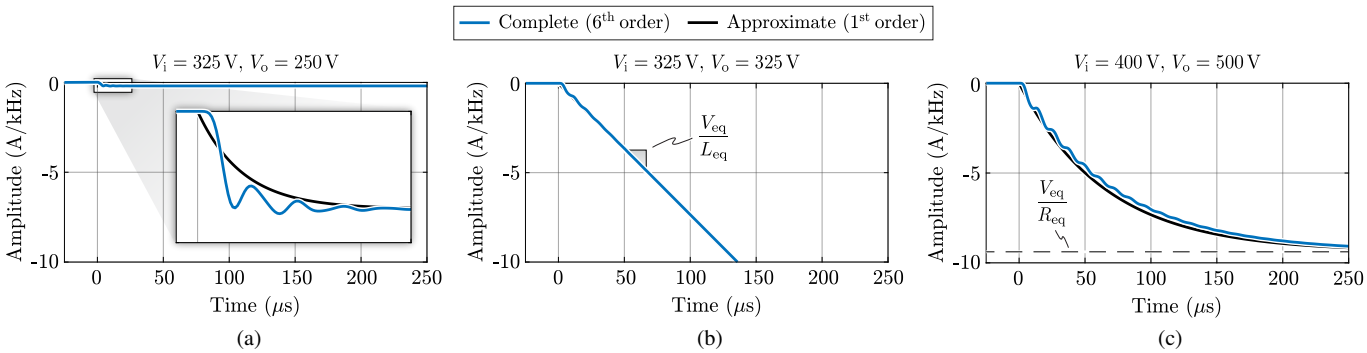

Fig. 9. Time-domain comparison between the open-loop step responses of the switching frequency-to-output current transfer function $\tilde{i}_\mathrm{o}(s)/\tilde{f}_\mathrm{sw}(s)$ for the full sixth order small-signal model and the proposed simplified first order small-signal model of the LLC converter AC subsystem: (a) buck mode operation ($M \approx 0.77$), (b) resonance/unity-gain mode operation ($M = 1$) and (c) boost mode operation ($M = 1.25$), assuming $I_\mathrm{o} = 10\,\mathrm{A}$. The system parameters and limits reported in Section IV are considered.

reported in (15) can be compared to the ones obtained for the complete sixth order AC subsystem model (1)–(6) to assess the validity of the performed approximations. This comparison is provided in Fig. 8, where the LLC system parameters and operating limits reported in Section IV are assumed. In particular, three operating modes are considered, namely buck mode ($M \approx 0.77$), resonance/unity-gain mode ($M = 1$) and boost mode ($M = 1.25$), evaluating the system transfer functions in both minimum and maximum load conditions. It is immediately observed that the simplified first order transfer functions accurately match the full order model up to high frequency values (i.e., 10–100 kHz) in all operating conditions. Notably, a very limited low-frequency error is observed also in buck mode, even though the simplified model disregards the beat-frequency double pole. In fact, the high-frequency location of the double pole does not substantially affect the full order transfer function in the control region of interest, thus leaving unaltered the accuracy of the simplified model.

A different point of view is provided in Fig. 9, where a comparison between the two models is carried out in the time domain, assessing the open-loop system response to a reference step in buck, resonance and boost modes (i.e., assuming $I_\mathrm{o} = 10\,\mathrm{A}$). The waveforms confirm the good accuracy of the proposed simplified model, especially at resonance (i.e., inductive behavior) and in boost mode (i.e., first-order low-pass filter behavior). Furthermore, the time-domain response in buck mode demonstrates that, even though the simplified model achieves a lower overall accuracy with respect to the other operating modes, it is able to correctly reproduce the low-frequency dynamics of the system (i.e., the main requirement for the design and tuning of the closed-loop control).

Case Study – Operation at Resonance: The LLC converter operation at resonance frequency (i.e., $f_\mathrm{sw} = f_\mathrm{r}$) is characterized by $M = 1$ independently of the converter load. This is expressed by (18) and can be observed in Fig. 7(c), where all constant-Q lines pass through a single point in $f_\mathrm{sw} = f_\mathrm{r}$. In particular, the reduced first order small-signal model (15) is simplified further, as $R_\mathrm{eq} = 0$ and thus

$$\left.\frac{\partial M}{\partial f_\mathrm{sw}}\right|_{f_\mathrm{sw}=f_\mathrm{r}} = -\frac{2\lambda}{f_\mathrm{r}}, \qquad \left.\frac{\partial Q}{\partial f_\mathrm{sw}}\right|_{f_\mathrm{sw}=f_\mathrm{r}} = -\infty. \tag{22}$$

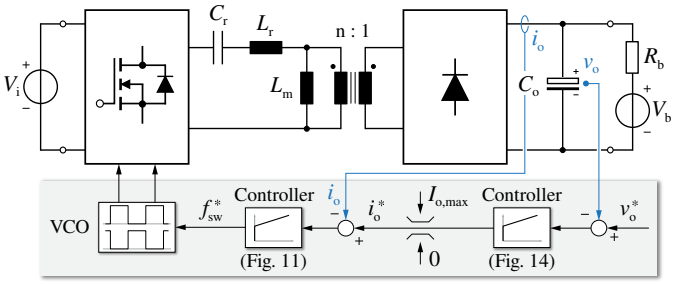

Fig. 10. Simplified schematic of the proposed multi-loop converter control, consisting of an outer voltage v_o loop (cf. Fig. 14) and an inner current i_o loop (cf. Fig. 11). The voltage controlled oscillator (VCO) is implemented by digital means.

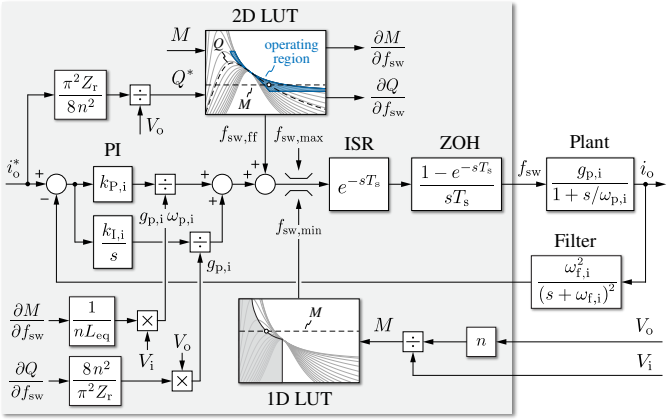

Fig. 11. Detailed schematic overview of the output current i_o closed-loop control. The digital controller is highlighted in grey.

Furthermore, the expression of V_{eq} becomes

$$V_{eq}|_{f_{sw}=f_r} = -2\,\frac{V_i}{n}\,\frac{L_r}{L_m}\,\frac{1}{f_r}\,\tilde{f}_{sw}, \tag{23}$$

differently from what previously reported in [21], [28].

Therefore, a substantial circuit simplification is obtained, as the system behavior becomes load-independent, the dominant pole moves to the origin of the root locus and the resonant tank behaves as an equivalent inductor.

III. Controller Design

In this section, the adopted cascaded digital dual-loop control scheme is described, consisting of an outer voltage control loop (v_o) and an inner current control loop (i_o), as schematically illustrated in Fig. 10. The i_o control loop aims to provide tight output current regulation by acting on the switching frequency of the input bridge. The v_o control loop, instead, only plays an active role during start-up and constant-voltage battery charging (i.e., at the very end of the charging process), as the voltage reference is always set to the fully-charged maximum battery voltage value $V_{b,max}$, which is provided by the vehicle itself. During most of the time, the output of the voltage regulator is saturated to the maximum charging current value $I_{o,max}$, either limited by the vehicle battery management system (BMS) or by the converter current/power boundaries. As a consequence, the voltage control dynamics are not of primary importance in the present application. Nevertheless, for reasons of completeness, a design and tuning procedure for both i_o and v_o controllers is provided in this section.

A. Inner Current Control Loop

The main requirements of the output current i_o controller are tight current regulation with zero steady-state error, high dynamical performance, mainly to reject the low-frequency input voltage ripple (e.g., occurring at two times or three times the mains frequency, respectively when single-phase or three-phase three-level PFCs are adopted as first stage of the battery charger [31]), and consistent small- and large-signal behavior over the complete operating range. The last requirement, in particular, is typically hard to achieve and represents the major focus of the controller design.

The proposed digital output current control scheme is illustrated in Fig. 11. The current is measured at the output of the diode bridge (i.e., as a rectified sine wave) and is passed through a second-order filter with a 25 kHz corner frequency $f_{f,i}$ to obtain its average value. Overall, the control loop consists of the filter applied to the current measurement, a proportional-integral (PI) regulator, two gain adaptation blocks and a feedforward contribution obtained with a single LUT, a minimum/maximum frequency saturation block, a delay deriving from the digital control implementation and the plant itself (i.e., the frequency-to-current transfer function).

The transfer function of the second-order filter applied to the current measurement has the following expression:

$$G_{f,i}(s) = \frac{\omega_{f,i}^2}{(s+\omega_{f,i})^2}, \tag{24}$$

where $\omega_{f,i} = 2\pi f_{f,i}$ is the filter corner frequency.

The digital sampling and update processes are performed at a constant frequency $f_s = 1/T_s$ (i.e., the sampling or control frequency). To accurately tune the current control loop performance, the system delays introduced by the digital controller implementation must be taken into account, as each delay reduces the achievable control bandwidth and/or decreases the closed-loop stability margin [32], [33]. The first delay component is directly related to the digital interrupt service routine (ISR), which introduces a one sampling period delay T_s between input and output signals. The second component is linked to the ZOH effect of one sampling period T_s introduced by the digital update process of the output switching frequency. Even though the ZOH does not result in a pure delay effect (i.e., as it affects also the system gain), if the control bandwidth is sufficiently lower than the Nyquist frequency it can be considered as an ideal $T_s/2$ delay. Therefore, the total delay introduced by the digital control implementation is $T_d = 3T_s/2$, which can be approximated with a rational Padè transfer function

$$G_{d,i}(s) = e^{-s\,3T_s/2} \approx \frac{1 - s\,3T_s/4}{1 + s\,3T_s/4}. \tag{25}$$

The linearized plant transfer function, linking a small-signal switching frequency perturbation $\tilde{f}_{sw}$ to the resulting output current variation $\tilde{i}_o$, has been simplified to a first-order transfer function in Section II-C. The small-signal steady-state gain is

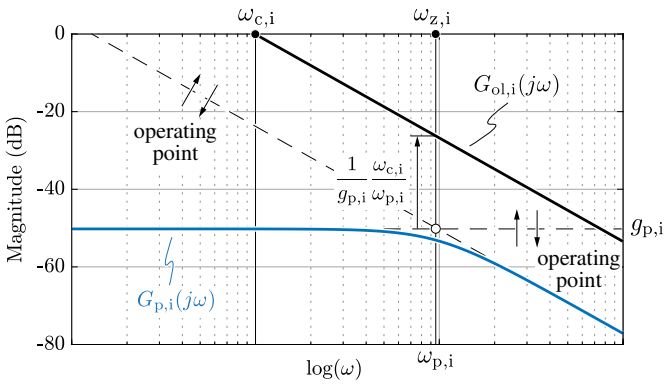

Fig. 12. Simplified first order $G_{\mathrm{p,i}}(s) = \tilde{i}_{\mathrm{o}}(s)/\tilde{f}_{\mathrm{sw}}(s)$ plant transfer function representation, highlighting the variable gain $g_{\mathrm{p,i}}$ and moving pole $\omega_{\mathrm{p,i}}$. The target constant open-loop control transfer function is also indicated.

obtained by setting $s = 0$ into (15), as

$$g_{\mathrm{p,i}} = \frac{1}{\tilde{f}_{\mathrm{sw}}} \frac{V_{\mathrm{eq}}}{R_{\mathrm{eq}}} = \frac{8}{\pi^2} \frac{n^2}{Z_{\mathrm{r}}} V_{\mathrm{o}} \frac{\partial Q}{\partial f_{\mathrm{sw}}}, \tag{26}$$

and the pole frequency is directly derived from the denominator of (15), as

$$\omega_{\mathrm{p,i}} = \frac{R_{\mathrm{eq}}}{L_{\mathrm{eq}}} = \frac{\pi^2}{8} \frac{Z_{\mathrm{r}}}{n^2} \frac{1}{M} \frac{\partial M/\partial f_{\mathrm{sw}}}{\partial Q/\partial f_{\mathrm{sw}}} \frac{1}{L_{\mathrm{eq}}}. \tag{27}$$

Therefore, the simplified plant transfer function can be expressed as

$$G_{\mathrm{p,i}}(s) = \frac{\tilde{i}_{\mathrm{o}}(s)}{\tilde{f}_{\mathrm{sw}}(s)} \approx \frac{g_{\mathrm{p,i}}}{1 + s/\omega_{\mathrm{p,i}}}. \tag{28}$$

Expression (28) shows that the system approximately behaves as a first-order low-pass filter with both a variable steady-state gain and a moving pole, as both $g_{\mathrm{p,i}}$ and $\omega_{\mathrm{p,i}}$ vary considerably with the operating point (cf. Fig. 12). For instance, at resonance (i.e., $f_{\mathrm{sw}} = f_{\mathrm{r}}$, $M = 1$) the ideal system behaves as a pure integrator, being $\partial Q/\partial f_{\mathrm{sw}} \approx -\infty$. In fact, the pole frequency $\omega_{\mathrm{p,i}}$ moves to zero and an infinite steady-state gain $g_{\mathrm{p,i}}$ is obtained. Notably, the large variation of the system gain and pole location during normal operation is a critical aspect of the LLC converter and must be taken into account within the current controller design.

Since the plant shows an integral behavior only at resonance, a PI regulator is selected to ensure a zero steady-state tracking error in all operating conditions and improved disturbance rejection capabilities with respect to a simple proportional regulator. To counteract the system gain/pole movement and ensure constant control bandwidth, the same approach proposed in [34] is adopted: the values of $g_{\mathrm{p,i}}$ and $\omega_{\mathrm{p,i}}$ are calculated in real-time and a controller gain adaptation is performed. In particular, the output of the proportional regulator is divided by the moving pole frequency $\omega_{\mathrm{p,i}}$, while the overall PI output is divided by the variable steady-state gain $g_{\mathrm{p,i}}$, obtaining the following controller transfer function:

$$G_{\mathrm{c,i}}(s) = \frac{1}{g_{\mathrm{p,i}}} \left(\frac{1}{\omega_{\mathrm{p,i}}} k_{\mathrm{P,i}} + \frac{k_{\mathrm{I,i}}}{s} \right), \tag{29}$$

where $k_{\mathrm{P,i}}$ and $k_{\mathrm{I,i}}$ are the proportional and integral regulator coefficients, respectively. Being the system open-loop transfer function defined as

$$G_{\mathrm{ol,i}}(s) = G_{\mathrm{f,i}}(s)\, G_{\mathrm{c,i}}(s)\, G_{\mathrm{d,i}}(s)\, G_{\mathrm{p,i}}(s), \tag{30}$$

the following expression is obtained substituting (28) and (29) into (30):

$$G_{\mathrm{ol,i}}(s) = k_{\mathrm{P,i}} \frac{s + \omega_{\mathrm{p,i}}\, k_{\mathrm{I,i}}/k_{\mathrm{P,i}}}{s\,(s + \omega_{\mathrm{p,i}})}\, G_{\mathrm{f,i}}(s)\, G_{\mathrm{d,i}}(s). \tag{31}$$

To compensate the plant pole $\omega_{\mathrm{p,i}}$ with the controller zero (i.e., $\omega_{\mathrm{z,i}} = \omega_{\mathrm{p,i}}\, k_{\mathrm{I,i}}/k_{\mathrm{P,i}}$), the ratio $k_{\mathrm{I,i}}/k_{\mathrm{P,i}}$ is set to 1, leading to a plant-independent open-loop transfer function expression:

$$G_{\mathrm{ol,i}}(s) = \frac{k_{\mathrm{P,i}}}{s} \frac{\omega_{\mathrm{f,i}}^2}{(s + \omega_{\mathrm{f,i}})^2} \frac{1 - s\,3T_{\mathrm{s}}/4}{1 + s\,3T_{\mathrm{s}}/4}. \tag{32}$$

Therefore, the controller coefficients $k_{\mathrm{P,i}}$ and $k_{\mathrm{I,i}}$ can be easily set to achieve the desired value of open-loop 0 dB cross-over frequency $\omega_{\mathrm{c,i}}$. In particular, assuming $\omega_{\mathrm{c,i}} \ll \omega_{\mathrm{f,i}}$ and solving $|G_{\mathrm{ol,i}}(j\omega_{\mathrm{c,i}})| = 1$, the following coefficients are obtained:

$$\begin{cases} k_{\mathrm{P,i}} = \omega_{\mathrm{c,i}} \\ k_{\mathrm{I,i}} = \omega_{\mathrm{c,i}} \end{cases}. \tag{33}$$

It is worth noting that $k_{\mathrm{P,i}} = k_{\mathrm{I,i}}$, since the gain adaptation process extracts the variable terms $g_{\mathrm{p,i}}$ and $\omega_{\mathrm{p,i}}$ from the proportional and integral coefficients, as shown in (29).

Since the open-loop transfer function has been expressed in rational form in (32), the tuning of $\omega_{\mathrm{c,i}}$ can be performed in the continuous time domain employing conventional techniques. In the present work, a phase margin tuning criterion is adopted, therefore $\omega_{\mathrm{c,i}}$ is expressed as a function of the desired phase margin in radians m_φ by solving $\angle G_{\mathrm{ol,i}}(j\omega_{c,i}) = -\pi + m_\varphi$ and assuming $\omega_{\mathrm{c,i}} \ll \omega_{\mathrm{f,i}}$, as

$$\omega_{\mathrm{c,i}} \approx \frac{1}{T_{\mathrm{s}}} \left[-\tan(m_\varphi) + \sqrt{1 + \tan^2(m_\varphi)} \right]. \tag{34}$$

In the following, $m_\varphi = 60°$ is considered, ensuring both fast reference step response and enhanced disturbance rejection capability. For the system at hand (i.e., with $f_{\mathrm{f,i}} = 25\,\mathrm{kHz}$, $f_{\mathrm{s}} = 20\,\mathrm{kHz}$, $T_{\mathrm{s}} = 50\,\mu\mathrm{s}$, cf. Section IV), an open-loop cross-over frequency $f_{\mathrm{c,i}} \approx 1.1\,\mathrm{kHz}$ is obtained.

A key feature of the proposed control scheme in Fig. 11 is the inclusion of a feedforward contribution, namely the steady-state switching frequency in the desired operating conditions. This feature essentially allows to unburden the integral part of the PI regulator, counteract the non-linear nature of the system, and ensure the small-signal operation of the controller. Additionally, the feedforward term allows to instantaneously compensate the dynamical output voltage variations, effectively decoupling the small-signal AC and DC subsystems (cf. Section II) and thus eliminating the impact of the resonance between L_{eq} and C_{o} on the current control phase margin. The steady-state f_{sw} values, obtained as function of the operating voltage gain M and quality factor Q, are stored in a look-up table (LUT) and the desired feedforward value is extracted from the LUT by linear interpolation. The exploitation of M and Q allows to normalize the converter operating conditions and uniquely identify a working point in

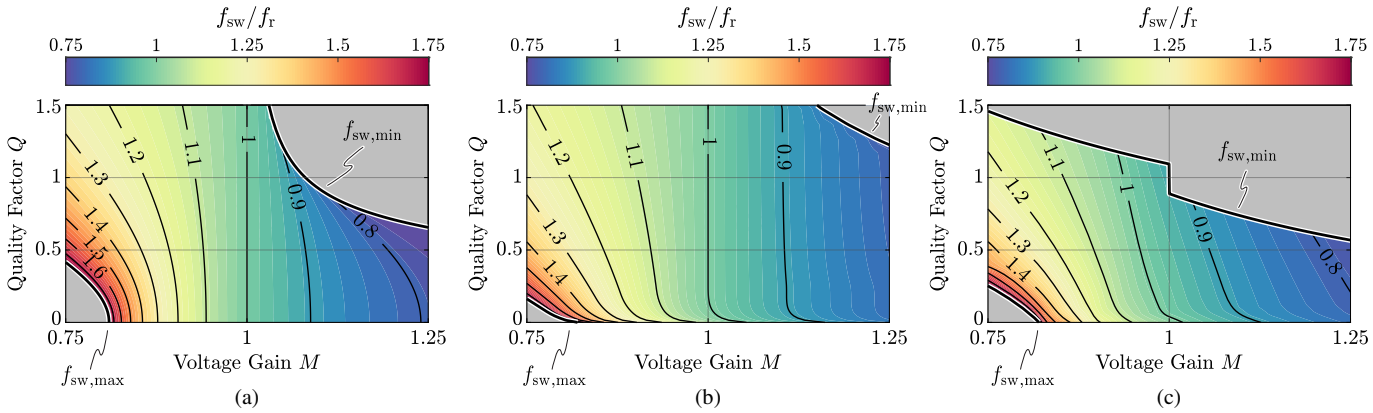

Fig. 13. Steady-state normalized switching frequency f_{sw}/f_r as a function of M and Q, with minimum and maximum frequency limits superimposed. 101x101 LUT extracted with (a) first harmonic approximation (FHA), (b) time domain analysis (TDA) and (c) experimental characterization (cf. Appendix B).

the inductive region (i.e., the stable region) with only two parameters, thus requiring a simple two-dimensional (2D) LUT. In essence, the feedforward f_{sw} contribution serves the purpose of unloading the PI controller from the major frequency steps, leaving to the controller the tasks of counteracting the dynamical perturbations around equilibrium and addressing the LUT steady-state error. Furthermore, the LUT inherently stores the information regarding $\partial M/\partial f_{sw}$ and $\partial Q/\partial f_{sw}$, which can be exploited for the controller gain adaptation in (26) and (27) in place of the analytical FHA expressions (20) and (21).

The simplest way to extract the $f_{sw}(M,Q)$ LUT is by numerically inverting the FHA gain expression (18), however yielding approximate and inaccurate results. Better methods, ensuring increasing accuracy at the expense of a higher realization effort, consist in solving a time-domain analysis (TDA) of the system operating modes [35], carrying out an extensive set of circuit simulations, or characterizing the real converter prototype with experimental measurements. In particular, the TDA method yields the exact same results as the extensive circuit simulations, however requiring far lower computational effort and time [36]. A comparison of the LUTs obtained with FHA, TDA and experimental characterization is provided in Fig. 13, assuming the converter specifications reported in Section IV, Table I. For reasons of completeness, the minimum switching frequency limit $f_{sw,min}(M)$ and maximum switching frequency limit $f_{sw,max} = 250\,\text{kHz}$ are superimposed to graphically identify the feasible operating region of the converter. While for FHA and TDA the value of $f_{sw,min}(M)$ is determined as the boundary frequency between inductive and capacitive regions, in the experimental characterization $f_{sw,min}(M)$ is determined either by the converter maximum output current $I_{o,max} = 37.5\,\text{A}$ (for $M \leq 1$ and $V_i \leq 400\,\text{V}$) or by the converter maximum output power rating $P_{o,max} = 15\,\text{kW}$ (for $M > 1$ and $V_i = 400\,\text{V}$), as explained in Section IV. It can be observed that the FHA method yields a wider operating frequency range with respect to TDA for the same (M,Q) values. Moreover, the behavior at low quality factors is extremely different between the two, as only the TDA method correctly predicts the necessary frequency increase at light load: for instance, with the FHA method the steady-state switching frequency for $M = 1$ is equal to f_r and is load independent, which is not the case for TDA. Therefore, since the TDA method is characterized by better accuracy and only requires a slightly higher computational effort compared to FHA, it is the preferred choice for the LUT extraction when an experimental characterization of the converter is not available. Nevertheless, if a complete characterization of the converter is performed (as explained in Appendix B), the best accuracy is obtained. Comparing Fig. 13(c) with Fig. 13(b), a substantial difference between the iso-frequency curve slopes is observed, translating into a larger frequency variation for a given M value in experimental practice. Other than component non-idealities and tolerances, the main reason behind this discrepancy can be attributed to the converter losses [37], mostly generated by the semiconductor devices, the resonant inductor/s, the resonant capacitor/s and the transformer/s. These losses increase substantially with the converter load and thus require a lower value of switching frequency (i.e., a higher voltage boosting) to get compensated. Furthermore, the converter losses largely reduce the value of $\partial Q/\partial f_{sw}$ around the unity voltage gain region, limiting the plant gain/pole variation and greatly decreasing the sensitivity of the control system with respect to the LUT discretization. Overall, only the LUT obtained by experimental characterization of the converter can provide sufficient accuracy for the proposed high-performance control strategy, as it provides the real converter steady-state switching frequency in the feedforward path and addresses the FHA and TDA small-signal gain/pole modeling errors by providing the experimental values of $\partial M/\partial f_{sw}$ and $\partial Q/\partial f_{sw}$ for a correct controller gain adaptation.

Finally, as illustrated in Fig. 11, a switching frequency saturation block (with integrated anti-windup scheme) must be present in the forward control path, to ensure that the converter operation remains within the minimum and maximum frequency design boundaries. As previously mentioned, the minimum switching frequency limit is a function of the voltage gain M, therefore $f_{sw,min}(M)$ is also stored in a one-dimensional (1D) LUT (cf. Appendix B).

B. Outer Voltage Control Loop

The output voltage v_o controller is responsible for adjusting the output current i_o to regulate the voltage across the output filter capacitor C_o. The main requirements for this controller

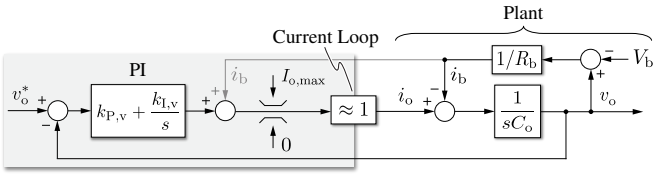

Fig. 14. Detailed schematic overview of the output voltage v_o closed-loop control. The digital controller is highlighted in grey.

are zero steady-state error and sufficient dynamical performance to properly reject system disturbances (e.g., the battery current, if not fed forward).

The complete output voltage control schematic is illustrated in Fig. 14 and consists of a PI regulator, an optional feedforward contribution, a maximum current saturation block, the output current control loop and the plant itself.

The plant transfer function is obtained from (10) considering the battery voltage V_b as a disturbance component:

$$G_{p,v}(s) = \frac{\tilde{v}_o(s)}{\tilde{i}_o(s)} = \frac{R_b}{1 + s\,R_b\,C_o}. \tag{35}$$

Since the measurement of the battery current i_b is normally available, its value can be fed forward. In such case, the compensated plant behaves as a pure integrator:

$$G_{p,v}(s) \approx \frac{1}{sC_o}. \tag{36}$$

Nevertheless, a PI regulator is selected to improve the controller dynamical performance and to ensure zero steady-state error when i_b is not known and cannot be fed forward:

$$G_{c,v}(s) = k_{P,v} + \frac{k_{I,v}}{s}. \tag{37}$$

The output of the regulator is then saturated between 0 and $I_{o,max}$ (i.e., either limited by the vehicle BMS or by the converter current/power boundaries) with an anti-windup scheme, thus becoming the reference for the inner current control loop. Since this loop is characterized by much faster dynamics with respect to the voltage control ones, the current loop can be considered as an ideal actuator (i.e., a unity gain block). Therefore, the v_o control open-loop transfer function can be expressed as

$$G_{ol,v}(s) = G_{c,v}(s)\,G_{p,v}(s). \tag{38}$$

If the open-loop 0 dB cross-over frequency $\omega_{c,v}$ is set sufficiently lower than the bandwidth of the current control loop (i.e., $\approx \omega_{c,i}$), the dynamics of the two loops do not interfere with each other. Therefore, $\omega_{c,v}$ is set to $\omega_{c,i}/10$, resulting in a 110 Hz open-loop cross-over frequency. The controller parameters are derived as

$$\begin{cases} k_{P,v} = \omega_{c,v}\,C_o \\ k_{I,v} = \omega_{z,v}\,k_{P,v} \end{cases}, \tag{39}$$

where the PI zero $\omega_{z,v} = k_{I,v}/k_{P,v}$ is set to $\omega_{c,v}/5$ in order to improve the closed-loop disturbance rejection capabilities.

TABLE I. LLC CONVERTER SPECIFICATIONS AND OPERATING REGION.

Parameter	Description	Value
n	transformer turn ratio	1
L_r	resonant inductance	8.7 µH
C_r	resonant capacitance	147.0 nF
L_m	magnetizing inductance	25.3 µH
C_o	output filter capacitance	220 µF
f_r	resonance frequency	140.6 kHz
Z_r	characteristic impedance	7.7 Ω
V_i	input voltage	325…400 V
V_o	output voltage	250…500 V
I_o	output current	37.5 A
P_o	output power	15 kW

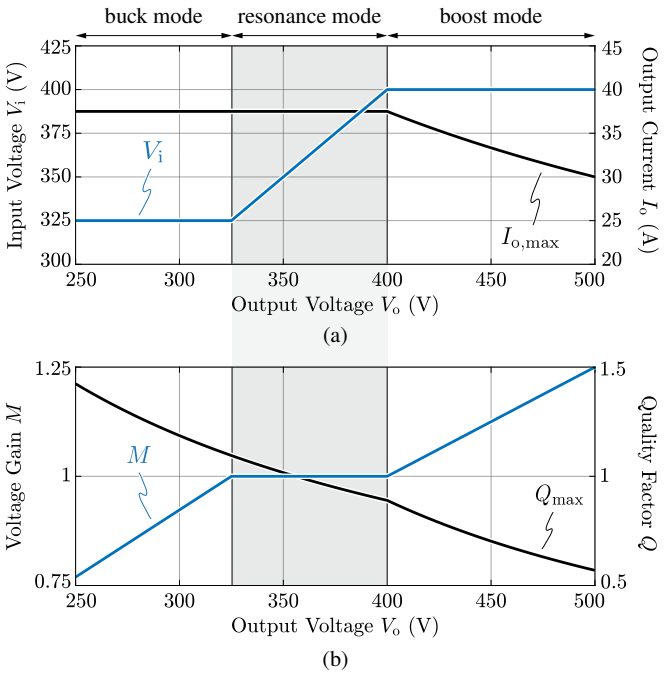

Fig. 15. Graphical representation of the LLC operating conditions and limits as functions of the output voltage V_o. (a) input voltage V_i and maximum output current $I_{o,max}$ (i.e., $I_{o,max} = 37.5$ A for $V_o \leq 400$ V, $I_{o,max} = P_{o,max}/V_o$ for $V_o > 400$ V), (b) voltage gain M and maximum quality factor Q_{max}. The interval where the active rectifier adjusts $V_i = V_o$ to maximize the LLC operation around resonance is highlighted in grey.

IV. Simulation and Experimental Results

The controller design procedure proposed in Section III is here validated on a 15 kW LLC converter for EV fast-charging applications, taking part in a modular and scalable structure presented in [9]. The specifications and the design operating region of the converter are reported in Table I. In particular, the input voltage of the LLC converter is adjusted during operation by the active rectifier stage [9], [38] in order to maximize the LLC operation at resonance (i.e., the highest efficiency point). Fig. 15 summarizes the LLC operating conditions and highlights the converter limits in terms of output current $I_{o,max}$ and quality factor Q_{max}, which directly affect the feasible region of the LUT reported in Fig. 13(c).

To validate the theoretical assumptions and the controller design methodology, the small-signal behavior of the output current i_o control loop is verified in simulation environment and both its steady-state and dynamical performances are experimentally assessed on a converter prototype. It is worth noting that the output voltage v_o control loop is not verified here for reasons of conciseness. Achieving high v_o control dynamics is not of primary importance in battery charging applications, as the voltage control loop actively operates only during start-up and constant-voltage battery charging. Furthermore, the v_o control loop structure is well known and does not feature fundamental differences with respect to conventional solutions employed in battery chargers, such as [34].

A. Simulation Results

The converter small-signal behavior is verified in circuit simulation, where the proposed control strategy is implemented by means of a custom C-code script in PLECS environment. To accurately simulate the discretized nature of the digital system, the control execution is triggered once every control period $T_s = 50\,\mu s$ (i.e., $f_s = 20\,kHz$), while the control outputs are updated at the following trigger instant.

To verify the tuning and performance consistency of the output current i_o controller, both the open-loop transfer function $G_{ol,i}$ and the closed-loop transfer function $G_{cl,i}$ are investigated in different operating conditions, namely buck mode, resonance mode and boost mode. In particular, the LUT extracted with TDA in Fig. 13(b) is employed, as it accurately represents the ideal LLC converter operation implemented in circuit simulation (i.e., without resistive terms). Moreover, to independently assess the small-signal response of the designed control loop, the feedforward contribution $f_{sw,ff}$ is disabled.

Several simulations are performed by setting sinusoidal references with different frequencies at the control input, measuring the system response and calculating its magnitude and phase. A DC offset is added to the i_o reference, in order to comply with the unidirectional nature of the LLC converter.

The results of this analysis are illustrated in Fig. 16 for different values of voltage gain M (i.e., from top to bottom $M \approx 0.77$, $M = 1$, $M = 1.25$) and quality factor Q (i.e., indistinguishable in the considered frequency range). The circuit simulation results are compared to their simplified analytical counterparts derived in Section III, i.e. considering the first-order plant approximation in (28) and the FHA-based expressions of $\partial M/\partial f_{sw}$ and $\partial Q/\partial f_{sw}$ in (20) and (21), respectively. It is observed that the simplified analytical models show a high-level of correspondence with circuit simulations over the full control frequency range, demonstrating the validity and accuracy of the proposed controller design/tuning procedure. Furthermore, Fig. 16 highlights the consistency of the open-loop cross-over frequency and phase margin with variable voltage gain M and quality factor Q, verifying the essential role of the proposed controller gain adaptation process in ensuring approximately constant control performance. It can be observed that a $-3\,dB$ closed-loop control bandwidth $f_{bw,-3dB} \approx 2$–$3\,kHz$ is obtained in all operating conditions.

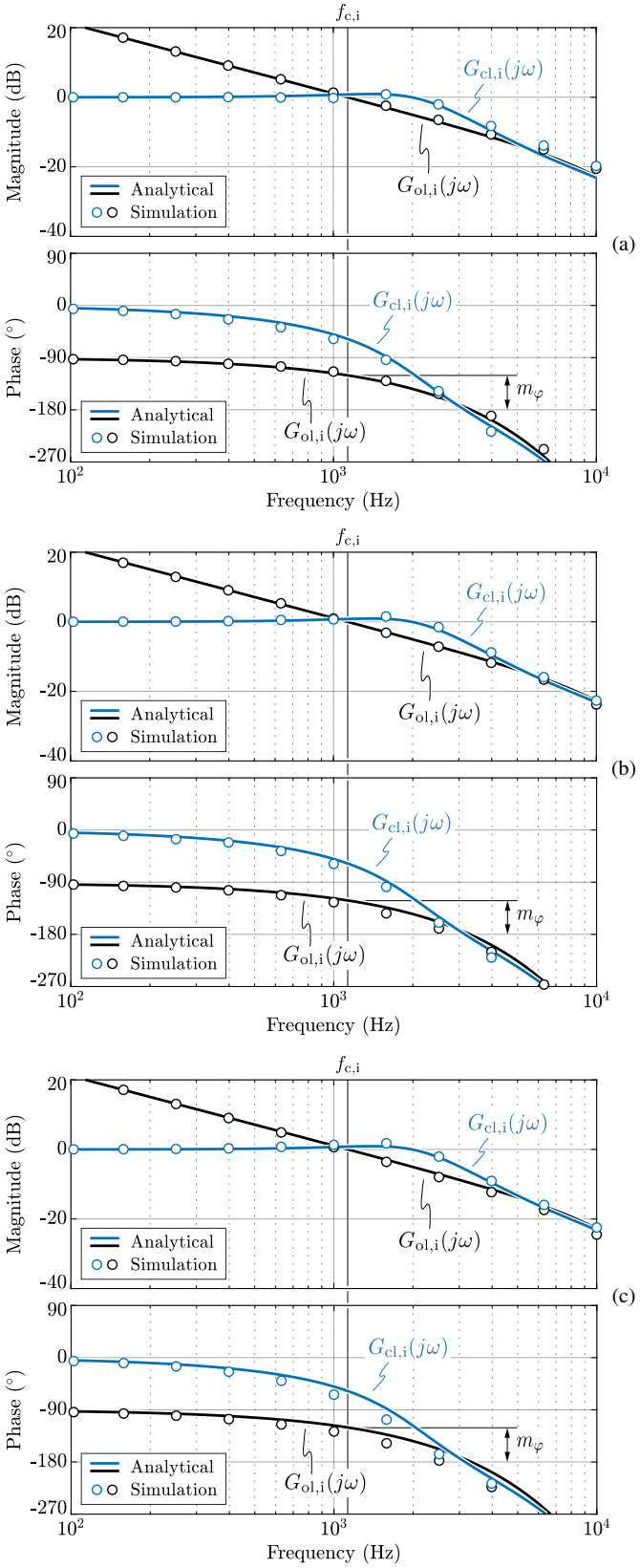

Fig. 16. Comparison between analytically derived and simulated open-loop transfer function $G_{ol,i}$ and closed-loop transfer function $G_{cl,i}$ in (a) buck mode (i.e., $V_i = 325\,V$, $V_o = 250\,V$), (b) resonance mode (i.e., $V_i = V_o = 325\,V$), and (c) boost mode (i.e., $V_i = 400\,V$, $V_o = 500\,V$). Thanks to the proposed gain adaptation of the controller, no visible influence of Q (i.e., I_o) on either analytical or simulated results is observed in the considered frequency range, therefore the results are only reported for $I_o = 20\,A$.

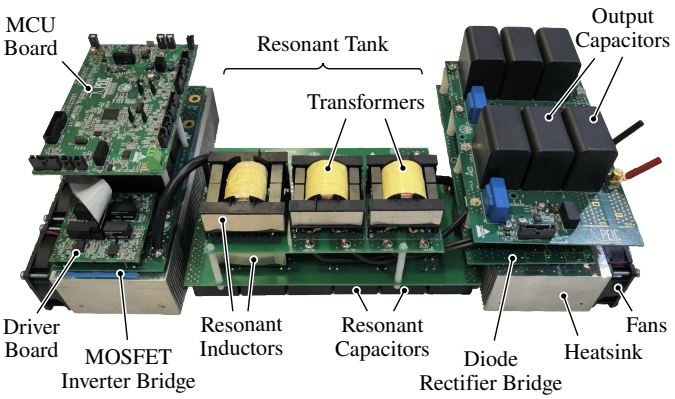

Fig. 17. Overview of the utilized 15 kW LLC converter prototype, described in detail in [9]. Since the boards are designed for two paralleled 15 kW modules, only half of the converter is utilized.

B. Experimental Results

The steady-state operation and the large-signal dynamical performance of the output current i_o controller are assessed on the 15 kW LLC converter prototype illustrated in Fig. 17. The circuit structure of this converter is unconventional, due to the adoption of two resonant inductors and two pairs of input-series/output-parallel connected transformers, as described in [9]. Nevertheless, from the control perspective, the prototype is equivalent to a traditional LLC converter with the parameters reported in Table I.

The converter closed-loop control is implemented on a STM32G474VE microcontroller unit (MCU) from ST Microelectronics, with an ISR running at $f_\mathrm{s} = 20\,\mathrm{kHz}$ to ensure sufficient calculation time for the dual-loop control. The corner frequency of the second order filter applied to i_o is placed at $f_\mathrm{f,i} = 25\,\mathrm{kHz}$, providing the necessary attenuation at the minimum switching frequency and negligible phase delay in the control loop feedback (i.e., $f_\mathrm{f,i} \gg f_\mathrm{c,i} \approx 1.1\,\mathrm{kHz}$). The 101x101 $f_\mathrm{sw}(M, Q)$ 2D LUT reported in Fig. 13(c) and the 101x1 $f_\mathrm{sw,min}(M)$ 1D LUT are stored in the MCU internal memory (i.e., 32 bit floating-point numbers, requiring a total of 41.2 kB of memory), allowing fast access to the data during the interpolation process. The PWM signals are generated by a sawtooth counter realized with a high-resolution timer unit. The MCU clock frequency is 170 MHz and the timer internal clock can be sped up 16 times, yielding a PWM resolution of 368 ps.

The experimental tests are performed using two independent bidirectional DC supplies operated in constant-voltage mode, respectively connected at the input and at the output of the converter. All measurements are carried out with a 500 MHz, 12-bit, 10 GS/s, 8-channel oscilloscope, employing isolated high-voltage differential probes for voltage measurements and high bandwidth current probes for current measurements.

Steady-State Operation

Some exemplary steady-state converter waveforms considering $i_\mathrm{o}^* = 30\,\mathrm{A}$ are reported in Fig. 18, including the input switched voltage v_inv, the primary-side transformer voltage v_t, the resonant tank current i_r, the output rectified current i_o and the battery-side current i_b. The waveforms are reported for (a) buck mode ($V_\mathrm{o} = 250\,\mathrm{V}$, $M \approx 0.77$, $f_\mathrm{sw} \approx 167\,\mathrm{kHz}$), (b) resonance mode ($V_\mathrm{o} = 315\,\mathrm{V}$, $M \approx 0.97$, $f_\mathrm{sw} \approx 140\,\mathrm{kHz}$), and (c) boost mode ($V_\mathrm{o} = 405\,\mathrm{V}$, $M \approx 1.25$, $f_\mathrm{sw} \approx 109\,\mathrm{kHz}$). All operating modes show that the LLC converter correctly operates with a phase lag between the primary switched voltage v_inv and the resonant tank current i_r, ensuring the zero-voltage switching (ZVS) operation of the primary MOSFET bridge-legs. It is observed that the closed-loop current controller ensures zero steady-state error in all operating modes, including buck and boost (i.e., when the plant does not behave as a pure integrator), as a result of the integral part of the PI regulator. Moreover, it is worth noting that the operation at resonance frequency (i.e., $f_\mathrm{sw} = f_\mathrm{r}$) does not take place at $M = 1$, but at slightly lower voltage gain values (i.e., $M \approx 0.97$ for $I_\mathrm{o} = 30\,\mathrm{A}$), as the system losses translate into an input-to-output voltage drop.

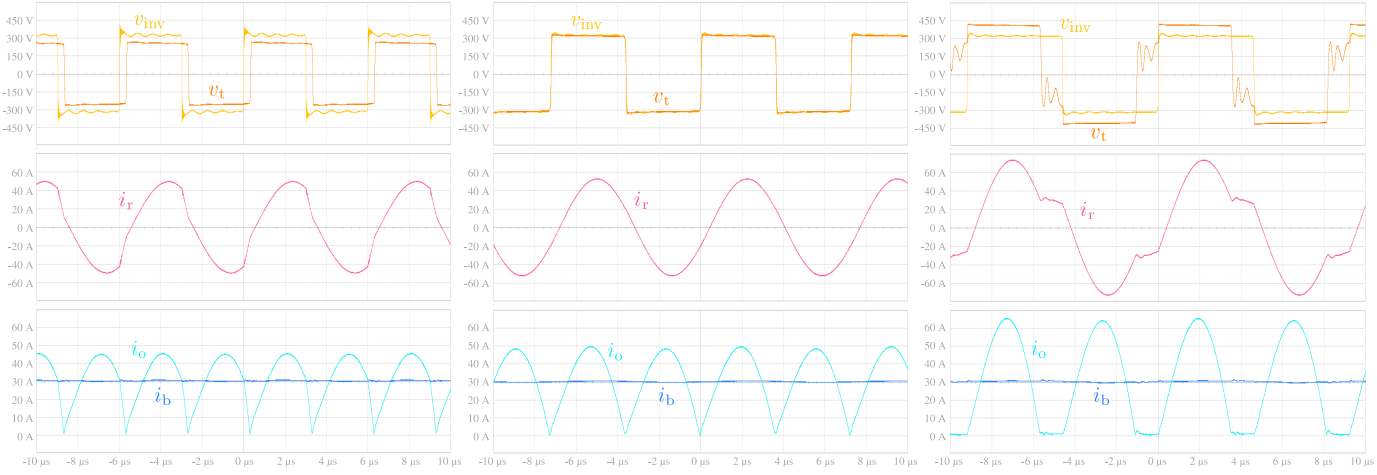

Fig. 18. Experimental converter waveforms at steady-state: input switched voltage v_inv, primary-side transformer voltage v_t, resonant tank current i_r, output rectified current i_o (i.e., obtained by taking the absolute value of the transformer secondary current) and battery-side current i_b. The waveforms are obtained for an input voltage value $V_\mathrm{i} = 325\,\mathrm{V}$ and a reference output current value $i_\mathrm{o}^* = 30\,\mathrm{A}$ while operating in (a) buck mode ($V_\mathrm{o} = 250\,\mathrm{V}$, $M \approx 0.77$, $f_\mathrm{sw} \approx 167\,\mathrm{kHz}$), (b) resonance mode ($V_\mathrm{o} = 315\,\mathrm{V}$, $M \approx 0.97$, $f_\mathrm{sw} \approx 140\,\mathrm{kHz}$), and (c) boost mode ($V_\mathrm{o} = 405\,\mathrm{V}$, $M \approx 1.25$, $f_\mathrm{sw} \approx 109\,\mathrm{kHz}$).

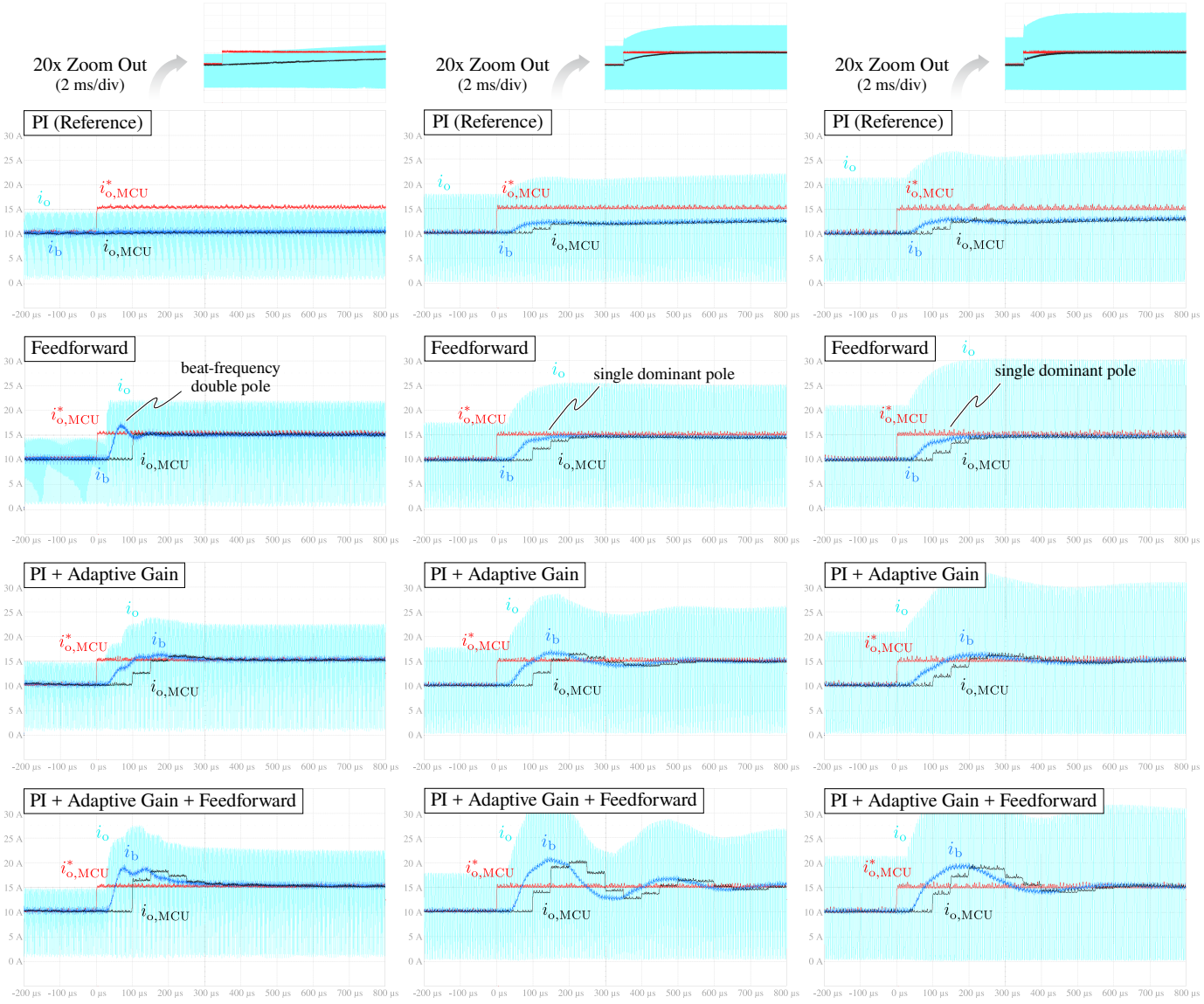

Fig. 19. Experimental reference step response of the output current control loop between $i_o = 10\,A$ and $i_o = 15\,A$. The waveforms of the rectifier output current i_o, the battery-side current i_b, the MCU reference current $i^*_{o,MCU}$ and the MCU sampled current $i_{o,MCU}$ are shown for $V_i = 325\,V$ in (a) buck mode ($V_o = 250\,V$, $M \approx 0.77$), (b) unity-gain mode ($V_o = 325\,V$, $M = 1$) and (c) boost mode ($V_o = 405\,V$, $M \approx 1.25$). $i^*_{o,MCU}$ and $i_{o,MCU}$ are measured at the output of two separate MCU digital-to-analog converters (DACs) with a 0–3.3 V scale, therefore they are properly rescaled. Four control strategies are compared, from top to bottom: *PI* (reference case), *Feedforward*, *PI + Adaptive Gain* and *PI + Adaptive Gain + Feedforward* (i.e., the adopted strategy).

Dynamical Operation

The dynamical performance of the output current control is verified by assessing (1) the response to a reference step, (2) the ability to follow a 150 Hz sinusoidal reference and (3) the rejection capability of a 150 Hz input voltage sinusoidal disturbance. In particular, to highlight the benefits of the complete control scheme of Fig. 11 (i.e., in the following referred to as *PI + Adaptive Gain + Feedforward*), several control solutions are compared.

1) Step Response: Fig. 19 shows the closed-loop control response to a current reference step from 10 A to 15 A in (a) buck mode ($V_o = 250\,V$, $M \approx 0.77$), (b) unity-gain mode ($V_o = 325\,V$, $M = 1$) and (c) boost mode ($V_o = 405\,V$, $M \approx 1.25$). The rectifier output current i_o, the battery-side current i_b, the MCU reference current $i^*_{o,MCU}$ and the MCU sampled current $i_{o,MCU}$ are reported. Both $i^*_{o,MCU}$ and $i_{o,MCU}$ are measured at the output of two separate MCU digital-to-analog converters (DACs) with a 0–3.3 V scale, therefore the measured signals are properly rescaled. It is observed that all responses feature a $T_s = 50\,\mu s$ discretization of the sampled current $i_{o,MCU}$ and a $2T_s$ delay between the $i^*_{o,MCU}$ reference step and the first $i_{o,MCU}$ current sample (i.e., due to discretized update of the DACs at the end of the control period). It is worth noting that, even though the battery-side current i_b seems to directly represent the mean value of the rectified current i_o, the real dynamics of the system should be directly observed from the envelope of i_o, as i_b is measured at the output of the filter capacitor C_o and thus includes a time delay.

The first control strategy is reported on top and represents the reference case (i.e., state-of-the-art). This strategy adopts a conventional PI regulator tuned to achieve the desired current control open-loop cross-over frequency $f_{\mathrm{c,i}} \approx 1.1\,\mathrm{kHz}$ with the methodology reported in [21], setting the PI zero to $f_{\mathrm{c,i}}/5$. Specifically, this controller design approach should ensure the desired controller bandwidth in resonance mode operation and lower dynamical performance in buck and boost modes, due to the non-adaptive controller gain. However, the results in (b) show that the target controller bandwidth is not achieved in resonance/unity-gain mode, as the response is much slower than expected. The main reason behind this discrepancy resides in the resistive nature of the real system, which does not behave as a pure integrator at the resonance frequency, as demonstrated by the experimental switching frequency LUT in Fig. 13(c). In fact, due to the first order low-pass filter behavior of the system, the controller tuning proposed in [21] is no longer effective. Furthermore, the absence of an adaptive controller gain leads to a large variation in the closed-loop dynamics, especially in buck mode operation, where the system open-loop gain drops significantly.

The second set of waveforms from the top shows the results obtained with the sole use of the feedforward term coming from the LUT interpolation. These waveforms provide a useful insight on the LLC system dynamics, as they highlight the open-loop system response to a switching frequency step. It is observed that the response in buck mode is substantially faster and less damped than in resonance and boost modes, as buck mode operation features an imaginary beat-frequency double pole that is located at higher frequency than the real dominant pole in the other two modes (cf. Fig. 8). Even though the LUT is very precise in the present situation, it must be noted that such an open-loop control strategy cannot ensure zero steady-state error in all conditions, mainly due to LUT inaccuracies and converter component tolerances. Therefore, the feedforward approach is typically complemented by an integral regulator with slow dynamical characteristics with the only aim of correcting the steady-state feedforward error. Anyhow, this integral regulator does not ensure a constant and/or controlled bandwidth, therefore this approach will not be considered for the following tests.

The third control strategy reproduces the schematic reported in Fig. 11 without implementing the feedforward term, therefore only exploiting the PI and the gain adaptation process. This strategy allows to verify the controller tuning and the consistent closed-loop bandwidth throughout the LLC operating region, decoupling the PI operation from the feedforward contribution. Even though the system small-signal steady-state gain changes by more than one order of magnitude between buck and boost modes, the experimental waveforms show that the output current step response remains mostly unaffected by the converter operating point. Moreover, the consistent rise-time $t_{\mathrm{r}} \approx 150\,\mu\mathrm{s}$ translates into a constant closed-loop bandwidth

$$f_{\mathrm{bw,\text{-}3dB}} \approx \frac{0.35}{t_{\mathrm{r}}} \tag{40}$$

of approximately $2.3\,\mathrm{kHz}$, closely matching the simulated transfer functions in Fig. 16.

Finally, the last set of waveforms is obtained with the complete control strategy reported in Fig. 11, i.e., adding the feedforward term at the output of the PI regulator with adaptive gain. It is observed that the step responses feature significantly higher overshoot and lower damping than in the previous case. The reason behind this is the overlap between the feedforward term and the proportional part of the PI regulator, as they both act instantaneously in correspondence of the reference step and cause an excessive switching frequency response, which generates the current overshoot and the subsequent oscillation. In general, all solutions featuring a high performance PI regulator together with a feedforward block are not suited for reference step changes, because of the mentioned reasons. Nevertheless, in battery charger applications reference step changes are not required, as the target charging current is typically ramped up/down with a finite slope and output current steps are unnecessary. Therefore, due to the combined action of feedforward and PI regulator with adaptive gain, this control strategy features the most promising dynamical performance, particularly needed for the disturbance rejection of high frequency components (e.g., input voltage oscillations).

2) Sinusoidal Reference Tracking: The control loop capability to track a large-signal sinusoidal reference is illustrated in Fig. 20, where the system response to a $150\,\mathrm{Hz}$, $10\,\mathrm{A}$ peak-to-peak current reference is reported. The resonant tank current i_{r}, the rectifier output current i_{o}, the battery-side current i_{b}, the MCU reference current $i^{*}_{\mathrm{o,MCU}}$ and the MCU sampled current $i_{\mathrm{o,MCU}}$ are shown. Also in this case, the control performance is assessed in three operating points (i.e., buck, resonance and boost modes) and adopting different control strategies, namely *PI*, *PI+Adaptive Gain* and *PI+Adaptive Gain+Feedforward*. It is immediately observed that the conventional *PI* control is not able to track the reference, as the real control loop bandwidth is much lower than the target value. In resonance and boost modes, this translates in substantial amplitude reduction and phase delay, while in buck mode the system appears to completely neglect the reference due to the large and uncompensated small-signal gain drop of the plant. These issues are addressed by the *PI + Adaptive Gain* control strategy, which closely follows the sinusoidal reference. However a noticeable phase shift is observed, as expected from the simulated closed-loop transfer functions in Fig. 16. Thanks to the added feedforward contribution, the *PI + Adaptive Gain + Feedforward* control strategy eliminates the phase shift, demonstrating enhanced dynamical performance.

3) Disturbance Rejection Capability: The last experimental tests assess the control loop capability to reject a large-signal sinusoidal disturbance applied to the input DC-link voltage V_{i}. Specifically, a $150\,\mathrm{Hz}$, $10\,\mathrm{V}$ peak-to-peak oscillation is superimposed to $V_{\mathrm{i}} = 325\,\mathrm{V}$ and a $15\,\mathrm{A}$ reference output current is targeted at steady-state. The sinusoidal input voltage disturbance emulates the typical DC-link mid-point voltage oscillation of three-phase three-level rectifiers connected to the $50\,\mathrm{Hz}$ European low-voltage grid [31] and thus assumes the specific LLC connection configuration described in [9], typically adopted in modular battery chargers. Nevertheless, a similar situation is also encountered in all single-phase dual-stage (i.e., AC/DC + DC/DC) battery chargers, where the power

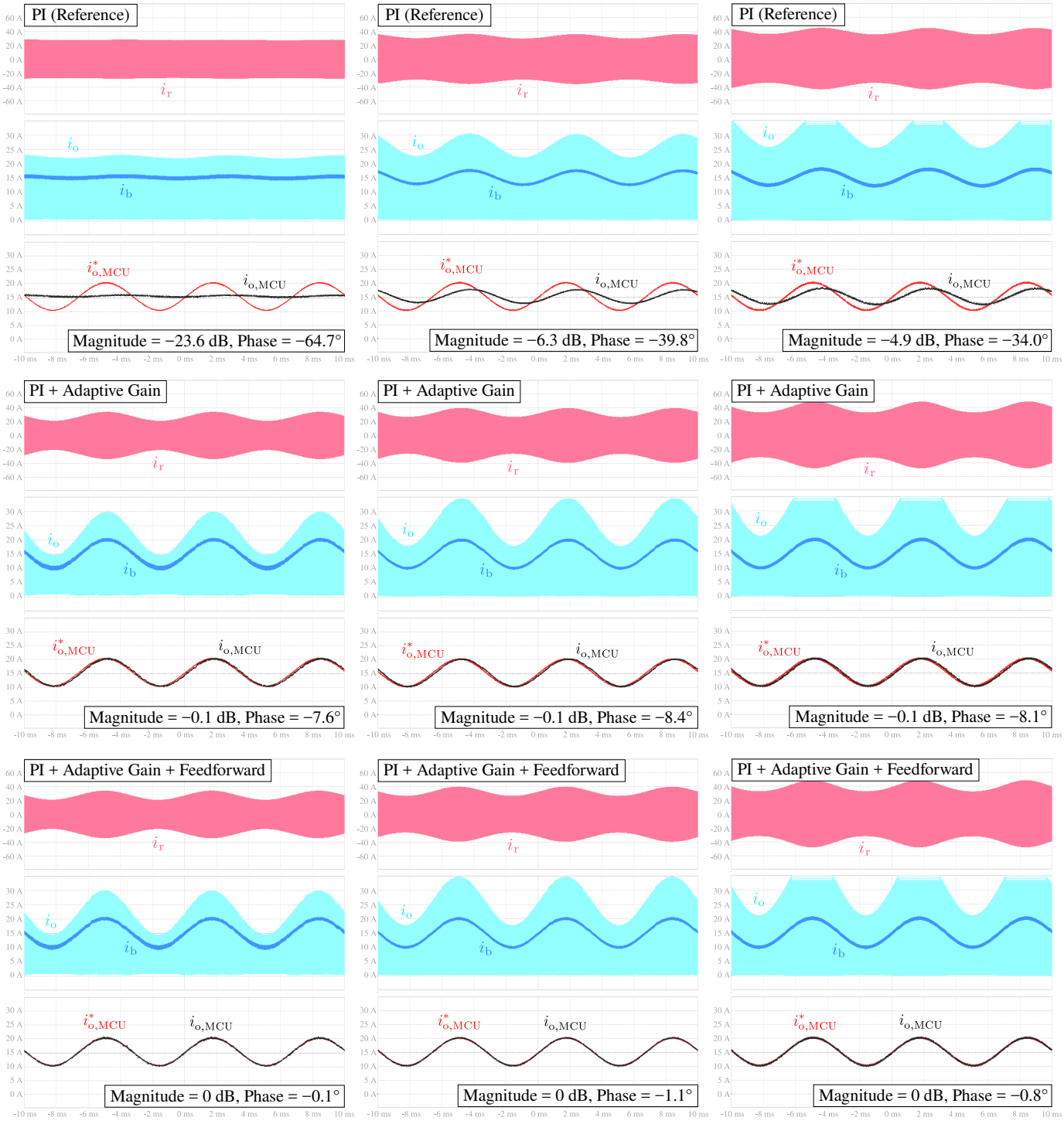

Fig. 20. Experimental steady-state response of the output current control loop to a 150 Hz, 10 A peak-to-peak sinusoidal reference. The waveforms of the resonant tank current i_m, the rectifier output current i_o, the battery-side current i_b, the MCU reference current $i^*_{o,MCU}$ and the MCU sampled current $i_{o,MCU}$ are shown for $V_i = 325$ V in (a) buck mode ($V_o = 250$ V, $M \approx 0.77$), (b) unity-gain mode ($V_o = 325$ V, $M = 1$) and (c) boost mode ($V_o = 405$ V, $M \approx 1.25$). $i^*_{o,MCU}$ and $i_{o,MCU}$ are measured at the output of two separate MCU digital-to-analog converters (DACs) with a 0–3.3 V scale, therefore they are properly rescaled. Three control strategies are compared, from top to bottom: *PI* (reference case), *PI + Adaptive Gain* and *PI + Adaptive Gain + Feedforward* (i.e., the adopted strategy). The magnitude and phase of the closed-loop response $i_{o,MCU}/i^*_{o,MCU}$ are indicated at the bottom of each figure.

factor correction (PFC) stage generates a voltage ripple at two times the grid frequency (i.e., 100 Hz or 120 Hz) at the input of the following DC/DC stage. Therefore, the proper rejection of the input voltage oscillation (i.e., the minimization of the induced output current ripple) is a fundamental requirement in battery charging applications and represents the most demanding control requirement for an LLC converter, due to its strongly non-linear behavior.

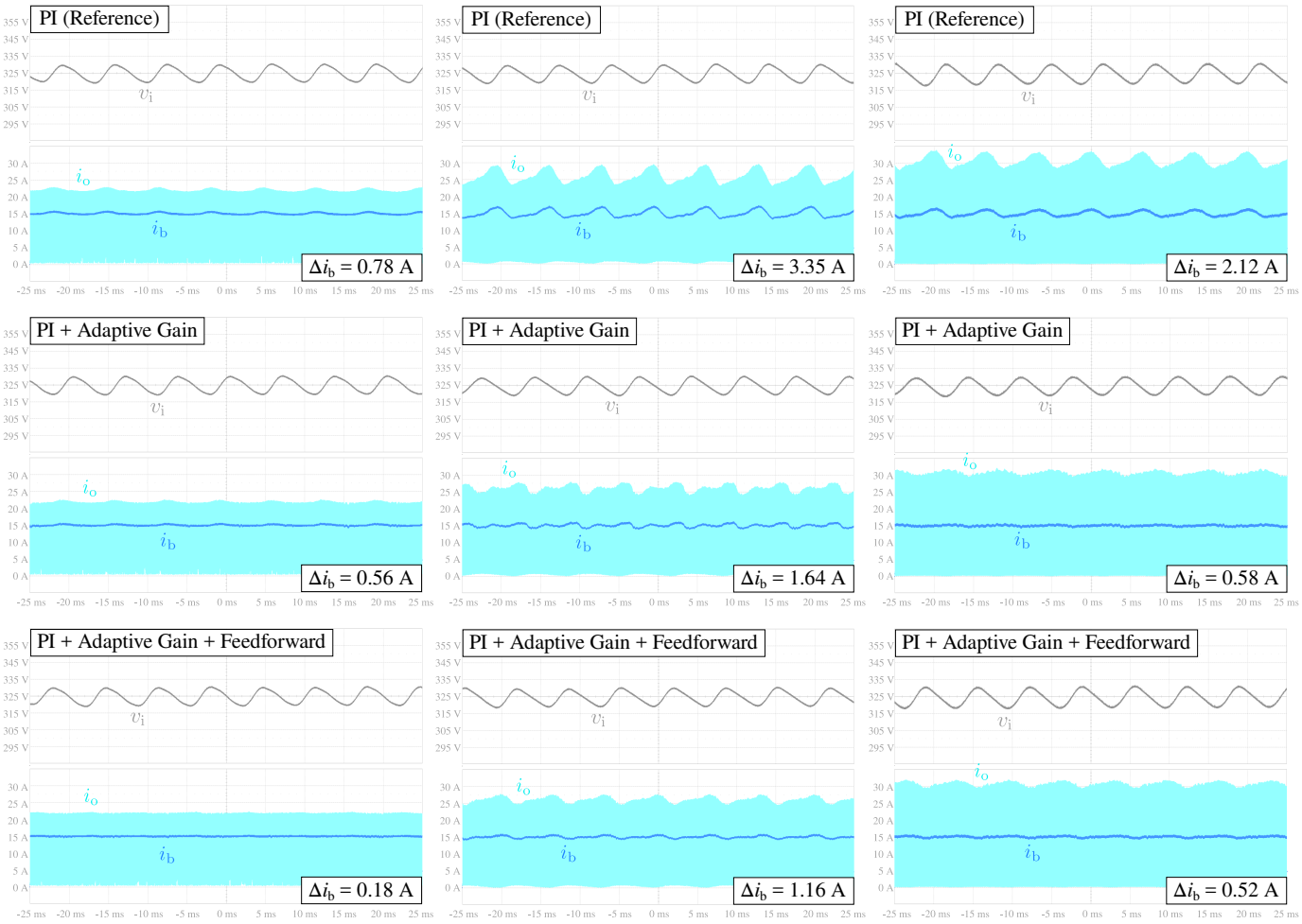

Fig. 21. Experimental steady-state response of the output current control loop to a 150 Hz, 10 V peak-to-peak input voltage pseudo-sinusoidal disturbance. The waveforms of the instantaneous input voltage v_i, the rectifier output current i_o and the battery-side current i_b are shown in (a) buck mode ($V_o = 250$ V, $M \approx 0.77$), (b) unity-gain mode ($V_o = 325$ V, $M \approx 1$) and (c) boost mode ($V_o = 405$ V, $M \approx 1.25$). Three control strategies are compared, from top to bottom: *PI* (reference case), *PI + Adaptive Gain* and *PI + Adaptive Gain + Feedforward* (i.e., the adopted strategy). The value of the battery-side peak-to-peak current ripple Δi_b is indicated at the bottom of each figure.

The results of these tests are illustrated in Fig. 21, where the instantaneous input voltage v_i, the rectifier output current i_o and the battery-side current i_b are shown in three operating points (i.e., buck, resonance and boost modes) and adopting different control strategies, namely *PI*, *PI + Adaptive Gain* and *PI + Adaptive Gain + Feedforward*. It is observed that in all cases the shape of v_i is visibly distorted, as the available DC power supply was not able to perfectly synthesize a 150 Hz sine waveform. Therefore, the v_i disturbance features higher order harmonics, which are substantially harder to reject by the closed-loop control. Nevertheless, the experimental results still provide a fair performance comparison among control strategies. The conventional *PI* strategy shows the worst overall rejection performance, due to the design bandwidth overestimation and the uncompensated small-signal gain variation of the plant. Better performance is achieved by the *PI + Adaptive Gain* control, which features a lower output current ripple as a result of the adaptive gain and the consistent control bandwidth over the complete LLC operating region. Finally, the *PI + Adaptive Gain + Feedforward* strategy demonstrates the best disturbance rejection capabilities, approximately eliminating the current ripple in buck and boost modes, while strongly reducing it around resonance operation. In particular, resonance operation represents the most challenging condition to reject the input voltage ripple, since the derivative $\partial Q/\partial M$ (i.e., proportional to the output current variation induced by the input voltage oscillation $\partial I_o/\partial V_i$) reaches its maximum, as attested by the slope of the iso-frequency lines in Fig. 13(c).

V. Conclusion

This work has presented a digital multi-loop control strategy for LLC resonant converters, ensuring constant control bandwidth and excellent disturbance rejection across the complete converter operating range (i.e., variable load and voltage gain).

A novel simplified dual first order small-signal model of the LLC converter has been derived from the well-known seventh order model, aiming to provide a straightforward tool for the design of the closed-loop controllers. Therefore, a dual-loop control scheme consisting of an outer voltage loop and an inner current loop has been designed and a complete (analytical)

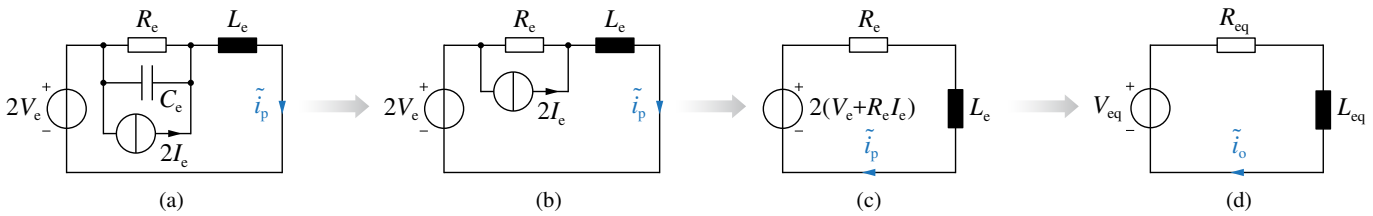

Fig. 22. Overview of the step-by-step simplification process from the equivalent circuit of Fig. 4(a) to the equivalent circuit of Fig. 5(a).

tuning procedure for both controllers has been described. In particular, the non-linear behavior of the frequency-to-current transfer function has been counteracted by a real-time controller gain adaptation process ensuring constant control bandwidth. To achieve best compensation accuracy, the adaptive gain values have been derived from a static switching frequency look-up table (LUT) obtained by experimental characterization of the converter. Moreover, the steady-state switching frequency value has been fed forward at the output of the current loop regulator to further enhance the system dynamical performance.

The effectiveness of the proposed control strategy has been verified both in simulation environment and experimentally on a $15\,\mathrm{kW}$ converter prototype, assessing for the first time the reference step response, the sinusoidal reference tracking ability and the input DC-link voltage ripple rejection degree of the current control loop. The results have demonstrated the quasi-constant closed-loop bandwidth of the proposed control strategy and its superior dynamical performance with respect to a state-of-the-art solution based on a PI regulator.

As a final remark, even though the proposed control strategy has been developed for electric vehicle battery chargers, it may as well provide significant benefits in all those applications requiring fast and tight output current and/or voltage regulation.

Appendix A
Dual 1st Order Model Derivation

The proposed dual first order LLC small-signal model is directly derived from the third order model described in [24] and reported in equivalent circuit form in Fig. 4. Since the DC subsystem remains unaffected by the simplifications, this section only focuses on the AC subsystem.

Assuming a complete decoupling between AC and DC subsystems (cf. Section II), the voltage source related to $\tilde{v}_\mathrm{o}$ in Fig. 4(a) can be disregarded, obtaining the equivalent circuit of Fig. 22(a). Notably, since the original circuit in [24] is derived for a half-bridge LLC converter, the voltage source $V_\mathrm{e}=2\pi K_\mathrm{d}\tilde{f}_\mathrm{sw}$ and the current source $I_\mathrm{e}=2\pi G_\mathrm{d}\tilde{f}_\mathrm{sw}$ (i.e., expressions reported in [24]) are here multiplied by 2, due to the considered full-bridge implementation of the converter. Neglecting the beat-frequency double pole dynamics in buck mode operation (cf. Section II-C), the equivalent capacitor C_e can be disregarded, obtaining the equivalent circuit of Fig. 22(b). By applying the Thevenin theorem to the current source, the circuit in Fig. 22(c) is derived. Since the aim of the AC subsystem model is to link the small-signal frequency perturbation $\tilde{f}_\mathrm{sw}$ (i.e., contained in V_e and I_e) to the output current variation $\tilde{i}_\mathrm{o}$, the equivalent circuit components in Fig. 22(c) must be modified according to the equivalent transformer ratio $i_\mathrm{p}/i_\mathrm{o}=\pi/2n$. Additionally, to obtain more compact expressions (cf. Section II-C), all circuit component values are divided by 2 (i.e., leaving unaffected the relation between $\tilde{f}_\mathrm{sw}$ and $\tilde{i}_\mathrm{o}$). Therefore, the equivalent circuit of Fig. 22(d) is obtained, where:

$$V_\mathrm{eq}=\frac{\pi}{2n}\left(V_\mathrm{e}+R_\mathrm{e}I_\mathrm{e}\right),\quad R_\mathrm{eq}=\frac{\pi^2}{8n^2}R_\mathrm{e},\quad L_\mathrm{eq}=\frac{\pi^2}{8n^2}L_\mathrm{e}. \tag{41}$$

Appendix B
Look-Up Table (LUT) Extraction

The same experimental setup described in Section IV is used to extract both the $f_\mathrm{sw}(M,Q)$ 2D LUT and the $f_\mathrm{sw,min}(M)$ 1D LUT, required by the proposed control scheme reported in Fig. 11. In particular, an automatized extraction procedure has been developed, exploiting MATLAB® environment to communicate with the DC supplies and the MCU.

Fig. 23(a) shows the schematic of the implemented control strategy for the LUT extraction, where a fixed reference input voltage $V_\mathrm{i}^*=325\,\mathrm{V}$ is assumed for the whole procedure. Each LUT point is defined by a reference value pair (M^*,Q^*) with a sequential index k, which identifies the element number starting from the lower-left corner of the LUT (i.e., $M=M_\mathrm{min}$, $Q=Q_\mathrm{min}$), as illustrated in Fig. 23(b). All references are provided through the MATLAB® interface. Specifically, the reference input voltage V_i^* is directly sent to the input DC supply, the reference voltage gain M^* is translated into and equivalent reference output voltage value V_o^* and sent to both the output DC supply and the MCU, and the reference quality factor Q^* is directly sent to the MCU. In the present case, the extraction procedure targets a 101x101 2D LUT and a 101x1 1D LUT, with $0.75\leq M^*\leq 1.25$ and $0\leq Q^*\leq 1.5$. In particular, the value of Q^* is saturated to the maximum allowed value $Q_\mathrm{max}(M)$ described in Section IV and illustrated in Fig. 15(b), so that no LUT points located outside the LLC operating region are extracted.

Once the MCU receives the reference quality factor value Q^*, this is directly translated into a reference i_o^* for the current control loop. In this case, however, the control loop is simplified with respect to Fig. 11, as the required LUTs are still not available and the dynamical control performance is not of interest. Therefore, a purely integral regulator with a small gain k_I is adopted, featuring a slow but stable response and ensuring zero steady-state error (i.e., the primary goal of the controller). In general, the maximum switching frequency $f_\mathrm{sw,max}=250\,\mathrm{kHz}$ should be fed forward at the output of the regulator, so that the converter always operates in the stable (i.e., inductive) region. Nevertheless, to speed up the transient, the last switching frequency value $f_\mathrm{sw}[k-1]$ can be

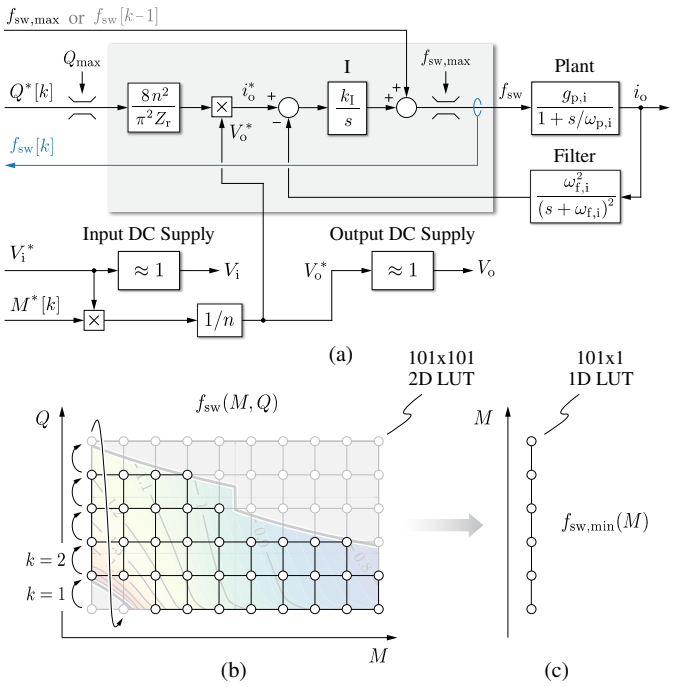

Fig. 23. (a) detailed schematic of the implemented LUT extraction procedure (i.e., MCU digital controller indicated with grey background), (b) $f_{sw}(M,Q)$ 2D LUT with highlight of the extraction sequence, (c) $f_{sw,min}(M)$ 1D LUT.

fed forward, leaving a substantially lower frequency error to be addressed by the integral regulator. In all cases, the reference output frequency is saturated to $f_{sw,max}$ and, once the specified time interval is over (i.e., 50 ms in the present case) the final switching frequency value is stored as $f_{sw}[k]$.

Depending on the total number of LUT elements, on the controller transient time and on the time allocated for the communication of the results, the 2D LUT extraction time can vary widely. In the present case, the overall time required for the complete LUT extraction was less than 1 hour, being the total number of LUT points ≈ 6700 (i.e., lower than 101x101 due to the Q_{max} limit) and the total time allocated to a single point ≈ 0.5 s (i.e., including communication).

Once the $f_{sw}(M,Q)$ 2D LUT is obtained, the $f_{sw,min}(M)$ 1D LUT can be directly extracted by identifying the minimum switching frequency value for each value of M, found in correspondence of $Q = Q_{max}(M)$ (i.e., the upper limit of the 2D LUT).

As a final remark, it is worth noting that, even though the 2D LUT is extracted assuming a single value of $V_i = 325$ V, the $f_{sw}(M,Q)$ values can be considered approximately independent of V_i and have broad applicability. In fact, the main V_i-dependent phenomena affecting the value of $f_{sw}(M,Q)$ are the converter losses, which generate an input-to-output voltage drop and thus affect the real converter voltage gain M. However, since the M value is in direct proportion with the converter efficiency (e.g., a 3 % efficiency drop translates into a ≈ 3 % gain drop), only the V_i impact on efficiency affects the $f_{sw}(M,Q)$ LUT. Therefore, as long as the ratio between losses and transferred power remains approximately unchanged with V_i (i.e., typically valid when V_i varies within a limited range), the extracted LUT maintains a high level of accuracy.

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