Doctoral Dissertation
Doctoral Program in Physics (34.th cycle)

The deep *Al*-based JTE

Development and industrialization of a novel termination design for high-power semiconductor devices

Abstract & Extended Summary

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Summary

Abstract:

Fast Recovery Epitaxial Diodes (FRED) are a class of high-voltage ultrafast rectifiers that have gained wide acceptance during the last few years due to their low reverse recovery loss, forward voltage drop, and leakage current characteristics, which make these devices attractive for disparate power electronics applications. To withstand the competition of wide bandgap semiconductors and to face the increasing demand for raw material availability, FRED technology significant progress over the past decade has dealt with the reduction of chip size to increase power capacity. While the rectifier forward bias performances directly involve a proper optimization of the active area, the design of the termination region is strictly connected to the device voltage handling capability and a proper layout can guarantee a greater efficiency with a lower silicon consumption. This thesis project aims to provide a thorough framework for the design, development, and release in production of a novel high-voltage silicon power diode termination structure that re-adapts the technology scaling trend ruled by Moore's law to the discrete branch of electronic devices.

The deep aluminium-based junction termination extension is identified as a manufacturable concept that is analysed in detail. The structure design optimization via TCAD finite element method simulation and the development of a process flow for the device fabrication in a cleanroom environment are therefore presented from both a theoretical and practical point of view. The prototype structural and electrical characterizations allow a thorough understanding of the physical foundations behind its working principles, while an accurate parametric study provides predictive models consisting in the device characteristics empirical forecast in case of deviations from the optimal set of input data. As ultimate accomplishment, the novel 1.2kV, 1A rated rectifier family would allow the industrialization of the smallest planar termination region that promises up to the mark electrical performances.

Extended Summary:

Power electronics is a complex and interdisciplinary technology that allows humankind to control the flow of electrical current from sources to loads. Power electronic systems are mainly based on semiconductor devices. Among them, silicon power diodes represent the simplest electronic component to control the direction of the current flow. Therefore, a clear understanding of their working principles can be considered essential for the physical interpretation of more advanced devices. In particular, power rectifiers main attractiveness derives from their ability to switch from the "on-state", a condition for which the current can ideally flow without losses, to the "off-state", a condition for which the current is ideally blocked without leakages (Fig. 1).

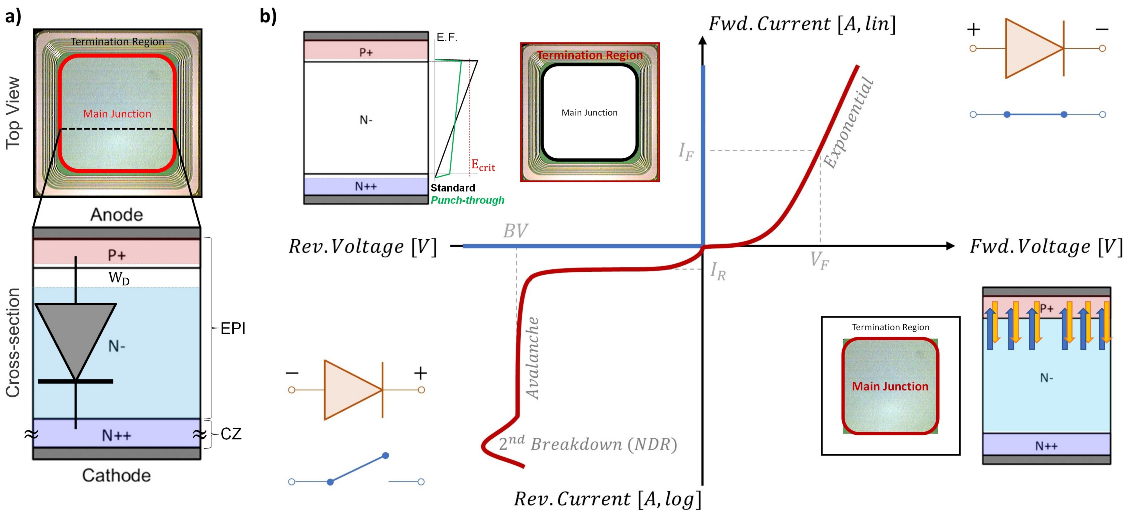


Figure 1: **a)** typical power rectifier top view and schematized cross-section of the P-i-N structure. **b)** comparison of the ideal (blue) and actual (red) diode IV characteristic. The main junction design is directly responsible for the device forward bias performances (V_F and I_{nom}). On the other hand, for a constant silicon substrate specification the termination region critically influences the reverse bias capability (BV and I_R).

Due to their pervasiveness in a huge variety of applications, from communication technologies to transportation, from industrial to medical sectors, going through computational or consumer tools, power semiconductor devices have a great impact on the world's economy and play a key role in terms of energy-saving and efficiency. In this view, the current main trend in power systems deals with the reduction of chip size to increase power capacity while improving silicon consumption. These advancements are strictly correlated to technology scaling. Referring to silicon power diodes, this goal can be achieved by optimizing the design of the device periphery or *termination region*. While the rectifier application performances are mainly governed by its nominal current, forward voltage drop, and duration of the recovery transient, directly involving a proper optimization of the *active area*, the design of the termination area is strictly connected to the device voltage handling capability and a proper layout can guarantee a greater efficiency with a lower silicon consumption.

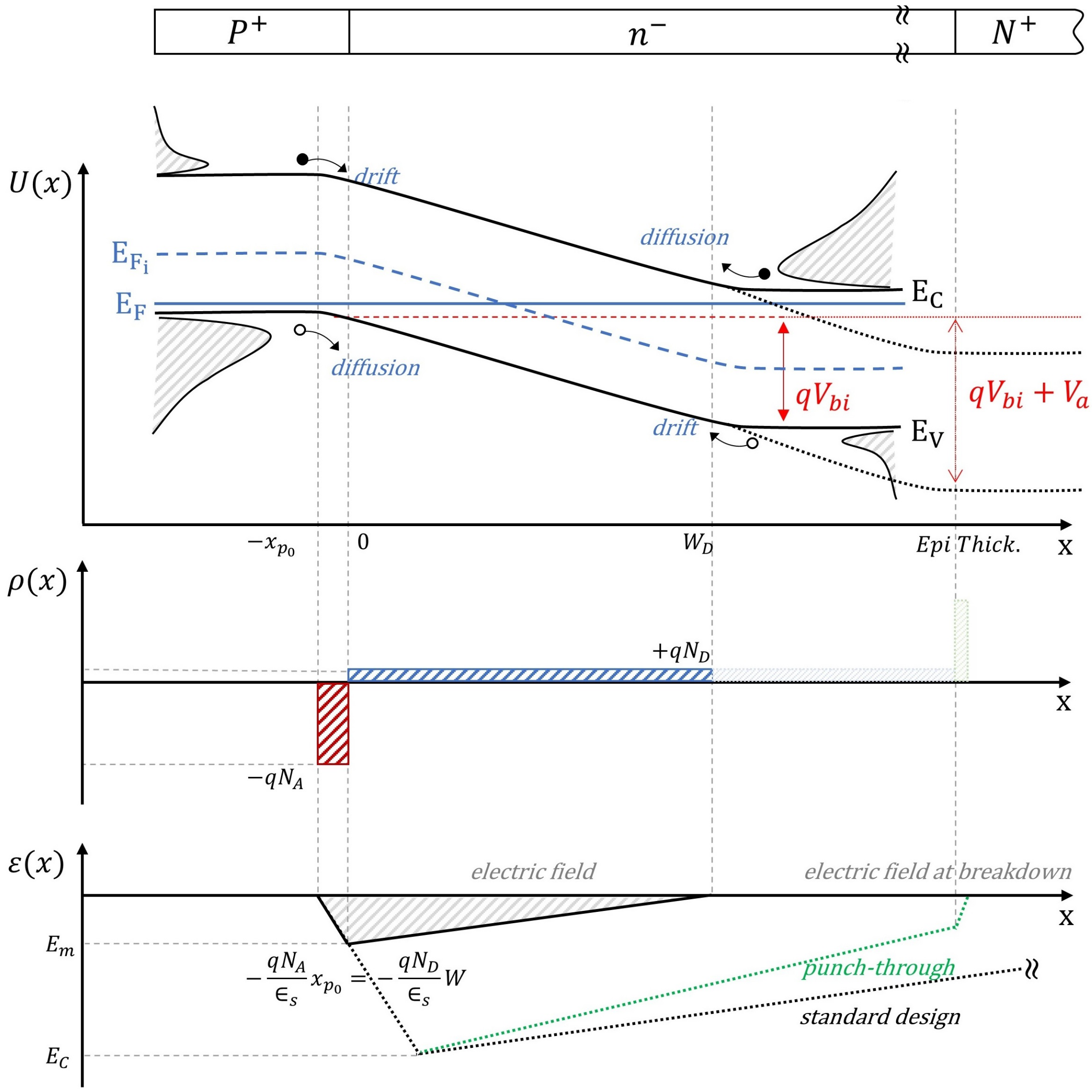
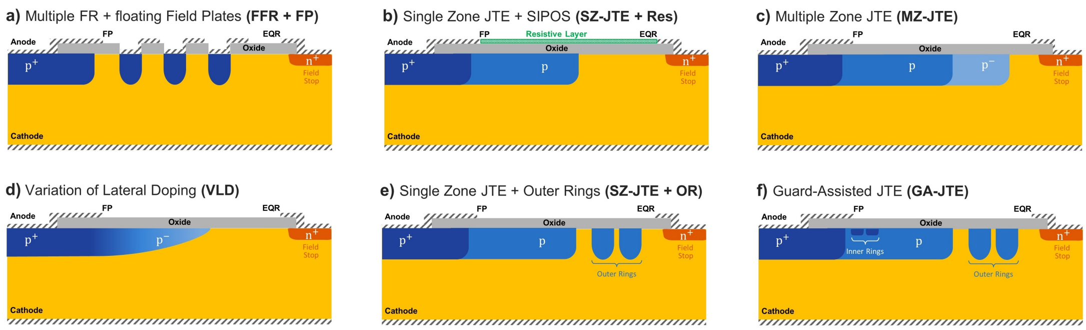


Figure 2: P-i-N Diode energy band diagram, charge density and electric field distributions at equilibrium and reverse bias condition. It is worth noticing the electric field different shape at breakdown for a standard and punch-thorugh design.

This thesis project aims to provide a thorough framework for the design, development, and release in production of a novel high-voltage silicon power diode termination structure. All the relevant aspects needed to carry out the project are divided into three main chapters:

Chapter 1 briefly recalls the mathematical model for semiconductor materials, which allows the physical interpretation of the P-i-N diode working principle (Fig. 2). A detailed review of the avalanche breakdown mechanism taking place within a *p*-*n* junction highlights the necessity for the adoption of dedicated design solutions for the periphery area of power devices. The state-of-the-art termination structures are therefore analysed, and their performances compared (Fig. 3).



Termination Type	Efficiency (BV/BV_{pp})	Design Layout	Manufacturability (Industrial level)	Avalanche Robustness	Silicon Consumption
Multiple FFR + Field Plates	90% - 95%	+	+++	+	+
Single Zone JTE + Resistive Layer	90% - 95%	++	++	++	++
Multiple Zone JTE	> 99%	++	+	+++	++
Variation of Lateral Doping	98%	++	++	+++	++
Single Zone JTE + Outer Rings	95% - 98%	+	++	++	++
Guard-Assisted JTE	95% - 98%	+	++	++	++
Deep Trench	> 99%	+++	+	+	+++

Figure 3: Hybrid termination structures and performance comparison.

Chapter 2 opens with an overview of the limitations of current technologies and sheds a clear light on the ideal solution. The *deep aluminium-based junction termination extension* is identified as a manufacturable alternative and analysed in detail (Fig. 4). The structure design optimization via TCAD Finite Element simulation (Fig. 5) and the development of a process flow for the device fabrication in a clean-room environment are discussed.

Chapter 3 reports the structural and electrical characterization of the prototypes. A benchmark study compares the devices performance while the results

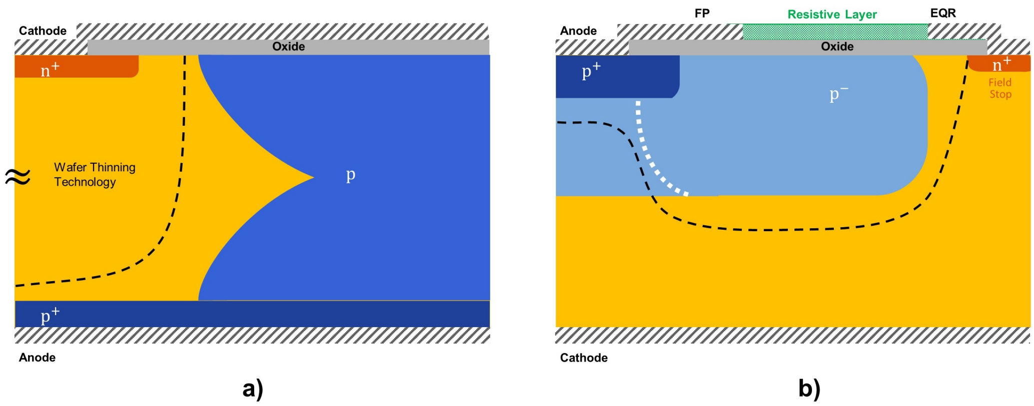


Figure 4: Illustration of **a)** the manucturing implementation of a concave junction, and **b)** the deep JTE feasible alternative structure.

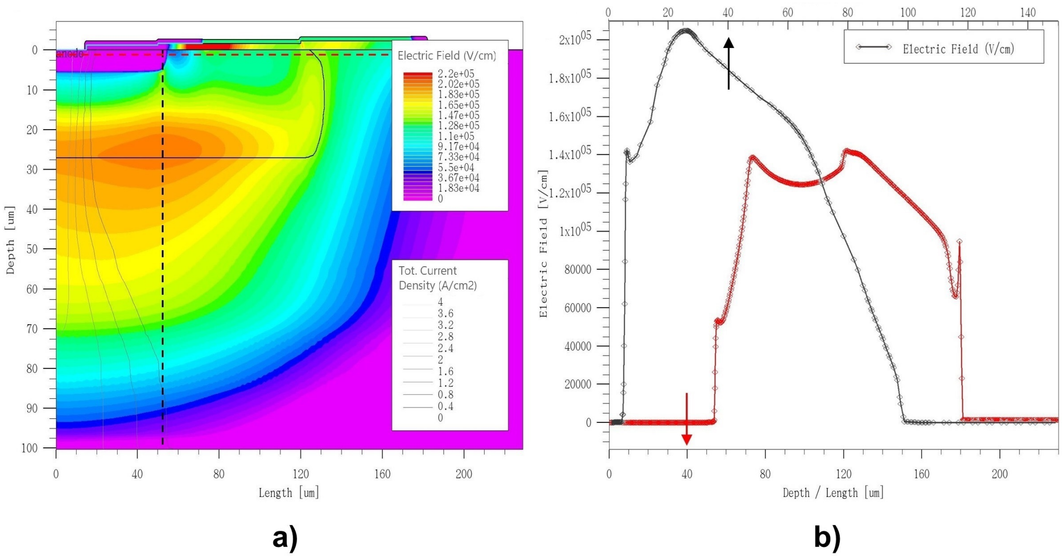


Figure 5: **a)** JTE RESURF contour plot for electric field and total current density distibutions at breakdown. **b)** Electric field cutline along the device width (red line, SiO_2/Si interface), and depth (black line, main junction edge).

are physically interpreted. Thorough statistical data analysis allows the predictive modelling of the so-realized novel type of 1.2kV, 1A rated silicon power diodes family. Finally, a look forward toward the next-generation devices and computational tools concludes the manuscript.

A "lean" methodology will outline the faithful investigation of the procedures that drove the project development from its early stages to the release in production, which allow the hosting institution VISHAY Semiconductor Italiana S.p.A. to break into a rapidly expanding segment of the market while following the state-of-the-art trends of power semiconductor electronics (Fig. 6).

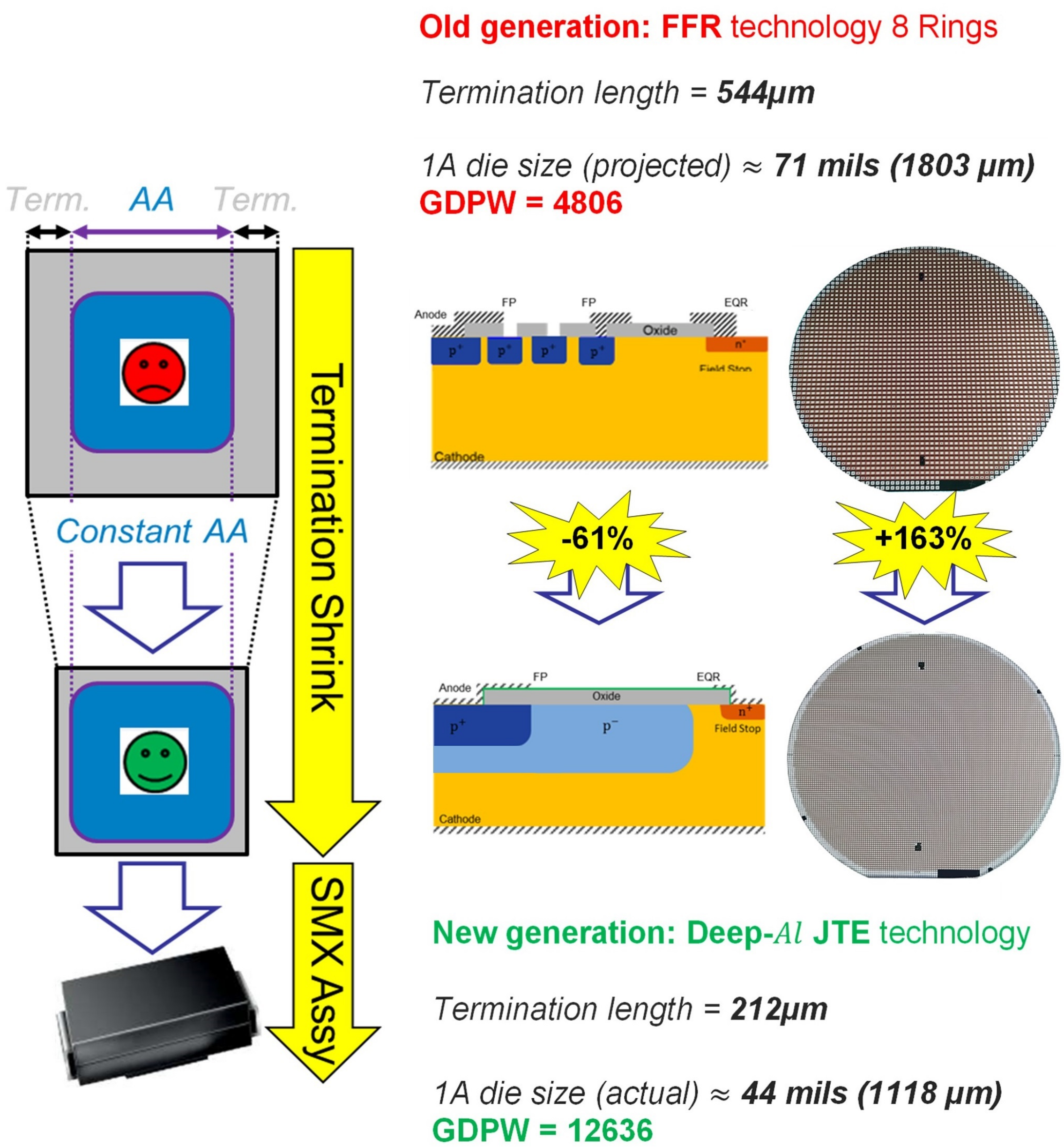


Figure 6: Illustration of the project purposes and summary of the improvements to previous generations of HV silicon power diodes.

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