Doctoral Dissertation
Doctoral Program in Electrical Engineering (34th cycle)

A novel fully depleted monolithic active CMOS microstrip sensor

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December 25, 2021

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Turin, December 25, 2021

Summary

Romantically speaking, sensors are the way experiments see the universe while, the electronics, the way they can process and understand it. In recent years the complexity and performance of integrated circuits adopted for sensing purposes has increased at an amazing pace. The commercial adoption of monolithic and hybrid pixels has led the scientific community to always find new solutions to improve the design of sensors and electronics while keeping the costs and power dissipation of the devices under control.

Monolithic devices, differently from traditional sensor/electronics couples are the perfect candidates for experiments requiring large area detectors while keeping production costs to a bare minimum. This is due to their intrinsically low material budget and to a decreased number of steps required for production compared to conventional or hybrid sensors.

This thesis presents the research and development of a custom fully depleted monolithic active CMOS sensor produced within the ARCADIA collaboration. In particular, through a close contact between Italian Universities and the INFN (Istituto Nazionale di Fisica Nucleare), the design, simulation and production of a novel active monolithic microstrip detector has been possible.

A set of evaluation structures, both passive and active, has been experimentally tested via electrical, radiation and particle characterization. The results are shown within this thesis proving full device depletion and a correct sensor to electronics monolithic coupling.

The electronics schematic and layout design of a configurable readout IC chip, ASTRA, are discussed. ASTRA (Adapatable Space sTrips Readout ASIC) features configurable gain, peaking time and readout architecture. This configurability makes it a good candidate for readout of commercially available microstrip sensors and also for adoption with active monolithic strip sensors.

Concluding, theoretical studies of the input capacitance and electronic simulation results are shown in the final chapter proving a correct channel functionality and programmability.

*Dedicated to my family
and friends*

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Chapter 1

Monolithic active sensors

Great advances in the electronics field have increased the adoption of silicon detectors in High Energy Physics (HEP) experiments. In particular, Complementary Metal-Oxide Semiconductors (CMOS) have seen a great shrinkage in size and, in turn, an increase in complexity per unit area.

An implication of smaller size is the production of detectors with higher granularity and more complexity in signal processing in smaller areas. Furthermore, following Moore's law, the cost per transistor, which is proportional to the transistor node (figure 1.1), has greatly decreased in the last few decades rendering silicon detectors extremely convenient also for large area detectors. [52, 69, 53] This is of paramount importance for future particle detectors which will require a great surface coverage with a high granularity for vertex reconstruction [18, 80].
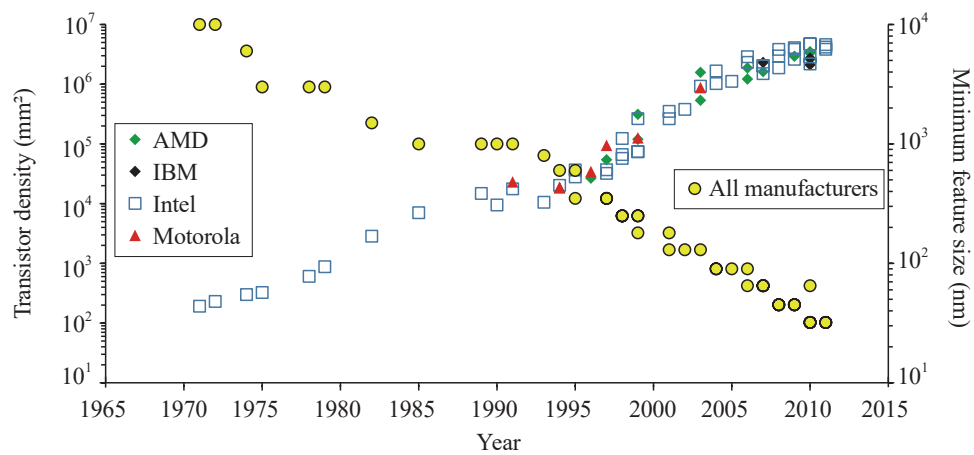
Figure 1.1: Reduction of transistor node (gate length) and increase in transistor density in microprocessors over time [28].

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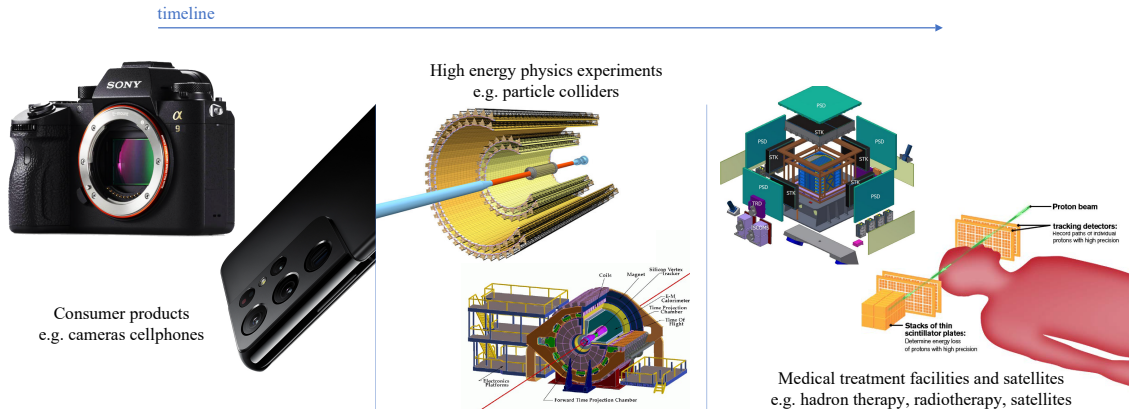
Figure 1.2: Timeline of future MAPS developments. In the *past* MAPS have been adopted mainly in CMOS image sensors in the commercial field. *Presently*, MAPS have been mounted on the STAR and ALICE vertex detectors and are being used in favor of hybrid active pixel sensors thanks to their low material budget. In the *future* we can envision micro-satellites and detectors for space applications adopting MAPS in order to reduce possible mechanical faults and the payload for space exploration. Also, remaining on Earth, radio- and hadron therapy will embrace the adoption of MAPS thanks to the possibility of having extra thin active sensor layers for beam localization.

In order to address the need for high granularity, two different technologies can be adopted. The first one adopts hybrid pixels, where a device comprises two different layers, one to detect and one to amplify the signal from radiation or impinging particles. The first layer is a silicon sensor used as sensitive volume while the second layer includes the CMOS electronics for the signal processing and readout. The separation between the sensor and the ASIC (Application Specific Integrated Circuit) implies the possibility of developing the layers using different technologies and materials. This leads to a good degree of device optimization [10]. The second technology adopts one single substrate for both the sensor and the electronics. Devices produced with this technique are called Monolithic Active Pixel Sensors (MAPS) [73, 75].

Considering the adoption of a single substrate to fabricate the detector, MAPS are much cheaper than hybrid pixels implying a great interest for HEP applications requiring large active areas. Nonetheless, hybrid active pixels sensors (HAPS) have been historically preferred due to their higher degree of customization and inherited performance. To reduce the performance gap, various R&D companies and laboratories are working on improving MAPS technologies to make them the mainstream devices adopted in future experiments. A timeline showing the progress

of MAPS is shown in figure 1.2. The greatest focus is on enabling full thickness (epitaxial layer or bulk) depletion. The ability to fully deplete the sensor would lead to a high radiation hardness, a higher signal to noise ratio per power dissipated and drift charge collection. Furthermore, the adoption of thick depleted substrates can be of great interest in X-ray imaging for medical purposes.

In cases where an extremely low power budget is fundamental, microstrips are adopted in place of pixels. Microstrips can either be a set of single strips of collecting electrodes or an arrangement of pixels connected along a single direction. This arrangement implies a one-dimensional particle localization, but with a lower processing complexity. Nevertheless, a set of thin microstrips planes can yield a precise x-y particle localization while keeping power consumption below the corresponding power dissipated by pixel arrays of the same pitch. Historically, a drive to reduce stray capacitances has led to the inclusion of parts of the front-end electronics onto the microstrip sensor wafer.

This chapter includes an overview of the state of the art in monolithic sensors and monolithic microstrips.

1.1   State of the art technologies
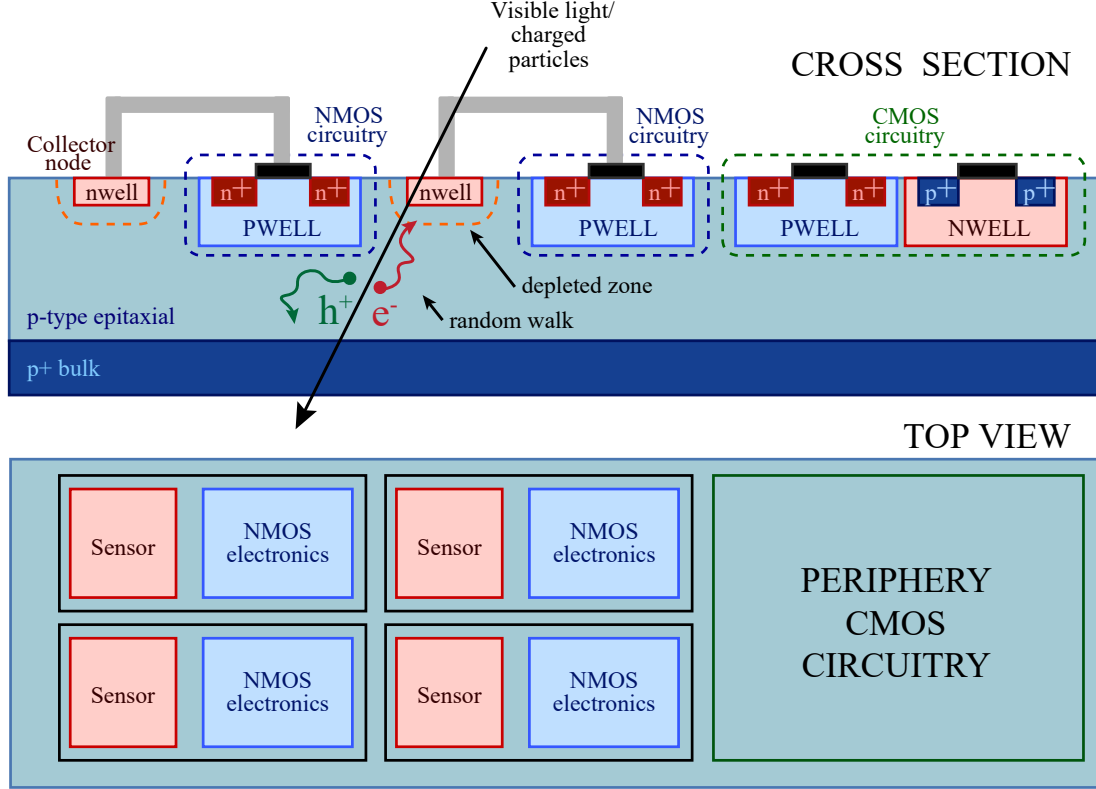
Figure 1.3: Illustration of conventional MAPS design. Visible light or charged particles cross the sensing volume generating charged couples of electrons and holes which are collected by the top electrodes. In conventional MAPS most circuitry is designed adopting N-JFET or NMOS technology with the complementary devices located at the edge of the device.

Conventional MAPS are detectors which adopt a single silicon wafer layer capable of particle or radiation detection and signal processing as seen in figure 1.3. These detectors are widely adopted in industrial applications and are now being focused on by the scientific community.

Historically, most experiments have adopted HAPS (section 1.1.5) rather than MAPS due to their high customizability, resulting from the independent fabrication of the electronics and sensor layers. Nevertheless, in HEP experiments, careful attention is focused on costs and the material budget of the sensing devices. In fact, it is of paramount importance to reduce the quantity of materials adopted for particle tracking in order to reconstruct the trajectory with high precision near the vertex. In addition to the sensing devices, also cooling and holding structures are

found in the detecting layers which lead to a higher material budget. Considering the sensor to electronics volume ratio, MAPS have an advantage over HAPS when pushing the material budget to its lower limits. Moreover, since the electronics are directly connected to the small collecting electrodes, the analog power required for a high SNR decreases. The decrease in power consumption also leads to smaller cooling systems.

Moreover, HAPS have been historically favored in high-rate experiments where faster electronics were required, while MAPS were adopted mainly in low-rate detectors due to the adoption of less scaled technologies. Nevertheless, the decreasing transistor size and small electrodes increase the granularity of the sensor. By adopting, in recent years, smaller technology nodes, MAPS are narrowing the gap with HAPS in rate capability. Nevertheless, the increase in transistor density and rate capability will drive up digital power density in MAPS. The narrowing performance gap and lower material budget are favoring the development of MAPS in place of HAPS for high-rate vertex detectors [76].

Furthermore, a higher number of interconnections, and, in turn, points of structural weakness are found in HAPS due to the extreme precision required for the sensor-to-electronics connection. This issue is non-present in modern MAPS due to having, at least, the very front end (VFE) with some sort of low level communication protocol with the outside world to reduce the number of interconnections and their parasitics. Moreover, the precise bump bonding (typically adopting PbSn) required for connecting pixels with a pitch below 50µm can be realized only by a few companies worldwide. The adoption of extra production steps and precise bump bonding techniques leads to a final fabrication cost, for a large area detector, much higher than that of MAPS produced with standard CMOS technologies.

As aforementioned, sensor and CMOS wafers are very different. In particular, the main difference is in the silicon crystalline purity which affects the minority carrier lifetime. This parameter is important in sensors where a longer lifetime implies that the recombination of the radiation generated electron-hole pairs is less likely, thus it is easier to collect the generated charge. The reticle optimization is done by using float-zone silicon which is dislocation-free and with a low density of impurities. This production method enables the fabrication of high resistivity wafers which, coincidentally, also favors the full depletion of the sensor. In fact, the full depletion depth can be expressed as:

$$x_{dep} \approx \sqrt{\frac{2\varepsilon_0 \varepsilon_{\mathrm{Si}} V_{\mathrm{bias}}}{q\, N_{\mathrm{eff}}}} = \sqrt{2\varepsilon_0 \varepsilon_{\mathrm{Si}}\, \rho\, \mu\, V_{\mathrm{bias}}} \qquad (1.1)$$

where V_{bias} is the reverse bias biasing voltage, N_{eff} the effective doping, q the electron charge, ε_0 and $\varepsilon_{\mathrm{Si}}$ are, respectively, the free space permittivity and the dielectric constant of silicon. ρ is the resistivity and μ the carrier mobility.

On the other hand, CMOS electronics do not require substrate optimization,

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thus the substrate is grown with the Czochralski method which decreases carrier lifetime through the impurities. Once the substrate is produced, IC are UV printed on a thin layer grown epitaxially on the substrate. The epi-layer is lightly doped and exhibits a low resistivity $1-10\,\Omega\,cm$. This implies that sensors built with these characteristics would exhibit an early breakdown and a small depletion depth.

The different requirements for the two detector components required smart engineering to merge the possibility of maintaining a high production yield and collection efficiency. Various designs have been proposed for monolithic sensors. The first proposal for sensors with embedded processing electronics dates back to the first 1990s where pin collecting electrodes generate signals processed by PMOS-only electronics. The amplified signal was then processed in the matrix periphery where CMOS readout and control electronics were harbored [71, 73]. Various interesting technological breakthroughs have led to different flavors of MAPS, each with their strengths and issues.

The first MAPS adopted in HEP are in the STAR experiment at the RHIC (Relativistic Heavy Ion Collider) of the Brookhaven National Laboratory [33, 23, 26]. Now many experiments adopt MAPS in their tracking detectors, this section gives an overview of modern monolithic active pixel sensors and also includes an overview of the latest hybrid active pixel sensors.

1.1.1 HV and HR CMOS MAPS sensors
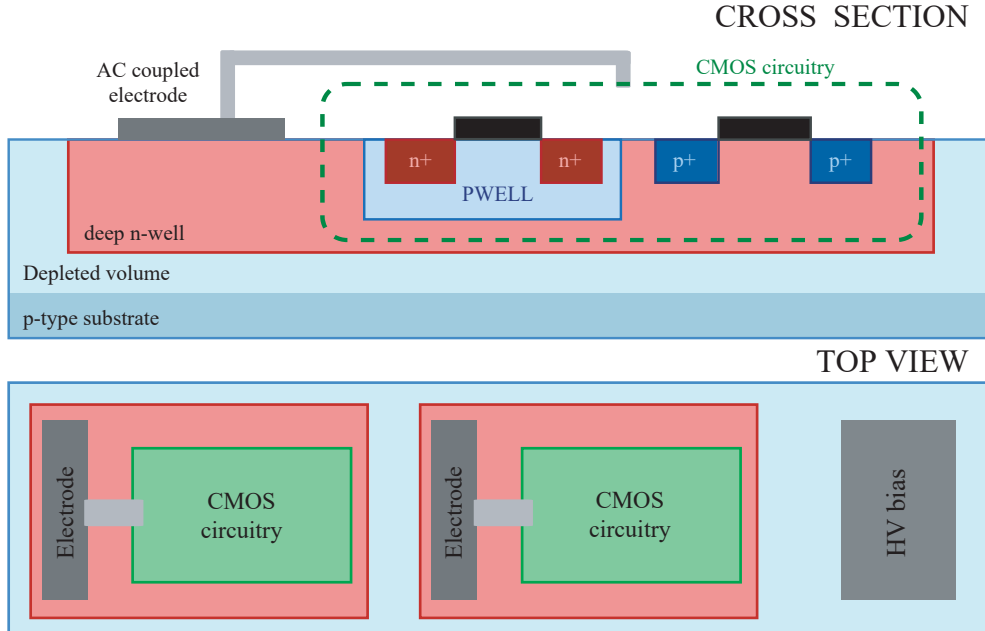
Figure 1.4: Illustration of HV-CMOS MAPS design. A large deep n-well in a p-type epitaxial layer is adopted to collect charges. The large n-well also acts as the CMOS electronics host.

High voltage MAPS (Fig. 1.4) employ low-voltage CMOS transistors within structures capable of sustaining high voltages. The first HV-MAPS inherit HV-CMOS technologies which are adopted by automotive and industrial devices meant to sustain voltages above typical low-voltage CMOS chips. The technology includes a large area deep n-well featuring a high breakdown voltage thanks to the low doping values. The n-well is repurposed, in radiation and particle detectors, as the cathode in a depleted p-type substrate. The front-end electronics is embedded within the n-well collecting electrode with the positive power supply latched to it in order to reverse bias the source and drain diodes of the PMOS transistors [65].

The sensor design leads to a few design problems that must be solved. Firstly, considering that the whole processing chain is contained in each pixel, the size of the electrode cannot be arbitrarily small. Furthermore, the shorted n-well requires a large value resistor per each pixel (in the GΩ order of magnitude) to prevent the signal loss through the power net. In addition, the p-well and PMOS p+ diffusions are capacitively coupled to the cathode implying that a small crosstalk signal (due to the bulk effect) between transistors can lead to an output response similar to that of an impinging particle. Thus, a larger adoption of NMOS transistors, in

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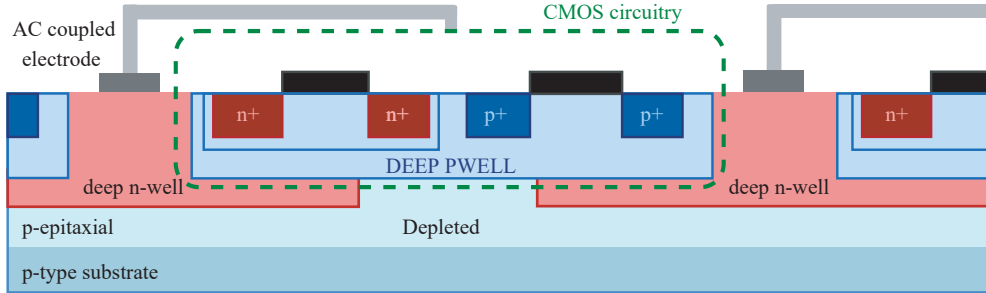
Figure 1.5: Illustration of HR-CMOS MAPS design. The design issues of the HV-CMOS are fixed by adopting a deep p-well which hosts the CMOS electronics, while a deep n-well is adopted as a collecting electrode within the p-type epitaxial layer.

spite of PMOS ones, is found within the pixel circuitry.

The typical depletion depth within an HV-CMOS sensor is $x_{dep} \approx 30\,\mu m$ which makes the technology a good candidate in vertex detectors requiring a very low material budget sensor such as in the Mu3e experiment [9, 70]. Here a biasing voltage between 30 and 70 V is adopted. On the other hand, the depletion region is not sufficient in cases where a larger sensitive volume is required such as X-ray imaging. In these cases a depletion region larger than $200\,\mu m$ is preferred which implies a modification of the substrate resistivity.

To overcome these issues, the ATLAS collaboration has developed a process variation adopting $1\,k\Omega\,cm$ resistivity epitaxial layers to increase the depletion region while keeping the biasing voltage below 150V. Preliminary results with high resistivity substrates a depletion region of $\approx 80\,\mu m$ can be achieved with 120 V biasing voltage [27].

High Resistivity CMOS MAPS, illustration shown in figure 1.5, are being studied in the CLIC (Compact Linear Collider) collaboration. In this case $300 \times 30\mu m^2$ cells include eight small n-type collecting electrodes each connected to their own analog and digital electronics. The cells are arranged in a 16×128 matrix and are independently shielded by a deep p-well implant. The small electrode ensures a low parasitic capacitance while keeping a high fill factor and a fine segmentation [55, 45, 44].

1.1.2   SOI sensors
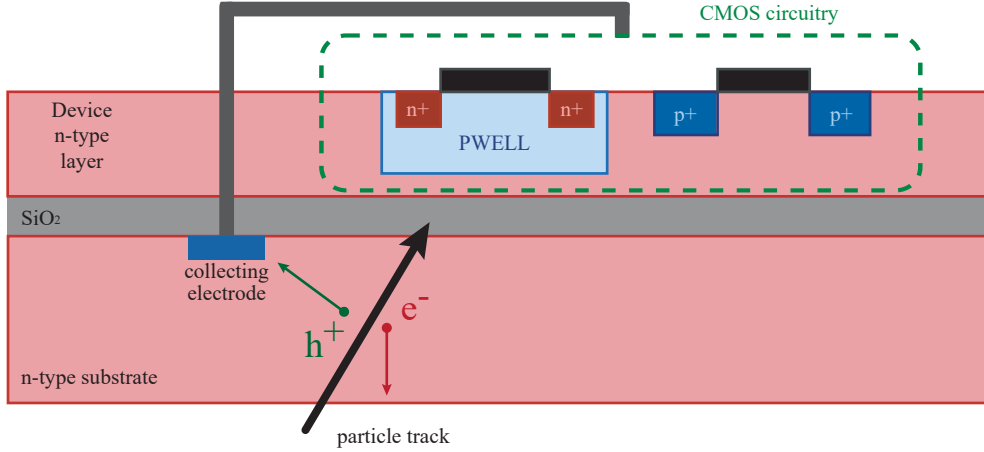
Figure 1.6: Illustration of SOI MAPS design. A buried oxide divides the CMOS electronics layer from the sensing substrate.

Silicon On Insulator (SOI) CMOS electronics (Fig. 1.6) have been in the engineering world for quite some time and are often found in consumer devices thanks to their transistor isolation technique. In fact, in the SOI technology each transistor resides on its own island and there is no connection to the bulk. This isolation is made possible through the adoption of a buried oxide (BOX) which separates the CMOS layer from the mechanical support wafer bulk. Clearly, the intrinsic separation between the CMOS epi-layer and the possibility of using a high resistivity bulk wafer would be the monolithic dream [46, 57]. Nevertheless, the usage as sensors in HEP experiments has not been prolific. This is due to two reasons. Firstly, the high resistivity bulk couples with the transistor channel acting as a secondary gate. This is because the BOX effectively acts as a capacitor accumulating charge at the bottom Si-SiO$_2$ interface giving rise to the back-gate effect. The most noticeable result of this effect is the threshold shift in the CMOS electronics. Secondly, the main weakness of the SOI sensors is their radiation hardness. In fact, total ionizing dose effects (TID) are harmful due to the buried oxide which, when hit by radiation, is actively filled with positive charges further varying the transistor threshold voltages. Clearly, a solution to the BOX effects on SOI devices is required for HEP experiments. Various R&D groups are working on this issue proposing various solutions. In particular, the adoption of p+ implants below the electronics and the design of a thicker or double BOX have been proposed to increase the radiation hardness to 500 kGy and will also mitigate the back-gate effect [40, 19, 76, 35, 34].

1.1.3   ALPIDE
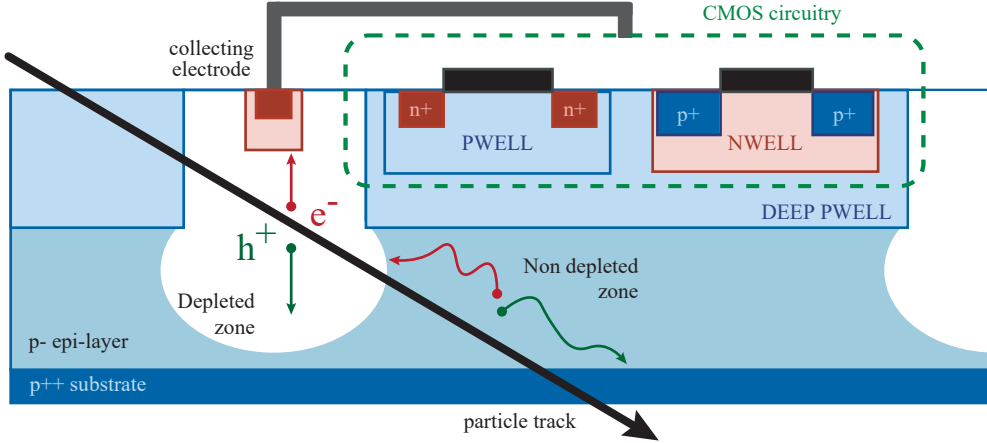
Figure 1.7: Illustration of the ALPIDE MAPS. Similar to HR-CMOS, the CMOS electronics are harbored within a deep p-well in a p-type epitaxial layer. The depleted volume is limited to the first tens of microns leading to diffusion charge collection in areas away from the collecting electrodes.

The increase of luminosity within the HEP experiments has led scientists to researching better ways to detect particles with MAPS. In particular, researchers at CERN have designed MAPS capable of fulfilling the harsh requirements needed for operation in the future high luminosity large hadron collider (LHC) experiments (up to $6 \times 10^{27} \, \mathrm{cm^2 s^{-1}}$).

The ALICE experiment Inner Tracking System (ITS) is being updated during the second long shutdown with ALPIDE (ALICE PIxel DEtector) [67, 48]. The MAPS, shown in figure 1.7, feature a small pixel pitch of $27 \times 29 \, \mathrm{\mu m^2}$ with 4 small n-well collecting electrodes yielding a small detector capacitance and a high SNR. The CMOS processing electronics, designed in Towerjazz $0.18 \, \mathrm{\mu m}$ CIS technology, are built in deep p-wells within a thick $25 \, \mathrm{\mu m}$ epi-layer. The substrate, where the biasing voltage is applied, features a p++ doping and a reverse bias up to $-6 \, \mathrm{V}$ is possible. The pixel hit-map is generated on chip and sent out through priority encoding [78, 4].

Due to the adoption of standard CIS technology on a p-type epi-layer, the depletion region does not reach the p++ back. This implies the separation of the active sensor in areas with drift charge collection and areas where charges move by diffusion. Clearly, in the depleted areas the charge collection is quick, but, in the non-depleted areas the diffusion of carriers generated by the impinging radiation leads to longer signal acquisition times and charge spreading to neighboring pixels. Investigator chips and new designs have been developed at CERN to solve these issues [5, 37, 72].

1.1.4   DEPFET Pixels
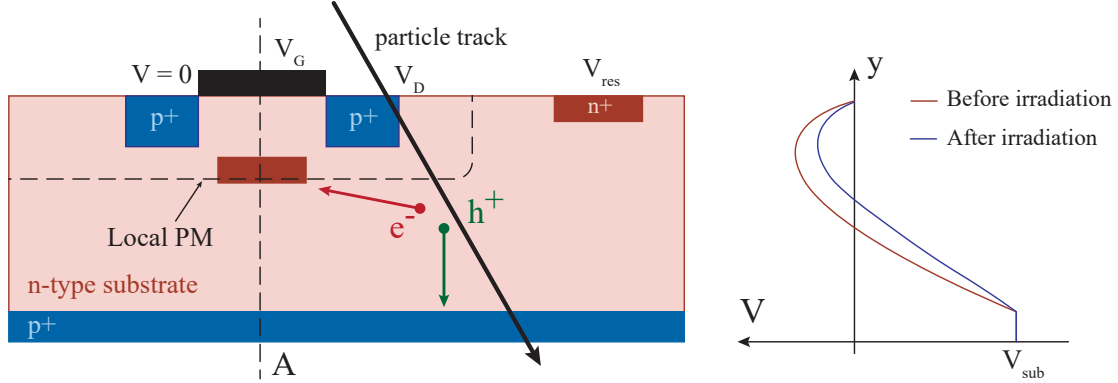
Figure 1.8: Illustration of the DEPFET. On the right is the voltage profile along the cut line A. The potential variation is shown which generates a threshold change in the mosfet characteristics [42].

DEPMOS (depleted MOSFET) and DEPFET (depleted field effect transistor) refer to an interesting variation in standard MOSFET and JFET technologies. Based on semiconductor drift chambers (SDC), DEPMOS technologies (figure 1.8) adopt a tapered potential in the bulk to convey the collected charge (e) in a small n-doped area below a PMOS transistor. Here, this charge actively varies the threshold voltage of the transistor modifying, in turn, its source-drain characteristic current. This location coincides with the local potential maximum (PM), thus, the carriers will be slowly discharged by the PMOS current until a reset signal is sent through an n+ electrode on the top to remove the remaining charge stored in the potential pocket [42].

The n-deposition below the gate can thus be effectively considered a second gate for the transistor. These double gate transistors can then be arranged in matrices and readout in a rolling shutter method or can be coupled with a secondary charge transfer gate in order to enable correlated double sampling on pixel.

Nevertheless, the DEPFET technology does not have in-pixel electronics or digitization due to its extremely customized bulk potentials. This implies that the pixel currents are either amplified on a separated chip or in the matrix periphery not making it yet a viable option for experiments where an extremely low material budget is required [47, 49].

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1.1.5 3D CMOS and hybrid pixel sensors
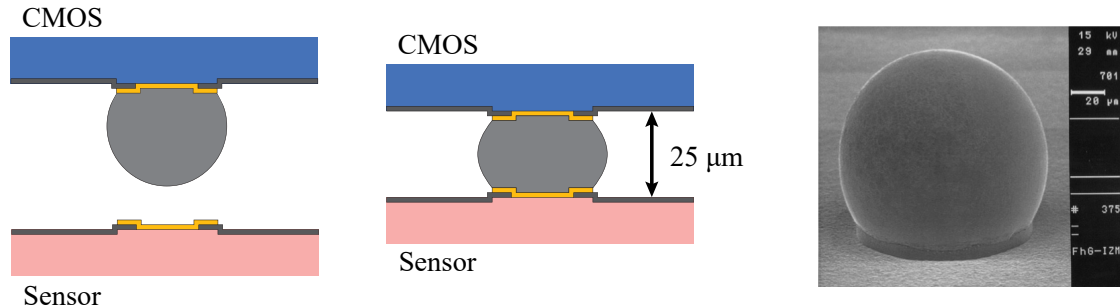
Figure 1.9: *left* Illustration of the bump bonding process. The *orange* layer is an Under Bump Metallization (UBM) which is adopted to improve the yield of the bump bonding process and facilitates the interconnection between the layers by providing a solder wettable surface. On the *right*, a SEM micrograph of a SnAg bump [29].

Differently from the sensors previously described, hybrid active pixel sensors are not monolithic sensors. Nevertheless, the impressive consumer adoption and evolution of this sensor-electronics couple requires an inclusion within the state-of-the-art chapter.

HAPS, illustrated in figure 1.9, are composed of two stacked layers of detecting and processing CMOS wafers. The independent processing of the layers implies the possibility of customizing the detector for each experiment [66].

HAPS, which are widely adopted in HEP experiments, such as Timepix3, adopt the bump bonding technique to connect the sensor to the CMOS readout chip. The technique adopts solder spheres precisely located between the two layers. Depending on the adopted materials the diameter of the bonding contacts ranges from 25 to 50µm. On the other hand, the most common bump bonding pitches found in HEP detectors are $50\,\mu m$ wide, while the ultimate pitch could be around $5-10\,\mu m$ [29]. Nevertheless, presently, small pitches below $30\,\mu m$ can hardly be achieved with a high yield, thus are not yet the HEP HAPS standard.

Furthermore, considering, as explained in the chapter's preamble, the high costs for small production volumes (compared to consumer devices) required for building large detecting surface detectors with customized HAPS, the future adoption of these sensors becomes less appealing compared to MAPS.

A large R&D effort in HAPS is found in modern consumer cameras and cell phones which require a transistor count that cannot be fitted onto a single substrate. This R&D has led to the adoption of through silicon vias (TSV) for the connection
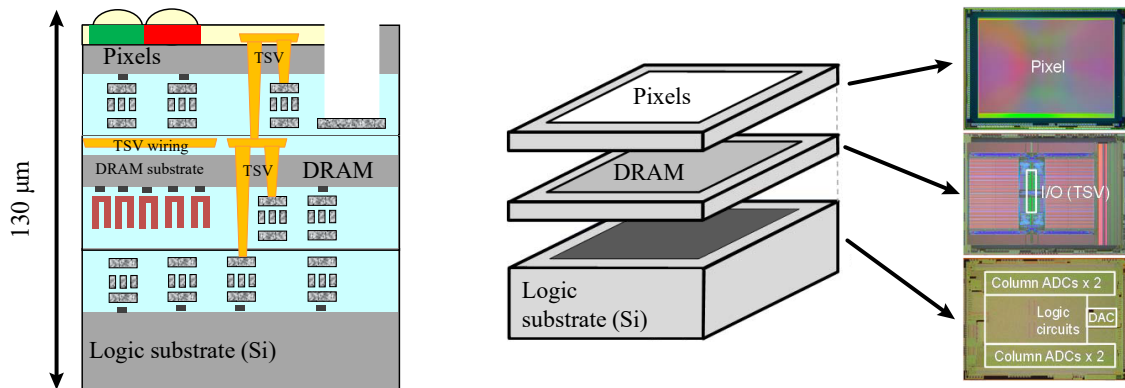
Figure 1.10: Illustration and layout of a three layered HAPS designed for visible light detection [74].

of the various layers, which can be more than 2, creating a new branch of detectors categorized as 3D CMOS detectors. Until now, due to the consumer application scope and much higher non-recurrent engineering costs, they have been adopted in visible light detection rather than particle or high energy radiation detection. The specific visible light application implies the possibility to have extremely small pixel pitches down to $0.8\,\mu m$ [62].

Concluding, in cases where the detecting areas are not too large (e.g. medical X-ray imagers and hadron therapy) and advanced on-chip digital signal processing (DSP) is required, HAPS are a highly competitive option. Moreover, the adoption in HEP detectors of the state-of-the-art 3D CMOS developments found in consumer cameras (figure 1.10), such as TSV and direct wafer bonding, could improve the manufacturability yield and final costs for very large productions [10].

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1.2 MAPS Recap

Considering the great number of MAPS flavors, an overview of all the previously explained technologies is required.

Various proposals have been brought up for MAPS each with their positive features and drawback. Due to the high speed at which MAPS technologies are evolving it is difficult to categorize each one in a single snapshot. Nevertheless, in table 1.1 a categorization of the most prominent advantages and issues of each technology is given. In order to have a simple reference, the characteristics of each technology are taken from the experimental designs of some the most prominent collaborations in HEP experiments.

The expected total ionizing dose is referred to the experiment in which the MAPS will be used, thus they are not the maximum achievable doses before failure. In particular, when considering SOI-MAPS, the maximum achievable TID should be above $500\,\mathrm{kGy}$ with double-BOX technology [35], in the table the column refers to the adoption of SOI-MAPS in the FORCE (Focusing On the Relativistic universe and Cosmic Evolution) satellite. Thus, a high radiation hardness is not required.

Concluding, a great benefit in pixel size and power density can be expected by the custom design of fully depleted monolithic pixel sensors. However, most technologies require a custom processing of the device wafer and, thus, a higher production chain load for a standard CMOS foundry. In the following chapters the design of the novel FD-MAPS will be introduced and explained in a detailed manner.

	HV-CMOS	HR-CMOS	SOI	ALPIDE	DEPFET	HAPS
Experiment	STAR	CLIC	FORCE	ALICE	Belle II	Timepix 3
Standard CMOS	Yes	Yes	No	Yes	No	Yes
Tech node [nm]	350	180	200	180 TJ CIS	custom	130
Pixel Size [μm^2]	20.7×20.7	37.5×30	30×30	27×29	50×50	55×55
Sensor Thickness [μm]	50	200	300 - 500	50	75	700
Material Budget [% X_0]	0.3	1 - 1.5	N. A.	<1 %	0.2	few %
Spatial Resolution [μm]	~3.7 - 6	~7	1.5 - 3	~5	10	~5
Time Resolution [μs]	~186	0.156	65	30	20	0.0016
Power Density [$mW\,cm^{-2}$]	150	100	N. A.	300 to 100	N. A.	225
Expected TID [$kGy\ y^{-1}$]	0.9	1	0.001	4.5	15	N. A.
Reference	[23]	[44]	[34]	[48]	[51]	[22]

Table 1.1: Comparison of most advanced MAPS designs. Full description in section 1.1.5.

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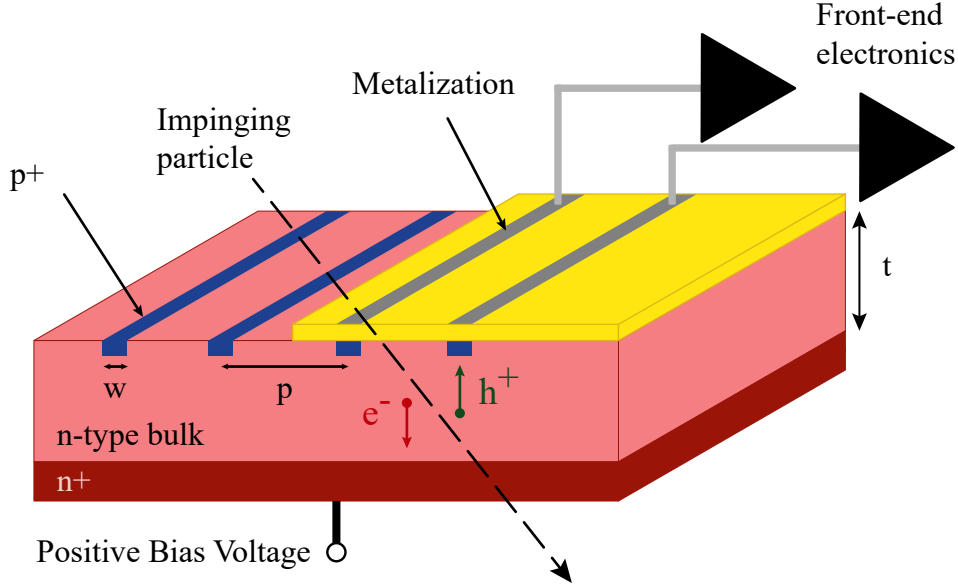
Figure 1.11: Illustration of a microstrip detector. The main geometrical parameters are indicated.

1.3 Microstrips

In various experimental applications the adoption of microstrips is advantageous compared to the usage of pixelated sensors. In particular, when the particle flux is below tens of kHz using microstrips arranged in a perpendicular or slightly slanted formation yields good track reconstruction while keeping the dissipated power lower than pixel detectors. This particle flux is found in aero-spatial applications and satellite detectors which aim at achieving a particle hit-rate in the order of 1 kHz.

Furthermore, in order to reduce the dissipated power in MAPS a trade-off is required between the pixel area and number of processing transistors. Thus, most MAPS with pixel pitches below 30 µm do not measure the particle's energy, but a binary hitmap coupled with the hit timestamp [48].

The illustration of a common AC coupled p-in-n microstrip section is in figure 1.11. Here, the main parameters are depicted: w, strip electrode width; p, strip pitch; t, sensor thickness. Common pitch values range from 25 to 280 µm. A key parameter in the design of microstrips is the width-to-pitch ratio w/p. A compromise must be found between the minimization of the strip capacitance and a high voltage stability, respectively solved designing a microstrip sensor with a small or a large w/p ratio.

1.3.1 Depletion voltage and strip capacitance

Approximating a microstrip sensor to a planar diode of thickness t and width p, the thickness of the depleted layer is, remembering equation 1.1:

$$t_{dep} = \sqrt{\frac{2\varepsilon_0 \varepsilon_{\mathrm{Si}} V_{\mathrm{bias}}}{q\, N_{\mathrm{eff}}}}.$$ (1.2)

Thus, rearranging the terms, the full depletion voltage, $V_{\mathrm{fd,diode}}$, for a given thickness is:

$$V_{\mathrm{fd,diode}} = \frac{q\, N_{\mathrm{eff}}}{2\varepsilon_0 \varepsilon_{\mathrm{Si}}} t^2.$$ (1.3)

Considering the back-plane capacitance per unit length at full depletion:

$$C_{\mathrm{B,diode}} = \varepsilon_0 \varepsilon_{\mathrm{Si}} \frac{p}{t}.$$ (1.4)

When considering the finite pitch and width of the microstrip detector two main effects arise [16, 39]. The first is an increase of the required voltage to reach full depletion. This effect can be understood considering the modification of the equi-potential lines with the variation of w. In particular, when the width decreases, the equi-potential lines will curve near the collecting electrode requiring an increase in voltage to be straightened near it. A more realistic depletion voltage equation is thus:

$$V_{\mathrm{FD}} = V_{\mathrm{fd,diode}} \left[1 + 2\frac{p}{t} f\left(\frac{w}{p}\right) \right]$$ (1.5)

where $f(w/p)$ is a universal function depending on the width over pitch ratio. In the range $0.1 < w/p < 0.6$ the function f monotonically decreases from 0.65 to 0.10. [11]

The second effect arising from the finite pitch and width is the decrease in the back-plane capacitance:

$$C_{\mathrm{B}} = C_{\mathrm{B,diode}} \frac{1}{1 + \frac{p}{t} f\left(\frac{W}{p}\right)}.$$ (1.6)

Considering also the interstrip capacitance, a total capacitance for a detector thickness $t = 300\,\mu\mathrm{m}$, standard pitch $p = 100\,\mu\mathrm{m}$ and a ratio $0.1 < w/p < 0.55$:

$$C_{\mathrm{tot}} = \left(0.8 + 1.6\,\frac{w}{p} \right) \frac{\mathrm{pF}}{\mathrm{cm}}.$$ (1.7)

The total capacitance of a microstrip is one of the most important parameters a front end electronics designer must consider. In particular, by reducing the

input capacitance to the electronics the equivalent noise charge figure can be reduced without increasing the dissipated power as will be discussed in the electronics chapter 5.

1.3.2 Microstrips in Space Applications
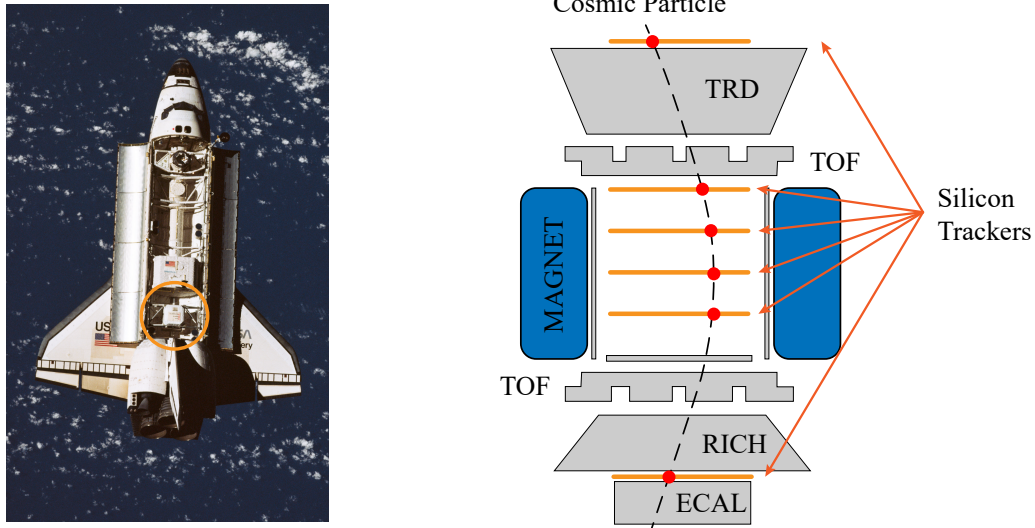
Figure 1.12: *left* Photograph taken from the Russian Mir space station while Space Shuttle Discovery passes below it. In the cargo bay the AMS-01 detector can be noticed near the aft firewall (circled in orange) [3]; *right* illustration of the updated AMS-02 detector aboard the ISS.

The most common application for silicon strips is in high energy physics experiments, but they are also often found in satellite particle detectors. Cosmic ray detectors, found in orbit, adopt silicon microstrips as particle trackers in order to evaluate the particle's charge, energy and interaction points within the detectors.

An interesting example is the AMS-02 detector deployed onto the ISS (International Space Station). Precursor detectors such as the AMS-01 and the PAMELA experiments also used microstrips sensors [8, 64, 15]. The detector employs a total of 2264, $41.360 \times 72.045 \times 0.300\text{mm}^3$, double-sided Si microstrip sensors. In particular, the two sides of the microstrips have n and p doping profiles arranged in a perpendicular direction which collect, respectively, the generated electrons and holes [12]. The collecting electrode regions are AC coupled to low power external ASIC chips. Most detecting layers, as illustrated in figure 1.12, are located within a large permanent magnet which deviates the charged particles crossing the detector. The silicon trackers measure, with a location standard deviation below 10µm, the
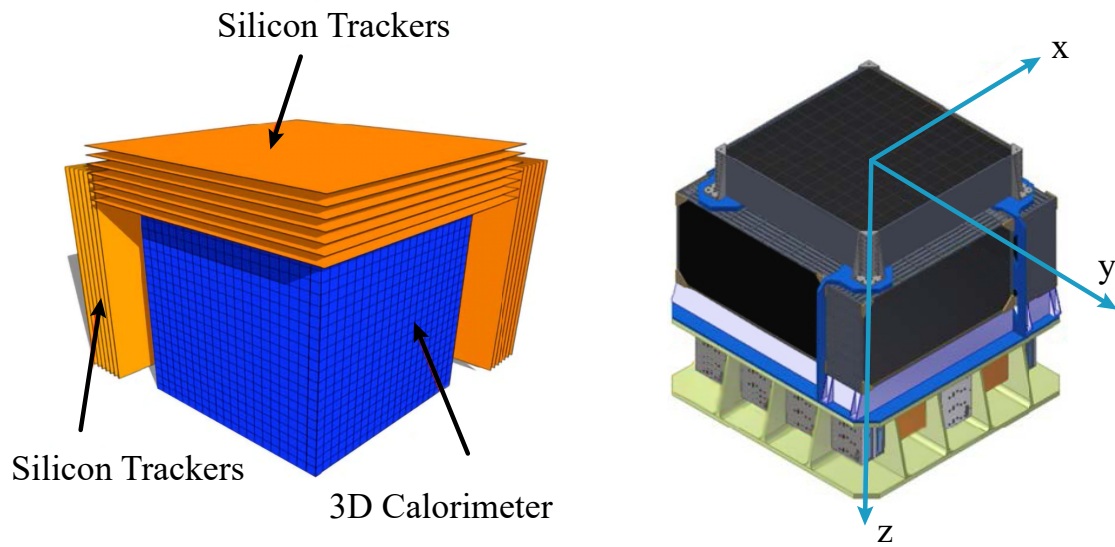
Figure 1.13: *left* illustration of HERD's internal detectors; *right* realistic rendering of the HERD detector

interaction coordinates of the impinging particles with the active layers and extract information regarding the particle's charge and energy.

An example of future adoption of microstrips is in the HERD (High Energy cosmic-Radiation Detection) experiment [30, 77]. The illustration of the detector and a realistic rendering are in figure 1.13. The detector will be hosted in 2025 by the Chinese space station and study cosmic rays and, through indirect detection, look for dark matter.

The silicon trackers are designed for a precise cosmic ray trajectory tracking, gamma ray conversion and tracking and complementary charge measurements (up to Z = 26). While the central detector volume will use $\approx$ 7500 LYSO crystals for novel 3D energy studies with a large acceptance.

1.3.3 Monolithic Microstrips
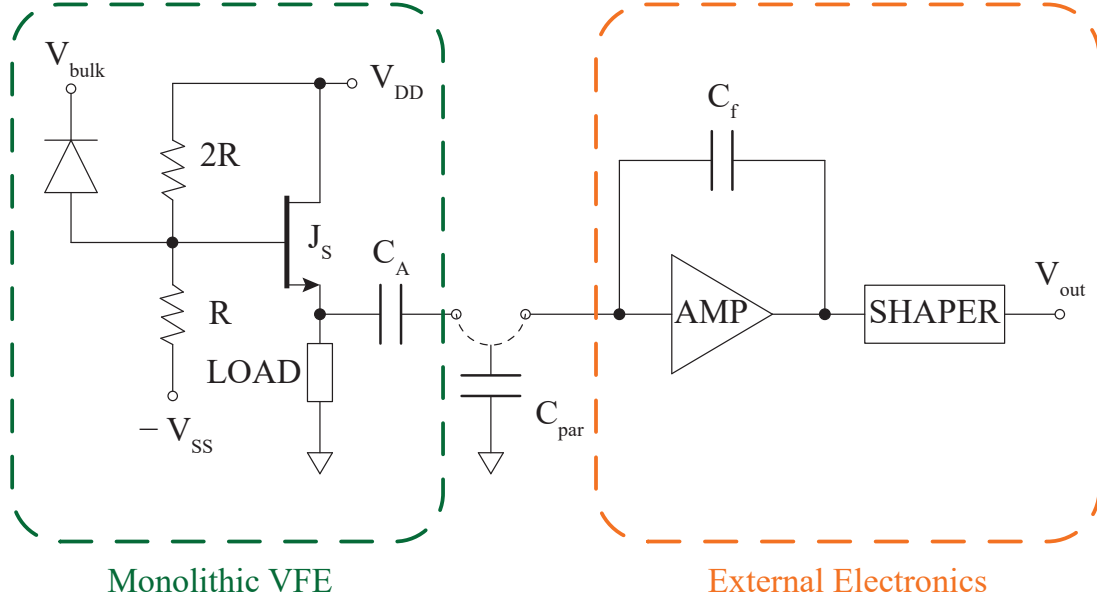
Figure 1.14: First Monolithic Microstrip front-end [14]. On the *left* side the internal monolithic circuitry is shown, while on the *right* the external electronics. Between the two parts, a bond wire is shown with its parasitic capacitance, C_{par}.

The harsh environment and stringent specifications required in space have led to the research and development of methods to include a very front-end onto the silicon sensor substrate.

Many issues surface when sending electronics to space. On take-off the strong acceleration and the random and sinusoidal vibrations felt by the payload can break the metal bondings between the electronics and the sensors. In particular, the pyroshock due to the rocket stage separation can influence the equipment even before deployment. When deployed, the orbiting electronics must be able to withstand thermal stresses due to sun light (seasonal and day/night effects) and also be able to cool down in space vacuum.

To mitigate the first issue, a reduction of the total number of bondings and interconnections is favorable, making MAPS or monolithic microstrips appealing to the space community. For the second issue, a reduction of the power dissipated implies a lower temperature increase of the electronics due to its operation. In this case, the adoption of microstrips with integrated electronics also implies a reduction of required dissipated power thanks to the higher signal-to-noise (SNR) achievable with monolithic CMOS sensors.

Silicon sensor grade substrates differ from standard CMOS ones because of their

high resistivity $(4 - 6\,\mathrm{k\Omega\,cm})$ and pureness. In fact, sensor grade substrates require purification techniques in order to remove contaminants which would act as particle traps within the active volume.

The different steps required for higher silicon pureness found in sensor grade wafers implies a customization of the production chain to also include a very front end within the detector.

Nevertheless, microstrips including the first electronic amplification stages have been designed to prove monolithic microstrips feasibility [14, 25]. A schematic and a microphotograph of the monolithic structures are in figures 1.14 and 1.15. The first amplifying stage, composed of a common source N-JFET with a diode connected load transistor, is monolithically designed on chip and AC coupled to a charge sensitive amplifier (CSA) through an internal coupling capacitor, C_A.

By the inclusion of a simple source follower amplifier the signal loss due to the parasitic capacitance due to the bonding and pad is avoided and a higher SNR per dissipated power can be achieved. The monolithic array, thus enables the possibility of moving the external electronics further away from the microstrip sensor and improve the experimental flexibility.

Concluding, various studies have been published on fully integrated preamplifiers onto high resistivity sensor grade wafers proving the clear advantage in including the front end electronics onto the detecting sensor chip [50]. However, these new devices are only adopting NMOS or N-JFET technology in the electronics, leading to a non-complementary and a less complex analog and digital design.
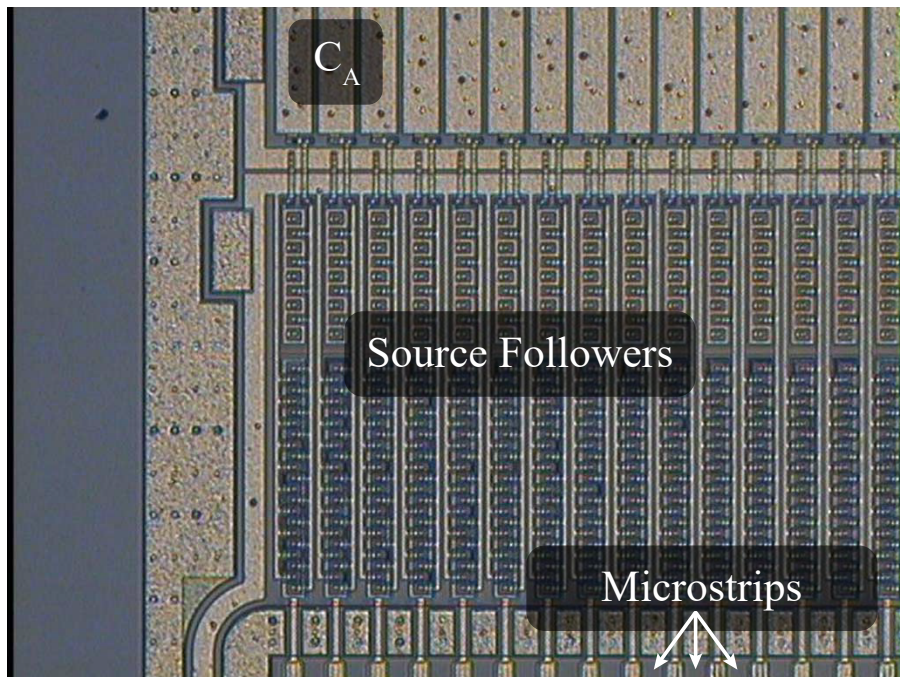
Figure 1.15: Microphotograph of one of the first monolithic microstrip very front-ends [25]. On the *top* the internal to external electronics coupling capacitor, C_A, is visible, while, at the *center* the internal source follower topology N-JFET are pictured. At the *bottom* the connection between the gate of J_S and the microstrip top metal plate can be seen.

Chapter 2

The SEED and ARCADIA monolithic sensor technology

The INFN (*Istituto Nazionale di Fisica Nucleare*) has proposed a new monolithic technology within the ARCADIA collaboration.

ARCADIA's (Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays) objective is to manufacture fully depleted MAPS for HEP experiments adopting commercial CMOS image sensing technologies.

An Italian collaboration started at INFN Torino has been signed enabling a competitive research and development aimed at optimizing both the substrate and CMOS characteristics. The collaboration started in December 2013 with a shared vision between physicists and engineers with a broad background in image sensors and radiation detectors. At the time, a Sensor with Embedded Electronics Development (SEED) was the primary objective, proving the possibility of including transistors on a fully depleted substrate ranging from 100 to 300 µm. In 2016, the prototypes have been submitted in different flavors. A set of $2 \times 2 \, \text{mm}^2$ ASICs designed in a 6 metal-layer 110 nm BSI (Back-Side Illumination) CMOS technology have been produced. In particular, a set of passive test-structures providing insights in substrate depletion regions and sensor capacitance are the first step for the characterization of sensor. A second test chip, with active pixel amplification and readout, has been produced proving the functionality of the sensor-electronics ensemble.

Since 2018, ARCADIA, relying on the positive results of SEED, has continued the development creating a variety of new large area test structures and continuing the evaluation of the test-structures developed in the SEED time-frame.

The ARCADIA collaboration is currently working on a series of large-area prototypes. The main demonstrator for the technology is a FD-MAPS enclosing an active matrix of 512×512 pixels with a 25µm pitch implying a total active area of $1.3 \times 1.3\text{cm}^2$. Additional test structures designed to test the manufacturability

and characteristics of pixels with pitches ranging from 10 to 50 µm and total thicknesses from 50 to 200 µm have been produced. In particular, the test structures designed are both passive and active sensors for the detailed study of the sensor to electronics couplings and the study of different pixel geometries.

Furthermore, various strip-like sensors have been designed on the ARCADIA reticle in order to test the sensor efficiency also for strip sensors. Moreover, an active monolithic sensor has been included which chapter 4 and 5 will focus on.

In this chapter, an overview of the sensor characteristics and simulations is given. The sensors, designed at the University of Trento have been simulated using advanced CAD (Computer Aided Design) software. On the other hand, the electronic design and validation steps have been done with advanced integrated circuit simulators adopting the commercial CMOS foundry PDK (Process Design Kit).

2.1   The ARCADIA Sensor
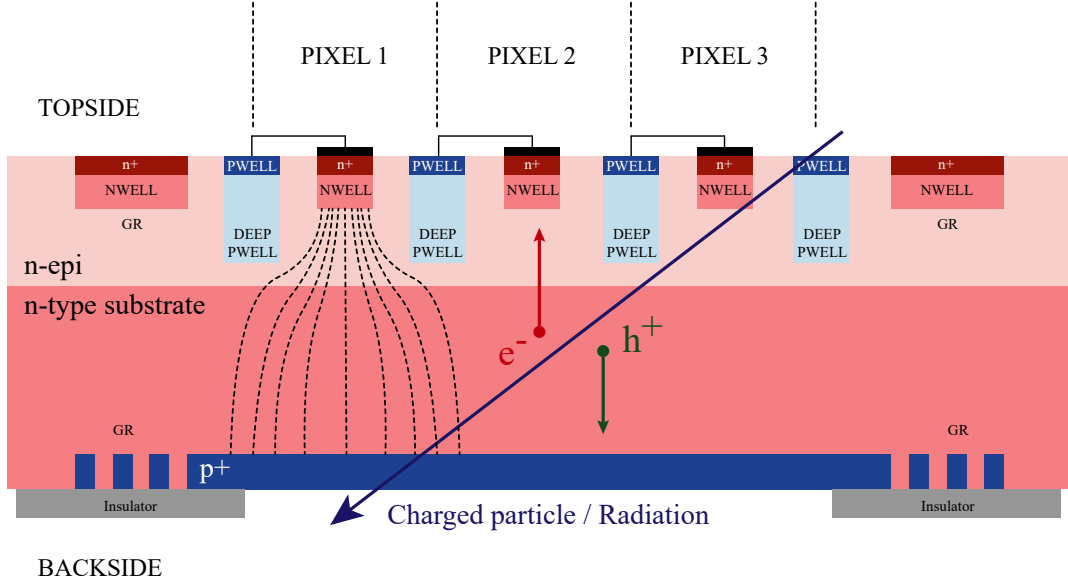
Figure 2.1: Illustration of the ARCADIA FD-MAPS.

The novel sensor developed within the ARCADIA collaboration, in figure 2.1, aims at mitigating the issues present in the state-of-the-art technologies adopting a fully-depleted substrate, a small collecting electrode and shielded CMOS electronics.

Full depletion implies the possibility of collecting carriers by drift throughout the sensor thickness, increasing the signal response speed. As aforementioned, a fully depleted bulk, having a larger detecting volume, leads to a larger amount of charges generated by the impinging radiation, thus generating a larger signal output. On the other hand, drift collection implies a higher spatial resolution due to a lower horizontal charge spread within the active area. Furthermore, the strong electric field produced within the substrate increases the charge collection efficiency (CCE) in two ways. Firstly, the recombination probability decreases noticeably increasing the probability of collection of a generated carrier. Secondly, it increases the radiation hardness of the bulk. In fact, when high energy particles or radiation impinge onto the crystalline lattice of the device their interaction through strong or electromagnetic force can result in atoms being displaced. The displacement leaves behind a vacancy or can effectively lead to an interstitial atom within the lattice. These defects can, through various capture mechanisms, actively generate new energy levels within the silicon band gap trapping the charge carriers and reducing the CCE.

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The small collection electrode implies a low capacitance seen by the front-end electronics which improves the SNR. This also implies, differently from HV-CMOS MAPS and HAPS, the possibility of reducing the size of the pixels to pitches below $50\,\mu m$.

In most MAPS technologies, it is complicated to fully deplete the sensor due to the voltages in play being too high for the electronics, the substrate resistivity too low for full depletion or because the n-wells including the PMOS transistors compete with the electrode for the charge collection. In ARCADIA, this is not the case due to a few design characteristics developed to increase the high voltage while keeping the CMOS electronics decoupled from the collecting electrodes.

Firstly, the sensor bulk is a lightly n-doped substrate with a small n-type epitaxial layer above it. The low doping implies the possibility, remembering equation 1.2, of adopting a lower voltage to increase the depletion region within the sensor thickness. This is, in general, the reason why sensor substrates have high resistivity. The epi-layer harbors the electronics and the n-type collecting electrodes. On the back, a p+ region is implanted after the completion of the BEOL (Back End Of Line) layers. The choice of adopting a p+ back implant electrode has been designed to start the depletion from the back rather than from the front as illustrated in figure 2.2. In fact, to bias the sensor, the high voltage can be negative and provided from the back implying that the biasing voltages of the electronics and top electrodes are well within the low voltage CMOS standard.

Secondly, the CMOS electronics are harbored within deep p-wells. The adoption of deep p-wells leads to the isolation of the PMOS n-wells and n+ collecting electrodes. Thus, complete CMOS designs are possible within the pixel area.
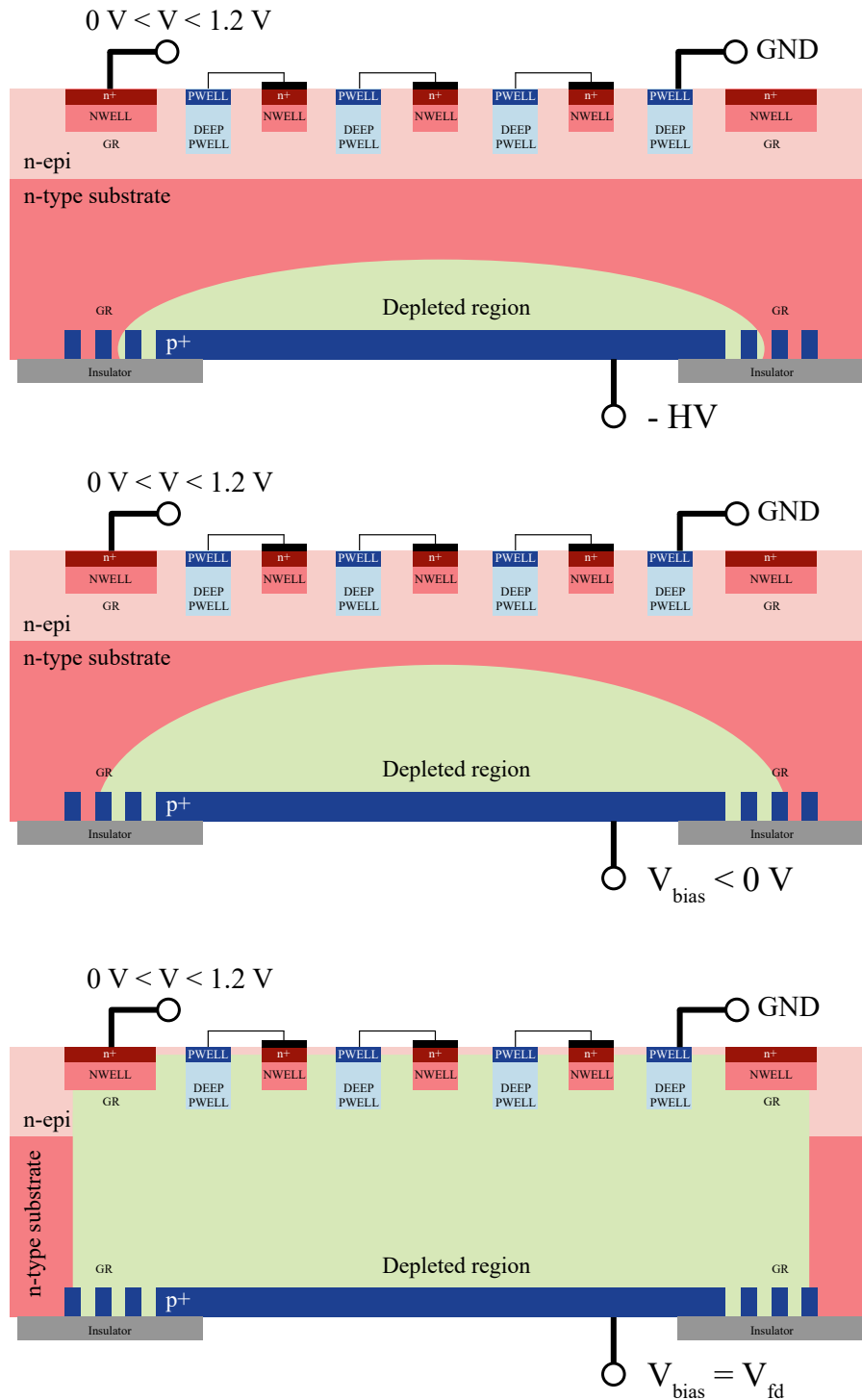
Figure 2.2: Illustration of the ARCADIA depletion. The p-n junction is at the back, thus the depletion region extends towards the front side as the negative back voltage increases in absolute value.

2.1.1 Pixel optimization
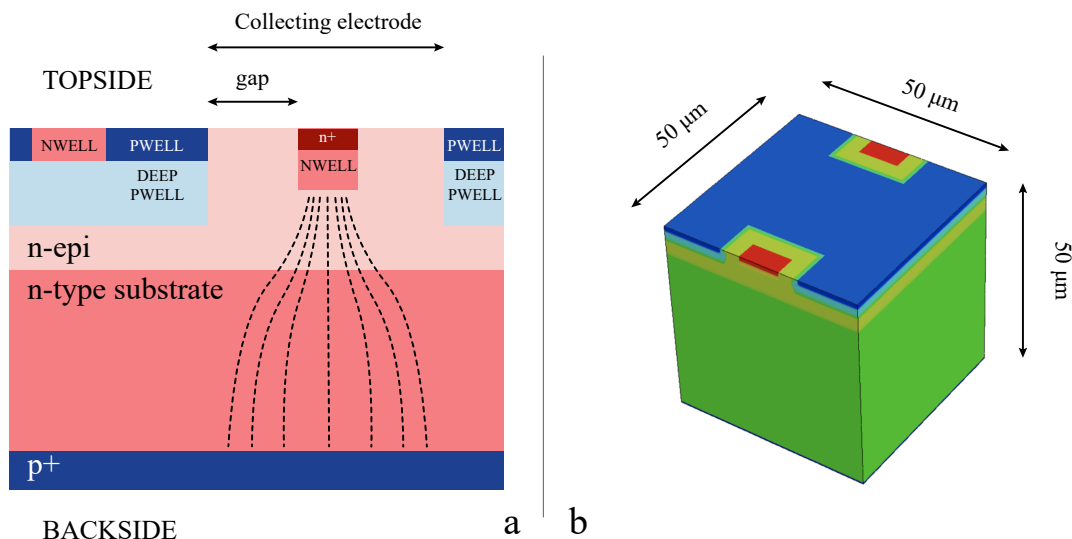
Figure 2.3: Single pixel simulation domain. *left* single pixel parameters illustration. *right* 3D simulation domain, the cell size is $50 \times 50 \times 50 \mu m^3$ and the cuts are performed along the collecting electrode center. The color scale represents the doping concentration.

In order to maximize the efficiency of the charge collection and the available area for the CMOS circuitry within a pixel, various TCAD simulations have been done varying sizes and doping parameters.

The simulations parameters do not take into account the n-wells required for the PMOS transistors and are all performed at 300 K.

In figure 2.3, a single pixel and its 3D pixel simulation domain are illustrated. For illustration purposes a 50 µm thick domain has been selected, but the final production flavors start from 50 and reach 400 µm. For the simulations, the collection electrode is biased at a voltage $V_{c.e.} = 0.8\,V$ this voltage is picked because this way a small portion of the n-well-to-n-epi interface results depleted. In fact, increasing the n-well voltage with respect to the deep p-wells leads to a lower punch-through probability (this effect will be discussed later in the section) and decreases the voltage at which full depletion occurs. This last effect is important to increase the operating region of the sensor as can be seen in figure 2.4. Furthermore, this voltage is near the maximum supply voltage for the CMOS electronics and is, coincidentally, a good biasing voltage for the front-end input PMOS transistor.

In order to evaluate the electrical characteristics of a single pixel, the results of the simulations focus on capacitance-to-voltage (C-V) and current-to-voltage (I-V) curves. The results of the simulation for the pixel domain in figure 2.3b are plotted
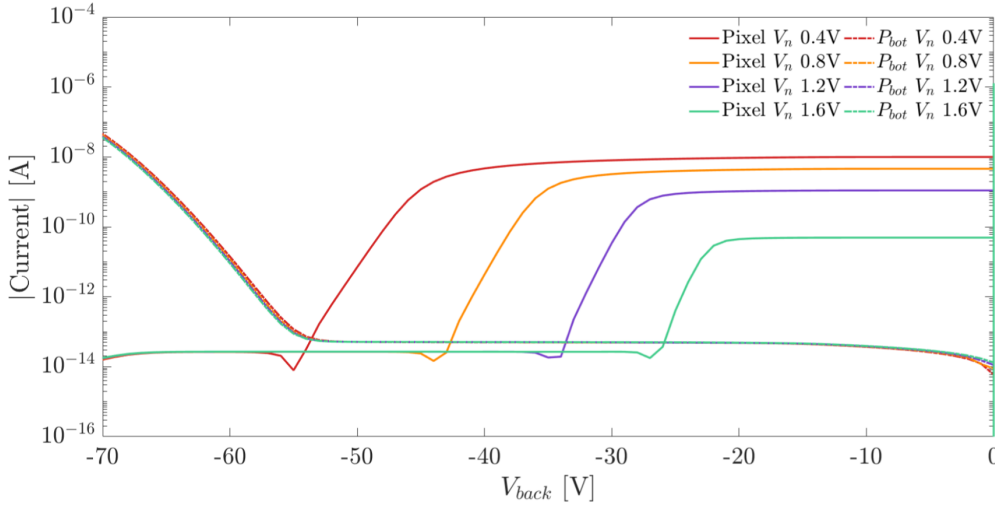
Figure 2.4: Single pixel simulated currents at varying $V_{c.e.}$. As the electrode voltage increases the voltage required for full-depletion decreases widening the operating region. Simulation run with a sensor thickness of $100\,\mu m$.

in figure 2.5. The currents from the top the electrodes are illustrated in black. The depletion voltage, V_{dpl}, is marked with a vertical black dotted line. The onset of depletion is easily identifiable because the current changes polarity due to the depletion region reaching the top and effectively removing cross pixel currents. The cross pixel current is present mainly due to the fact that the two half electrodes are, in this kind of simulations, biased with a small voltage difference $\Delta V = 10\,mV$. Nevertheless, this would not explain the value if not considering that, due to the electrode biasing voltage being positive (standard $V_{c.e.} = 0.8\,V$), the region below the p-wells results un-depleted connecting the two electrodes.

The red curve follows the current flowing through the grounded p-well. Similarly to the n-well current, the current changes polarity, but in this case it is due to the onset of the punch-through. The punch-though voltage, $V_{p.t.}$, identifies the value at which the front p-wells and the p^+ back deposition become electrically connected. Once the biasing voltage reaches $V_{p.t.}$ the current sunk from the p-wells increases exponentially and, if not carefully taken care of, could harm the sensor. Nevertheless, the onset of punch-through is not the limiting factor when depleting the sensor. In fact, the sensor still works beyond $V_{p.t.}$, but the currents in play are much higher than normal. Thus, to limit the power consumption to $0.1\,mWcm^{-2}$, V_{pw} is marked as the ultimate voltage adoptable for normal usage.

Lastly, the blue curve indicates the capacitance of the single pixel at varying back bias voltage. The curve is simulated in AC (Alternated Current) with a frequency of $10\,kHz$. As the depletion region reaches the top side a sharp capacitance

decrease is noticeable. Nevertheless, the minimum capacitance is only reached at higher voltages due to the lightly doped epi-layer, which is more difficult to deplete compared to the high resistivity substrate.
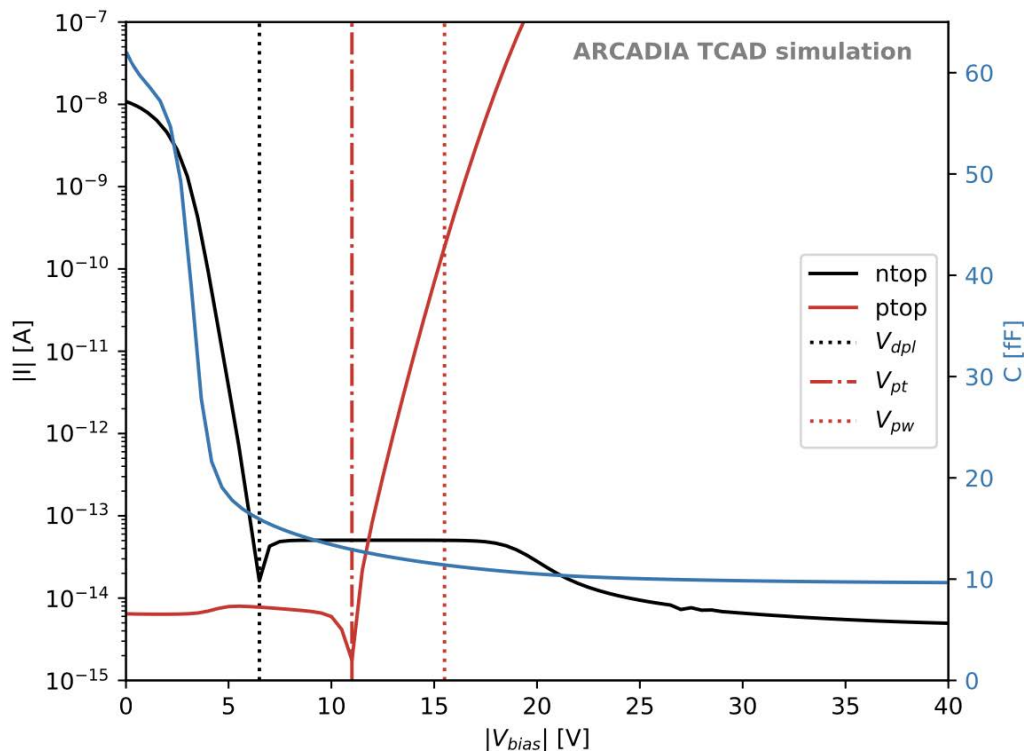
Figure 2.5: Single pixel simulated current and capacitance curves [56]. The *black* curve shows the pixel current. Here the full depletion voltage is marked with a vertical dotted black line. The *red* curve shows the current passing through the p-well. The punch-through voltage and the voltage where the maximum available power is dissipated are marked with, respectively, a dot-dash red line and a dotted red line. The *blue* curve represents the capacitance of the electrode with varying voltage.

2.1.2 Backside processing

Following the BEOL step on the front side of the sensor, the back side must be processed. The layout view of a test diode and an illustration of the back structures are shown in figure 2.6. In order to bias the back side at the high voltages required for full depletion of the sensor, a few steps must be taken care of.

Firstly, the backside p$^+$ junction must be wide enough to cover the whole active

Metalization

Guard Rings

n-electrodes with front contacts

back side pad

floating guard rings

p$^+$ electrode
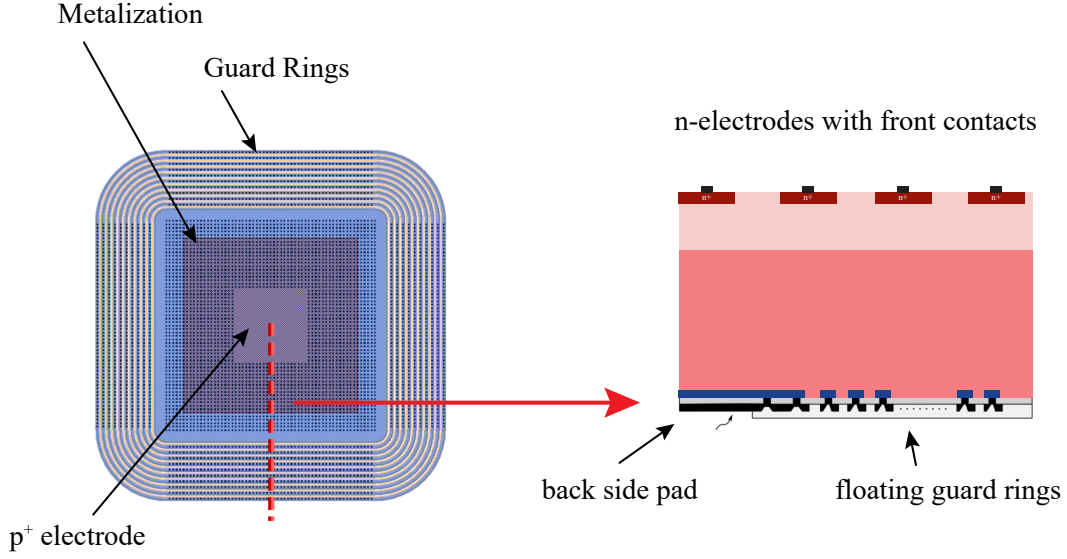
Figure 2.6: Backside guard ring layout of a diode test structure with GRN = 10 and a vertical cut of the test structure.

area. This is done to ensure that the electric field lines are identical in all the pixels in the matrix. Furthermore, a metallization is required to bias the whole junction with low resistivity to reduce voltage drops throughout the electrode. Unfortunately, if the whole surface is covered in metal the sensor would become blind to light. Thus, a window is designed in order to only have a metallic frame for the biasing of the back electrode.

Secondly, a set of guard rings around the p$^+$ electrode is necessary. In fact, it is well known that the performance and stability of a silicon sensor can be improved by adopting guard ring structures around the electrodes [13]. In particular, various studies have been done via TCAD simulations to select the best performing geometries for these termination structures.

Clearly, in the simulations the objective is to increase the operating region which is limited by the full-depletion voltage and the onset of punch-through and breakdown of the p$^+$-n diode.

The customization of the guard rings leads to a variation of the punch-through voltage and is, thus, fundamental to increase the sensor's performance.

The guard rings share the p+ doping with the p+ junction and have been simulated varying number and geometrical parameters. Another important factor is the number of surface traps at the backside interface, N$_{ox}$. These traps are generated during the manufacturing process due to the silicon to passivation interface creation technique. In particular, due to the low temperature oxide deposition, in place of thermal oxidation, a varying number of traps at the interface is produced. Thus,

the simulations also vary the trap density within the silicon near the guard rings.

As can be seen in figure 2.7, the breakdown voltage, defined as the voltage at which the backside current exceeds the value of $1\,\mu A$, increases with number of guard rings. This simulation has been evaluated on a domain similar to that in figure 2.3b, but with a $100\,\mu m$ thickness. On the right hand side of figure 2.7, the pitch optimum value results to be between 6 and $7\,\mu m$.

The adoption of a current threshold for the definition of the breakdown voltage is a conservative method to identify the breakdown voltage of devices where an abrupt variation of the current is not present [24].
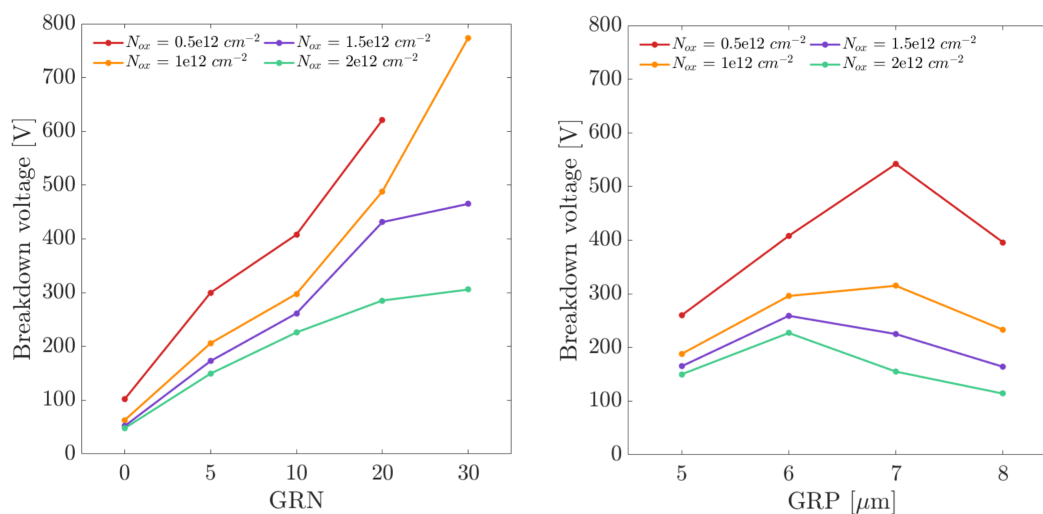
Figure 2.7: Study of the variation of the breakdown voltage with varying number of traps and on the *left* number of guard rings (GRN) and on the *right* pitch between the guard rings (GRP). The simulations have been done on a $100\,\mu m$ thick domain. More information in [24].

2.1.3 Pixel radiation tolerance

In order to predict the radiation tolerance of the ARCADIA sensors a set of simulations have been done varying the sensor geometry a doping profiles.

In particular, ionizing and non-ionizing radiation can damage various parts of the sensor both on the surface and in the bulk. On the surface, the damage, due to ionizing radiation, takes form of oxide charge build-up at the interface between the Si and Si_2 surfaces. On the other hand, considering also the device bulk, impinging non-ionizing radiation can create silicon crystal lattice defects which actively create new energy levels within the semiconductor band gap. These extra energy levels act as traps within the bulk and lead to a variation of the electrical properties of the

device by changing the depletion voltage (due to the effective doping concentration variation) and the leakage current of the sensor.

In order to predict the sensor damage in the most realistic manner as possible the *new Perugia model* has been adopted [54, 63].

An example of the effects of radiation damage is shown in figure 2.8. Here, the variation of the signal from a single pixel is shown. The results show a good response to incoming radiation up to 10^14 neq/cm^2. Furthermore, the CCE timings are shown in the bottom plot showing the time required for integrating 95% and 99% of the total generated charge.
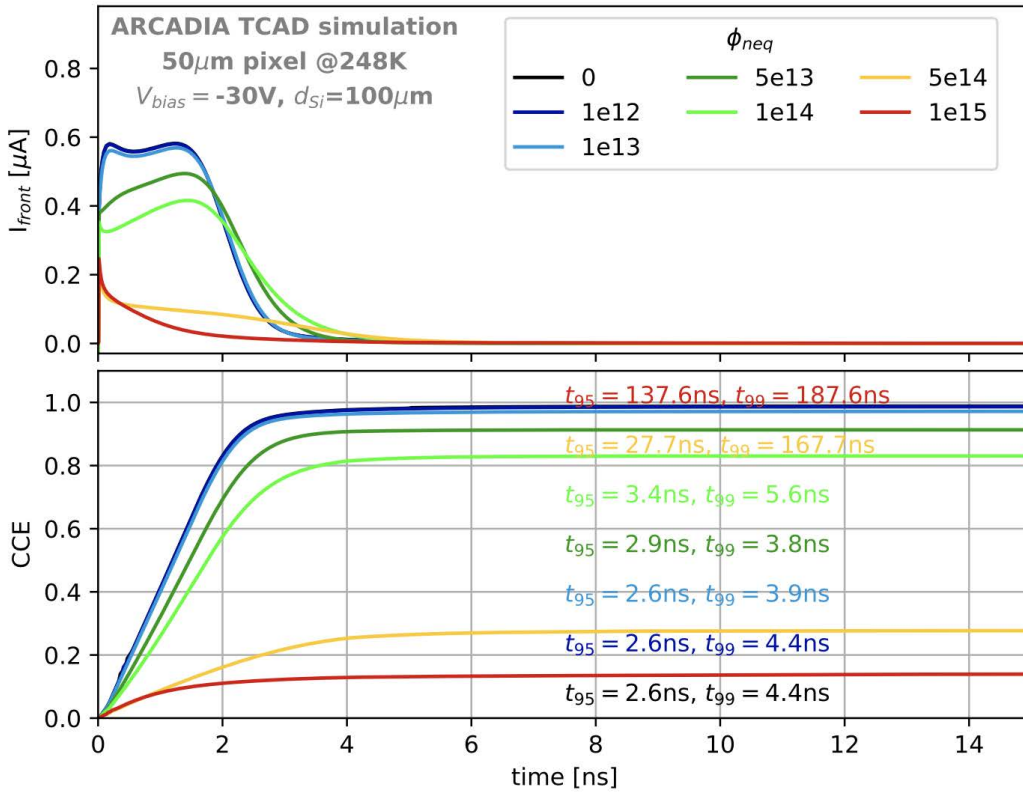
Figure 2.8: Pixel current radiation damage effects [56]. On *top* the currents simulated in a single $50 \times 50 \, \mu m^2$ pixel at a temperature of 248 K. At the *bottom* the total collection times are shown. The simulated fluxes range from 0 to 10^{15} neq/cm^2.

2.2   ARCADIA test structures

In order to test the concept and functionality of the simulated sensors, a set of test structures has been designed and produced. At the end of the section. in figure 2.14, a photograph showing part of the produced test structures can be found. In chapter 3 the most significant results of the test structures described in this section will be shown.

2.2.1   Passive Test Structures

In the first engineering run, within the SEED project, a set of passive test structures has been produced. The test structures have been fitted in a $2 \times 2\,\text{mm}^2$ area chip and designed in 110 nm CIS process. The structures were laid out with simplicity in mind making the test procedures as easy as possible. Nevertheless, these structures have been produced with the same double side process adopted for the fully depleted MAPS. This implies that the test chip has different testable structures on the two sides. The scope of these structures is to study the sensor properties like depletion, leakage, breakdown and radiation tolerance.

The passive structures include:

- Set of 8 diodes;

- A gated diode;

- MOS capacitance;

- Pseudo-matrices.

The chips have been produced in 3 different thicknesses: $100\,\mu\text{m}$, $300\,\mu\text{m}$ and $400\,\mu\text{m}$. Each thickness is expected, following the simulation results, to have different operating regions and, obviously, different full-depletion voltages. The diodes and the MOS capacitor are testable from the backside which is visible in figure 2.9, while the pseudo-matrices must be tested from the front as will be explained in the next subsections.
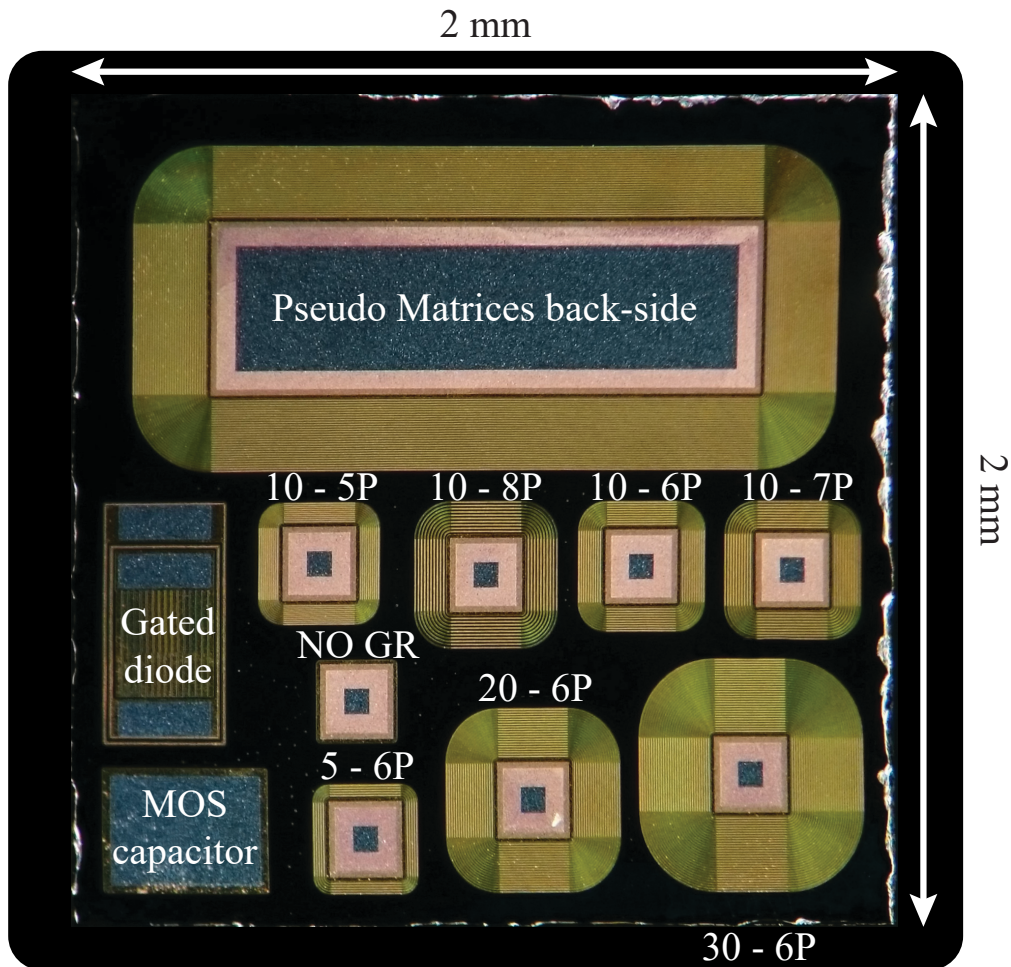
Figure 2.9: Photograph of the back side of the produced test structures. The pseudo-matrices backside p$^+$ implant is visible on the top, while on the bottom left the MOS capacitor and gated diode are shown. A large area of the chip is dedicated to the study of the p$^+$-n-substrate diodes and the number of guard rings adopted. The first number indicates the GR number, while the second indicates the pitch in µm.

Test diodes

Within the test structures chip there are 8 diodes. A layout example of the backside of the diodes is on the left in figure 2.6. The number of p$^+$ guard rings varies from 0 to 30, while the pitch varies from 5 to 8 µm. Since the depletion volume starts from the back p$^+$-n-sub junction it's extension is not influenced by the top p-wells. Thus, the diodes exhibit a set of collecting n$^+$ electrodes on the

top which can all be biased at the same time in order to study the variability of their characteristics with varying number of guard rings or their pitch.

The area of each diode is $200 \times 200\,\mu m^2$. The biasing of each one can be done through a metallization frame surrounding the p$^+$ implant. As expected, and simulated in figure 2.7, an increase in number of guard rings and a small pitch between them increase the stability of the structures leading to a higher breakdown voltage. Nevertheless, when increasing the number of guard rings also the area required for their proper design increases decreasing that available for the sensor back electrode. For this reason, a trade-off between the area for the guard rings and the minimum acceptable breakdown voltage has to be weighed.

The backside structures and the designed test diodes are photographed in figure 2.9. The diode performance can be evaluated by studying their I-V curves.

On the chip, two study sets can be identified. The first set of diodes adopts a pitch of $6\,\mu m$ with three different GRN = 5, 20 and 30 guard rings. The second set includes 4 diodes each with 10 rings, but varying pitch of 5, 6, 7 and $8\,\mu m$. Lastly, a diode without guard rings and a gated diode have been included. The latter can be tested to study the surface generation velocity, while, the former, shows the early breakdown effect due to no GR adoption.

Pseudo-matrices
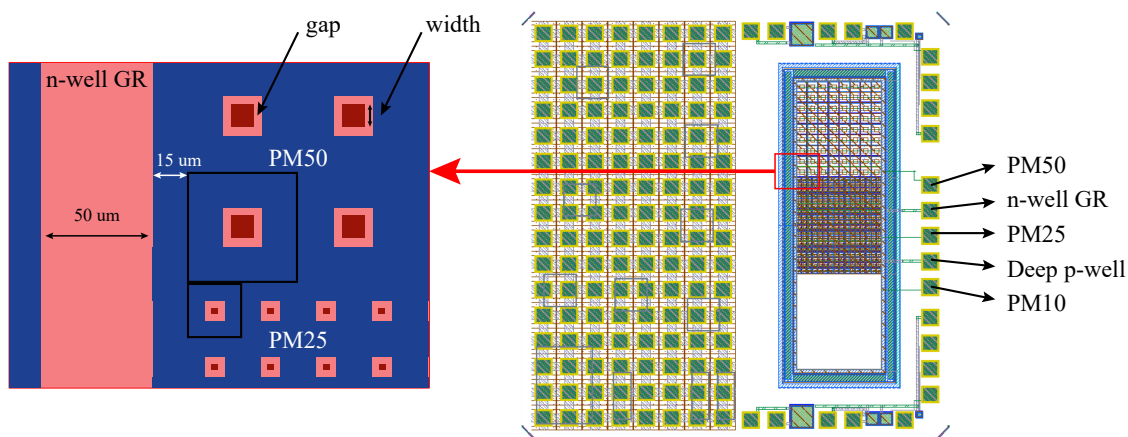
Figure 2.10: Test structures layout. *left* An illustration of the area between PM50 and PM25 is zoomed into. *right* The layout of the front-side of the test structures. All the yellow squares represent the metal pads for external contact. On the left side of the chip an 8×16 array of pads is found which can be used to bias the collecting electrodes above the test structure's diodes.

A pseudo-matrix (PM) is a set of passive collecting electrodes connected in parallel. In particular, the chip includes three sets of electrode arrays with varying

electrode pitches. The pitches chosen for production are 50 µm, 25 µm and 10 µm. The matrices are arranged in a set of 8×9, 16×18 and 40×45 pixels. The three arrays are surrounded by a single 50 µm wide n-well guard ring on the front side in order to collect stray carriers generated outside the active volume. The GR-to-pixel-border distance is 15 µm and it includes both a p-well and a deep p-well. On the back side of the PMs a structure similar to that seen in the diode is present. In fact, a p^+ implant covering the whole area of the arrays framed by a metallic plate used to bias the diode has been designed on the back. In order to stabilize the sensor depletion, a set of 10 floating guard rings has been implemented surrounding the back side p^+ electrode.

Differently from the diodes, these test structures must be tested from the front side of the chip. In fact, as can be seen in figure 2.10 *right* there are 5 dedicated pads designed for the biasing of the pseudo-matrices, p-wells and the n-well guard ring.

Pitch [µm]	50	25	10
Gap [µm]	5	5	3.75
Electrode size [µm]	10	5	2.5

Table 2.1: Pseudo-matrices electrode geometries.

2.2.2 Active Test Structures

Within the ARCADIA engineering run wafers, also a set of active test structures are present. In particular, the wafers, with an 8-inch diameter, include 3 important test structures:

- The ARCADIA main demonstrator;

- A process evaluation FD-MAPS named MATISSE;

- A fully depleted monolithic strip detector.

ARCADIA Main Demonstrator
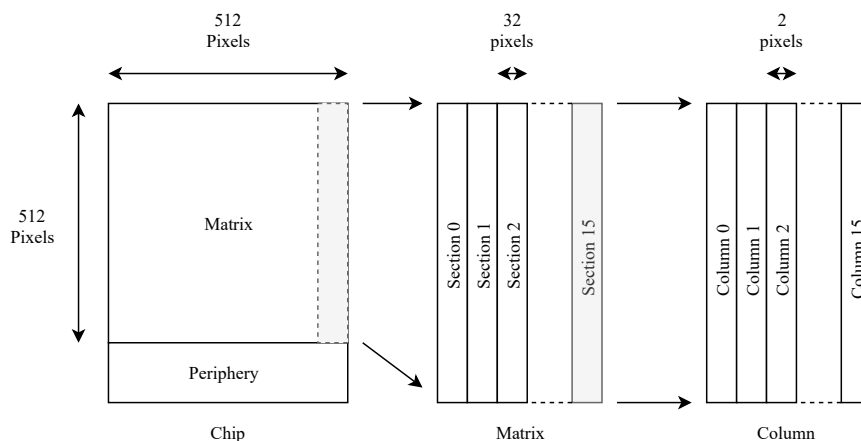
Figure 2.11: Illustration of the ARCADIA Main Demonstrator pixel matrix organization.

The ARCADIA main demonstrator is a FD-MAPS which scope is to demonstrate the manufacturability at a large scale of the technology adopted. In particular, the active sensor features a $25 \times 25\,\mathrm{\mu m}^2$ pixel area enclosed in a 512×512 pixels array. The matrix core is side abuttable which implies that a total of $2.56 \times 1.28\,\mathrm{cm}^2$ total active area enclosing 1024×512 pixels is possible. Once the FD-MAPS has been tested and verified to be fully functional, the next step will be the scaling of the matrix, end of column (EoC) and data links up to 2048×2048 pixels via wafer stitching.

The demonstrator is designed to withstand an event rate up to $100\,\mathrm{MHz/cm}^2$ with a trigger-less binary data readout. The dissipated power with this hit rate capability is $20\,\mathrm{mW/cm}^2$. However, in order to render the device usable in space applications a low power mode consuming half the power is available.

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The pixel readout is organized in 16 sections composed of 16 double columns of 2×512 pixels as shown in figure 2.11. The column is divided in 2×2 pixel cores which are read out in a master-slave configuration in order to decrease the data rate from the pixel regions to the EOC. In the high rate capability readout mode, each section has its own output unit while in low power mode only one output section will be activated.

MATISSE
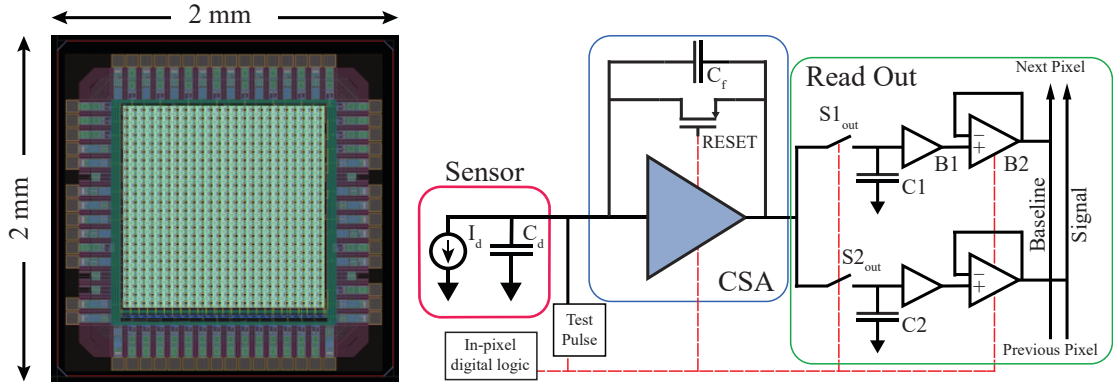
Figure 2.12: MATISSE Layout and Read-Out logic. *left* The layout of the MA-TISSE ASIC. *right* The block logic of the single pixel logic.

Inherited from the SEED project, MATISSE (Monolithic AcTIve pixel SenSor Electronics) is a fully depleted MAPS based on the sensor structure described in chapter 2. The ASIC has demonstrated the small-scale manufacturability of the monolithic ensemble and is included in the ARCADIA engineering run in two flavors [59, 60, 58, 32, 61]. The first flavor is the standard FD-MAPS found in the SEED active test structures, while the second is a low power small scale demonstrator chip for space applications.

The ASIC is integrated into a $2 \times 2 \, \text{mm}^2$ package and exhibits a $50 \, \mu\text{m}$ pixel pitch. The backside p^+ implant area, which defines the active area of the sensor, is $1.25 \, \text{mm} \times 1.25 \, \text{mm}$. In the SEED engineering run the thicknesses, which define the active volume of the sensor, produced ranged from 100 to $400 \, \mu\text{m}$. Considering the prototypic scope of the ASIC, the designed array encloses 24×24 pixels with a global shutter acquisition. The front-end adopted is a charge sensitive amplifier with correlated double sampling. The maximum readout rate possible is of $5 \, \text{MHz}$.

Furthermore, in order to study the variation of the input capacitance with size and radiation damage, two versions of MATISSE have been produced each with their matrix divided in 4 sectors each having a different collecting electrode geometry.

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The layout of the produced monolithic sensor is shown on the left in figure 2.12, while on the right the block logic of a single pixel is illustrated. The layout shows the pads designed on all four sides and, at the bottom of the pixel array, the EoC is present. The EoC uses a rolling shutter acquisition process to extract the data from the array. On the right side of figure 2.12, from left to right, the sensor scheme, the charge sensitive front-end amplifier and the output buffers are shown. The two busses on the right, used for the correlated double sampling, can be seen, adopting which firstly the baseline and then the integrated signal are sent to the FPGA.

Monolithic Strips
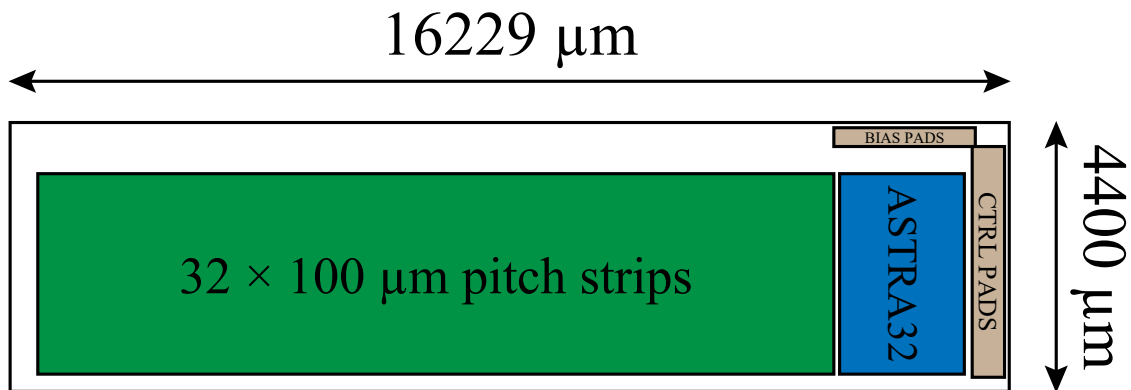
Figure 2.13: Illustration of the Monolithic Strips included in the engineering run of the ARCADIA collaboration.

The last monolithic active sensor designed within the ARCADIA engineering run is an array of pixelated strips. The strips adopt the same sensors verified in the SEED engineering run through MATISSE and the pseudo-matrices. The concept of the microstrips is illustrated in figure 2.13 and adopts a front-end designed in the same 110 nm technology as the main demonstrator and MATISSE. In the first engineering runs, the electronics have not been embedded within the strip p-wells in order to easily test and verify the performance of the electronic chip with commercial strips by producing the same layout on a separate chip. The design of the pixel-to-electronics layout assembly and read-out electronics chain will be discussed in depth in chapters 4 and 5.

Figure 2.14: Microphotograph some of the new test structures included in the first engineering run of the ARCADIA collaboration. The long test structures are passive microstrips with different pitches, while the square ones are mostly pseudo matrices with different pixel geometries. At the bottom an active pixel array has been included to test new readout architectures.

Chapter 3

Experimental Campaigns

Due to the innovative nature of the FD-MAPS developed by the ARCADIA collaboration a full set of experiments has been done on both passive and active test structures. Regarding the former, a large characterization campaign has been carried out including:

- IV and CV curves on the diodes and pseudo-matrices;

- Light irradiation tests on the pseudo-matrices;

- Proton beam irradiation tests on the pseudo-matrices.

Considering the monolithic nature of the FD-MAPS, a stable test-bench must be designed. In the following tests, the devices are firmly located onto metallic plates adopting conductive tape or, if specified, adopting conductive glue. This has been done due to the small size of the test structures. In particular, the back biasing chuck on which prototypes are usually positioned has a suction pump with a 1 mm diameter hole, this leads to positioning difficulties and the possibility of the back structures not perfectly adhering to the biasing chuck. Which would, in turn, lead to electro-static discharges (ESD) due to air's dielectric rupture at the high voltages in play.

When studying the pseudo matrices, the tested device list, on which the scans have been performed on, is in table 3.2.

The chapter will be divided into experimental sections with the test setup and the test results for each characterization. In the last section, a summary of results on the active test structure, MATISSE, is given.

3.1 I-V curves
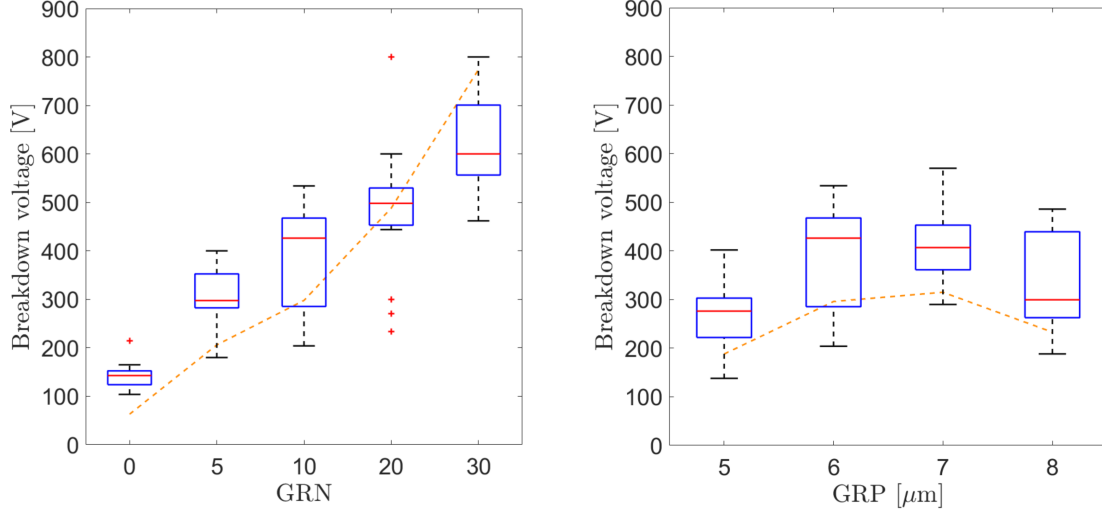
Figure 3.1: Diode GRN and GRP test results from 22 devices extracted from 7 different wafers [24]. On the *left* the increase of the breakdown voltage correlated to the GR number is plotted. The *red* dots indicate the outliers. On the *right*, the breakdown voltage to GR pitch correlation is shown. In both plots, the simulation results for an oxide charge of $1 \times 10^{12}\,\mathrm{cm}^{-2}$ are plotted with an *orange* dotted line.

Considering the passive test structures described in section 2.2, a set of I-V and C-V characterization tests have been done on the produced devices. In particular, the IV curves have been performed on the diodes and pseudo-matrices in order to study the operating region of the latter and the breakdown voltage of the former. On the other hand, through CV curves on the pseudo matrices, the characterization of the collecting electrode capacitance is possible. The paragraph will describe the experimental test-benches adopted for both characterizations. The results in this section are published in [32, 24]

3.1.1 Test Setup

Two sets of tests have been performed. A set studying the variation of the breakdown voltage with varying guard ring number or pitch and another studying the onset of depletion within the pseudo-matrices. The first tests set required probing the test chips from the backside (seen in figure 2.9) while the second set was performed by bonding the pseudo matrices pads to a PCB in order to render the devices easier to handle. The I-V characterization of the sensor has been carried out using a KEYSIGHT B1505A power device analyzer.

3.1.2   Test Results

Diodes

The test results of the diode probing are shown in figure 3.1. The experimental results fit the simulations shown in figure 2.7. As expected, the breakdown voltage increases with the guard ring number indicating that a higher number of guard rings lead to a more stable substrate depletion. Studying the right plot, the expected result of a most stable GR pitch configuration at a pitch between 6 and 7 µm is shown.

Pseudo Matrices
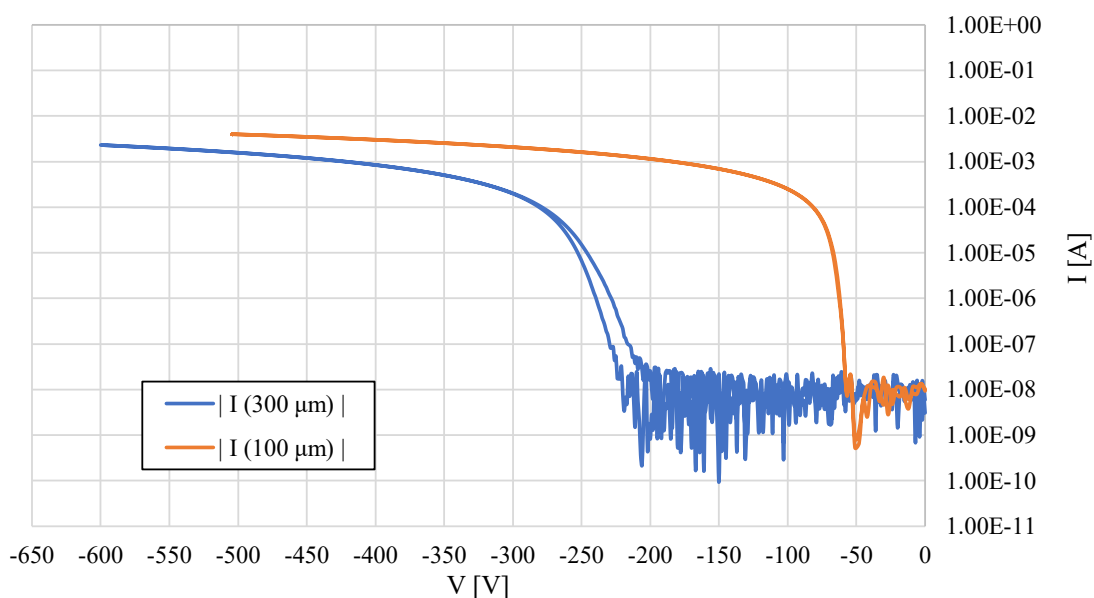
Figure 3.2: Experimental I-V curves showing the punch through effect for 100 and 300 µm thick PM sensors.

Following the diode tests, the pseudo matrices electrical characterization has been done. The characterization yields information on the onset of full depletion and the different punch-through voltages between the 100 and 300 µm thick sensors.

In order to perform these tests, each pseudo matrix has been connected to its pad and individually tested with voltage sweeps on both the backside voltages and collecting electrode biasing voltage.

By sweeping the high voltage at the back of the sensors, the onset of the punch-through is extracted and the results are shown in figure 3.2. Due to the different thickness of the sensors tested and following equation 1.3, the punch through voltage

is smaller, in absolute value, in the $100\,\mu m$ thick sensor compared to the thicker one.

When not explicitly mentioned, the diode voltage has been fixed to $1.2\,V$, while the p-wells were tied to GND.

To find the different full depletion voltages the current of the single pseudo matrices is shown in figure 3.3. Considering both thicknesses, two regions are identifiable. The first region, at low backside voltages, exhibits a higher current due to intra-pixel and pixel to GR currents. As the voltage increases, the current sharply decreases as the charges within the resistive paths below the central pixels are removed by the depletion region. Once the whole pseudo-matrix is engulfed in the depletion region, the second region is identifiable indicating the full sensor depletion. The currents measured in this region are dark currents and the variation between the different thicknesses could be due to different wafer process conditions.

Finally, in order to optimize the operating region of the different sensors and their correlation to the electrode biasing voltage, a set of I-V curves has been extracted for each bias. The curves are presented in figure 3.4. Here, the broadening of the operating region with the increase of the front-side electrode biasing voltage is clearly visible. This effect is expected due to the depletion of the region near the collecting electrodes (within the epitaxial layer) with increasing bias voltage. This effect helps the depletion region, starting from the back, to reach the top electrodes at lower, in absolute value, backside biasing voltages.
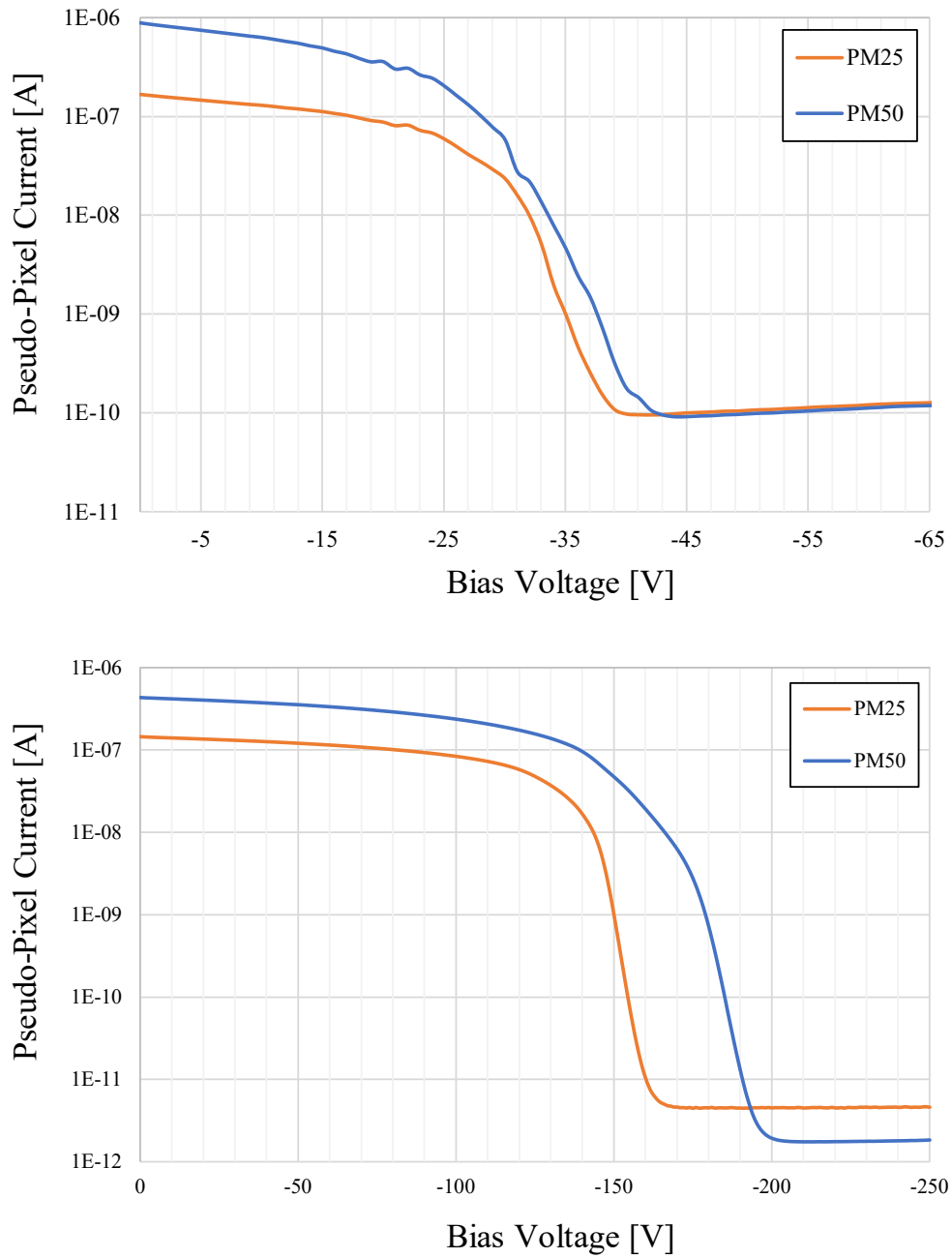
Figure 3.3: Experimental I-V Curves showing the full depletion voltage for 100 and 300 µm thick PM sensors and different pixel pitches. The electrodes were biased at $V_{bias} = 1.2 V$.
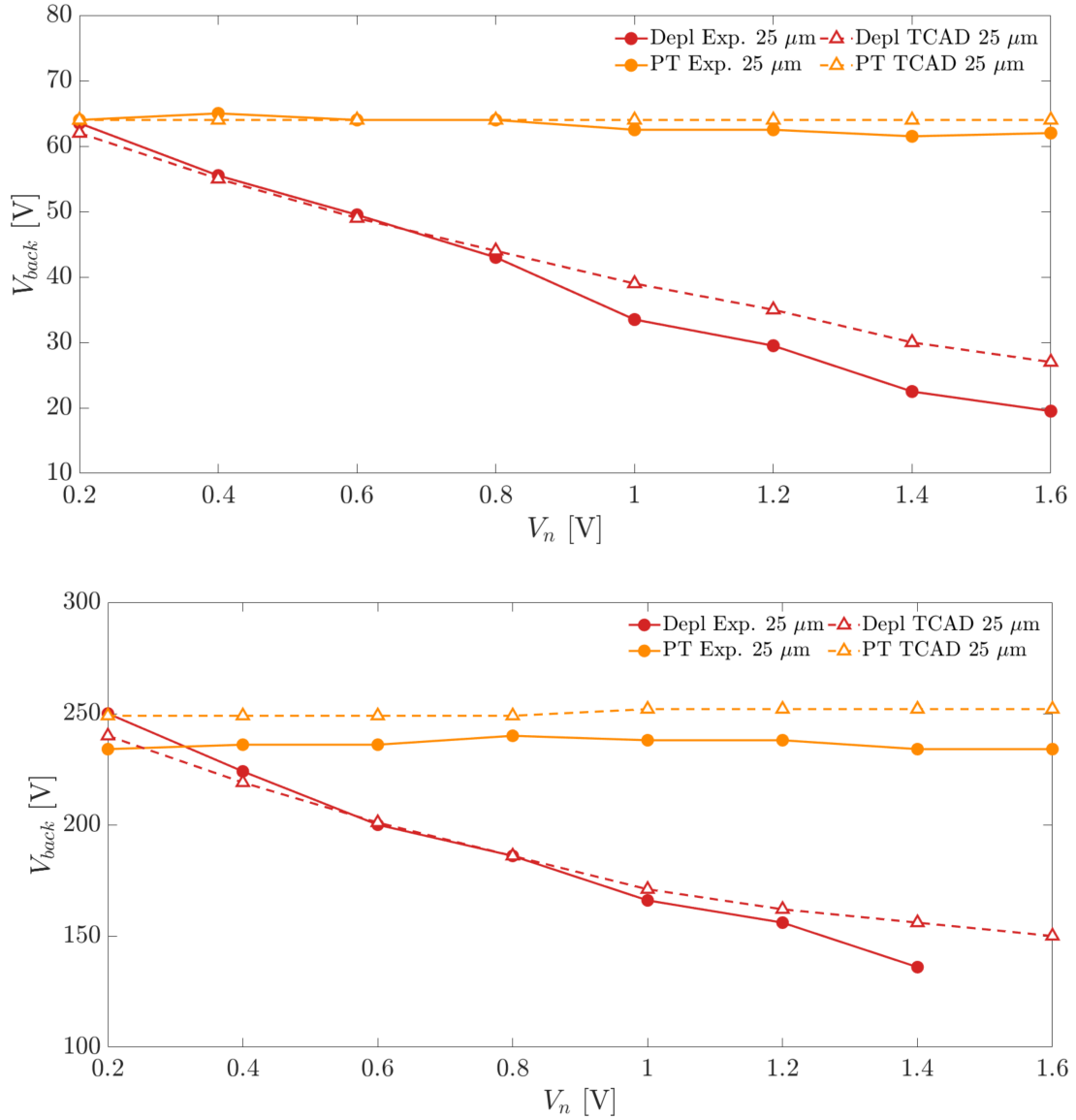
Figure 3.4: Operation region to V_n correlation for different thicknesses. The curves show the broadening of the operating region with increasing electrode bias voltage, V_n. [24]

C-V Curve

In order to validate the sensor capacitance, a C-V curve has been performed using the same KEYSIGHT B1505A power device analyzer. The resulting plot, shown in figure 3.5, has been evaluated setting the analyzer in the parallel capacitance model mode, a 10 kHz frquency and a voltage step of 1 V. The C-V curve proves that the onset of depletion, where the curve flattens, is, as expected, above 140 V. This result, paired with the I-V curves in the previous paragraph, proves the correct sensor depletion. As expected, due to depletion of the substrate, the capacitance drops sharply to a stable value after depletion from 22 pF to ≈ 1 pF in agreement with the simulated results.
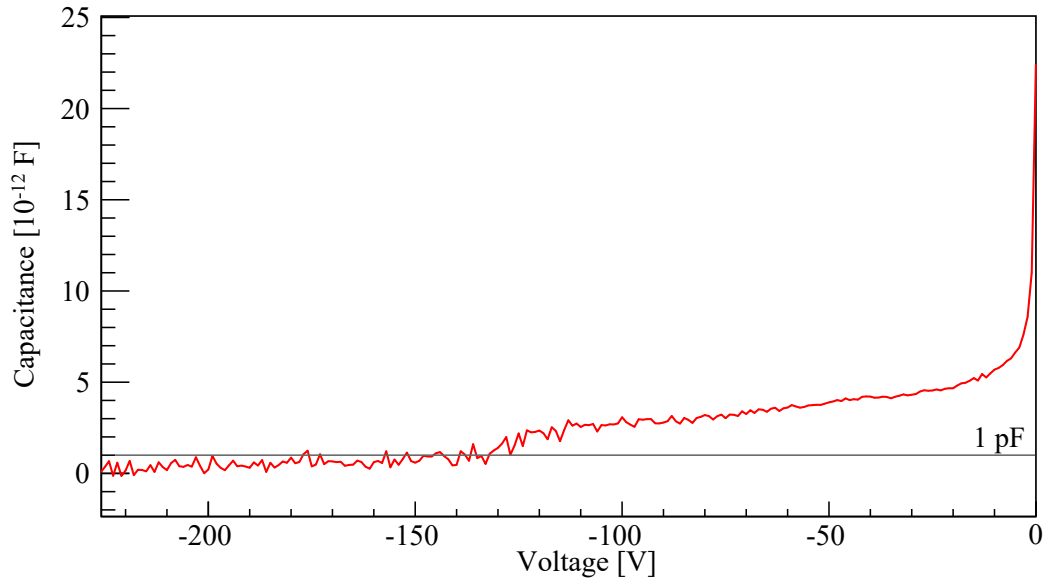
Figure 3.5: Experimental C-V curve showing the 50 µm pitch array capacitance before and after full depletion for a 300 µm thick PM sensors. The electrodes were biased at a DC voltage $V_{bias} = 1.2$ V, with a 10 kHz frequency [32].

3.2 Light irradiation
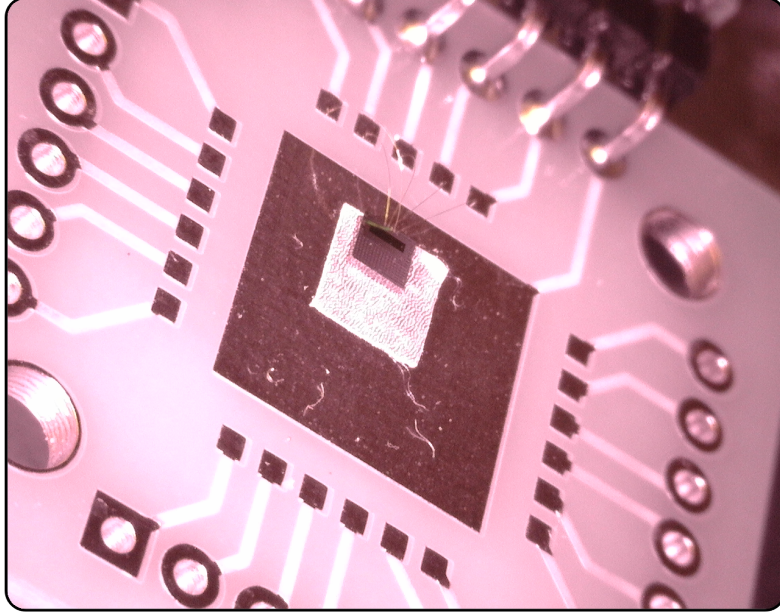
Figure 3.6: Picture of the test structures under UV light during positioning.

For the light irradiation tests the $25\,\mu$m pixel pitch pseudo matrices have been picked scanning the central area. The light sources adopted were a $\lambda_{IR} = 1064\,$nm and a $\lambda_{red} = 660\,$nm wavelength LASER sources. The output difference between the two light sources depends on the penetration depth in silicon. In particular, λ_{IR}, $\mathrm{x}_{depth} \approx 800\,\mu$m, is not fully absorbed in the $300\,\mu$m sensor implying that the ionization trail is similar to that of minimum ionizing particles (MIP). On the other hand, λ_{red} is fully absorbed within the first 3 to $5\,\mu$m yielding information on the structure and charge collection profiles of the surface. Moreover, due to the shallow penetration depth comparable to that of the deep p-wells, these structures are identifiable through this scan due to the fact that charge couples generated within these areas are not collected by the n$^+$ electrode. The tests have been carried out at the Ruđer Bošković Institute in Zagreb with a transient current technique setup provided by Particulars [43, 17] and the results are published in [31].

3.2.1 Test Setup
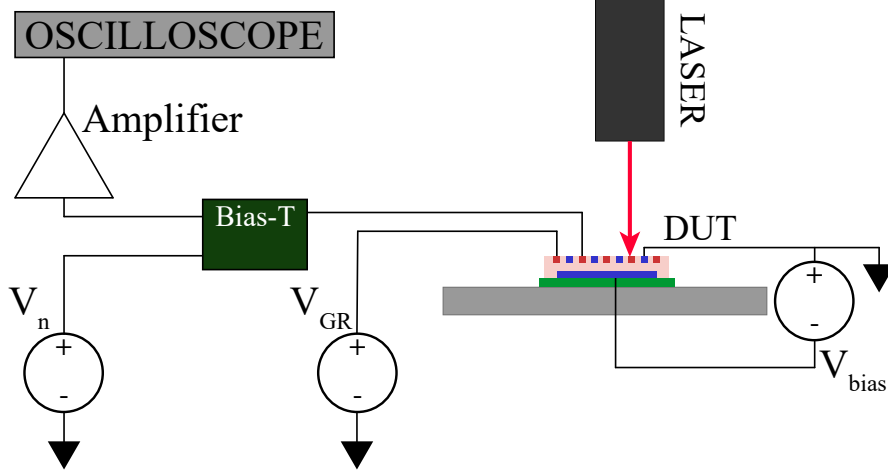
Figure 3.7: Illustration of the LASER setup adopted for the PM25 matrix scan. A Bias-T is adopted to decouple the high-frequency signal from the DC biasing voltage of the collecting electrodes.

The test-bench setup can be seen in figure 3.7. The sample is firmly located onto a micrometrically controlled stage which is directed perpendicularly to the incoming LASER beam.

Considering the passive nature of the pseudo matrices, the signal coming from the pixels requires biasing and amplification. This can be achieved at the same time through the usage of a Bias-T. The device decouples the DC voltage provided to the collecting electrodes from the AC component which is formed when current passes through the detector due to impinging radiation. In particular, the signal, collected from the electrode, after the Particulars BT-01 Bias-T is amplified by a Particulars wide-band amplifier providing a 53 dB gain.

The laser beam profile can be modified by varying the peak power, frequency and collimation. In particular, the parameters adopted are in table 3.1.

Wavelength [nm]	1064	660
Collimation [%]	40	60
Frequency [Hz]	50	50
Peak Power [mW]	100	10

Table 3.1: TCT parameters adopted for the surface and bulk scans with light sources with wavelengths $\lambda_{IR} = 1064$ nm and $\lambda_{red} = 660$ nm.

3.2.2   Test Results
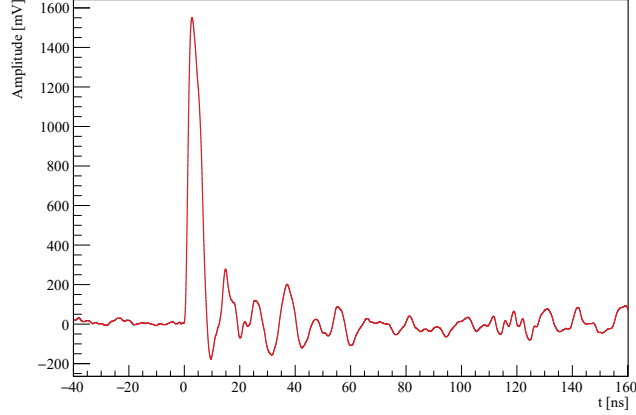
Figure 3.8: Output waveform acquired at the chain end after λ_{IR} LASER light has impinged on the 25 μm pseudo matrices.

Once the sensor has been positioned, a functionality test has been done hitting the pixels with the λ_{IR} LASER light. A sampled waveform is shown in figure 3.8. Here the charge collection speed is noticeable, in fact, the signal is mostly included within the first 8ns. This value has been picked as the integration time, T_{int}, for both the λ_{IR} and λ_{red} scans.

The results of the tests with λ_{IR} are shown in figure 3.9. Here, a $100 \times 100 \, \mu m^2$ cut of the scanned area is shown. In particular, each cell value is proportional to the integrated value of the first T_{int} of the output waveform. As expected, only the metal lines stack, which reflects light, is clearly visible in the map. The width of the stack in the acquired map is compatible with the designed width. The acquisition of a signal at the metal stack location is due to the laser beam profile being wider than the metal stack width.

A set of vertical cuts have been done in order to extract the standard deviation over value ratio. The low value extracted, s = 3.9%, implies a high charge collection uniformity.

Furthermore, a numerical integration has been done to evaluate the number of MIPs acquired. In particular, a waveform over the metal lines and one over the collection electrodes have been integrated yielding:

$$\begin{cases} I_{IR,n-well} = 14.45 \text{ nWb}, \\ I_{IR,metal} = 8.47 \text{ nWb}. \end{cases} \tag{3.1}$$

A rough estimation implies, for the sensor thickness adopted, ≈ 170 MIP crossings. Interestingly, studying the ratio of the signals and not taking into account

the beam profile, the maximum effective beam spot diameter can be estimated as $d < 20$ µm.

Adopting the second LASER wavelength, λ_{red}, the same area has been scanned and is shown in figure 3.10. As expected, the integrated signals in the deep p-well areas, which do not collect charge, are lower than the collecting electrode areas. This is due to the penetration depth of λ_{red} being only superficial and, thus, not deep enough to ionize charges below the deep p-wells.

With this set of tests the full depletion of the sensor substrate has been proved considering:

- the high sensitivity below the p-wells adopting λ_{IR};

- the equivalent charge collection efficiency below the n-wells and p-wells when adopting λ_{IR};

- the 8 ns time required for complete charge collection, which implies drift-dominated collection dynamics.
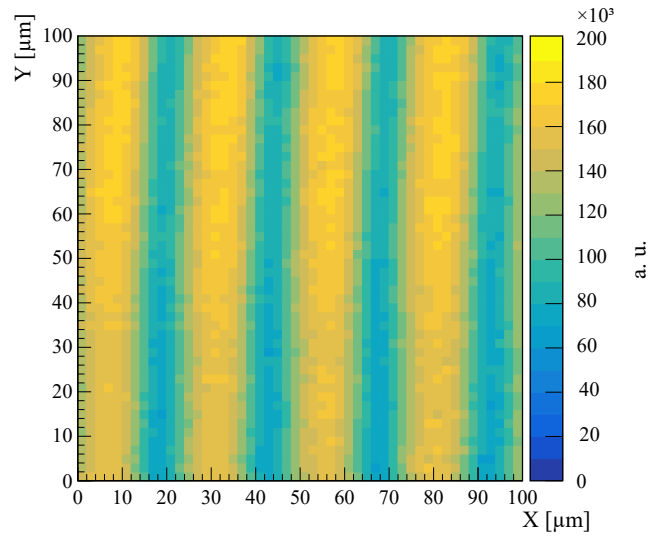
Figure 3.9: TCT scan of a $100\,\mu m \times 100\,\mu m$ sensor area using the $\lambda_{IR} = 1064\,nm$ laser source [31].
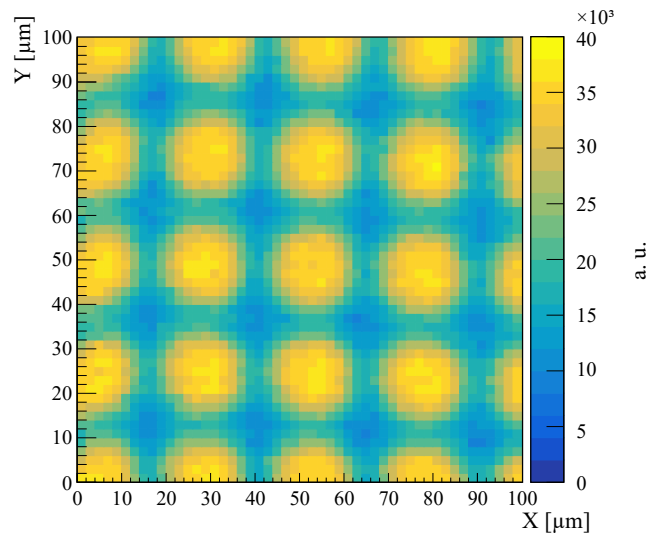
Figure 3.10: TCT integral scan of the previously studied $100\,\mu m \times 100\,\mu m$ sensor area using the $\lambda_{red} = 660\,nm$ laser source [31].

3.3 Proton beam
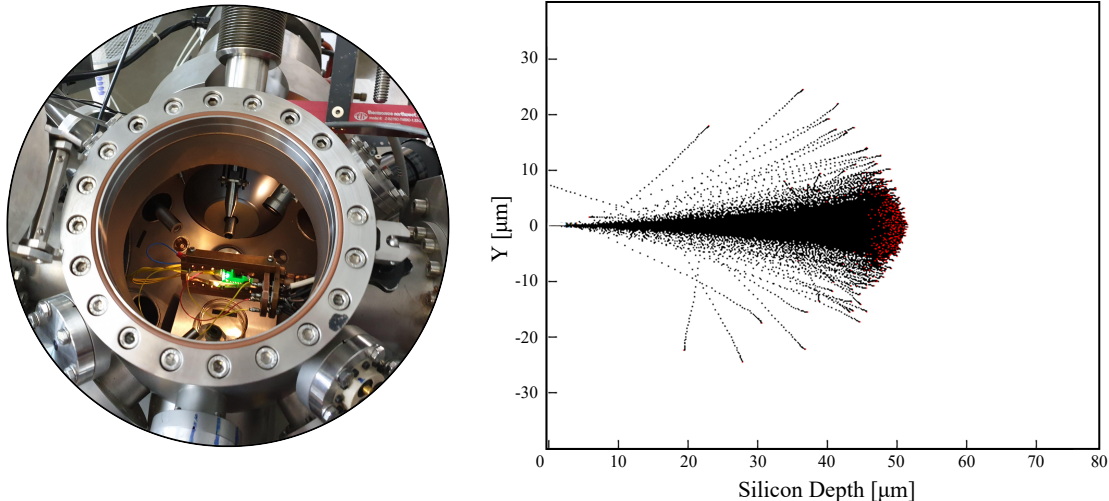
Figure 3.11: *left* Picture of test structures set-up within the vacuum chamber. *right* 2 MeV proton penetration depth in silicon. Simulation run with SRIM [79]. The first 2.32 µm of the simulated material are the metal lines (Al), while the remaining material is silicon.

In order to fully characterize the pseudo matrices and prove the charge collection efficiency uniformity with different sensors (sensors tested in table 3.2), a set of proton beam irradiation tests have been operated onto the passive MAPS. The experiments adopted the ion beam induced charge (IBIC) technique at the microbeam facility of the Ruđer Bošković Institute in Zagreb [41]. A picture of the sensors within the chamber is shown on the left of figure 3.11. The facility is capable of generating a microbeam focused up to $\sigma_{\mathrm{spot}} \approx 2\,\mu\mathrm{m}$. The beam is generated through a 1 MV Tandetron accelerator capable of accelerating protons from 0.5 to 2 MeV. Yielding a maximum penetration depth of $\lambda \approx 47\,\mu\mathrm{m}$ in silicon, as shown in figure 3.11. This implies that the signal output must be identical in both the 100 and 300 µm thick sensors. The experimental results in this section have been published in [61].

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Sensor type	Thickness [µm]	Pixel Pitch [µm²]
PM	100	$25 \times 25,\ 50 \times 50$
PM	300	$25 \times 25,\ 50 \times 50$

PM Pixel pitch [µm]	# of pseudo-pixels	Metal width [µm]
25×25	16×18	8
50×50	8×9	15

Table 3.2: Tested Sensor samples

3.3.1 Test Setup
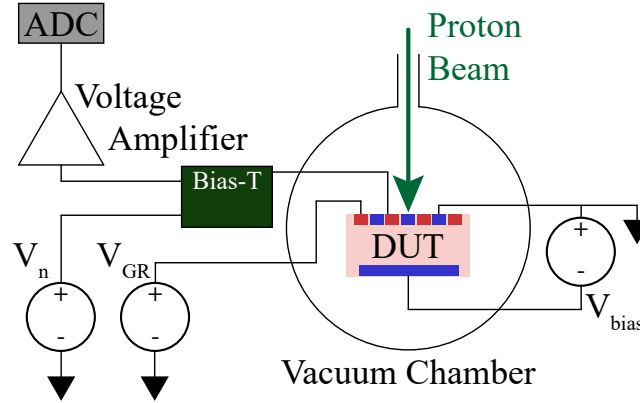
Figure 3.12: Proton microbeam test setup illustration.

The test bench adopted is illustrated in figure 3.12. The beam energy has been set in order to accelerate protons up to 2 MeV. By adopting a calibration reticle the beam has been focused to $\sigma_{\text{spot}} \approx 2\,\mu\text{m}$. The low and high voltages have been supplied respectively with a HAMEG HMP2030 power supply and an NHQ 202M. In a similar fashion, as per the light irradiation tests, a Bias-T has been connected to the pseudo-matrices. The adopted device is a 20 mV/MeV gain ORTEC 142-A preamplifier. In series to the Bias-T, an ORTEC 570 voltage amplifier and a CANBERRA 8075 12 bit 10 V ADC have been connected.

Through preliminary testing, the particle hit frequency has been set to 2 kHz in order to maximize the gain and SNR of the readout chain without signal pile-up. The final output gain, per impinging particle energy, is estimated as follows:

$$G = G_1 \times G_2 = 20\,\frac{\text{mV}}{\text{MeV}} \times 1.5 \times 100\,\frac{\text{mV}}{\text{mV}} = 3\,\frac{\text{V}}{\text{MeV}} \tag{3.2}$$

where G_1 and G_2 are, respectively, the preamplifier and voltage amplifier gain.

Considering the maximum beam energy, E = 2 MeV, which is fully absorbed within the first 60 μm of silicon, the following theoretical output voltage is expected:

$$V_{th} = G \times E \approx 6\,\text{V} \tag{3.3}$$

3.3.2 Test Results
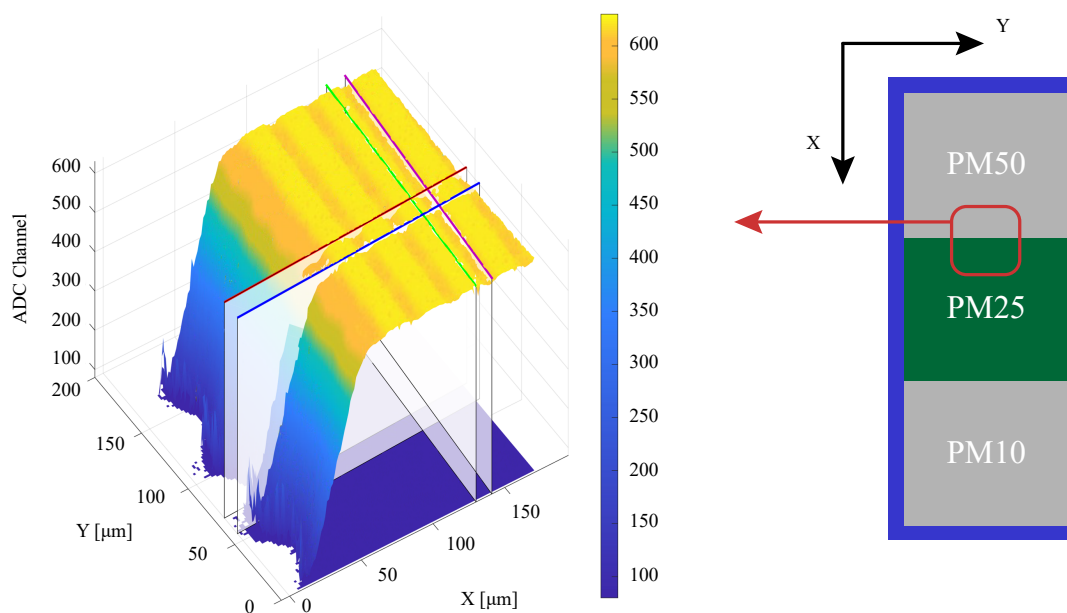
Figure 3.13: 3D plot showing a 100 μm thick sensor PM25 edge. The 50 μm pitch profile near the Y axis is due to the charge collection effect of the PM50, also biased and able to collect charges.

After focusing the 2 MeV proton beams to a $\sigma_{\text{spot}} \approx 2$ μm various sets of bi-dimensional scans, composed of 128×128 points, were performed varying the sensor bias voltage. Various areas of the sensor have been studied, both at the center of the matrices and at the edges near the GRs and nearby PMs. The scope has been to measure the uniformity of the CCE, by scanning the PM centers, and to characterize the boundary between the pixels and the guard rings. A 3D figure is shown (fig. 3.13) of the 100 μm thick sensor edge. In particular, the adopted structure is the PM25. Interestingly, due to the biasing of the nearby PM50 collecting electrodes, a competitive charge collection effect arises drawing a 50 μm pitch charge collection outside the PM25 collecting volume. Various cuts have been performed on the maps in order to evaluate the CCE uniformity along the n-wells (green) and metals (purple). Extra cuts applied perpendicularly have been performed to evaluate the

energy loss above the metal lines and are depicted as the blue and red lines. In particular, the former indicates a cut above the n^+ electrodes and the latter a cut above the p-wells.

A comprehensive comparison of 2 different thicknesses and pixel pitches is shown in figure 3.14. The output is plotted in ADC channels and can be converted adopting equation 3.2. The left plots refer to a 100 µm thick sensor with a 50 µm pixel pitch, while the right ones refer to a 300 µm thick sensor with 25 µm pixel pitch. The top figures show the acquired maps in full depletion where, in particular, the adopted voltages are $V_{100\,\mu m} = 60\,V$ and $V_{300\,\mu m} = 200\,V$. In the two top figures, the cut lines are also shown and are plotted in the four bottom figures. The center figures show the first cuts which refer to the horizontal cuts along the n^+ collecting electrodes. The ADC output loss is due to the 2.32 µm thick metal stack energy absorption. As expected the signal values are identical in both sensors due to the Bragg peak being well within the detecting volume of both thicknesses. The second set of cuts, plotted in the bottom figures, have been performed vertically along the collecting electrodes and perpendicular to the PM edge.

Analyzing the uniform n-well regions in the top plots and the maps in the central regions, the mean value of $V_n = 6.10\,V$ is extracted once the sensor is fully depleted which agrees fully with the predicted value.

On the other hand, due to Lorentzian energy losses in the metals, the mean value is $V_n \approx 5.98\,V$. The value implies a 2% charge collection reduction, differently from the expected value of 3.5%. However, this discrepancy is due to the small width of the metal lines, namely 15 µm and 8 µm, which render impossible the disentanglement between a uniform response area and the finite spot size.

Interestingly, studying the bottom plots in figure 3.14, the charge sharing between the pixels and guard ring can be studied. In this case, an expected difference between the 100 µm and the 300 µm thick sensors is visible. In fact, the collected charge in the 100 µm sensor rises from 10% to 90% in 22 µm independently of the reverse bias. On the other hand, in the 300 µm sensor, the width of the transition region decreases from 34 µm to 26 µm as the reverse bias increases. These results are in good agreement with the ARCADIA simulations of the charge sharing between competing collecting structures found in [61].
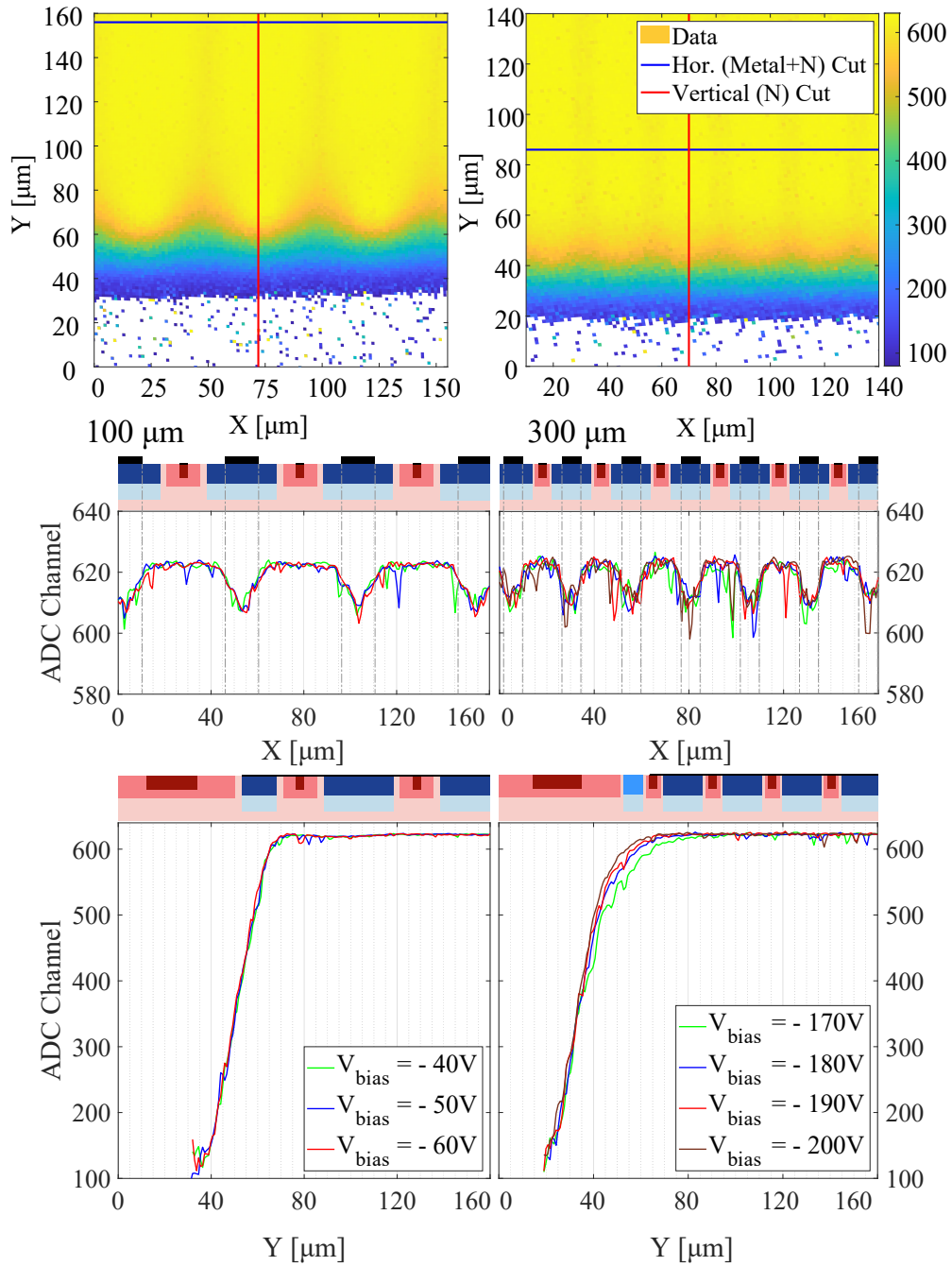
Figure 3.14: 2D plot showing a 100 µm thick sensor PM50 edge and a 300 µm thick sensor PM25 edge, both near the GR. Explanation in the text.

3.4   MATISSE tests

Differently from the previous devices, MATISSE also includes fully functioning CMOS electronics. This implies the need to test both the sensor and the electronics. A set of full depletion tests and electronics validation has been done.

In particular, the sensor's full depletion can be verified by flip chip testing the pn junction. Secondly, once connected to the DAQ, the electronics are able to detect the variation of the leakage current after full depletion. The experimental results in this section are published in [32, 61].

3.4.1   Sensor characterization

In order to verify the sensor functionality, the chip is flipped and adhered with conductive tape to a metalized plate. This implies that all the connectivity pads are biased at the same voltage from the top. By probing the back metallization, an IV curve, shown in figure 3.15, can be generated which yields the same punch through voltage results as seen in the passive test structures.
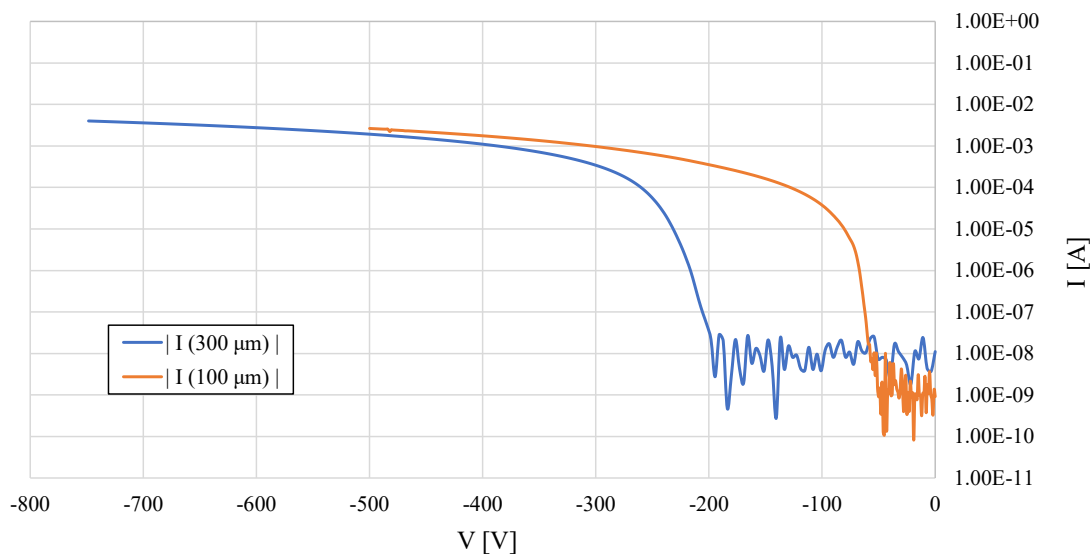
Figure 3.15: Plot showing the punch through voltages for different thicknesses of the MATISSE sensor.

3.4.2   Electronic characterization

The first electronics test is the linearity of the front end characterization. In particular, through a charge injection circuit, seen in figure 3.16a, an input voltage step can be used to characterize the linearity of the front-end. The adopted topology
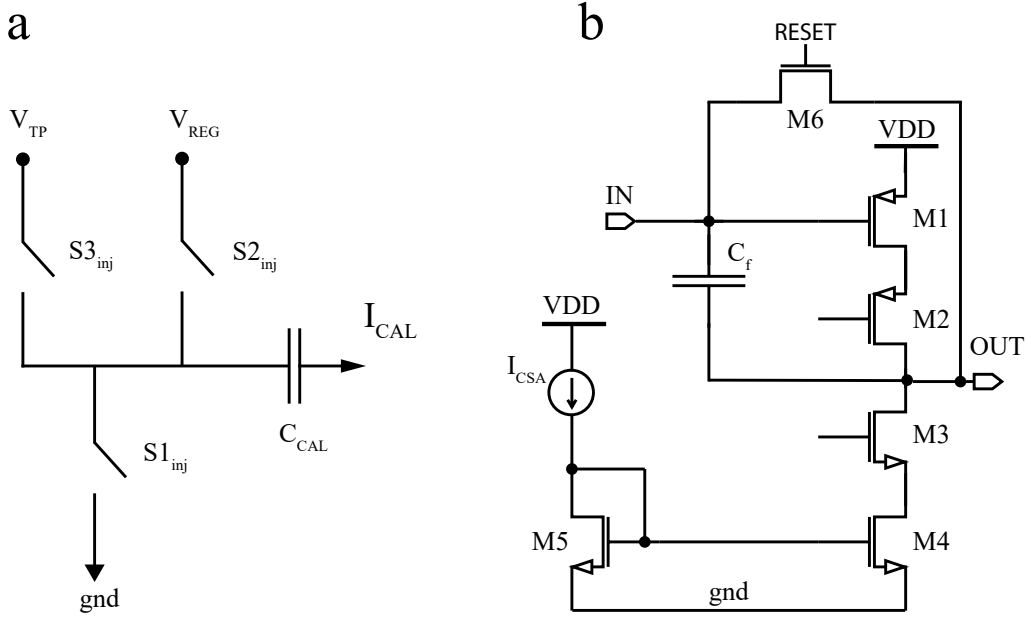
Figure 3.16: *a* Injection circuit found at the input node of the CSA; *b* Schematic level of the CSA adopted for the MATISSE FD-MAPS.

is that of a telescopic cascode charge sensitive amplifier (CSA), as seen in figure 3.16b. By tuning the output baseline to V= 400 mV the cascode current source, transistors M4 and M3, is kept in saturation and capable of biasing the CSA with a reasonable voltage margin.

The resulting linearity of the front-end is shown in figure 3.17. Here a range from 0 to 2.4 fC has been set. The expected gain through schematic and post-layout simulations is, respectively, $G_{sch} = 150$ mV/fC and $G_{p.l.} = 131$ mV/fC, while the experimentally measured gain is $G_{exp} = 118.7$ mV/fC. The discrepancy is due to parasitic capacitances which, in parallel with the feedback capacitance, reduce the effective closed-loop gain of the amplifier.

3.4.3   Electronic and sensor characterization

The second electronics test is the verification of the sensor depletion through the analysis of the reset voltage of the MATISSE front-end during the ramp up of the backside biasing voltage. In this case, by enabling the front-end reset, the feedback resistor actively short circuits the input and the output making it possible to sample the voltage at the electrode node. The voltage at the input node is set by the front-end biasing nodes to a $V_{in} = 0.8$ V. The result in figure 3.18 shows the depletion voltage reaching the surface in the central pixels and then in the pixels on the chip edges. In particular, the blue area indicates that the parasitic currents

passing through the resistive paths below the un-depleted pixels and GRs discharge the feedback capacitor pulling down the voltage.

Lastly, adopting a 980 nm UV LASER source, a single pixel functionality test has been performed. In particular, through a specifically designed LASER tracking system, the tracking capacity with LASER pulses at 10 µs period has been tested. The preliminary results of the front-side tracking are shown in figure 3.19. The second row shows a signal spread among pixels with a central black pixel. The possible explanations are two.

The first reason may be attributed to a diffraction of the light when passing through the metals on top the electronics (visible in the zoomed image of the microphotograph at the bottom of figure 3.19). This effect can be excluded by repeating the tracking tests with back-side illumination tests. A modification of the setup is underway to answer this question.

The second possible reason can be that the LASER and the double sampling readout architecture are in sync effectively sampling the same charge value in the baseline and the signal integrating capacitors.
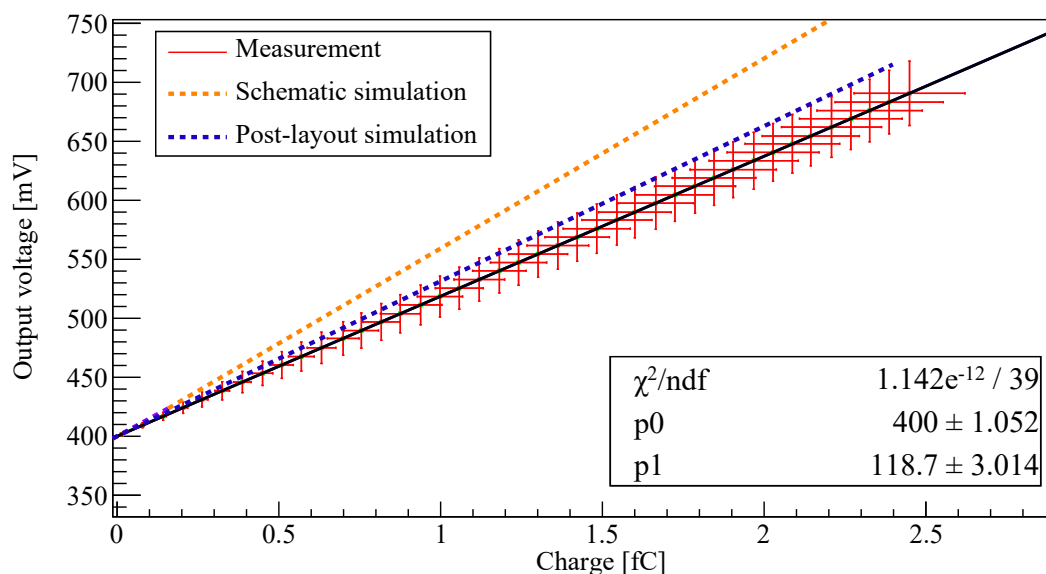
Figure 3.17: MATISSE front end linearity [32].
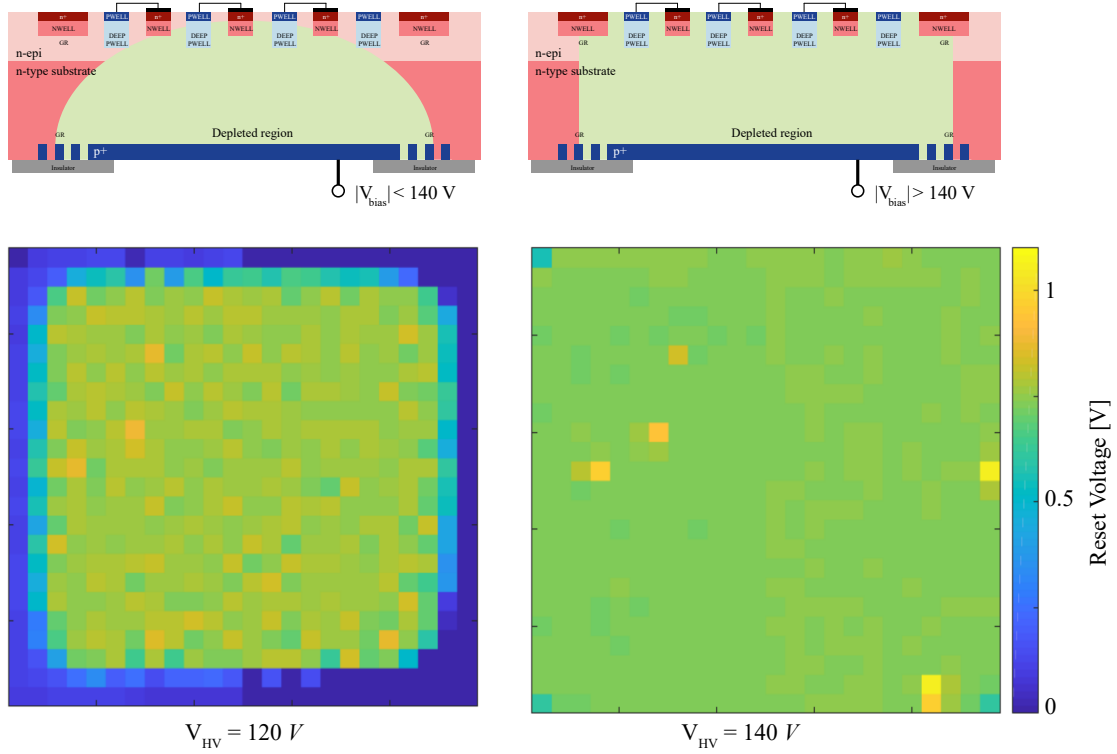
Figure 3.18: MATISSE depletion extraction through the front-end reset voltage [32].
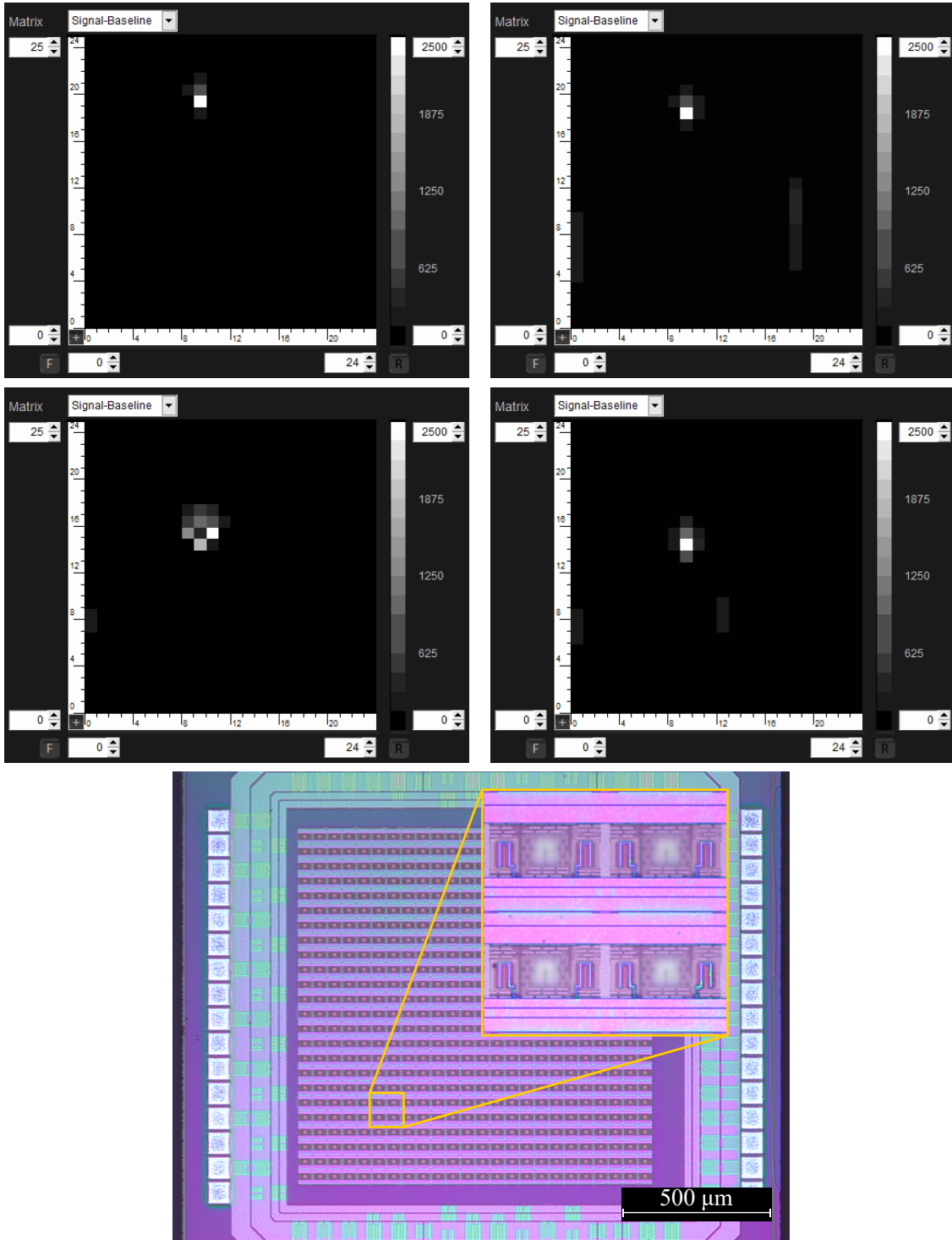
Figure 3.19: MATISSE LASER tracking functionality. The bottom image is a microphotograph of the MATISSE chip with a zoom in on a cluster of 4 pixels.

3.4.4 ^{55}Fe Characterization

The last tests on MATISSE have been performed with ^{55}Fe irradiation. Through the ADC bin separation of the ^{55}Fe X-ray peaks, the electronics can be calibrated and a good insight in the FD-MAPS resolution is extracted.

Firstly, an ^{55}Fe spectrum from all clusters is extracted for the calibration then, considering the different collecting electrodes shapes between sectors, a single sector has been picked to evaluate the single pixel resolution. The sensor was biased at $V_{HV} = -200\,V$ with an integration time of $12.8\,\mu s$. When studying a single sector the signal is acquired by picking seed pixels. A seed pixel is defined as a pixel where the SNR of the acquired signal is above 6. While a seed cluster is set of 5×5 matrix where the neighboring pixels have an SNR greater than 4.

The energy peak with all channels has a mean value of 439 ADC which leads to a gain, for the full readout chain, of $\approx 124\,mV/fC$. Considering the single pixel cluster, the energy resolution, defined as the full width half maximum, can be extracted. In particular, the resolution results to be $\sigma \approx 0.7\,keV$ for the $5.9\,keV$ photoelectrons centered at 449 ADC. Interestingly, the $6.5\,keV$ photoelectron peak is visible centered at 500 ADC.

From these results, the electronics noise is evaluated to be $\approx 40\,e^-$ at room temperature. All previous results are shown in figure 3.20.

Lastly, to study the charge sharing, the cluster size configurations for both front and back irradiation are plotted in figure 3.21. The clusters are limited to 4 pixels with a spill to a fifth in less than 1% of the total cases studied. This implies that the cluster shape is dictated by the photon conversion position proving a small charge sharing and a charge collection dominated by drift.
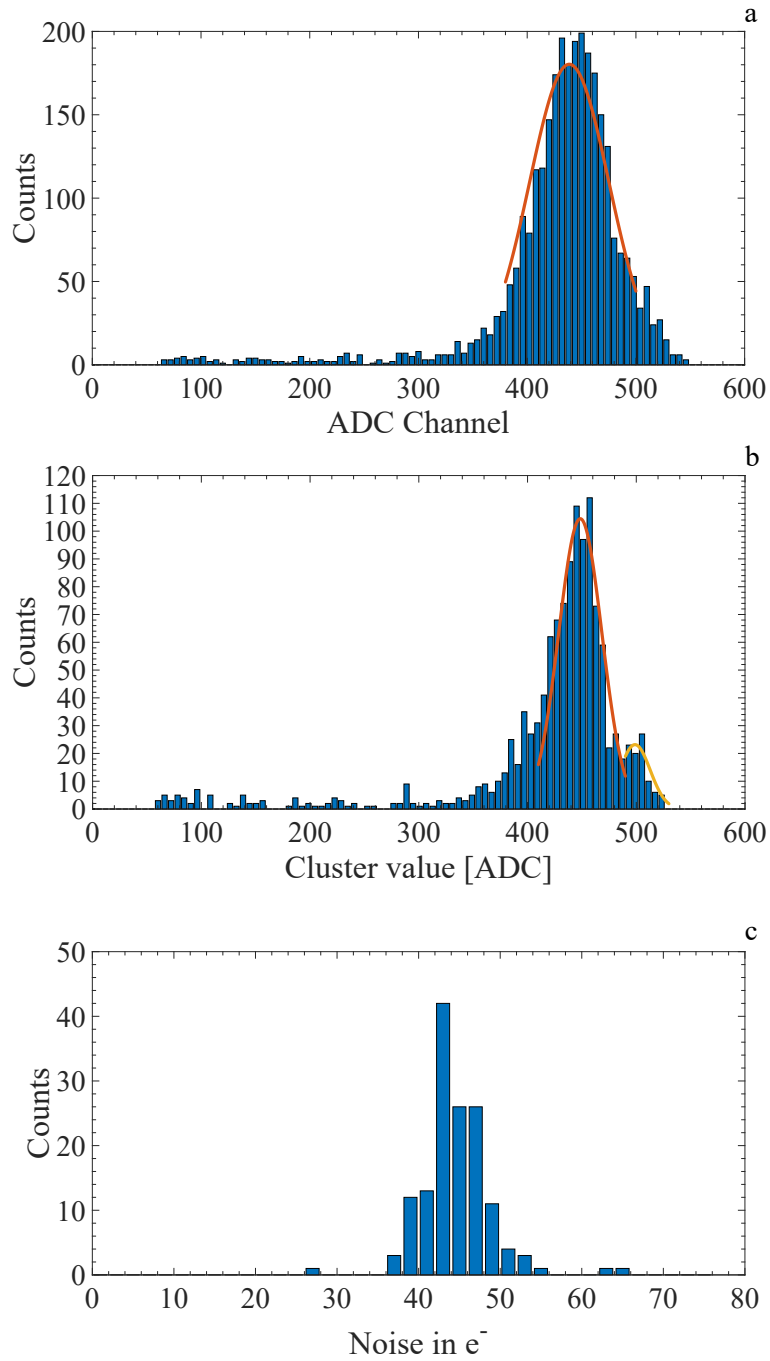
Figure 3.20: MATISSE ^{55}Fe X-ray results with bias voltage of -200 V. The *top* image shows the recontructed spectrum for all clusters, while, the *center* figure, of only the seed signals. The *bottom* figure, on the other hand, shows the evaluated noise in electrons [61].
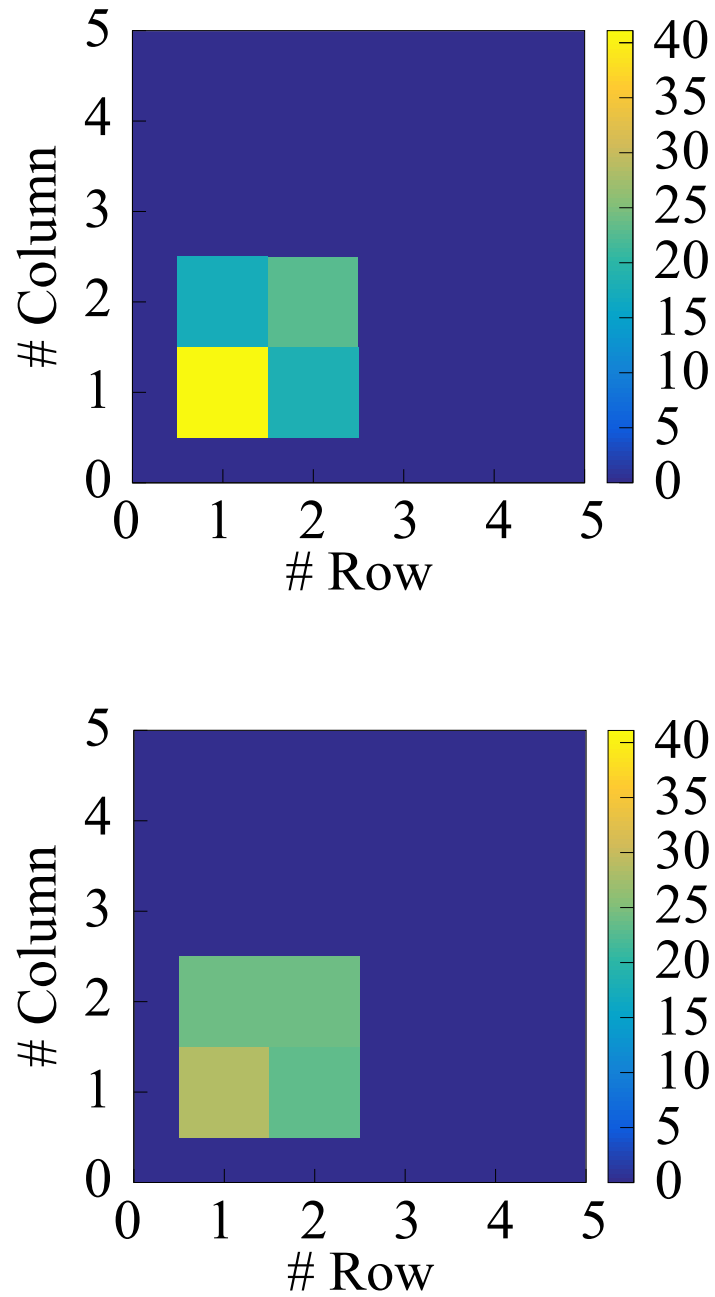
Figure 3.21: MATISSE ^{55}Fe X-ray cluster shape results with bias voltage of -200 V. The *top* image shows the clusters for front side illumination, while the *bottom* one shows the cluster shape for backside illumination [61].

Chapter 4

Monolithic Space Strips
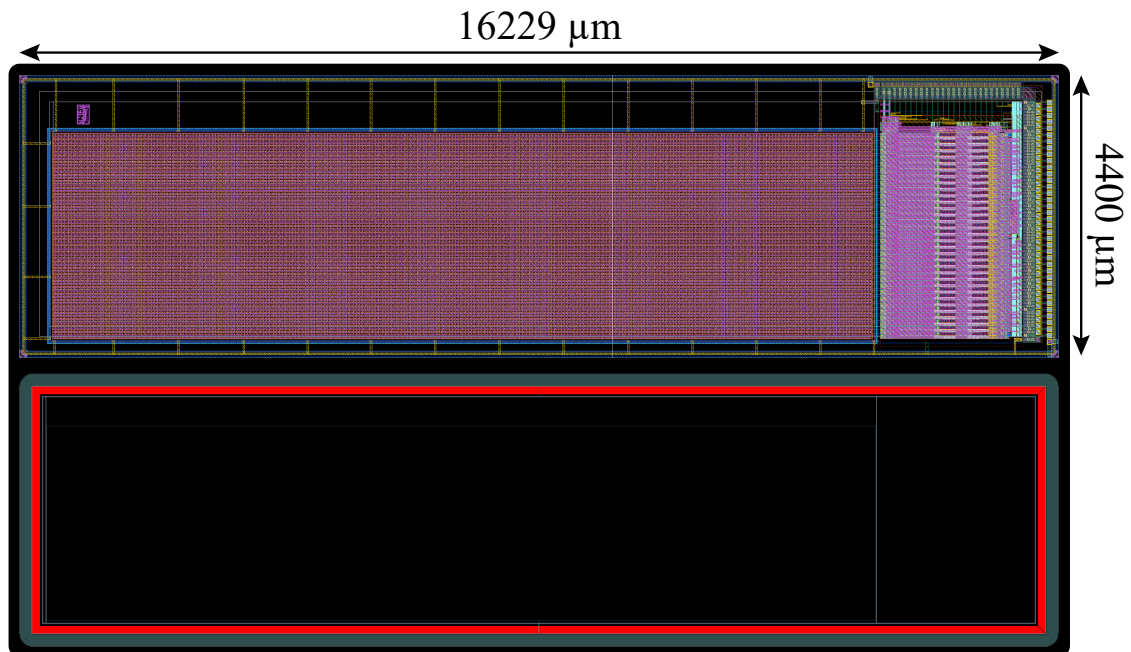
Figure 4.1: Layout of fully the depleted monolithic strips prototype. The *top* layout shows the top-side of the chip while the *bottom* shows the back-side. The bottom layout shows the guard rings in *gray* and the p$^+$ metallization biasing ring in *red*.

In the ARCADIA framework a novel design for a space strip sensor has been designed. Microstrips are commonly adopted in satellites and in low power applications where the particle fluxes are below a few kHz/cm^2.

By implementing the electronics within the silicon strip chip an increase in chip rigidity is achieved due to a large decrease in number of bondings in the detector chain. Similarly to state of the art MAPS, due to a direct sensor-to-front-end

connection, the stray capacitance at the input node influences sharply less the front-end and a lower current can be set in the biasing node leading to a lower power consumption.

Furthermore, the inclusion of the electronics within the microstrips area would drastically reduce the material budget and production steps leading to a reduction of payload and manufacturing costs.

The first version of the monolithic space strip detector, in figure 4.1, has been designed with a modular layout in order to characterize the electronics independently of the microstrips. The future versions envision the electronics fully included in the deep p-wells in the microstrips in order to allow wafer-level detector stitching. In this chapter, an overview of some layout peculiarities necessary to implement the first fully depleted monolithic microstrip design are explained. The next chapter, on the other hand, describes in depth the design process of the electronics included in the monolithic microstrips.

4.1   Sensor Design

The single microstrip found in the monolithic chip is composed of 2×256 pixels with a a $50\,\mu m$ pitch. Each pixelated microstrip is connected at the bottom to the front-end of the channel. In total the device includes 32 strips with a pitch of $100\,\mu m$ yielding a total sensitive area of $\approx 1.3\,mm^2$. The pixel design adopted is the same found in the $50\,\mu m$ pseudo matrices in order to use a well known and verified design, yielding a total detecting capacitor, C_D, between 5 and $10\,pF$. In particular, a $\approx 2\,\mu m$ n^+ collecting electrode is surrounded by an octagonal n implant $10\,\mu m$ wide. in total the collecting electrode n-well is a $18\,\mu m$ wide square surrounded by deep p-wells. A zoom in on the first pixel rows and interconnections between the electronics and the front end is shown in figure 4.2. Two metal lines running through the sixth metal layer, in pink, starting from the channel electronics are visible. The left-most Y-shaped lines connect the two pixel columns to the input PMOS of the front-end. On the other hand, the right-most straight line, connects the deep p-wells surrounding the pixels to the ground net of the electronics.

The first layer metal lines, in light blue, between the sensor and the electronics in figure 4.2 are required for the biasing of the p-wells and n-wells around the electronics and microstrips. In particular, the microstrips require an n-well around them to collect stray electrons generated in the depleted substrate outside the active sensor volume. The n-wells are surrounded by a p-well implant. The p-well is necessary to bias the default $1.2\,V$ implant the foundry deposits in the empty areas (in black) of the design. The n and p guard rings will be biased, respectively, to $V_n \approx 1.2\,V$ and $V_p = 0\,V$. The latter structures are, in fact, connected to the ground voltage of the electronics. The electronics enclosure design will be explained in the following sections.

70
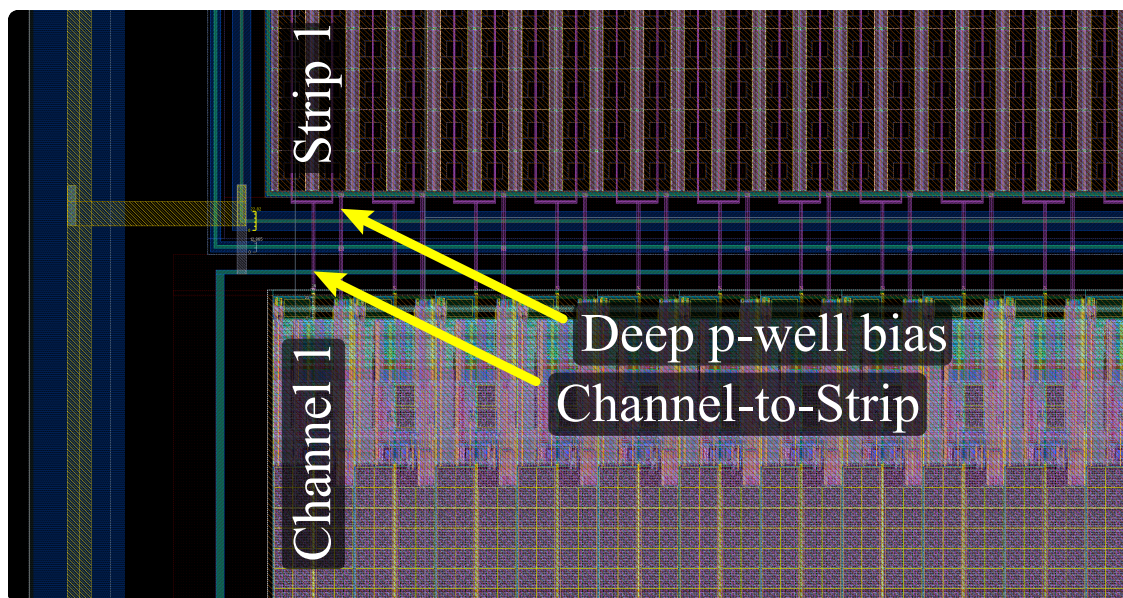
Figure 4.2: Monolithic front-end to microstrip interconnection layout. The arrows also show the GND connection to the deep p-wells. On the left side, the yellow metal biases the n-wells surrounding the microstrips and, as will be explained in section 4.2, the electronics.

4.1.1   In-Pixel Metal Density

The adoption of a commercial CMOS PDK implies the necessity to respect, in the whole design, a set of rules distributed to designers and evaluated by the CAD software. The software evaluates the design versus the rule list in a process called Design Rule Check (DRC).

One layout issue faced when designing the device has been to respect, above the sensor area, the minimum density threshold. In order to reduce R-C parasitics a tradeoff between the metal lines size and number has been evaluated through simulations. The minimization of the resistivity has been achieved adopting the whole metal stack above the pixel and running down the metals to the electronics. While the minimization of the parasitic capacitance has been done reducing the width of the metal lines. Nevertheless, this design effort is not sufficient to fulfill the minimum density required for production. Thus, a set of metallic stacks has been interleaved between the pixel columns above the deep p-wells. The placement of these metal lines ensures the manufacturability of the top sensor area.

In order to render the microstrips sensible to front-side illumination, a metal filler blocking layer has been superimposed on the pixel layout. This layer vetoes the automatic creation of metal fillers within the pixel layout which is one of the post-processing foundry manufacturability steps.

4.2 Electronics Enclosure
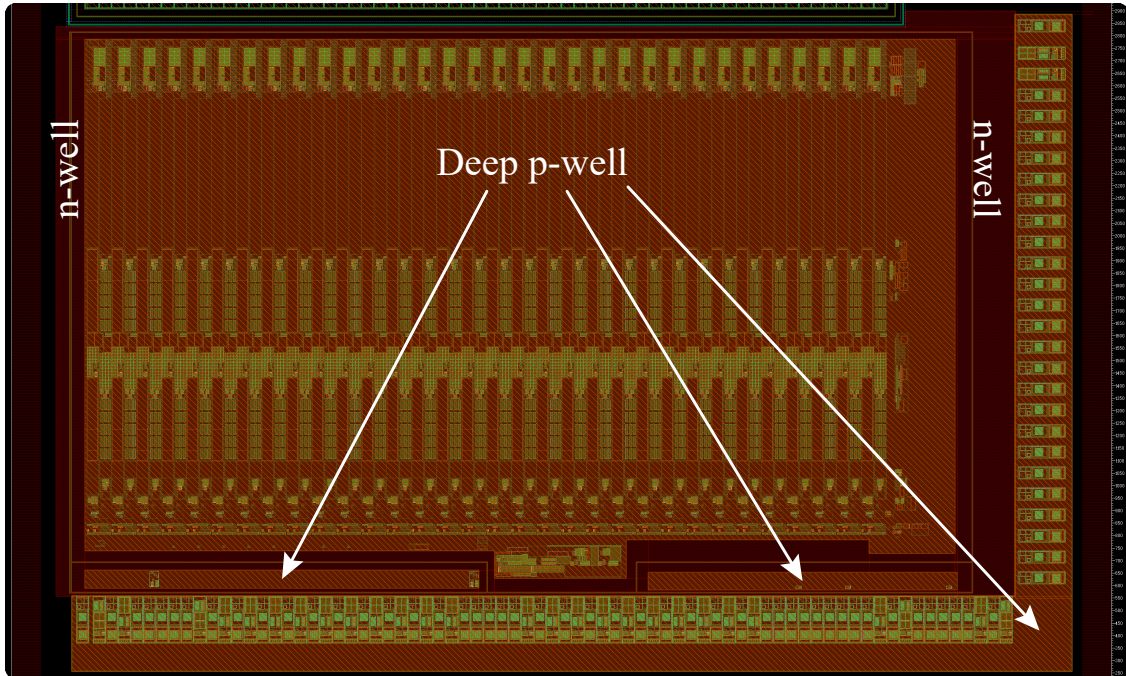
Figure 4.3: Electronics enclosure layout. The metal, poly-silicon and pad layers are hidden to focus on the n/p-well structures. The enclosure includes the deep p-well layer below the electronics in *orange* and the n-well guard rings which collect stray electrons generated in the substrate directly below the electronics in *red*.

Due to the monolithic nature of the device, the whole volume of the chip is sensitive to incoming radiation. In the case of a particle impinging in the substrate volume directly below the electronics, the charge couples generated could be carried to the n channel of the NMOS devices in the circuitry, effectively compromising the performance and stability of the electronics. To prevent this event, a large deep p-well, shown in figure 4.3, has been laid out below the electronics area which actively prevents the n implants from collecting charges. However, the uncollected electrons below the electronics would still diffuse below the electronics away from the high voltage applied to the p^+ back implant. This effect leads to noise in the deep p-wells and, consequently, in the ground level of the electronics. To eliminate this effect a n^+ collecting guard ring surrounding the electronics has been designed. The guard ring is biased at the same voltage as the external n^+ guard ring in order to collect stray electrons generated in the bulk below the electronics.

4.3   Top-Side Biasing

The chip includes a new type of biasing technique not yet explored within the ARCADIA collaboration. The technique enables the depletion of the substrate through specially designed pads on the top side of the chip. The pads are connected through the highest metal lines to a p-well structure that surrounds the boundary of the chip. From simulation results, the technique will be able to bias sensors up to 200 μm thick substrates without the need for back-side guard rings.

The structure is illustrated in figure 4.4 and the layout of the south-west pads shown in figure 4.5. In the latter, the high voltage pad is shown and is composed of a metal stack running from metal layer 4 to 6 in order to sustain the voltages necessary for biasing and not exhibit ESD with bottom metals. The blue dotted area on the west side is a rendering artifact showing the edge structures area and not a layer 1 metal area.
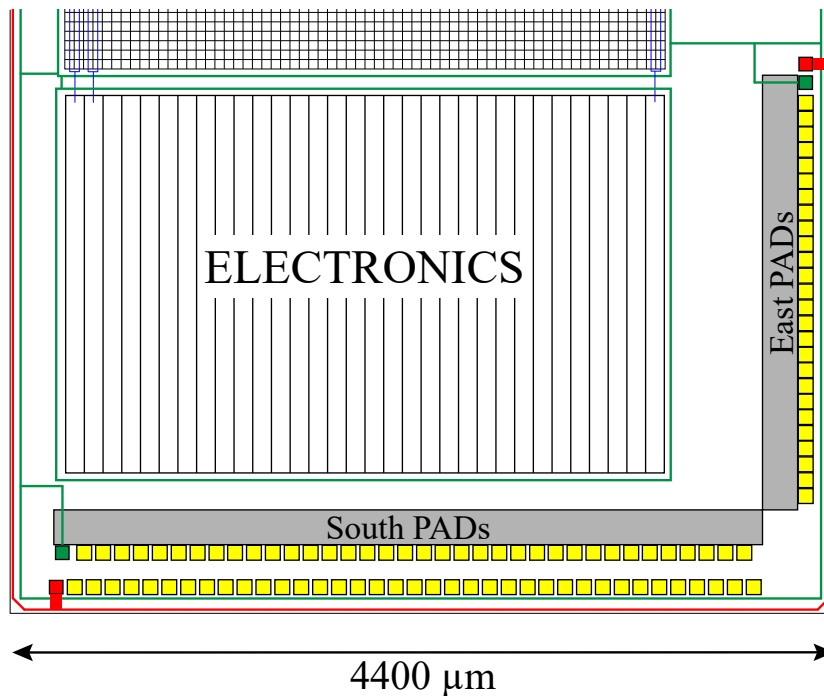
Figure 4.4: Illustration of the biasing structures surrounding the electronics and the south side of the chip. The *green* path follows the n-well 1.2 V guard ring surrounding the internal structures of the chip, the electronics and the microstrips. The *red* path, on the other hand, follows the top-side back biasing p-well structure surrounding the chip.
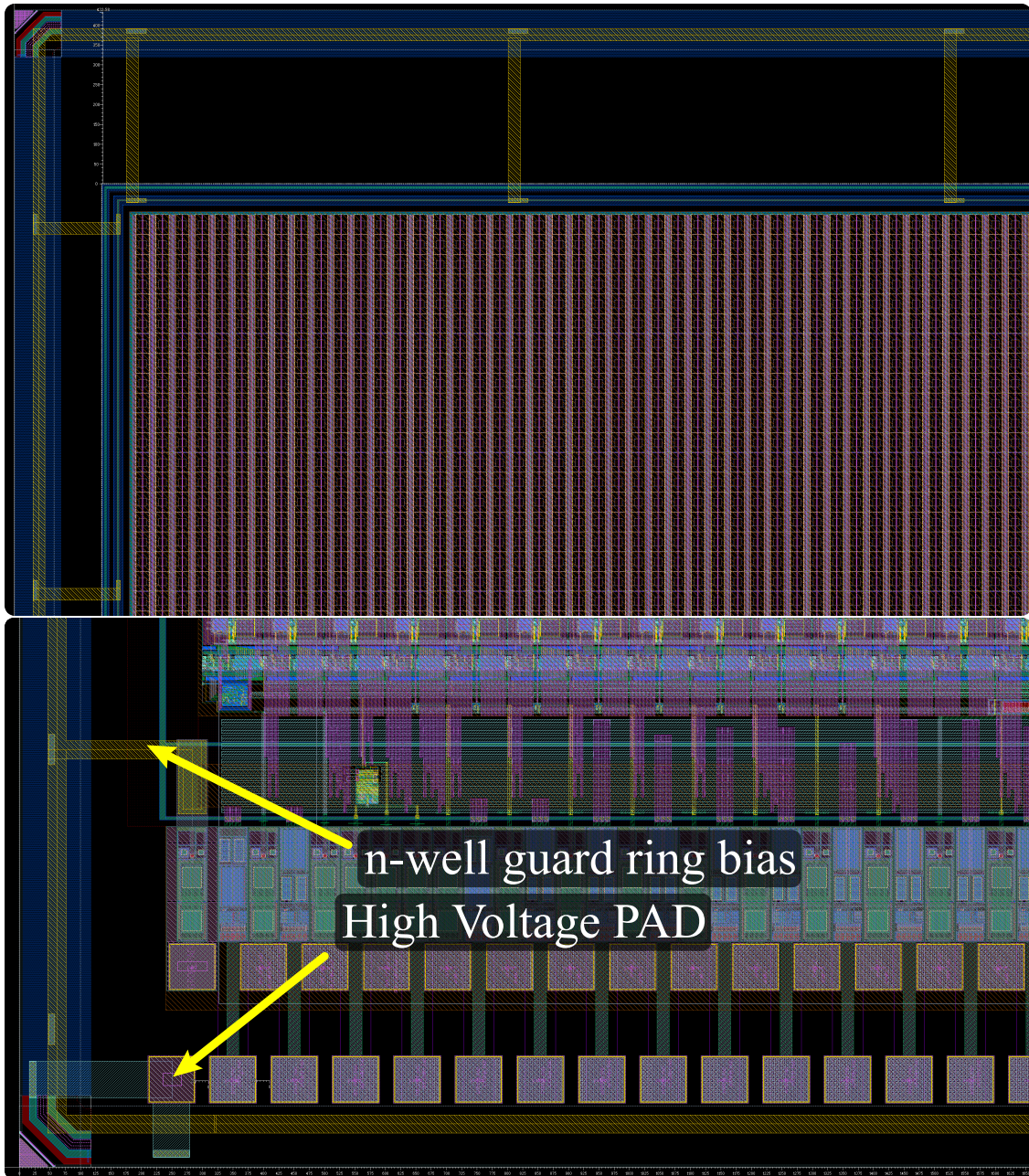
Figure 4.5: *top* Layout of the north-west chip area. The connection of the microstrip GR with the external is identifiable as the fourth metal line in yellow. *bottom* Layout view of one (SW) of the two areas on chip for front-side biasing of the sensor guard rings and high voltage.

Chapter 5

The ASTRA ASIC

ASTRA, Adaptable Space sTrip Readout ASIC, is an integrated circuit implemented in 110 nm technology. Two chips have been produced with the designed architecture in a 64 channel standalone ASIC and a 32 channel monolithic version. The electronics have been designed in a modular manner in order to simplify the layout design. In particular, ASTRA-64 is composed of two identical mirrored ASTRA-32 chips. Thus, the chapter will focus on the functionalities and features found within the electronics of the 32 channel chip.

- Designed in 0.11 μm CMOS Image Sensor Technology

- Die size ASTRA-32: 4.4 mm×16.229 mm

- Die size ASTRA-64: 8.0624 mm×3.1 mm

- CMOS Power supply: 1.2 V

- Signal amplification and discrimination for each channel

- 2 gain settings for input dynamic range up to 80 or 160 fC

- Configurability for positive or negative input signal polarity

- 4 peaking time configurations ($1.5 - 9\,\mu s$)

- Input capacitance C_{in} up to 100 pF

- ENC < 1000 e$^-$ for $C_{in} = 100$ pF

- Dual readout mode (analog and digital)
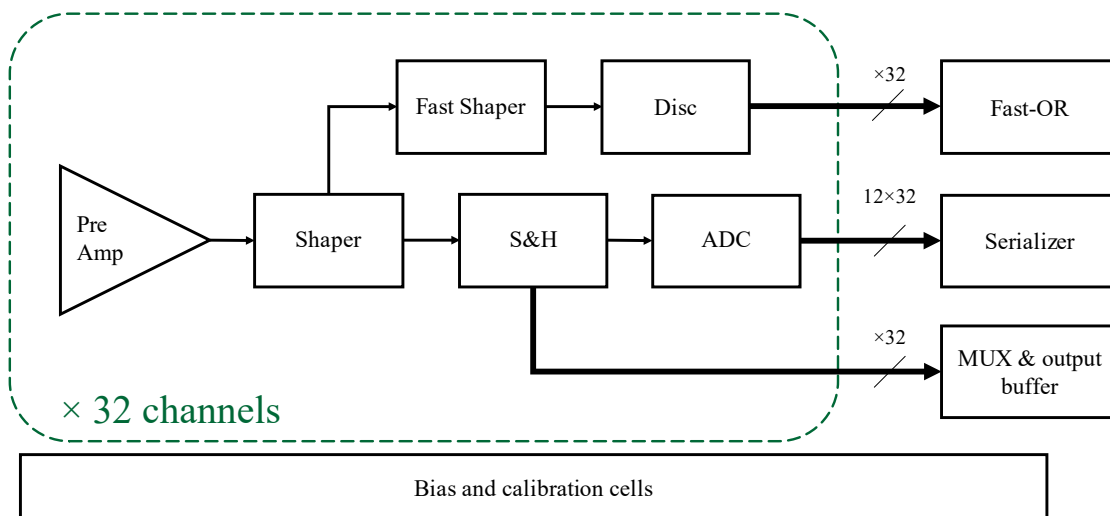
Figure 5.1: ASTRA Building Blocks.

5.1   ASTRA Building Blocks

The 32 channel ASTRA ASIC building blocks are shown in figure 5.1. For each channel, a preamplifier with varying feedback has been designed. This enables the adoption of the front end for MIPs for thick or thin sensors where, in the latter case, the detected charges are less due to a smaller detecting volume. Following, a configurable peaking time CR-RC shaper has been included to minimize the noise in relation to the input capacitance. In parallel to the shaper input, a fast shaper (below 1 µs peaking time) coupled to a discriminator has been designed. The output of the discriminator enters a fast-OR designed to trigger the acquisition of the amplified signals requesting an external FPGA for a HOLD signal.

The signal amplified by the shaper is continually tracked by a sample and hold circuit, S&H. The S&H is composed of a switched sampling capacitor. Once a HOLD signal is issued to the S&H switch from an external FPGA, each capacitor stores the sampled values until all channels have been read out. Thus, the readout scheme adopts a global shutter technique to sample the amplified signals.

Connected to the S&H circuit are two different branches: an analog readout set of buffers (as illustrated in figure 5.2) and a Wilkinson ADC.

In the first branch, the capacitor is coupled to a switched output differential topology buffer capable of piloting the metal lines to the analog output circuitry. Furthermore, the output circuitry is composed of 3 blocks: a multiplexer, a single-ended-to-differential amplifier and two output buffers capable of piloting low impedance nodes.

In the second branch, connected to the sampling capacitor, before the buffer, an analog to digital converter (ADC) has also been included in order to digitize the
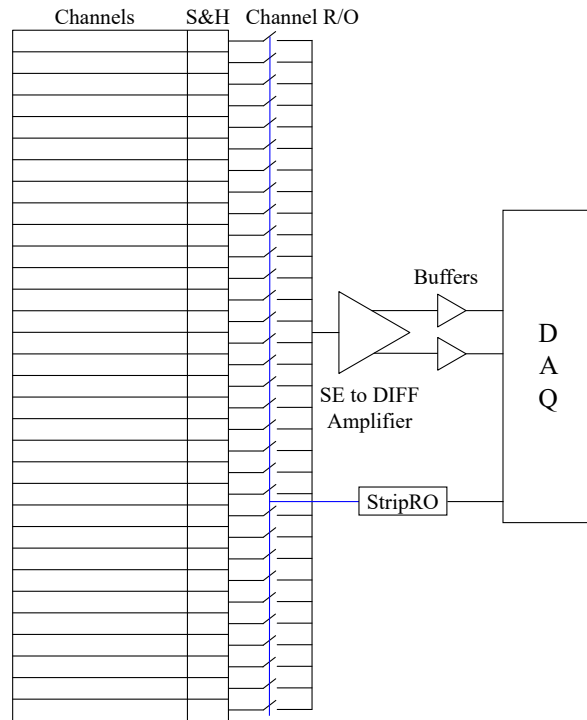
Figure 5.2: ASTRA Analog Readout Scheme.

sampled values and decrease the processing required off chip.

These two branches can be either used in a stand-alone configuration or in quick succession to acquire both analog and digital samples (analog first).

Concluding, an important constraint on the design of the electronics adopted in ASTRA has been the adoption of high threshold voltage transistors in the AR-CADIA engineering run. This has led to design tweaks to overcome the difficulties arising when requiring a large headroom voltage to bias all transistors correctly.

5.2 Front-End Design

Figure 5.3: Schematic level design of the ASTRA charge sensitive amplifier. The feedback capacitor is configurable in order to vary the CSA gain.

Each strip is connected to its own charge sensitive amplifier (CSA). The adopted topology, shown in figure 5.3, is a telescopic cascode amplifier with a configurable gain. The topology is excellent to improve the transconductance of the input PMOS transistor while still keeping the output impedance high. The latter condition is required to maximize the open loop gain of the front-end:

$$
\begin{aligned}
A_v = -g_{m1} R_L = -g_{m1} \left(r_{0casN} // r_{0casP} \right) \approx \\
\approx -g_{m1} \left[r_{01} r_{02} + \left(g_{m2} + g_{mb2} \right) r_{01} r_{02} \right] // \left[r_{03} r_{04} + \left(g_{m3} + g_{mb3} \right) r_{03} r_{04} \right].
\end{aligned}
\tag{5.1}
$$

Here, the r_0 contribution of the M5-6 branch has been neglected due to its small influence. The input transconductance is augmented by increasing the current in M1 through the bias branch composed of transistors M5 and M6. The branch contributes $150\,\mu\text{A}$ while the output branch, composed of transistors M2 to M4, contributes $50\,\mu\text{A}$. The lower current in the output branch leads to a higher r_0 improving the gain of the amplifier. The final open loop gain of the front end is $64.6\,\text{dB}$.

The feedback net adopts a variable capacitor, between the input and output node of the CSA, to enable compatibility with thin sensors and a continuous reset through a large feedback resistance.

Figure 5.4: ASTRA VFE blocks. All feedback and mirror blocks employ CMOS switches in order to select the correct operating polarity. The p-type feedback requires an extra current mirror block to invert the polarity of the output current.

The front end feedback resistance has been implemented with a current mirror g_m feedback technique shown in figure 5.5. In order to render the electronics compatible with most commercial microstrips, a switchable n to p type feedback has been developed. The block design of the two feedback branches connected to the CSA is illustrated in figure 5.4. The two branches maximize the front end compatibility by accepting signals of either positive or negative polarity by switching the POL and POLb bits. In order to adopt the same shaper topology for both polarities, a secondary current mirror, which actively inverts the current polarity, is placed between the output of the n-type feedback and the input of the shaper.

Nevertheless, two issues must be solved. Firstly, due to the adopted technology, only high threshold voltage transistors are available, thus a way to improve the common source transistor voltage headroom is required for large signals. Secondly, the high output impedance condition would lead to a voltage deterioration once a feedback resistance is connected. To prevent these issues, a differential op-amp buffer is connected in series to the CSA output pin stabilizing the amplifier's gain.

In order to test the front end linearity, a calibration circuit has been added on the input node. Through an external test pulse, in the form of a voltage step, the ASIC functionality can be assessed with no sensors connected at the input. In particular, a switched capacitor, C_{TP}, differentiates the input step generating an input waveform similar to that acquired when a particle or radiation impinge onto a microstrip.

As aforementioned, the gain of the amplifier can be approximately doubled by the removal, through a CMOS switch, of half of the feedback capacitors. In fact, the feedback capacitor decreases from $0.4\,\mathrm{pF}$ to $0.2\,\mathrm{pF}$ increasing the CSA gain

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from 2.1 mV/fC to 3.8 mV/fC.

The output of the CSA is AC coupled to the shaper input node. The 20 pF pole-zero cancelation capacitance acts as a high pass filter and, in order to have greater signal amplification, a current mirror, which reproduces the feedback current, is connected in parallel as shown in 5.5.

The current mirror feedback also provides charge amplification towards the shaper input with a 20 pF pole-zero cancelation capacitor.

The only electronics design difference between ASTRA64 and the monolithic ASTRA32 version is found in the input PMOS. In particular, to improve the noise figures and SNR ASTRA64 adopts a 3V3 input PMOS transistor, while the monolithic version a 1V2. The different design was forced due to the higher threshold voltage found in the 3V3 which would lead to a DC voltage for the collecting electrodes below the minimum value of 0.8 V. This requirement is not present in commercial strips since they are commonly AC coupled to the electronics, implying that the DC voltage at the input node of the electronics does not influence the functionality of either parts of the detector.
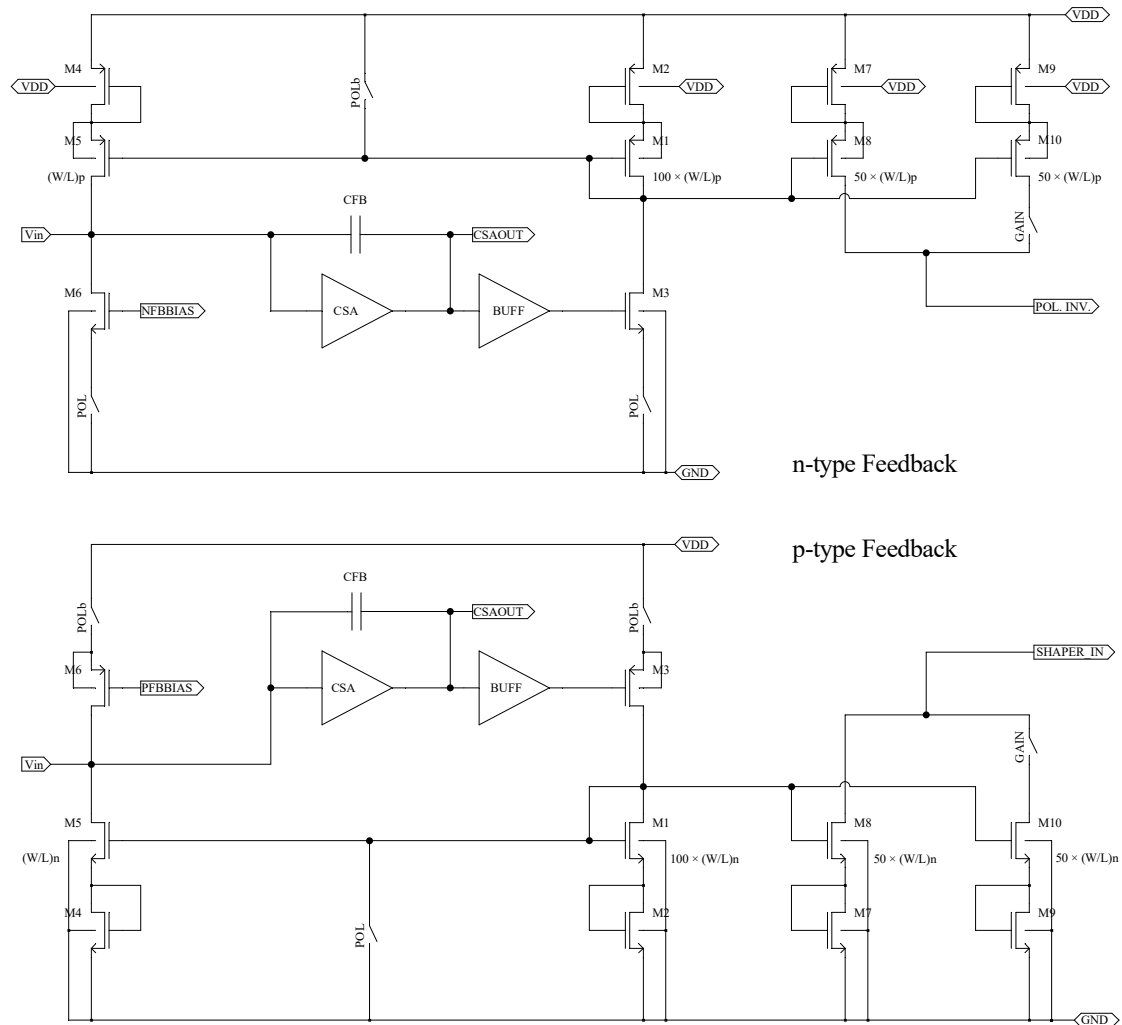
Figure 5.5: ASTRA feedback schematic. On the top the negative topology feedback is shown while, at the bottom, the negative one. The polarity switches, adopting either PMOS or NMOS transistors as switches, are shown for the selection of the negative (POL) or positive polarity (POLb).

5.3   CR-RC Shaper Design
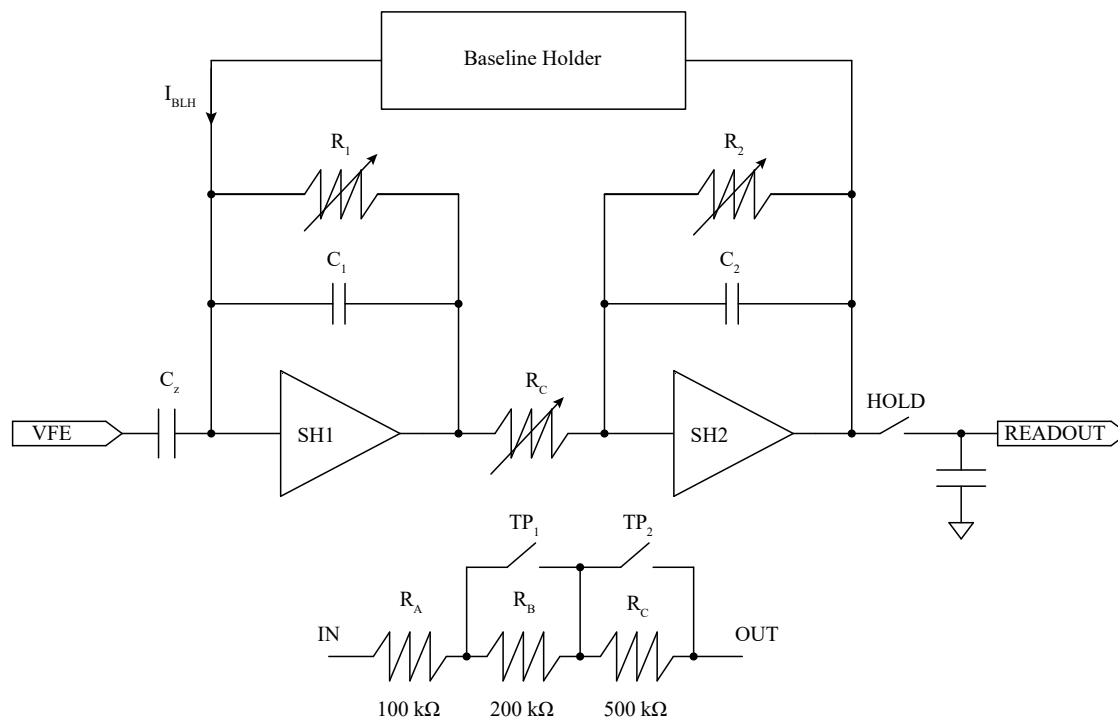
Figure 5.6: ASTRA shaper block design. On the top the building blocks of the CR-RC shaper is shown in parallel to the baseline holder. At the bottom the configuration schematic of the variable resistors adopted to implement different peaking times.

The shaper, shown in figure 5.6, is a CR-RC shaper with programmable peaking time [68]. By varying the feedback net, the peaking time can be tuned allowing for an optimization of the noise figures with various input capacitances. A study has been performed on ENC minimization with peaking time configuration in the next subsection. Being AC coupled to the front end, the CR-RC shaper requires a baseline holder circuit to maintain a stable baseline in input and output. A trade-off between the shaper dynamic range and a comfortable operating point of the output transistors of the second shaper core was done by choosing an output baseline voltage of 870 mV.

To implement the CR-RC shaper the time constants of the two cores must be equal implying a peaking time set via the simple equation:

$$\tau_{sh} = R_1 \, C_1 = R_2 \, C_2. \tag{5.2}$$

Furthermore, the shaper gain should ideally remain constant when switching from one peaking time to another, thus, following the output voltage formula in

the time domain:

$$V_{out}(t) = Q_{in} \frac{C_z}{C_1 \, C_f} \frac{R_2}{R_c} \frac{t}{\tau} e^{-\frac{t}{\tau}}, \tag{5.3}$$

we require a shaper core coupling resistance to vary as proportionally as possible to the shaper feedback resistors. The chosen resistance values and peaking time configuration bits are in table 5.1. Clearly, the values of R_c have not been picked in a perfectly proportional manner. This has been done to improve the layout resistor mismatch by building reproducible resistor blocks which would lead to a better match between resistance values.

PT bits	Peaking Time [µs]	$R_1 = R_2$ [kΩ]	R_C [kΩ]	I_{BLH} [µA]
00	9.0	800	280	0.816
01	6.5	600	210	1.067
10	3.5	300	105	2.095
11	1.5	100	35	6.138

Table 5.1: ASTRA Peaking time configuration bits.

Concluding, the shaper output results for a schematic simulation adopting $T_p[1,0] = 6.5 \, \mu s$ are shown in figures 5.7 and 5.8. The first figure shows the input charge parametric waveforms at the output node of the shaper, while the second shows the peak voltage value sampled at 6.5 µs for different input charges.

Figure 5.7: Input charge parametric ASTRA shaper output waveform. The output saturates around 140 fC. The T_p bits have been configured as follows: $T_p\,[1,0] = 6.5\,\text{µs}$
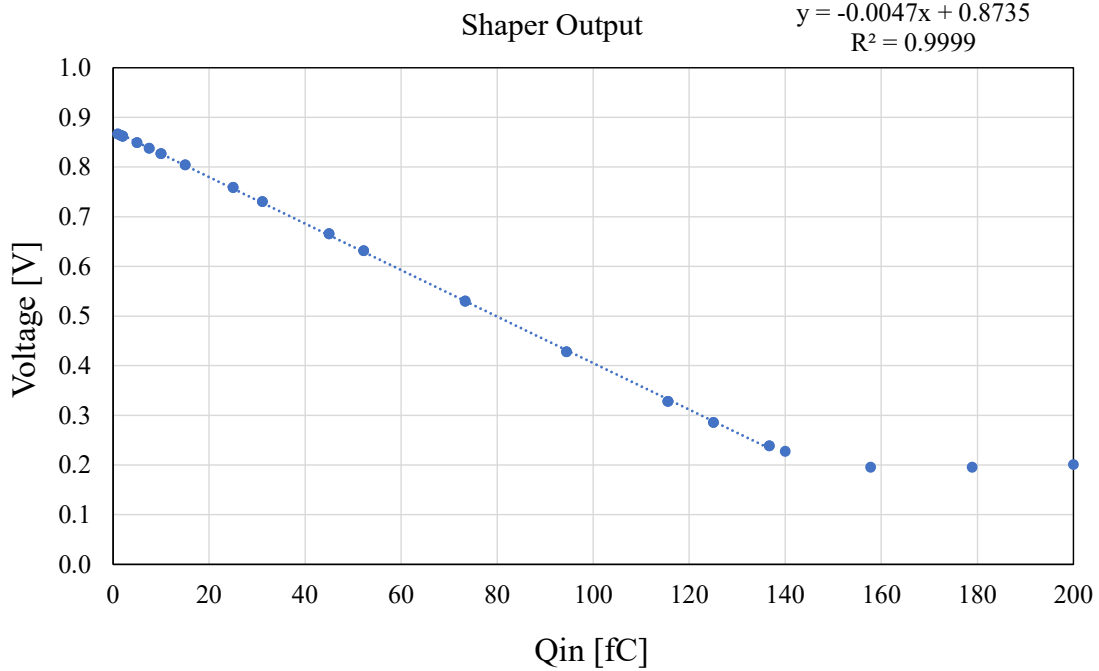
Figure 5.8: ASTRA shaper linearity. The trend line limits have been set from 0 to 140 fC.
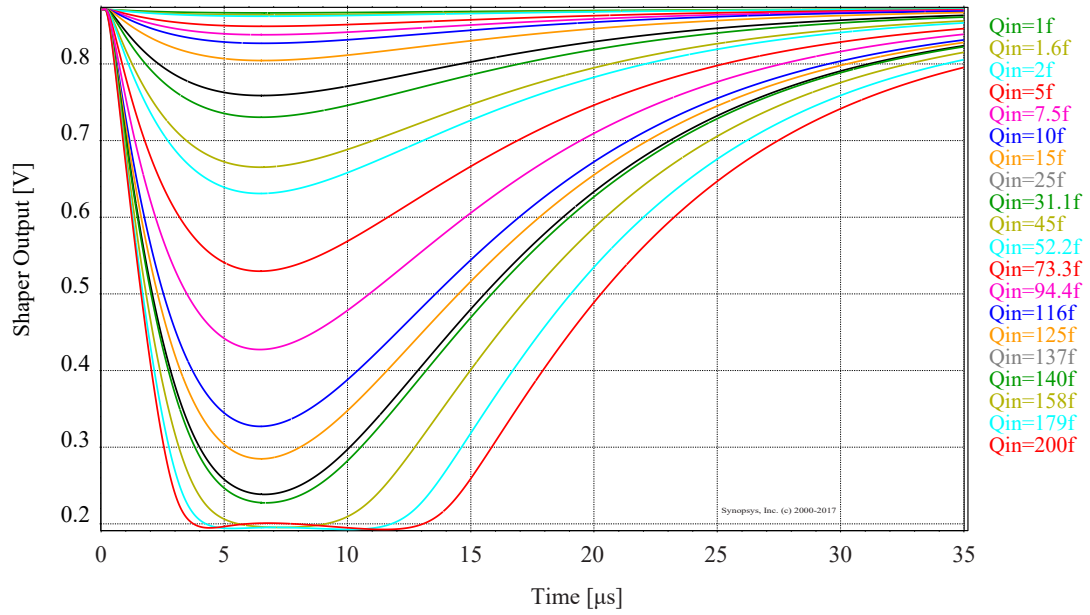
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5.3.1 Input capacitance study

It is well known that the equivalent noise charge, ENC, is strictly connected to the input capacitance and peaking time, T_p, through:

$$\text{ENC}^2 = C_T^2 \left(\frac{A_w V_n^2}{T_p} + A_f K_f \right) + A_i i_n^2 T_p \qquad (5.4)$$

where $C_T = (C_d + C_{in})$ is the total input capacitance, in particular C_{in} is the sum of all the capacitances, not detector related, in parallel to the input. A_w, A_f and A_i are, respectively the noise transfer functions for white, flicker and input parallel noise. V_n^2 and i_n^2 are the input-referred voltage and current spectral noise density and K_f is a device specific constant. Through a study of the foundry PDK, a set of scripted simulations were done to find the optimal peaking time for various input capacitances. The resulting minimization plots are shown in figure 5.9. Here 3 plots studying the ENC for 5, 10 and 100 pF are shown. As expected from electronics theory, an increase in the input capacitance results in an ENC increase. Nevertheless, following this study and by tuning the baseline holder required for the CR-RC shaper, an optimal configuration with 4 possible peaking times has been designed: 1.5, 3.5, 6.5 and 9 μs. The resistance values required for these peaking times and the respective configurations bits, are in table 5.1.

5.3.2 Fast-OR Architecture

The ASTRA chip has been developed with an auto-triggering component in the form of a 32 channel fast-OR. The architecture includes a fast shaper, a discriminator and a fast-OR connected to its own Scalable Low-Voltage Signaling transmitter (SLVS TX) set of pads.

The fast shaper adopts the same core amplifiers found in the main CR-RC shaper, but with a different resistance topology. In particular, a PMOS, set to work in the linear region, has been adopted as a feedback resistor. The resistance can be tuned by varying the PMOS voltage through a dedicated pad. The nominal gain of the fast shaper is 30 mV/fC.

The amplified signal is sent to the discriminator, a single stage differential amplifier with hysteresis. The threshold, same for all channels, is controlled off-chip through a dedicated pad. Furthermore, the output of each discriminator can be disabled through a channel configuration register. This prevents the fast-OR triggering for faulty channels.

The 32 discriminator outputs are fed into a fast-OR circuit in order to provide a fast trigger signal adopted for the HOLD signal in the sample and hold circuitry.
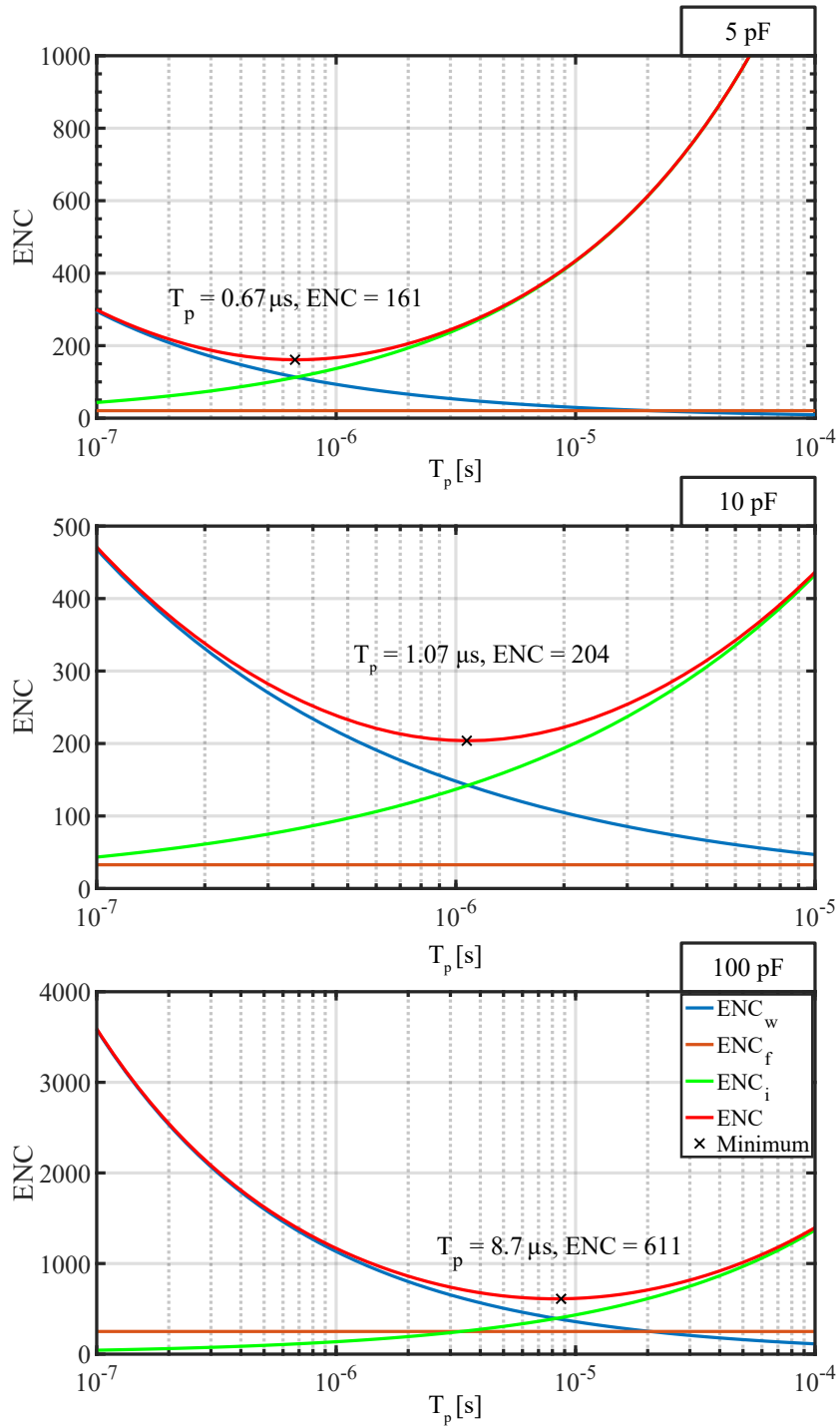
Figure 5.9: ASTRA Noise minimization study. Starting from the top, the ENC study from 5 to 100 pF. The minimization of the peaking time, extracted from equation 5.4, yields the minimum of the noise figure at 0.7, 1.1 and 8.7 µs for detector input capacitances of 5, 10 and 100 pF.
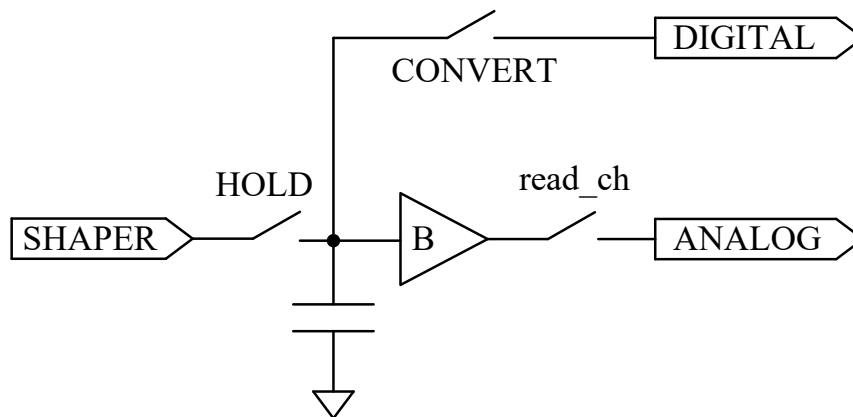
Figure 5.10: ASTRA Sample and Hold connection to the shaper and output branches.

5.3.3   Sample and Hold circuit

The sample and hold circuit, shown in figure 5.10, is composed of a switched capacitor and a switched buffer. The $0.3\,\text{pF}$ sampling capacitor is connected to the output of the shaper through a CMOS switch. The switch is opened when a HOLD signal is issued by the FPGA. At this point the charge is stored with a maximum parasitic current of $30\,\text{pA}$ for the smallest signals (near the baseline voltage of $870\,\text{mV}$).

The switched buffer is adopted in order to pilot the metallic lines to the analog output circuitry. In particular, when the readout of a channel is enabled the output of the buffer is read.

Between the capacitor and the buffer, a metal line connects the capacitor to the input of a Wilkinson ADC.

5.4 Analog Readout
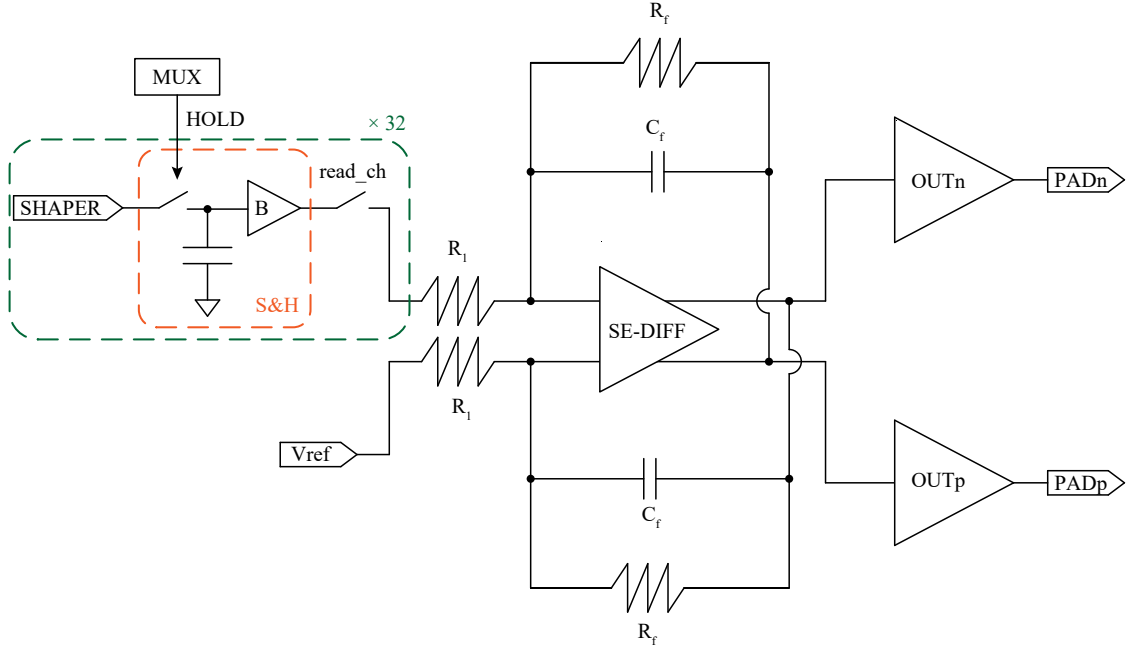
Figure 5.11: ASTRA Analog Readout Scheme.

The analog output chain, illustrated in figure 5.11, comprises a multiplexer, a single-ended-to-differential amplifier and two Class-AB output amplifiers, one per each polarity. The circuits are always active, regardless of the status of the front-end. However, when considering the power per channel the output amplifier and buffers yield a power dissipation within an acceptable level, dissipating approximately 8 and $37\,\mu\text{W/ch}$ each. Nevertheless, a redesign with the possibility of turning completely off the output buffers is planned.

The output has been designed differential in order to improve the output signal swing, supply and substrate immunity and to reduce possible electromagnetic noise when connecting the output buffers to an external discrete ADC.

Concluding the analog readout section, a table (Tab. 5.2), describing the sizes of the main transistors, is found.

5.4.1 Multiplexer

In order to read out the values sampled in each channel, 3 signals are required: a HOLD signal, a 5 MHz clock and a read reset. The signals are provided by the FPGA through 3 pads. The HOLD signal is issued to all channels at the same time. In order to reduce IR drops along the control bit metal lines, a set of simple digital buffers are included. The buffers are composed of two CMOS inverters in series with double output driving strength.

The read out of the single channel is controlled by a 32-1 multiplexer at the end of column (EOC). While the signal acquisition is through a global shutter technique, the sampled voltage extraction adopts a rolling shutter readout process. Thus, the S&H capacitors of each channel are read out sequentially through a set of positive edge D-flip-flops which are part of the EOC.

In particular, the signal extraction is as follows:

1. The HOLD signal is issued to all channels from the FPGA through buffers;

2. The clock signal is sent to the chip from the FPGA;

3. The read reset bit is flipped to 1 and the readout of the first channel is initiated;

4. At each positive edge of the clock, the following channel is read out.

To initialize the read-out, the first adopted flip-flop in the EOC has an active low set. This implies that the output is fixed low, as long as the reset bit is high. Once the reset pin is switched to 0, the output of the first FF flips to 1 for the first clock period. Due to the architecture of the read reset being active high, an inverter is added at the reset pin of the first FF to flip the incoming read reset signal from 1 to 0.

5.4.2 Single ended to Differential Amplifier
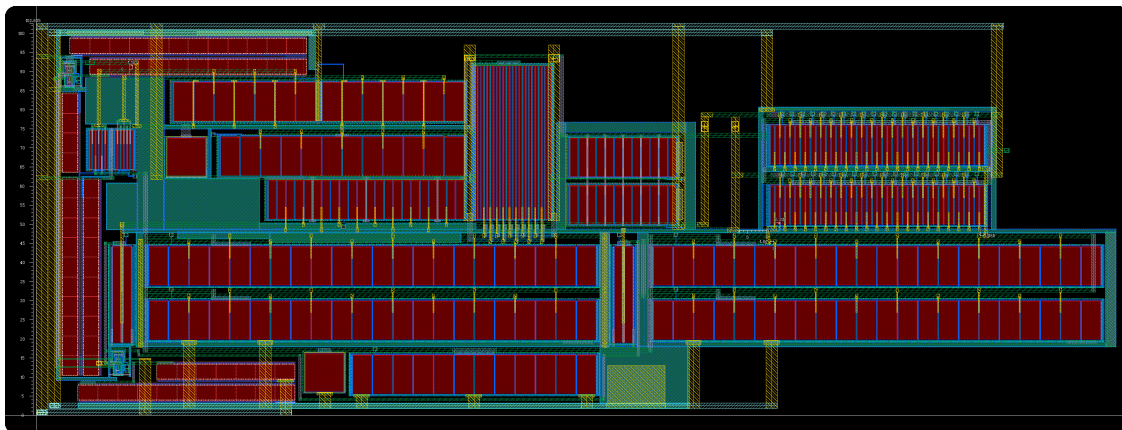
Figure 5.12: ASTRA single-ended-to-differential amplifier layout.

The single-ended-to-differential amplifier has been designed adopting a differential folded cascode topology with a differential current common mode sense feedback. The transistor level design is shown in figure 5.13, while the layout is shown in figure 5.12.

The topology has been chosen to avoid a reduction of the transistor operating voltage range, both for the overdrive and drain-source saturation voltages. In particular, due to the adoption of high threshold voltage transistors the adoption of telescopic topologies, or more than 4 transistors piled between VDD and GND, would have rendered a lower dynamic range and stability.

The outputs of the 32 S&H buffers are connected to the input marked $V_{in,p}$ while the $V_{in,n}$ terminal is connected to its own external pad and nominally tied to 0.6 V. The common mode sense circuit has been picked to ensure a quick signal response for differential signals and ensure that the transistors are kept in saturation. The reference voltage for the common mode feedback has been set to $V_{CMFB} = 0.6$ V.

The gain of the amplifier has been set to unity by picking $R_f = R_1$ and is defined by the feedback over series resistance ratio:

$$G = \frac{R_f}{R_1} = \frac{55\,\text{k}\Omega}{55\,\text{k}\Omega} = 1. \tag{5.5}$$

The feedback capacitors have been selected in order to stabilize the amplifier preventing ringing and oscillations. Through simulations a value of C_f capable of keeping the bandwidth large enough for the 5 MHz channel readout clock frequency has been selected. In particular, the values are identical and equal to $C_f = 0.55$ pF. An improved version could be designed with a higher gain in order to improve the resolution of the output circuit.
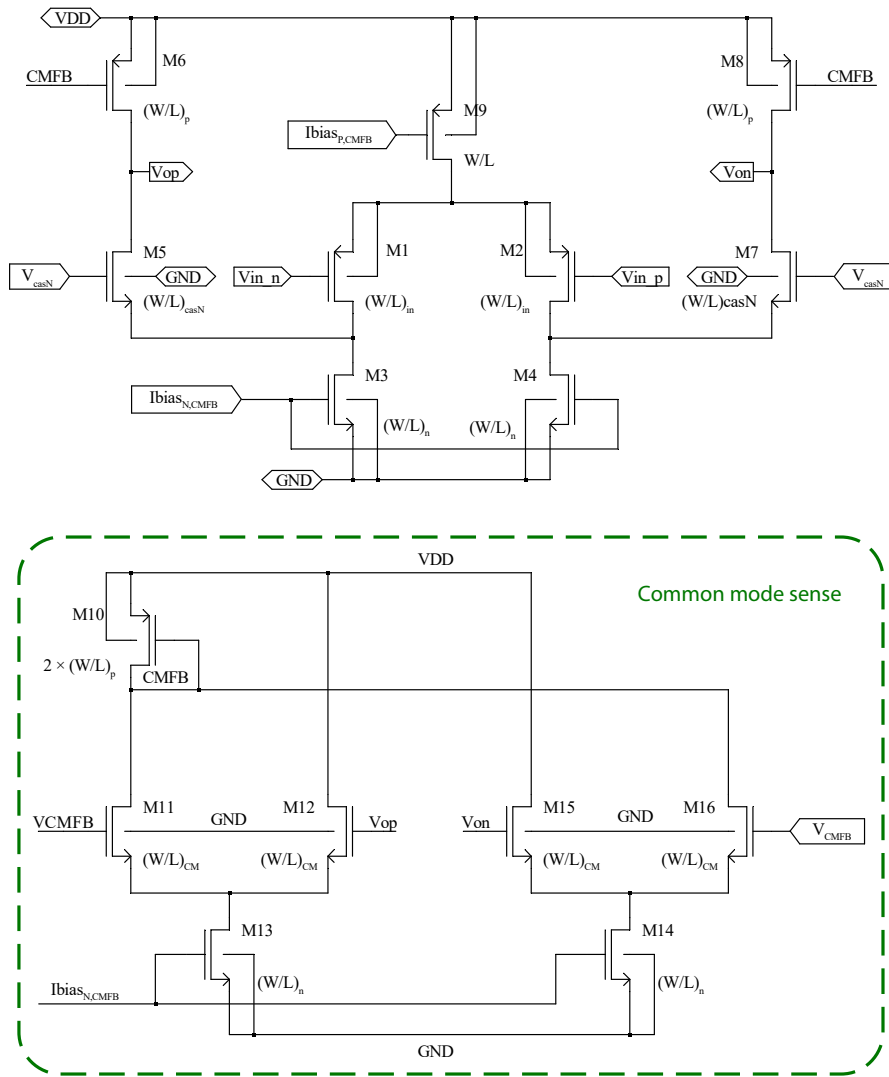
Figure 5.13: ASTRA single-ended-to-differential amplifier Schematic.

5.4.3 Large Output Buffers
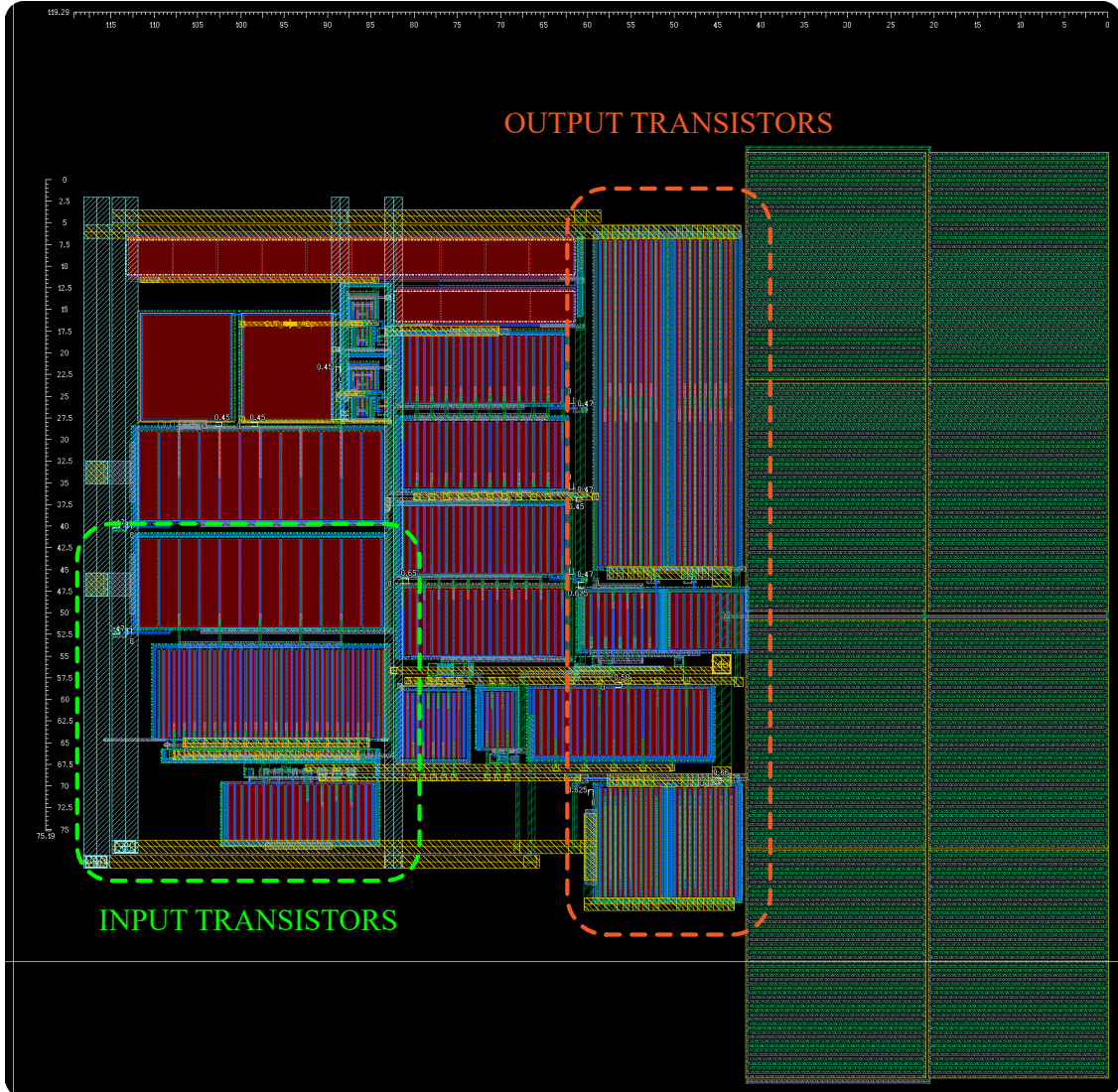
Figure 5.14: ASTRA Output Buffer Layout. The input transistors are visible in *green*, while the output ones are highlighted in *orange*. Due to the current reaching the mA order of magnitude in output, the fingers adopt both METAL1 and METAL2 layers with vias throughout the width of the devices. On the right side the output transistor gate stabilizing capacitors are located.

The output buffer pair adopts a symmetrical OTA topology with a class AB output capable of driving standard termination circuitry composed of a 20 pF capacitor and a 50 kΩ resistor [36]. The layout and schematic views of the buffer are shown, respectively, in figure 5.14 and 5.18. The differential input transistors have
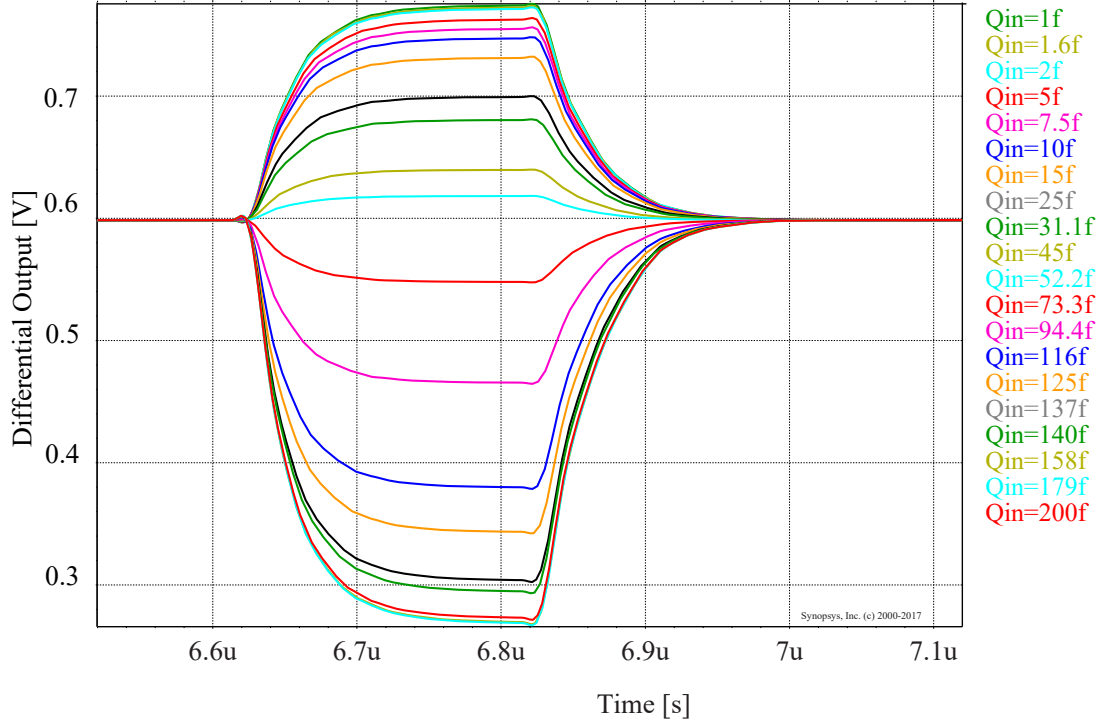
Figure 5.15: ASTRA Readout Simulation. The differential output after the buffers is shown. In particular, the plot is of the signal: $Diff.Out. = V_{out,n} - V_{out,p} + 0.6\,\text{V}$ The waveforms shown here are the analog readout of the parametric simulations done with the shaper output shown in figure 5.7. Thus, the peaking time adopted is $T_p\,[1,0] = 6.5\,\text{µs}$

.

been designed with the same W/L ratio. The input transistors and the current mirrors have been designed adopting an inter-digitized finger layout.

The AB output is implemented with transistors M10 to M13 in figure 5.18. The adoption of a class-AB output leads to the possibility of having a higher power efficiency compared to a class-A amplifier which adopts output transistors always in conduction, while delivering an almost rail to rail output voltage. In particular, the AB output draws power from the VDD net only when a signal must be amplified leading to a lower idle power consumption. The transistors M12 and M13 are Feed-Forward Biased, FFB, in class-AB by the two head-to-tail connected transistors M10, M11. Considering the roughly 3 times higher mobility ($\mu_n \approx 3 \times \mu_p$) of NMOS transistors compared to PMOS ones all the latter included in the design are sized 3 times larger in width then their n-doped counter part ($3 \times (W/L)_P = (W/L)_N$). A particular exception is the size of the output transistors which are larger than the biasing transistors by a factor 10.

The technical difficulty of adopting a class-AB output is in the correct biasing

Differential Output
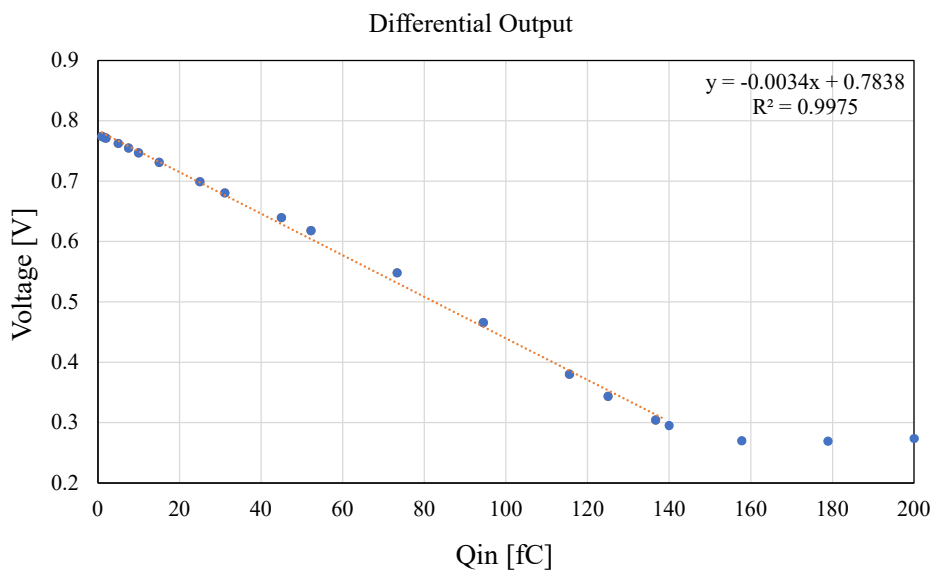
Figure 5.16: ASTRA Readout Linearity. The trend line limits have been set from 0 to 140 fC.

of the head to tail transistors M10 and M11. Here, proportional copies of the top PMOS, M9, bottom NMOS, M7, and the M10,11 couple are adopted in the biasing circuit, shown in figure 5.19, steering the same current in M10 and M11 at the nominal input value of 0.6 V.

Class-AB outputs are usually paired to telescopic folded cascode amplifiers [38]. However, this topology could not be implemented due to the high threshold voltage of the adopted transistor technology and low rail to rail voltage, which is not large enough for the biasing of more than 4 transistors in series between VDD and GND. In fact, the adoption of a folded cascode in the buffer would have reduced the voltage headroom in the head to tail transistors when a signal swing occurs at the input once the S&H capacitor has sampled a large signal. To overcome this limitation, a symmetrical OTA has been picked for the buffering of the voltage from the single ended to differential amplifier to the output couple.

Concluding, the linearity of the output buffer is shown in figure 5.16, while the differential output waveform is in figure 5.15. The former plot shows the output linearity of the values sampled at 6.8 µs of the following formula:

$$Diff.Out. (6.8\,\text{µs}) = V_{out,n} (6.8\,\text{µs}) - V_{out,p} (6.8\,\text{µs}) + 0.6\,\text{V} \tag{5.6}$$

where $V_{out,n}$ and $V_{out,p}$ are, respectively, the voltages at the negative and positive output pins of the output buffers. A small bump is noticeable in the plot around 0.6 V, this is due to the Class-AB output topology and can be mitigated off-chip via proper calibration. Concluding, a simulation showing the signals required to activate the output buffers and the resulting outputs is plotted in figure 5.17.

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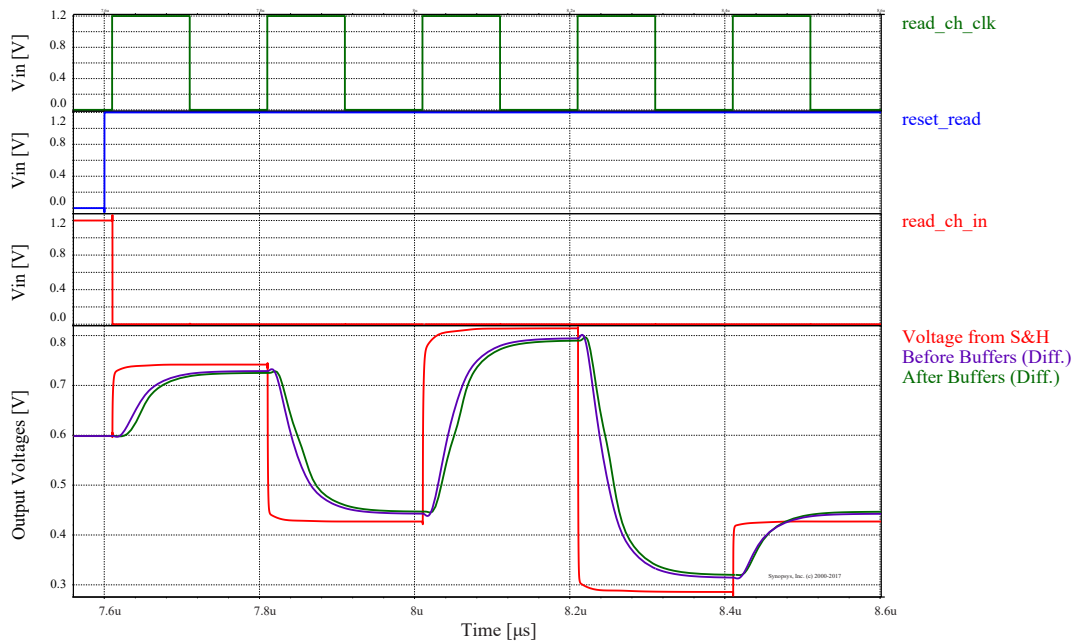
Figure 5.17: ASTRA Readout with digital control signals. Starting from the top, the MUX shift clock is shown, then the reset_read signal, adopted to start the readout process which transforms, on the rising edge of the clock into the read channel in and finally the output waveforms. In this case the voltage coming from the S&H circuitry is plotted in *red* while the differential signals from the SE-to-DIFF amplifier and after the output buffers are shown respectively in *purple* and *green*.
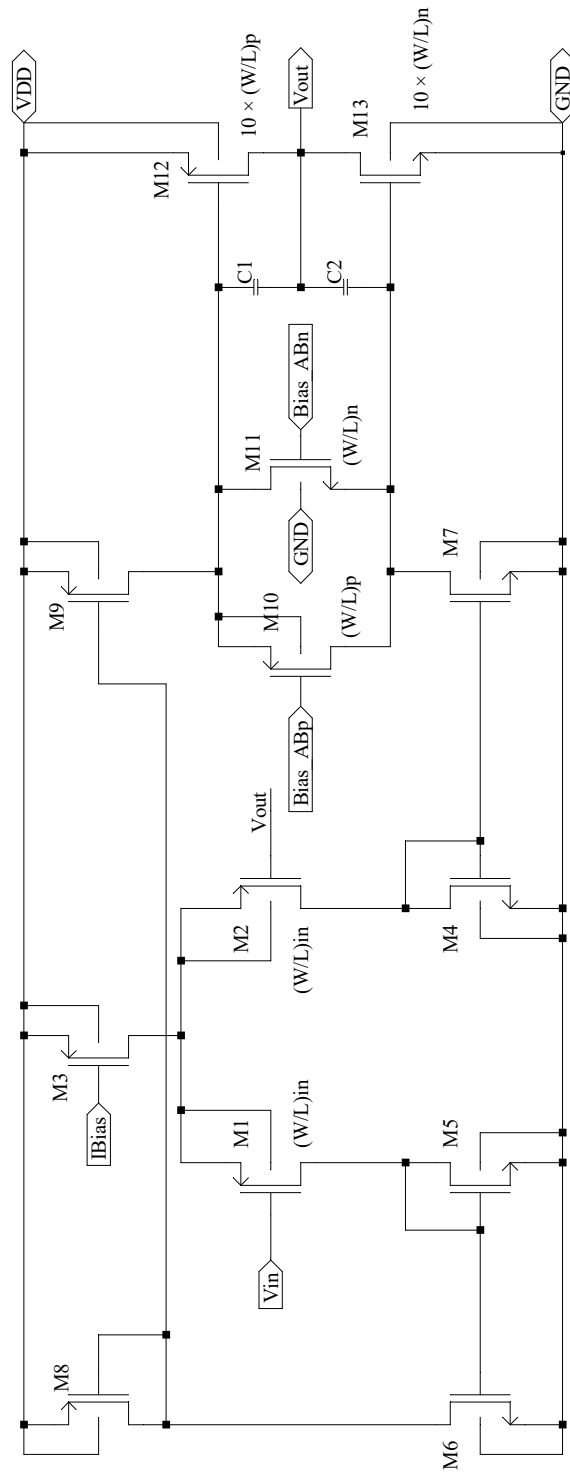
Figure 5.18: ASTRA Output Buffer Schematic.
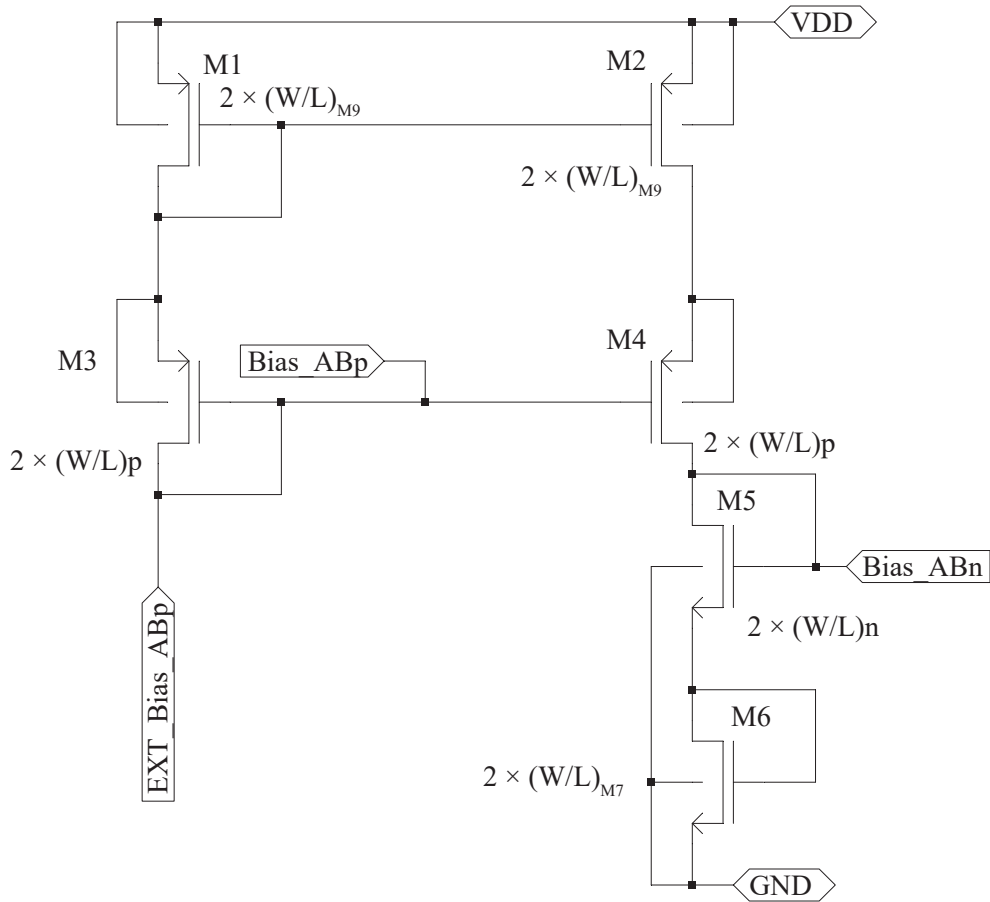
Figure 5.19: ASTRA Buffer Bias Circuitry. The sizes of the transistors in this schematic refer to the transistors in figure 5.18. The external bias circuit schematic is explained in section 5.6.4 and supplies double the current required to bias the head to tail pair M10 and M11 in figure 5.18.

Front-End	W [µm]	L [µm]
M1	3000	0.5
M2	100	0.5
M3	100	0.5
M4	250	1
M5	200	0.5
M6	300	2
R1	$1.5\,\mathrm{k\Omega}$	
R2	$500\,\Omega$	

SE-to-Diff	W [µm]	L [µm]
M1/2	400	0.5
M3/4	200	5
M5/7	50	2
M6/8	100	2
M9	100	5

Output Buffer	W [µm]	L [µm]
M1/2	200	0.25
M3	100	2
M4/5/6/7	25	0.5
M8/9	75	0.5
M10	75	0.25
M11	25	0.25
M12	750	0.25
M13	250	0.25
C1/2	$0.8\,\mathrm{pF}$	

Table 5.2: Sizes of the analog chain transistors. Here, the width of the input transistor stands out, in fact it has been picked to achieve the greatest transconductance and, thus signal-to-noise ratio. The same consideration is true for the input transistors of the other components.

5.5   Digital Readout
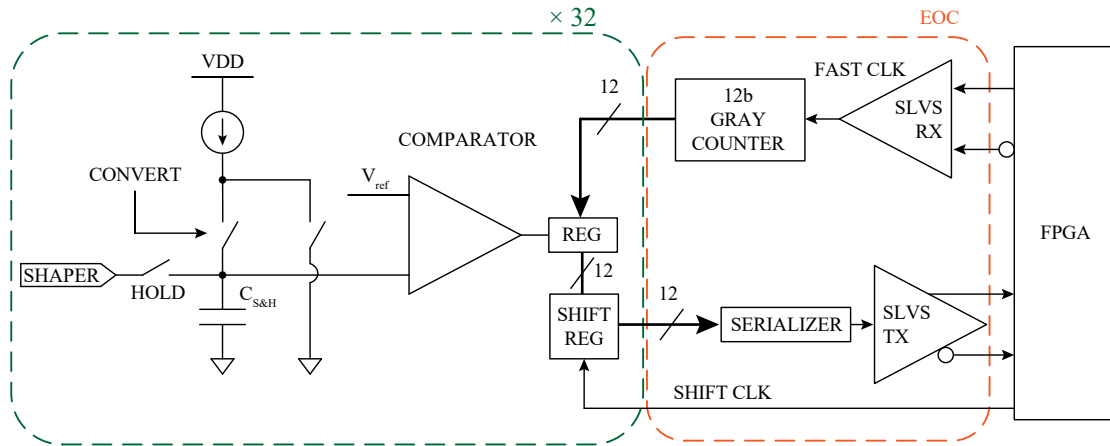
Figure 5.20: ASTRA Digital readout blocks. The input pin of the comparator is shared with the input pin of the switched analog buffer as shown in figure 5.10.

The digital readout branch has been connected to the node before the S&H buffer, as shown in figure 5.10. In particular, this branch is capable of digitizing the voltage sampled onto the S&H capacitor. The blocks composing the digital branch are shown in figure 5.20.
The blocks include:

- A Wilkinson ADC;

- A comparator;

- A set of 12b registers;

- A 12b Gray counter;

- A serializer;

- A set of SLVS TX and RX modules.

The Wilkinson ADC adopts a transistor in saturation as an ideal current source. The current flowing through the transistor can flow in one of two branches: one connected to the sampling capacitor and one to GND. The current flow is controlled by a CONVERT signal issued to a PMOS switch. When the conversion is initiated all the Wilkinson ADC current sources are connected to the sampling capacitor recharging it towards VDD and the Gray counter starts counting. One of the comparator's input pins is connected in parallel to this node, while the other is connected to an outside tunable reference voltage, V_{ref}, nominally set at $0.9\,V$.

Once the voltage on $C_{S\&H}$ reaches 0.9 V the output of the comparator toggles and the gray counter value is saved in the 12b registers. Following, the values stored into the registers are shifted by a slow clock towards the serializer which sends the stream of bits towards the SLVS transmitter. Here, the data is sent differentially towards an external FPGA.

The sampling resolution is controlled mainly by two parameters, the current flowing in the Wilkinson ADC and the master clock speed. The latter of which is shared between the counter and serializer and is nominally equal to $\text{FAST}_{\text{CLK}} = 100\,\text{MHz}$.

The current generator in the Wilkinson ADC is capable of providing a current from 5 to 200 nA and is controlled off chip through a dedicated pad. In order to reduce possible noise due to the small current values, the current provided off-chip is mirrored and de-multiplied by a factor $\times 1000$. To set the off-chip current a trimmable resistor (from 5 to 120 kΩ) is expected to be connected to VDD.

The current within the internal Wilkinson ADC PMOS is always flowing either to GND or to the sampling capacitor. This functional scheme has been designed to avoid transition phases that would affect the linearity of the voltage charging.

As aforementioned, the conversion comes to an end when the voltage on the capacitor reaches the V_{ref} set on the comparator. The time required by the ADC for the conversion is thus given by:

$$t_{ADC} = \frac{C_{S\&H}\,\Delta V}{I_{ADC}} \tag{5.7}$$

where ΔV is the voltage difference between the sampled voltage and V_{ref} and I_{ADC} the ADC current flowing through the Wilkinson ADC PMOS. Considering the shaper dynamic range, the maximum voltage difference to be converted is $\Delta V \approx 0.6\,\text{V}$. Thus, we can define the recharge time, t_r, as the time required to charge back up to 0.9 V the sampling capacitor. As a consequence, a variation in I_{ADC} would lead to a different recharge time and, in turn, the maximum number of bits adopted in each conversion. Moreover, this would lead to a varying resolution following:

$$V_{\text{LSB}} = \frac{V_{\text{ref}}}{2^N}. \tag{5.8}$$

The various configurations of the digital readout timings and resolution are in table 5.3. Here, the number of bits have been extracted considering the nominal counter clock frequency of $\nu_{FCLK} = 100\,\text{MHz}$.

$\mathbf{I_{ADC}}$ [nA]	$\mathbf{t_r}$ [µs]	# of BITs	$\mathbf{V_{LSB}}$ [mV]
70	2.7	8	2.34
35	5.4	9	1.17
17	11.1	10	0.59
9	20.9	11	0.29
4.5	41.9	12	0.15

Table 5.3: Number of bits and recharge time required for digitization with various Wilkinson ADC currents. (Values acquired for the maximum $\Delta V = 0.6\,\text{V}$)

As aforementioned, the time measurement is done adopting a Gray counter. The Gray counter is employed to reduce noise and errors due to a high number of bits switching at the same time. In fact, differently from a standard binary counter, the number of bits switching between successive digits is always equal to one.

Once the data conversion is over in all channels, the FPGA activates the serializer by sending a LOAD signal. The data from the first 12b register is serialized in 2 clock cycles and, once the SEND signal is sent to the serializer, it is conveyed to the transmitter to be sent off-chip. Correlated to the LOAD and SEND timings the shift clock signal is adopted to point to the correct registry to serialize. The data is sent off chip with in double data rate (DDR) mode, thus the time required for each SEND is correlated to the number of bits and clock period:

$$t_{\text{SEND}} = \frac{\#\text{BITS,s}}{2\,\nu_{FCLK}} = 80\,\text{ns}. \tag{5.9}$$

In this case, the number of bits sent is $\#\text{BITS,s} = \#\text{BITS} + 4$ due to a 4-bit handshake word 1010.

Concluding, the time required for the data serialization defines the maximum frequency for the SHIFT CLK signal. In fact, a single output cycle time is given by:

$$t_{\text{CYCLE}} = t_L + t_S + t_{LS} \tag{5.10}$$

where t_L and t_S are, respectively, the duration of the LOAD and SEND periods and t_{LS} is the time between the two. An example of the digital readout signals from a full simulation is shown in figure 5.21. Here, the full digital chain readout operation is shown:

1. FAST CLK: 100 MHz clock used in the ADC latched comparator, Gray counter and serializer;

2. RESET: active high signal sent to the digital electronics in order to ensure the correct initial conditions are set;

3. CONVERT: active high signal adopted to begin the analog to digital conversion. The signal must be kept high for at least the recharge time, t_r, duration;

4. SHIFT CLK: (not shown in the figure) it propagates the readout pointer towards the correct 12b register, loading the channel converted signals into the serializer;

5. LOAD: the active high signal loads the register bits in the serializer;

6. SEND: the active high signal enables the serializer output sending the bits to the FPGA through the SLVS transmitter.

The Wilkinson ADC linearity is plotted in figure 5.22. As aforementioned, the data sent off-chip adopts a Gray counter, thus a conversion to decimal numbers is required. A good linearity up to $\approx 140 - 150\,\text{fC}$ is shown with two possible LSB readout configurations.
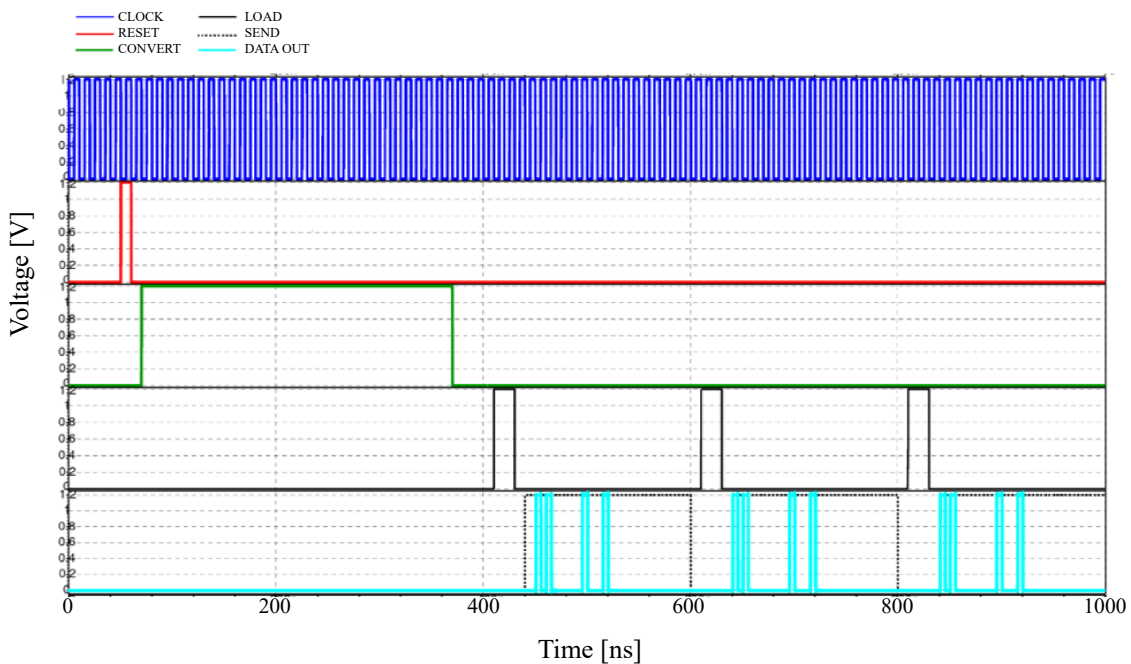
Figure 5.21: ASTRA Digital Readout Simulation. From the top, the digital clock signal is shown, which is turned on during digital readout operation. Following, the reset signal issued to the counter is sent. Once the registers have been restored, the convert signal is activated. Concluding the load and send signals are then enabled for each channel.

$R_{ADC} = 80\,k\Omega; \quad I_{ADC} = 10.9\,nA$

y = 17.023x + 176.59
R² = 0.9997

$R_{ADC} = 12\,k\Omega; \quad I_{ADC} = 62\,nA$

y = 3.0036x + 29.849
R² = 0.9996

Figure 5.22: Wilkinson ADC Linearity. The y-axis is the represents the Gray code to decimal conversion. On *top*, the results for a simulation with a $V_{LSB} = 0.28\,mV$, while, at the *bottom*, with a $V_{LSB} = 1.32\,mV$ The *orange* points in the plots are the values at which the shaper output saturates with the minimum gain at $\approx 140 - 150\,fC$.

5.6   General ASTRA features

In order to improve the manufacturability and adaptability of ASTRA, a set of measures have been taken. In this section the power dissipation of the chip and some examples of design features will be discussed. At the end of the discussion, a microphotograph (Fig. 5.25), showing ASTRA64 is provided.

5.6.1   Power Consumption

ASTRA has been designed in commercial a 110 nm CMOS technology. In particular the electronics operate with a 1.2 V power supply and is mostly analog. Nevertheless, in the chip's configuration and readout circuitry, digital standard cells have been adopted. In order to minimize digital to analog cross noise the power domains have been split in 4:

1. A0VDD: analog power supply adopted for the VFE and test-pulse injection circuit;

2. A1VDD: analog power supply adopted for the shapers;

3. A2VDD: analog power supply adopted for the S&H, MUX, Wilkinson ADC and analog output buffers;

4. DVDD: digital power supply adopted for the Gray counter, serializer, configuration register and SLVS TX and RX.

The power consumption of each block has been organized in table 5.4. Here the sum of the currents inside the blocks is tabled with the respective power dissipation per channel. Clearly, the power dissipated in power hungry blocks, such as the output stages, even though large it is shared between the 32 channels, thus the overall power consumption per channel does not diverge. In fact, when in analog readout mode the power dissipated remains well below 0.6 mW/ch. As previously explained, i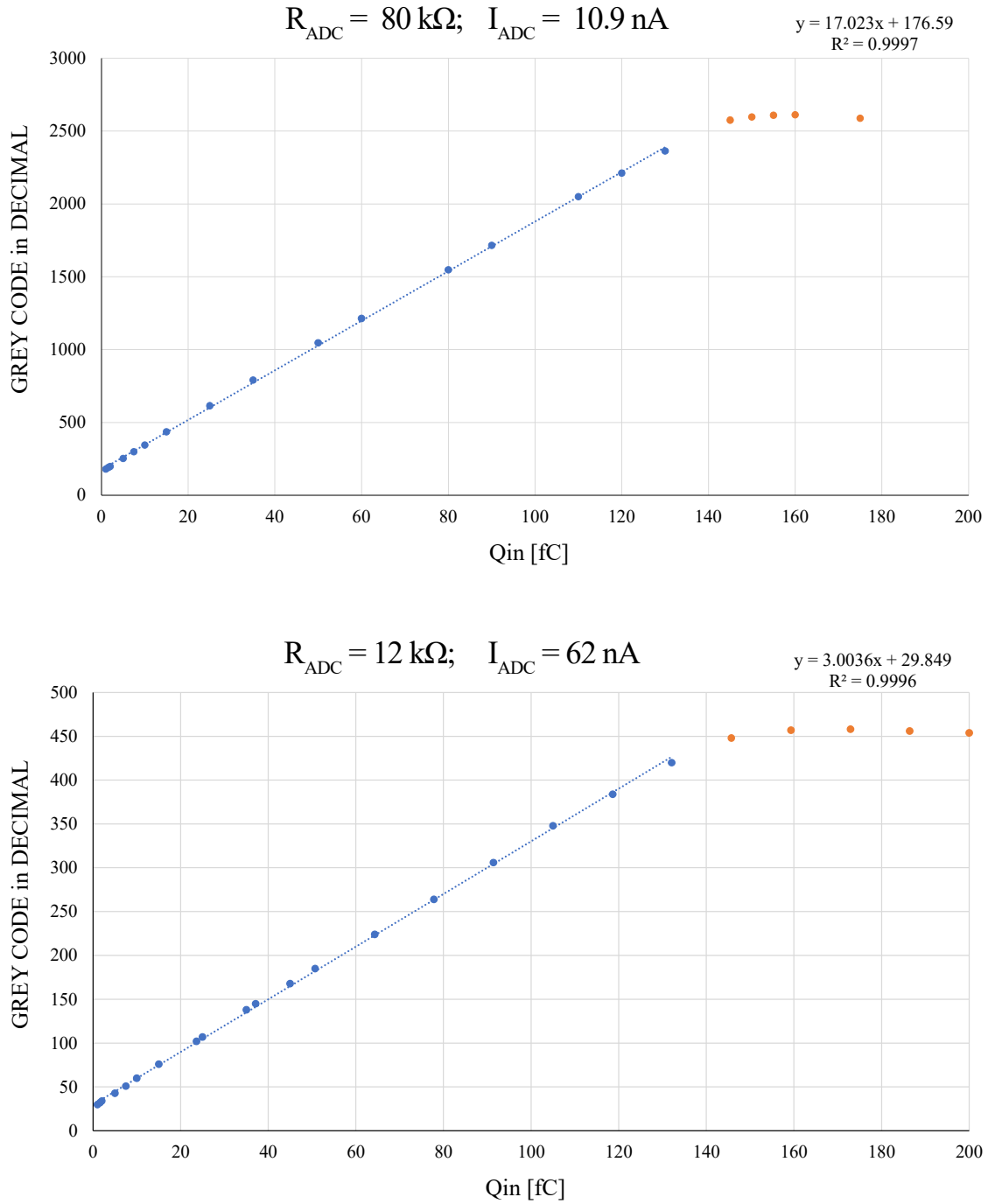n order to reduce the design effort, the monolithic strips adopt the same front-end found in ASTRA64 with the exception of the input PMOS. This implies that, since the front-end is designed to work with input capacitances up to 100 pF, the current flowing in the input stage is higher than necessary and more than usually seen in standard MAPS front-ends.

Nevertheless, a future version of the output buffers is envisioned where the output transistor couple is switched off. A possible solution would be by tying the PMOS gate to VDD and the NMOS gate to GND by including switches on their gates. Furthermore, also a set of CMOS switches would be required to detach the head to tail transistors from the output couple.

Stage	Current [µA]	Power/ch [µW]
Preamplifier	250	300
Inverting stage*	20	24
Shaper	55	66
Fast Shaper	27	32
Discriminator	15	18
S&H	90	108
ADC	30	36
Single-to-Diff. Amp.	210	8
Output Buffers (2)	980**	37
Counter + Serializer	3	0.12
SLVS RX (3)	80x3	9
SLVS TX (2)***	2500x2	190

Table 5.4: Power consumption of all blocks within the ASTRA chip. * The inverting stage is disabled when POL = 0 **The maximum current in the output node drawn by VDD is 10+2 mA for the largest signal swing ***The two SLVS TX links can be disabled if not used

5.6.2 CMOS Switches

Throughout the design of the ASTRA chip the adoption of switches has been required. Most analog and digital switches have been designed using CMOS switches which adopt two complementary transistors with the same channel size. This reduces the charge injection noise when the gate is turned off [21]. In some cases, the usage of CMOS switches was not necessary due to either the switches being statically configured during operation or because they were connected to non-primary nodes with passing currents that would quickly remove the injected charge. In these cases, a PMOS or an NMOS would suffice.

5.6.3 Layout Features
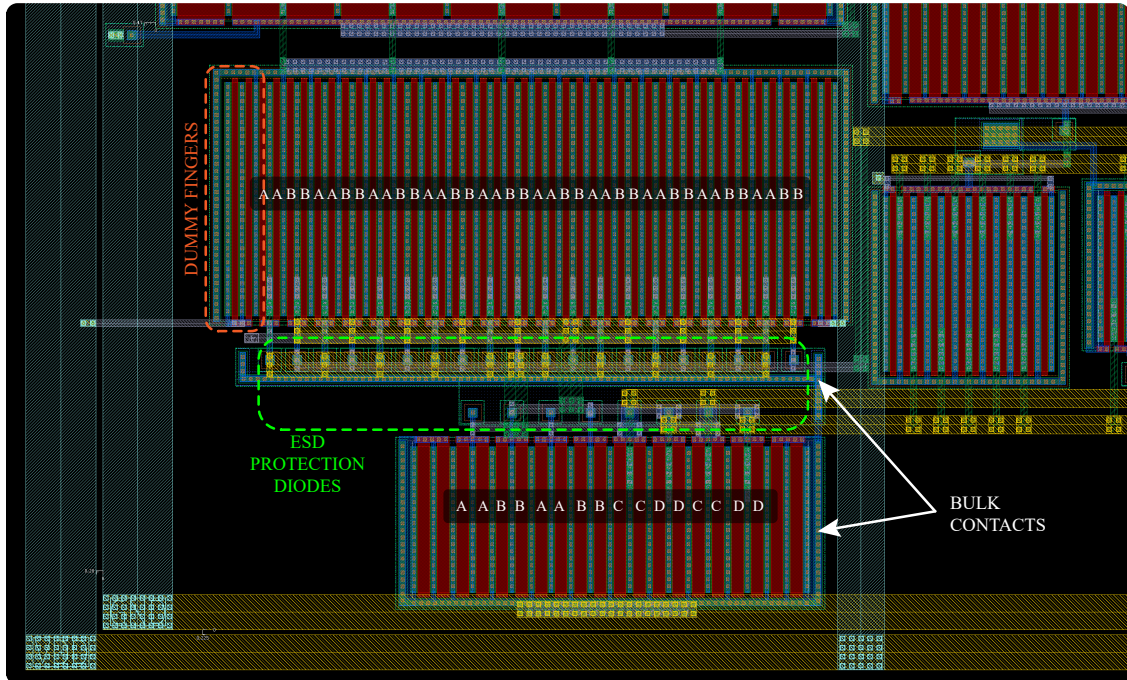
Figure 5.23: ASTRA Inter-digitized Transistors.

The design of the ASTRA electronics has adopted some measures to minimize mismatch issues in the layout design. One example is the design of current-mirrors or differential couples using inter-digitized fingers transistors. The adoption of an inter-digitized fingers layout yields a lower mismatch between the transistors leading to a better manufacturability and lower variability between devices on the same reticle and between different produced wafers. For example, the layout zoom on the input transistors of the output buffer in is in figure 5.23. Thanks to having the bulk connected to the same voltage, the fingers of the two input transistors have been inter-digitized. In the figure, the layout of the input transistor couple is on top and the four current mirrors (M4 to M7) are at the bottom. In particular, when designing inter-digitized transistors the most common configuration adopted has been the AA-BB configuration as shown in the layout zoom.

Another tweak adopted for lower mismatch has been the use of dummy fingers for all transistors. This reduces the variability of fingers within the same transistor or within a set of transistors that should share the same layout footprint, e.g. current mirrors.

Moreover, in the case of current mirrors or sets of transistors requiring scaled versions of a reference transistor (such as the class-AB output transistors), special care in keeping the transistors in the same direction has been taken.

Finally, in order to improve the functioning chip yield, a set of ESD protection diodes have been connected to the gates of all un-protected transistors in order to reduce the antenna effect and charge buildup during the manufacturing process.

5.6.4 Biasing Scheme

ASTRA has been designed with bias cells which propagate the correct currents and voltages within the electronics. Most bias cells have been designed to generate the required voltages and currents on-chip through the adoption of poly-silicon resistors. Nevertheless, most bias currents and voltages are over-writable by the adoption of the east biasing pads, once the ext_bias pad has been tied to 1.2 V. This bit opens the connection to the on-chip biasing resistors and enables the bias voltages and currents to be forced through the bias pads.

The bias topologies adopted are of two types:

- Current biases: a set of current mirrors biased through resistors propagate the correct currents to the transistors that act as current sources.

- Voltage biases: in order to bias cascode transistors or reference voltages, a set of resistor pairs, acting as voltage dividers, are adopted.

In figure 5.24 the two bias topologies and the switch required for external bias overwriting are shown. However, some more delicate biases, e.g. I_{ADC}, are not internally generated and must be generated off-chip.
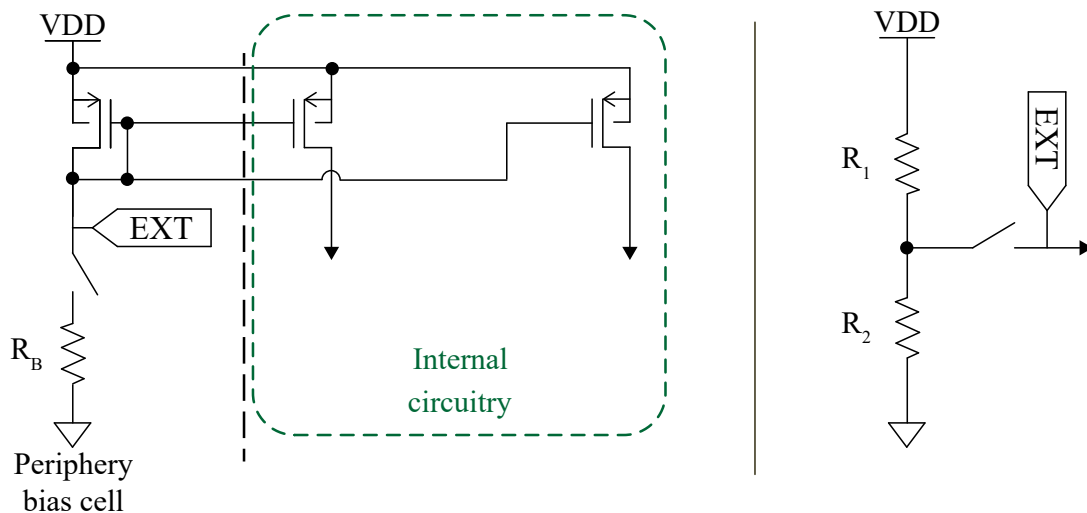
Figure 5.24: ASTRA Bias Circuitry. On the *left* the current biases are shown, whil, on the *right* the voltage dividers. The EXT labels indicate where the external pads connect to the internal bias cells.
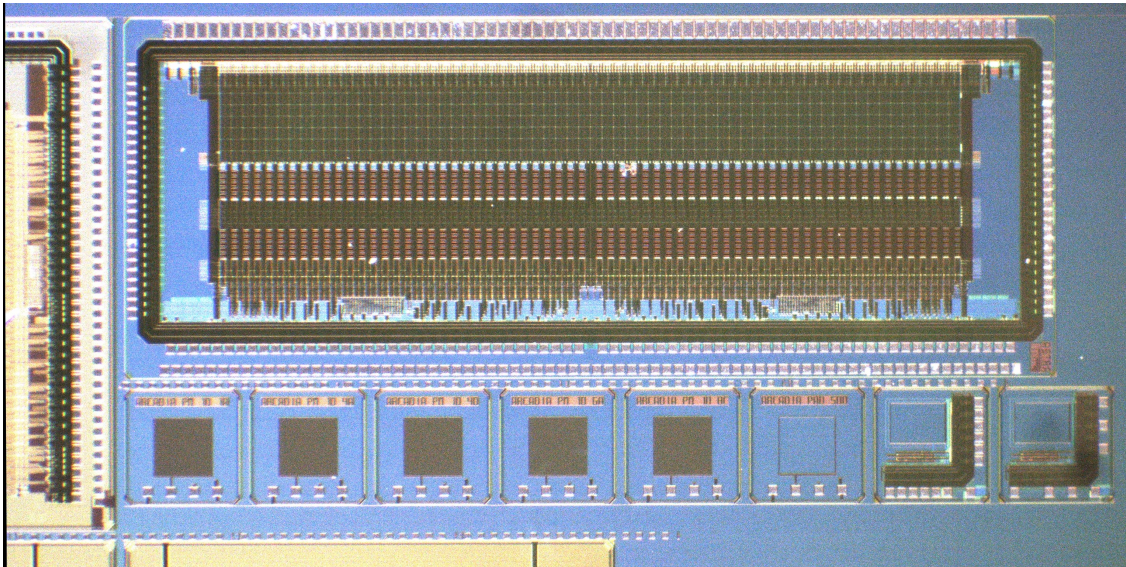
Figure 5.25: Microphotograph showing ASTRA64 of top. The pads connecting towards the microstrips are visible on top, while the control pads at the bottom. On the right and left side the bias pads are shown. The cut structure on the left, on the other hand, is the bottom end of the monolithic active microstrip sensor with ASTRA32 readout. The bottom squared structures are passive and active prototypes.

Chapter 6

Conclusions and future research

In this thesis, the research and development of a novel fully depleted monolithic microstrip detector has been presented. Starting from an overview of the latest state of the art technologies in monolithic active pixel sensors, the novel detector design proposed by the ARCADIA collaboration has been discussed. The sensor and electronics characteristics have been fully simulated and studied. Furthermore, the close Italian research centers collaboration between INFN and Universities from Torino, Trento, Bologna, Como, Pavia, Padova, Perugia and Milano has rendered the realization of the detector feasible. In particular, the fully monolithic devices have been produced adopting a high resistivity substrate combined with a commercial 110 nm CMOS BSI technology. The design criticalities and simulation results have been described and explained.

Extensive experimental campaigns have proven the full depletion of the sensor, precise electric characteristics simulation capability and a high and uniform charge collection efficiency. By testing the first active test structure, MATISSE, the sensor to CMOS connection has been proven functional and correctly predicted by previous simulations.

From the experience in the production of the passive and active test structures a new design for a novel fully depleted monolithic active strip sensor has been done. A practical layout description of the sensor manufacturability steps and foreseen possible issues have been summarized in chapter 4.

Finally, a fully modular front end with selectable analog or digital output, named ASTRA, has been designed and produced. In particular, the chip has been produced in two versions, one monolithically integrated at the end of 32 1.2 cm long 100 μm wide microstrips and one standalone version capable of reading 64 external commercial microstrips. In order to conveniently reduce the complexity of designing two different ICs for similar applications, the design shares the same 32 amplifying channel layout in both versions by including a mirrored version in the standalone 64 channel device.

ASTRA features configurable gain, peaking time and LSB resolution. The IC has been designed to work without the use of external non essential biases, but has kept the possibility of overwriting them through dedicated external bonding pads.

The layout of the monolithic version required extra care compared to the standalone version due to the possibility of collecting stray charges in the volume below the electronics. Thus, deep p-wells and guard rings have been designed to prevent electronic noise from degrading the device performance.

Thanks to these features, the active monolithic microstrip sensor is appealing to the space and particle tracking community thanks to its configurability, selectable readout method and low number of interconnections required to function correctly compared to a discrete electronics solution.

The author's contribution has ranged from the first characterizations of the SEED sensors to the design of the electronic blocks within the ASTRA design team. In particular, some of the first laser tracking performance tests on the active test structures and the initial IV and CV measurements on the passive test structures were performed in Turin. The results of the latter characterizations led to the experimental campaigns in Zagreb adopting the proton micro-beam and TCT evaluations on the pseudo-matrices. The experimental data acquired has been processed and studied leading to the publication in IEEE's transaction on electron devices journal [61]. The sensor improvements in the latest ARCADIA runs have been rendered possible by the thorough evaluation of the experimental results and by adapting the new TCAD sensor designs to the foundry's DRC rules. Lastly, the general design of the ASTRA electronics has been developed with help from the author. Moreover, the design of the analog readout chain and the channel verifications have been carried out by the author.

Concluding, future experimental activities are expected to fully characterize ASTRA's performance and prove the feasibility of fully depleted monolithic strips with embedded electronics. Furthermore, once the characterization has been completed, the design of a new version which embeds the CMOS electronics within the pixelated microstrip deep p-wells is envisioned. This would enable a high fill factor for each sensor and lead to large scale integrated microstrips for future physics experiments.

6.1   List of PhD Publications

- Depleted MAPS on a 110 nm CMOS CIS Technology [32];

- DarkSide-50 results and the future liquid argon dark matter program [20];

- Fully Depleted MAPS in 110 nm CMOS Process With 100–300 µm Active Substrate [61];

- Micrometric laser characterization of a 300µm fully-depleted monolithic active pixel sensor in standard 110 nm CMOS technology [31];

- Design and construction of a new detector to measure ultra-low radioactive-isotope contamination of argon [1];

- Sensitivity of future liquid argon dark matter search experiments to core-collapse supernova neutrinos [6];

- Separating ^{39}Ar from ^{40}Ar by cryogenic distillation with Aria for dark-matter searches [7];

- SiPM-matrix readout of two-phase argon detectors using electroluminescence in the visible and near infrared range [2].

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