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Optimal Tuning of AGDs Parameters and a Technique for Testing the Correct Mounting of Heatsinks on Power Transistors

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Summary

Nowadays, energy conversion is one of the most popular topics addressed both in research and industrial environment. The reason for that is, in the last decades, the energy consumption related to carbon fossil combustion has caused several negative effects on the environment, such as the global warming and the increase of the pollution level, leading the humanity to spend time and resources for increasing the utilization of energy sources with a low impact on the ambient, like the photovoltaic and the wind generated ones. Even if such forms of energy are "*green*", they need to be converted and delivered in order to be exploited in the best way. Such subject has brought the *Power Converters* and all the related topics, and components which make up the power module to become a burning issue of the last years.

When speaking about the conversion of the energy, the designer has to deal with several issues, among which the efficiency and thermal management of the system, which are two of the most critical aspects of the design flow, both mainly related to the most important components of a power converter, the *power switches*. These components are continuously under investigation, in order to improve their performance in terms of voltage and current handling, switching speed and power losses, leading the Silicon device to approach very close their theoretical limits. For such a reason, new semiconductor materials, the Wide Band-Gap (WBG), have been investigated to develop even more performant power switches, with the aim of replacing their Silicon counterpart. Such devices, with their faster switching transients and smaller parasitic capacitances, can excite high frequency resonant circuits resulting in oscillations, overvoltages and/or overcurrents that could destroy the power transistor and increase the level of the Electromagnetic Interference (EMI). Traditional approaches to solve such an issue consist of using snubber circuits and/or to reduce the strength of the driver, increasing the gate resistance. If such solutions remove the oscillations, reducing the overvoltages and the overcurrents, they can reduce excessively the switching speed of the transient, increasing the switching losses and so the temperature of the switches, which need even larger heatsinks to dissipate the produced heat and making ineffective the use of WBG devices.

A consolidate solution to fix such issues consists of using Active Gate Driver (AGD) to turn-on and to turn-off the power switches. Such solution allows the designer to control the switching waveforms during the transitions, by modulating

the strength of the driver and providing the user the capability to find the best trade-off between the power losses and the switching speed. Notwithstanding the effectiveness of the AGD techniques, it worth highlighting that in literature no method to derive the gate driving profile is provided, and the driving waveform is often obtained by means of trial and error approach.

The aim of the first part of this thesis is to fill such gap, by providing a mathematical model to obtain the optimal switching waveforms, i.e, the non oscillating and less dissipative ones is proposed, and then an algorithm to obtain the optimal gate current profile by means of simulation is proposed. The optimal switching waveforms, along with the parameters resulting from the proposed algorithm, are a step forward with respect to the trial-and-error or local optimization methods that can be found in literature. Indeed, the proposed approach provides the target output waveforms, thus knowing in advance the best trade-off between power dissipation and switching speed. The method discussed in this work is then applied on a prototype, resulting in the optimal switching waveforms expected from the proposed analysis.

In the second part of this thesis, the focus moves on the thermal management of power transistors, more precisely on the capability of a power MOSFET, on which is mounted an heatsink, to dissipate the heat. In particular, two manufactury test strategies are proposed, to check the correct assembling of an heatsink on the power switch. Such techniques are based on the linear relationship existing between the drain source on resistance ($R_{ds,on}$) and the junction temperature T_j, so they do not require any temperature measurements, once the calibration procedure is performed. The former technique can be applied to transistors whose gate can be reached with an Automatic Test Equipment (ATE) controlling the duration of the on phase of the device, the latter can be applied on power transistors mounted in hard switching power converters, while they are normally working. The proposed technique are both experimentally assessed considering several commercial heatsinks and different induced thermal faults, which simulate the incorrect behavior of the heatsink. The experimental validation has allowed for the identification of the thermal faults in more than 90% of the analyzed cases.

Keywords: Active Gate Driver, Optimal Switching Waveforms, Power Transistor Heatsink Testing.

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List of Acronyms and Symbols

AGD	Active Gate Driver
ATE	Automatic Test Equipment
AWG	Arbitrary Waveform Generator
BJT	Bipolar Junction Transistor
$\mathbf{C_{gs}}$	Gate Source Capacitance
$\mathbf{C_{gd}}$	Gate Drain Capacitance
$\mathbf{C_{ds}}$	Drain Source Capacitance
$\mathbf{C_{snb}}$	Snubber Capacitance
$\mathbf{C_{out}}$	Output Capacitance
$\mathbf{C_{p}}$	Parasitic Capacitance
$\mathbf{C_{p,eq}}$	Equivalent Parasitic Capacitance
$\mathbf{C_{t}}$	Test Capacitance
$\mathbf{C_{th}}$	Thermal Capacitance
CU	Control Unit
$\mathbf{D_{id}}$	Ideal Diode
$\mathbf{D_{HS}}$	High Side Diode
$\mathbf{D_{snb}}$	Snubber Diode
EMI	Electromagnetic Interference
$\mathbf{E_{snb}}$	Snubber Energy
$\mathbf{E_{off}}$	Turn-off Energy
$\mathbf{E_{on}}$	Turn-on Energy
$\mathbf{f_{r,i}}$	Resonant Frequency
$\mathbf{f_{sw}}$	Switching Frequency
GaN	Gallium Nitride
GTO	Gate Turn Off (Thyristor)
$\mathbf{G_t(t)}$	Time Variant Conductance
$\mathbf{I_{A,B,C,on}}$	ON Levels Gate Driver
$\mathbf{I_{A,B,C,off}}$	OFF Levels Gate Driver
$\mathbf{I_{c,p}}$	Parasitic Capacitance Current
$\mathbf{I_{d}}$	Diode Current

$\mathbf{I_{drv}}$	Driver Current
$\mathbf{I_g}$	Gate Current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
$\mathbf{I_{out}}$	Output Current
$\mathbf{I_{sw}}$	Switch Current
$\mathbf{k_i}$	Damping Coefficients
$\mathbf{k_{i,opt}}$	Optimal Damping Coefficients
$\mathbf{L_{an}}$	Anode Inductance
$\mathbf{L_{cat}}$	Catode Inductance
$\mathbf{L_{c,i}}$	Parasitic Inductance of Capacitance
$\mathbf{L_d}$	Drain Inductance
$\mathbf{L_g}$	Gate Inductance
$\mathbf{L_{in}}$	Input Inductance
$\mathbf{L_{output}}$	Output Inductance
$\mathbf{L_{p,i}}$	Parasitic Inductance
$\mathbf{L_{p,eq}}$	Equivalent Parasitic Inductance
$\mathbf{L_s}$	Source Inductance
$\mathbf{L_{t,i}}$	Trace Inductance
$\mathbf{L_{snb}}$	Snubber Inductance
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
$\mathbf{P_{diode}}$	Diode Power
$\mathbf{P_{dis}}$	Dissipated Power
$\mathbf{P_{on}}$	ON Power
$\mathbf{P_{snb}}$	Snubber Power
$\mathbf{P_{sw}}$	Switch Power
$\mathbf{P_{tot}}$	Total Power
$\mathbf{Q_{A,B,C,on}}$	Turn-on Charge
$\mathbf{Q_{A,B,C,off}}$	Turn-off Charge
$\mathbf{R_{in}}$	Input Resistance
$\mathbf{R_{out}}$	Output Resistance
$\mathbf{R_{snb}}$	Snubber Resistance
$\mathbf{R_t(t)}$	Time Variant Resistance
$\mathbf{R_{ds,on}}$	Drain Source ON Resistance
$\mathbf{R_g}$	Gate Resistance
$\mathbf{R_{th}}$	Thermal Resistance
$\mathbf{R_{load}}$	Load Resistance
SiC	Silicon Carbide
$\mathbf{S_{id}}$	Ideal Switch
SOA	Safe Operating Area
$\mathbf{T_a}$	Ambient Temperature
$\mathbf{T_j}$	Junction Temperature

$\mathbf{T_{HS}}$	High Side Transistor
TIM	Thermal Interface Material
$\mathbf{T_{LS}}$	Low Side Transistor
TSEP	Thermal Sensitive Parameters
PCB	Printed Circuit Board
PWM	Pulse Modulated Width
UART	Universal Asynchronous Receiver-Transmitter
$\mathbf{V_{ctrl}}$	Control Voltage
$\mathbf{V_{ds}}$	Drain Source Voltage
$\mathbf{V_{gs}}$	Gate Source Voltage
$\mathbf{V_{in}}$	Input Voltage
$\mathbf{V_{Miller}}$	Miller Voltage
$\mathbf{V_{od}}$	Overdrive Voltage
$\mathbf{V_{ps}}$	Power Supply Voltage
$\mathbf{V_{sw}}$	Switching Voltage
$\mathbf{V_{test}}$	Test Voltage
$\mathbf{V_{th}}$	Threshold Voltage
WBG	Wind Band-Gap Semiconductor

Chapter 1

Introduction

Nowadays, topics as pollution, global warming and petroleum resource depletion are of particular interest for humanity, because such problems have a considerable impact on the environment and consequently, on human life. Such an issue has addressed researches and governments to spend time and resource to develop and to improve the technologies related to the *alternative forms of energy*.

About 86% of the total energy in the world is generated by fossil fuel, the 4% comes from nuclear plants and only the 10% is generated by means of renewable energy sources [1, 2]. Burning of fossil fuel produces pollution, that leads to problems like acid rain and global warming, affect the environment, causing alterations, especially in the flora and fauna of the developing countries. Scientists have estimated that the average temperature will rise of 2-5°C every 100 years, with serious effect on climate changes, like the melting of the glaciers in the Arctic and Antarctic Oceans and the increase of droughts in the countries near to the equator, that will damage vegetation and agriculture [3]. As highlighted in [1–3], the fist step to mitigate the climatic change problems is to increase the consumption of energy in electrical form, focusing on the electrical energies produced by means of renewable energy sources like the wind and the solar ones, exploited with turbines and photovoltaic plants, respectively [4]. As already mentioned, the main cause of the pollution is related to the carbon fossil combustion. For such reason, internal combustion engine of the automobile could be replaced by electric vehicles [5]. Similarly, other fossil fuel based means of transportation could be replaced by electric ones.

All such forms of renewable energy have a common subject: the energy stored in the power cells and the energy produced by photovoltaic plants need to be converted and distributed. For example, the photovoltaic cell panels, the most popular technology for produce renewable energy, source a DC low voltage that need to be converted in AC in order to be distributed [3]. In fact, after its generation, the energy must be delivered to the consumers, since the energy sources are often far

away from the loads. This task is assumed by *Power Grids* that control the distribution of the energy from the source to the loads, that often requires a conversion of the energy from AC to DC. For such reason Power Electronics play a key role in the fight against the pollution and the global warming, as a means to convert and to distribute green energy. As highlighted in [3], *all the modern renewable energy systems cannot work, and the smart grid cannot be realized, without Power Electronics*.

The close involvement of power electronics in these critical issues for human life, has addressed several researcher to focus their work on the development of new and more efficient converter topologies, but also to study the introduction in the market of new, and more performing, technologies for producing *power switches*, the beating heart of each power converter. Referring to such new technologies, GaN and SiC power transistor, whose performances results to be much better than the ones of the traditional Silicon devices, must be mentioned, as well as the new challenges that these devices place in terms of *reliability*, another hot topic when dealing with power conversion system.

The aim of this chapter is to provide the reader with some basic information about the structure of the power conversion systems, focusing mainly on the power switches, the new technologies to produce them and on their reliability, that as introduced in the abstract, is the main topic of this work.

1.1 Power Electronics in Renewable Energy Systems

In order to transform the renewable forms of energy in electrical one, conversion equipments are needed. For example, referring to wind energy, turbines and generators are used to regulate the frequency and the voltage of the distribution systems, while, referring to solar energy, DC-AC converters are used to convert the the DC source of the cell-based solar panels to the fixed frequency AC voltage that the local system distribution requires [3]. In fact, all energy sources require to be converted in electrical ones before to be delivered for consumption. Also the distribution of the energy requires control and conversion, since it is transmitted for long distance and used in other forms respect to the one generated at the source. In fact, during its distribution, the voltage needs to be stepped up to reduce the losses along the lines and then stepped down and rectified to be exploited from the end user.

Traditional equipment to convert and share the electrical energy are based on electromagnetic or electromechanical systems. All such solutions are characterized by limited control capability or by a slow frequency response, so power electronic based converters are becoming an effective alternative to the traditional solutions [3]. This because power converters are based on electronic power devices, that are faster with respect to their electromechanical and electromagnetic counterparts;

moreover power switches have higher power handling capability, an higher flexibility and an higher capability. [6].

Nowadays, power electronics converters and controllers are an important part of equipment for electrical energy generation and its delivery, and their role is growing rapidly with the continuous improvement of power electronics technologies, as well as with emerging needs like renewable energy systems, smart grid, and electronic loads. All these motivations has led researchers and practitioners to focus their attention on the efficiency of these systems, but also on their reliability and robustness. Since the power electronic devices make up the heart of the power converters, in the last years they have been subjects of study, exhibiting also better performance.

1.1.1 Power Converter Topologies

Power converters can be classified in four different categories that depends on the function that the converter plays [7]. These categories are:

- Rectifiers, which convert an AC source to a DC output.
- Inverters, which convert a DC source in an AC output.
- DC-DC converters, that change a DC voltage level.
- AC-AC converters which change the amplitude and/or the frequency of of an AC source to an other one.

All these categories can be divided in other sub-categories, but in this work only DC-DC converters, in particular a step down hard-switched topology is considered as a case of study. The hard-switched converters are characterized by commutation that could takes place with simultaneously high values of voltages and currents. This phenomenon plays an important role both for efficiency of the converter and for its reliability, because an high value of dissipated power and this type of switching behavior can damages the fundamental component of the power converters, i.e. the power switch.

1.1.2 Power Converter Reliability

As already stated, one of the most important features of a power converter is its efficiency, so a lot of researchers work to reduce the power losses related to the energy conversion, obtaining even better results. When designing a power converter the efficiency is not the only important features that should characterize it, but its *reliability* is relevant as much as its efficiency. From a mathematical point of view, the reliability is the probability that a system performs its work without failure for a certain time in well defined environmental conditions [8]. The reliability of a

system affects its lifetime, that is the time in which the system can work properly with a constant failure rate. By referring to a power converter, that consists of several components and subsystems a failure can depend on different causes and on different parts of the whole structure, so its analysis could be a difficult and long process. In this work, the concept of reliability is addressed referring to power switches that, as discussed in [8], are one of the components that cause most failures in power converters, being behind only to the DC link capacitor. When speaking about the reliability of a power switch, points like overvoltages, overcurrents, overtemperature and safe operating area become critical.

1.1.3 Thermal Management of a Power Converter

When designing a power converter the thermal management is a critical issue. In fact, if a converter works at low temperature, besides avoiding the damaging of the system related to an high average temperature, a lower temperature increases the lifetime of the converter, as well as its performance. Indeed, power switches work better at lower temperature, maintaining their performance within the ones declared in the datasheet. For instance, for each 10°C of junction temperature increase, the lifetime of a silicon power switch becomes almost an half as highlighted in [7, 8].

In a generic system, after the estimation of the power losses it is possible to size the cooling system. The temperature estimation in a power converter is generally performed at three levels [8]:

- At device level. This thermal evaluation allows the user to choose the device packaging and eventually to select an heatsink for the device.
- At the converter level for calculating the power toward the external environment.
- At the equipment level for choosing the right enclosure for the converter.

As already stated, all the power switches dissipate conduction and switching losses, and the heat produced by this power should be removed as fast as possible to avoid damaging of these components. In this thesis, the thermal issue is analyzed from the stand-point of the power switches, by offering a technique to test the capability of an heatsink mounted on a power device to dissipate properly the heat. Thermal issues related to the whole converter are out of the purposes of this work. Further details and analysis on this topic are reported in Chapter 5, entirely dedicated to the thermal test of the heatsink mounted on power switches.

1.2 Power Semiconductor Devices

Regardless of the type of the converter, each of them contains at least a power switch. The duration of its on and off phases regulates the flow of power from the input to the output.

Power semiconductor switches are the most important and essential components that make up a power converter [7]. Each type of power switch can be chosen to be used in a specific application, according to its features and performances. The performance of a power switch is mainly characterized by voltage and current ratings, the conduction losses, as well as the switching speed and the corresponding losses. The most popular and used power switches are diodes, MOSFET, BJT and IGBT, but there are others, less common components like GTO, thyristors and IGCT [7]. Except for diodes, all the others mentioned devices can be turned on and off with a signal command, so they are called active switches, while diodes are called passive switches [3].

All these devices are silicon based and, since the invention of the first thyristor, the researchers continue to improve their characteristics in terms of blocking voltage, maximum current capability, conduction and switching losses and operation temperature, approaching to the material theoretical limitations. For this reason, in recent years, semiconductor devices based on Wide Band Gap (WBG) materials start to play an important role in the energy conversion [9]. Compared with silicon devices, the WBG ones feature a lower on resistance, a higher breakdown voltage, a higher junction temperature capability and are characterized by a higher switching speed [9–11]. All these characteristics are beneficial for efficiency, high power and voltage capability, size, and cost of power electronics converters, which are essential for the development of renewable energy systems and smart grid applications. On the other hand, such new devices need different topologies of gate driver to change their conductive state. A good power conversion system must be characterized by high reliability, high efficiency and must be small in size and low in cost. Many of these features depend on the converter topology and on the control system, but as stated before, the power switches play a key role for defining the performance of a power converter. There are several characteristics that allow one to establish the performance of a power switch. More precisely, all these features can be divided in different categories which are static, dynamic, control and thermal parameters. Among the most important static characteristics, it is possible to find the maximum current capability of the device and its maximum reverse blocking voltage. As far as the dynamic characteristics are concerned, it is possible to consider the switching times and the switching losses. Finally, referring to thermal performance of the device, the two most important parameters are the maximum junction temperature and the junction to case thermal resistance.

A power switch that operates in a power converter should be able to change its conduction state in a very short time, so that the switching losses are reduced to the

minimum value. The transition times depend both on the technology of the power switch and on strength of the control. On the other hand, short commutations times mean high dV/dt and high dI/dt that cause high levels of Electro-Magnetic Interference (EMI) and could produce cross conduction issues in converters in which the same leg contains more than one controlled switch. For these reasons, when a converter is designed, it is common that the designer looks for the best trade-off between the switching power and the commutation speed.

1.2.1 Safe Operating Area

When a power switch is used in a switching circuit the analysis of the its Safe Operating Area (SOA) is a fundamental step for the designer. The SOA of a power transistor can be defined as the area delimited by the current and the voltage boundaries within which the device can operate without being destroyed [11]. Typical SOA for a power device is shown in Fig. 1.1. For instance, the SOA current limit

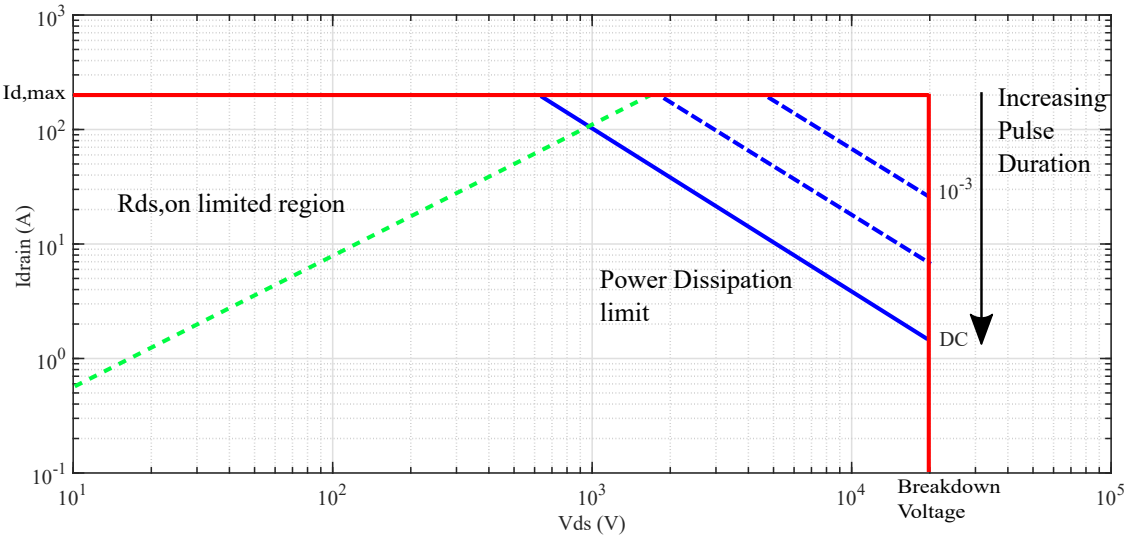

Figure 1.1: Ideal SOA for a power MOSFET.

for a power MOSFET is constrained by the maximum drain current. Generally, this upper limit depends on the melting temperature of the wire bonds used to link the device pads the leads of the package. On the other side, the SOA voltage limit is defined by the breakdown level. In fact, when the device is in the off state, its voltage drop cannot exceed the breakdown limit because the device, under these conditions, would start to conduct current, dissipating a lot of power an increasing the junction temperature. As far as a power MOSFET is concerned, the on resistance introduces a third limit in the SOA that does not allow the device to operate in the region above the green line in Fig. 1.1. The blue boundaries shown in the SOA depend on the maximum junction temperature (T_j), strongly related to the

power dissipated by the transistor. More precisely, the blue solid line refers to the power dissipation limit when the device operates under DC conditions. In fact, in these conditions the maximum junction temperature can be calculated as:

$$T_{\mathrm{j}} = I_{\mathrm{D}} \cdot V_{\mathrm{DS,ON}} \cdot R_{th,ja} + T_{\mathrm{A}}, \tag{1.1}$$

where $\mathrm{R_{th,ja}}$ is the thermal resistance between the junction and the ambient. So, (1.1) establishes a further limit in the drain current value that can be calculate as:

$$I_{D,max} = \frac{T_{J,max} - T_a}{V_{DS,ON} \cdot R_{th,ja}}. \tag{1.2}$$

If the device works in switching mode, as in the case of power converters, the device can sustain larger drain current, because in this case the thermal impedance is lower than the steady state one, and can be expressed as follows:

$$Z_{th} = \frac{Z_{DC} Z_k \sqrt{t_p}}{Z_{DC} + Z_k \sqrt{t_p}}, \tag{1.3}$$

where $\mathrm{t_p}$ is the pulse duration and $\mathrm{Z_k}$ is an impedance related to the device technology and to dissipation conditions [11]. As it is shown in Fig. 1.1, the SOA becomes larger if the transistor is used in pulsed condition and the device can be stressed with higher on current and off voltage, without incurring in thermal faults.

1.2.2 Wide Bandgap Semiconductor

After the brief on generic power switches, and the introduction of the SOA concept by referring to the silicon power MOSFET, in this subsection a short description of the new emerging WBG devices is provided. WBG semiconductors promise to change in better the next generation of power converters. Compared with Si devices, WBG are characterized by low on resistance, high breakdown voltage, high temperature capability and higher switching speed [12]. All these features have positive effects on the efficiency of converters, but also on their reliability. In fact, the high breakdown of these devices allow the designer to find high voltage power transistors smaller than their Si counterpart, and consequently with a lower on resistance and smaller parasitic capacitances that make these devices very fast. A comparison of the main features of WBG with silicon devices is shown in Fig. 1.2.

The high switching speed and the low on resistance make the WBG devices very low dissipative. These features, with the higher temperature capability allow the designer to reduce the size of cooling systems and to increase to switching frequency of the converters, so it is possible to reduce also the size of the EMI filters. The extremely fast switching of WBG semiconductor represents the most critical

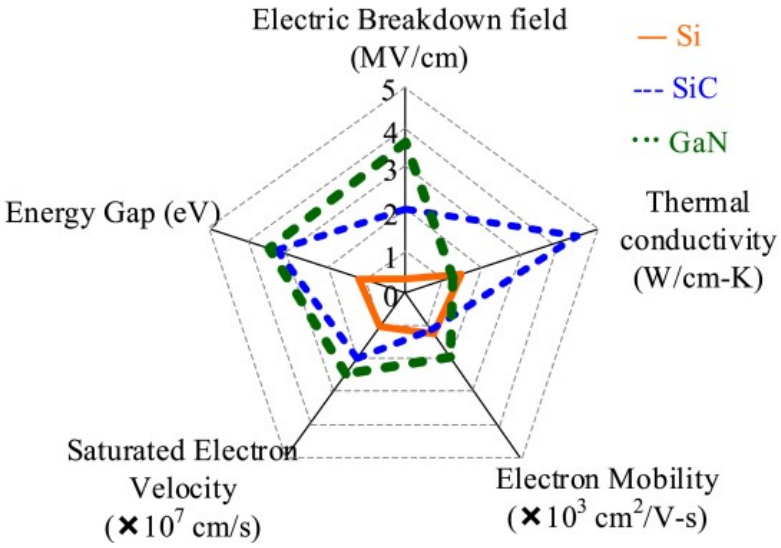

Figure 1.2: Comparison of GaN SiC and Silicon materials properties [12].

challenge for the designer. Indeed, the high slew rate of these devices, greater than 100V /ns and the high di/dt produce a very high level of EMI and could excite small parasitic components, causing voltage and/or current spikes that the commutations of a slower device would not generate.

Voltage Rating

When a power transistor is in the off state, its conductivity is very low since all carriers are blocked by an electrical barrier [3]. In this state it can supports a very high voltage limited by the breakdown of the device, that is when the device starts to conduct current in opposite direction compared to the normally on conduction state. Generally, the operation voltage of a power transistor is chosen to be much lower than its breakdown voltage. For Silicon material, the critical electrical field is about 20Vμ/m while for WBG semiconductors it can reach up to 300V/μm. This feature can be observed in Fig. 1.2[12].

Current Rating

The current rating is a parameter related to the conduction state of a power device. More precisely, this parameter depends on the maximum temperature that the device can reach and is strictly related to the current density of the device [3]. From this point of view SiC and GaN are much better than their Silicon counterpart, because these devices have two points in their favor. The first is higher current density, the second is the higher handling temperature of these materials. Both features give to SiC and GaN power switches better performance in terms of

current rating, if compared with Silicon devices.

Maximum Junction Temperature

The maximum junction temperature of a power device is an intrinsic characteristic that depends on the properties of the semiconductor material. More precisely, the leakage current when a power transistor is off increases with the increase of the junction temperature. This characteristic as well as other characteristics defined by the packaging, results in a temperature of 125°C in silicon power switches or, in better situations, it is possible to reach 150°C [3]. In fact, WBG materials can operate at much higher temperatures, because their leakage current at turn off are very low. In fact, for these devices, the maximum junction temperature is defined by their on state. Indeed, the on resistance of these devices rises up with the increase of the temperature [3].

1.3 Analysis of the switching waveforms in a buck converter

In order to analyze the switching behavior of a generic power switch in a power converter, in this section it is proposed a comparison of the switching waveforms that characterize a buck converter, including step by step the most common parasitic components, that affect the switching transients. The aim of this analysis is to understand how the parasitic components affect the switching trajectories during the turn-on and the turn-off of the switches, highlighting their effects on the SOA of these devices.

In this preliminary analysis, an ideal switch S_{id} and an ideal diode D_{id} are considered as switching components. Then, the ideal switch S_{id} is replaced with a real power transistor to analyze the effects of its parasitic capacitances. All the comparisons deal with the voltage V_{ds} and the current I_{sw} on the controlled switch S and with the voltage V_{sw} and the current I_d on power diode. The given converter is supplied by means the voltage source V_{in}, while its load is modeled with the current source I_{out}. In this analysis, both the ideal switch S_{id} and the real one T_{hs} are driven with an ideal Pulse Modulated Width (PWM) voltage source, because the comparison reported in this section refers only to the power loop, aiming to understand how the transitions and the parasitic elements affect the reliability of the power transistor. The analysis of the input driven loop is reported in the Chapter 3, dedicated to gate drivers.

The first analysis shows a comparison between the switching waveforms resulting from the ideal converter Fig. 1.3(a), in which the power flow is regulated by means of an ideal switch, and the same converter in which this elements is replaced by a power transistor Fig. 1.3(b), with its parasitic capacitances. Both the diodes of the

two circuits are characterized by an ideal behavior. The comparison between the

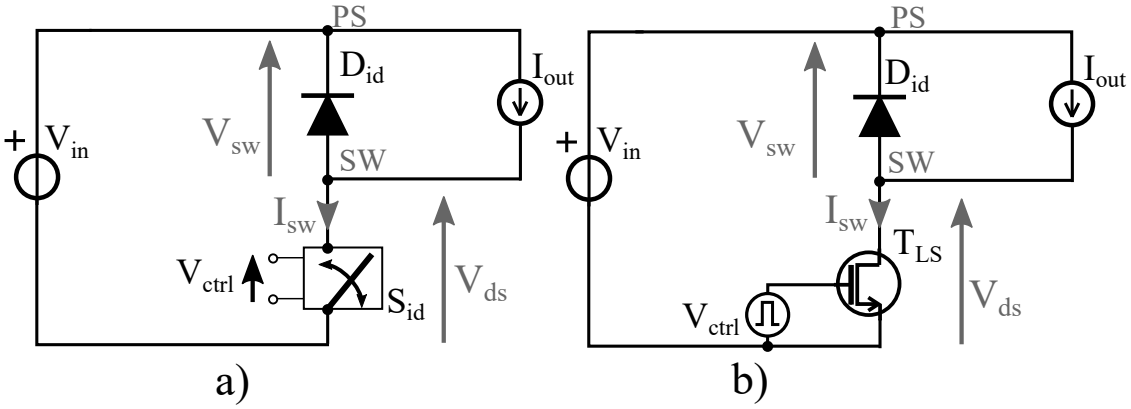

Figure 1.3: Simplified buck converter to analyze the switching waveforms. In a) both the switches are ideal ones while in b) the controlled switch is replaced with a real MOSFET driven with an ideal gate driver.

resulting switching waveforms is shown in Fig. 1.4(a) for the turn-on and in Fig. 1.4(b) for the turn-off. The transients of the dashed switching waveforms, resulting from the analysis of the ideal converter, are all perfectly synchronized with the control signal and take place instantaneously, while the transients resulting from the converter that includes the real transistor, shown in solid lines exhibit both a delay respect the control signal and slower transients if compared with the ones resulting from the analysis of the ideal converter. As far as the the power dissipation is concerned, the ideal converter results less dissipative, because it completely lacks of switching losses, while the limited speed of the transient of the circuit with real transistor, related to the output parasitic capacitances, increases the total losses of the converter reducing its efficiency, but also affecting the reliability of the transistor which reaches a higher temperature. By analyzing the switching waveforms of the converter in Fig. 1.3(b), it is possible to see that when $t = t_1$, i.e., the time instant in which the control signal V_{ctrl} triggers the turn-on, the current I_{sw} starts to increase, while the current I_d starts to decrease in the same manner. In $t = t_2$, both the currents reach their steady state while V_{ds} starts to decrease and V_{sw} to increase until, in $t = t_3$, they reach the steady state. In such a circuit the energy dissipated at the turn-on can be approximated as:

$$E_{on} = \frac{(t_3 - t_2)}{2} I_{out} V_{in}. \tag{1.4}$$

A similar analysis can be carried out at the turn-off of the transistor T_{LS}. After a certain delay from the triggering of the turn-off, in $t = t_5$ the voltage V_{ds} starts to increase while the voltage V_{sw} decreases in the same way. Once these two quantities have reached their steady state, the current I_{sw} starts to decrease, while the current

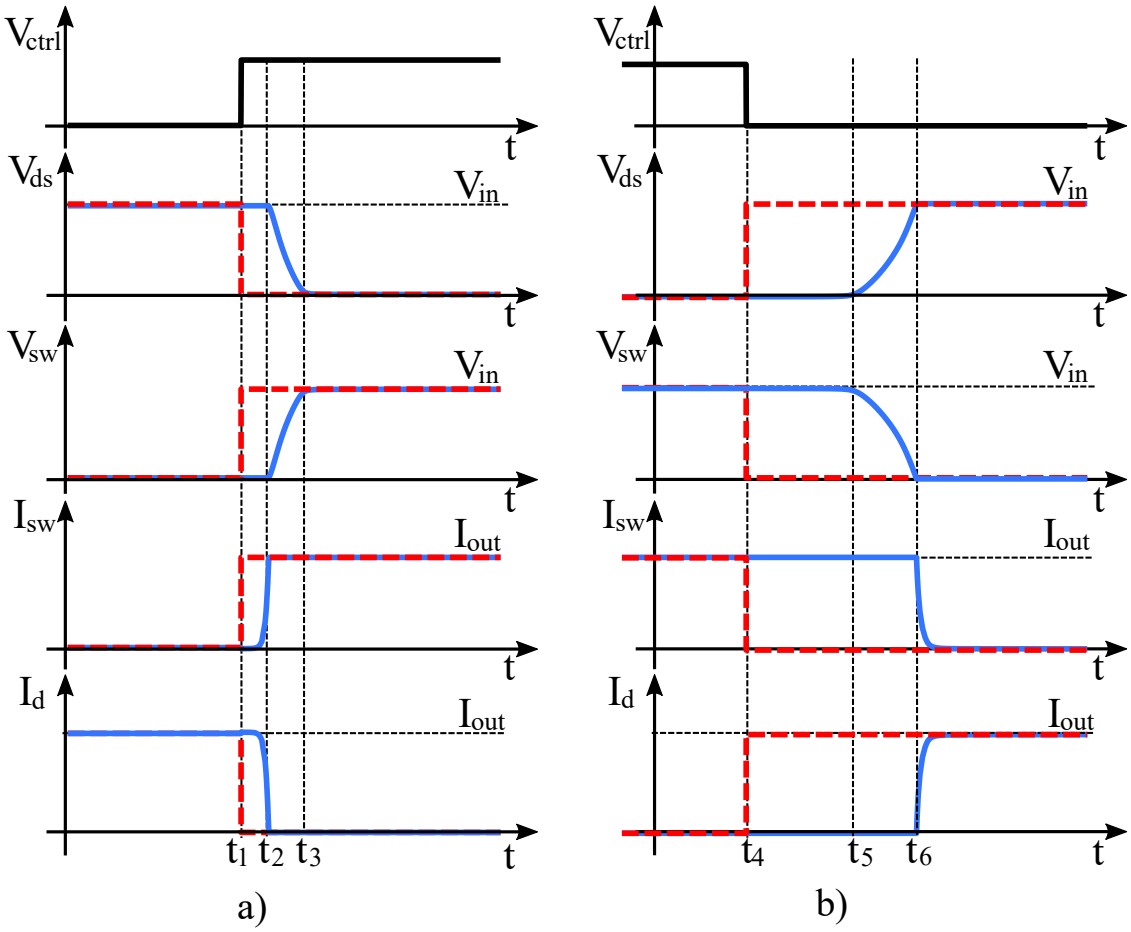

Figure 1.4: Comparison of the switching waveforms resulting from the analysis of the ideal buck converter without any parasitic components (dashed lines) and from the analysis of the same converter in which the switch S_{id} is replaced with a real transistor T_{ls}. In a) the turn-on while in b) the turn-off comparison.

I_d rises. Also in this case, the energy dissipated at the turn-off can be calculated as:

$$E_{on} = \frac{(t_6 - t_5)}{2} I_{out} V_{in}. \tag{1.5}$$

The switching characteristics of the circuit in Fig. 1.3(b) are shown in Fig. 1.5 for both the power switches, to highlight the effects of the commutations on the SOA of such devices. For the sake of simplicity, the same SOA is considered for both the switches. It is worth noticing that for the transistor T_{LS}, both at the turn-on and at the turn-off, the commutations take place with high voltage and current, without causing neither overvoltages and/or overcurrents, but with high dissipative transitions. On the other hand, the transients of the diode D_{id} take place without dissipating any power. Indeed, both at the turn-on and the turn-off, its voltage

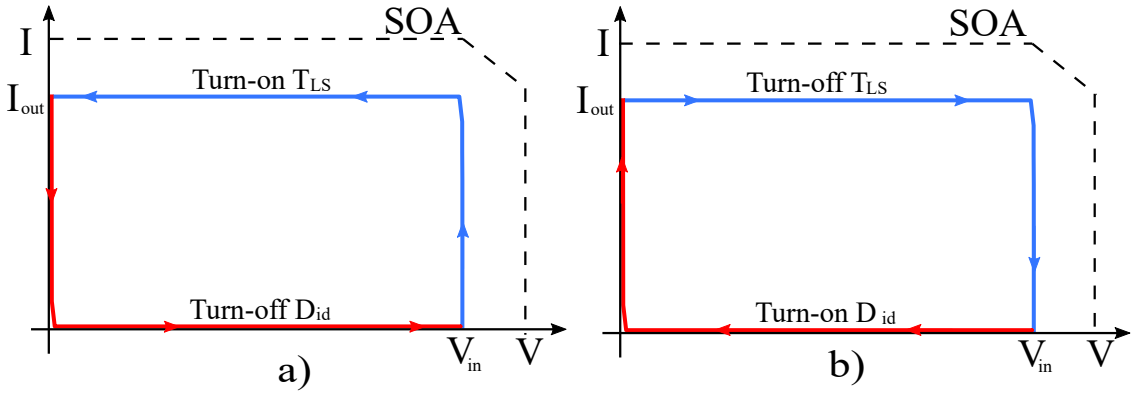

Figure 1.5: Switching characteristics of the transistor T_{LS} (blue lines) and of the diode D_{id} (red line) of the circuit in Fig. 1.3(b). In a) the trajectories refer to the T_{LS} turn-on, in b) to its turn-off.

transients take place with zero current while its current transients happen with zero voltage (Fig. 1.5 in red lines).

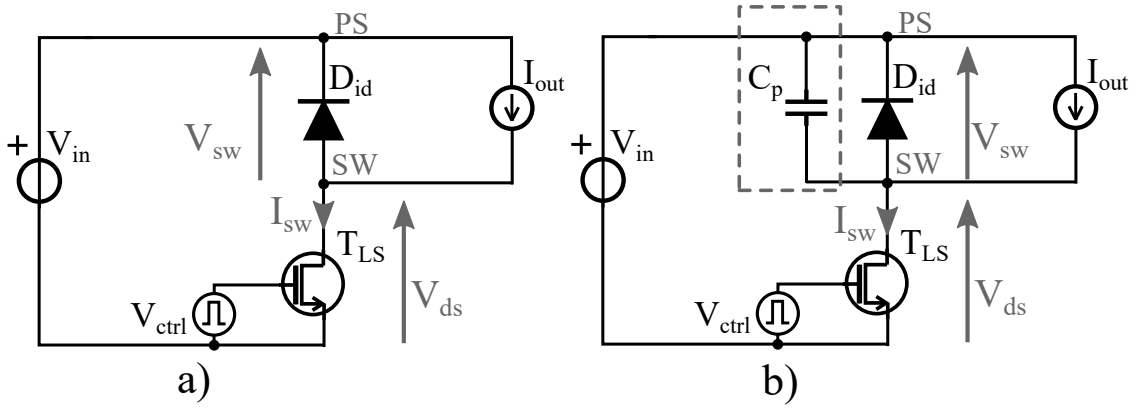

Figure 1.6: Simplified buck converter to analyze the switching waveform. In a) the controlled switch is a real power transistor. In b) a parasitic capacitance C_p is placed in parallel with the ideal diode D_{id}.

In the second step of the comparison, a parasitic capacitance C_p is placed in parallel with the power diode to consider a more realistic behavior of this device, and the the switching waveforms resulting from the analysis of this circuit are compered with the ones resulting from the last considered circuit. The schematics of these simplified converters are shown in Fig. 1.6. The comparison of the switching waveforms resulting from the analysis of these circuits are shown in Fig. 1.7. More precisely, the ones resulting from the converter without the C_p are shown in dashed lines, while those resulting analyzing the circuit that includes such parasitic capacitance are shown in solid lines. In this case, at the turn-on the both the voltage V_{ds}

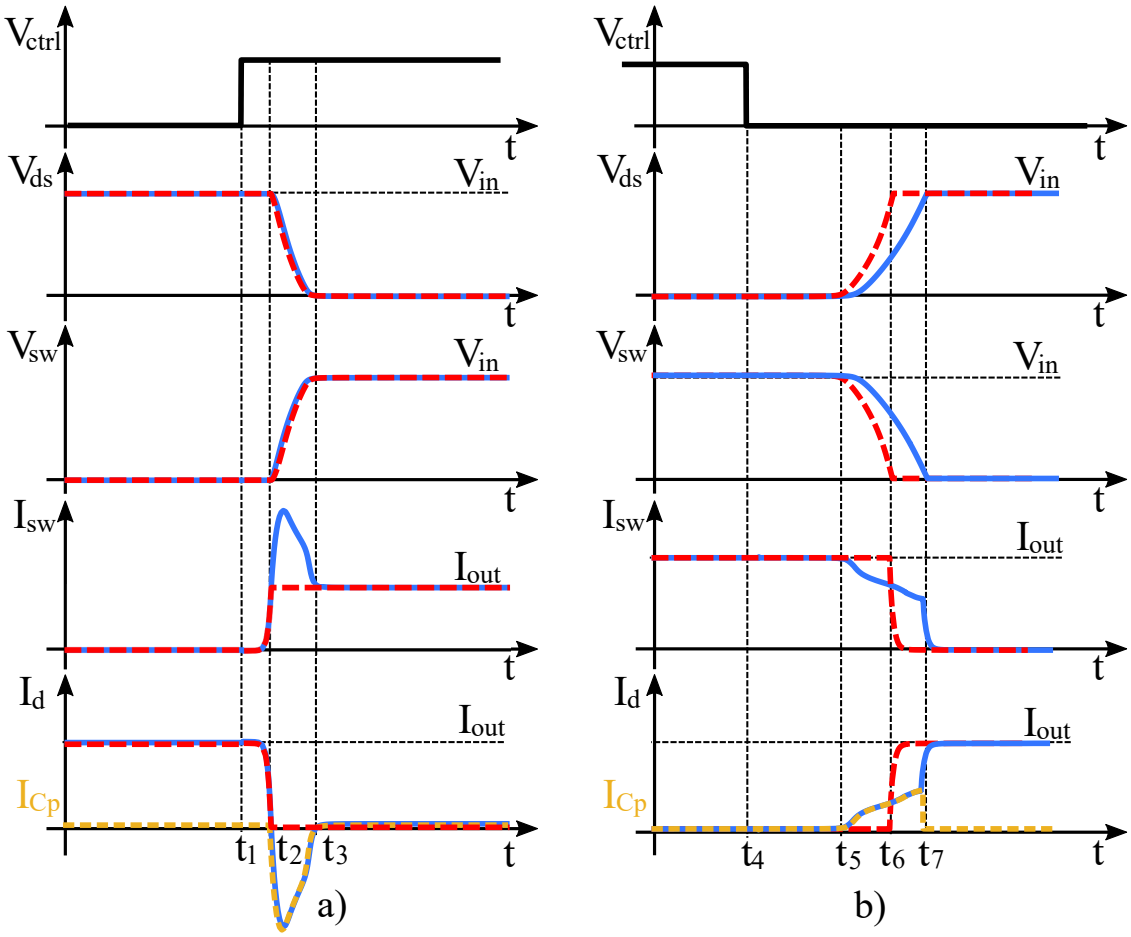

Figure 1.7: Comparison of the switching waveforms resulting from the analysis of the buck converter in Fig. 1.6(a) (dashed lines) and from the analysis of the same converter in which C_p is placed in parallel with D_{id} 1.6(b). In a) the turn-on waveforms while in b) the turn-off ones.

and the voltage V_{sw} preserve the same behavior, but the current I_{sw} and the current I_d are characterized by a peak, related to the charge of the capacitance C_p. From the reliability point of view, such peak means that an overcurrent could damage the power transistor and so compromise the functionality of the power converter. Also the instantaneous power dissipated by the transistor increases, because to charge the capacitance more power is absorbed from the input source. The effect of the capacitance C_p at the turn-on is more appreciable by analyzing the switching trajectory shown in Fig. 1.8(a), in which can be seen that the charging of C_p can destroy the transistor, resulting in a transients out from the SOA. The effect of this capacitance on the turn-off is slightly different because it affects the duration of the transients, changing the power dissipation, but without causing overvoltages or overcurrents. By analyzing 1.8(b), it is worth noticing that such capacitance

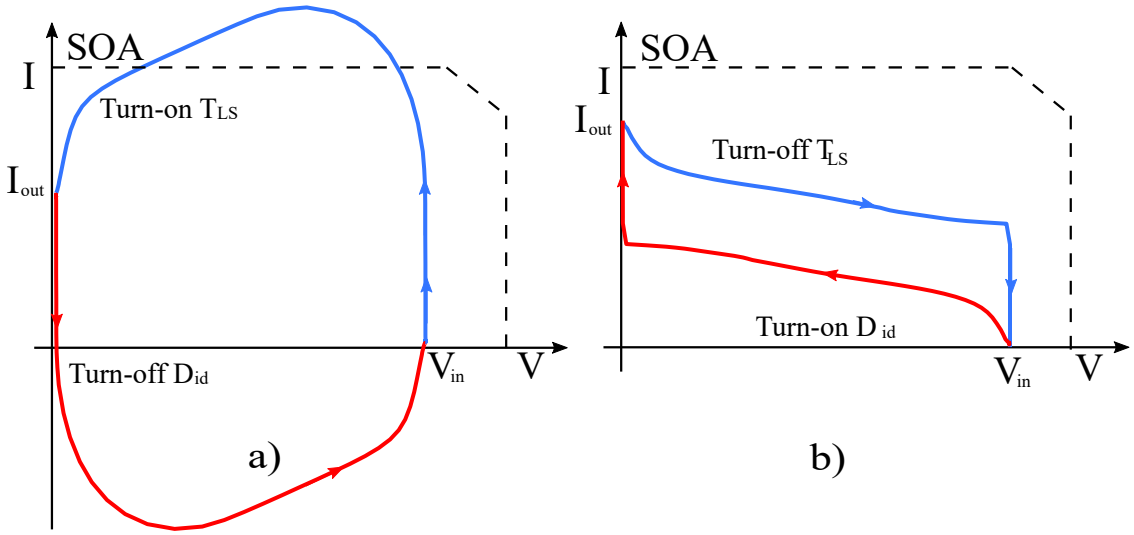

Figure 1.8: Switching characteristics of the transistor T_{LS} (blue lines) and of the diode D_{id} (red line) of the circuit in Fig. 1.6(b). In a) the trajectories refer to the T_{LS} turn-on, in b) to its turn-off.

makes softer the transistor transient, moving away these transients from the SOA boundaries, making dissipative the turn-on of the diode D_{id}.

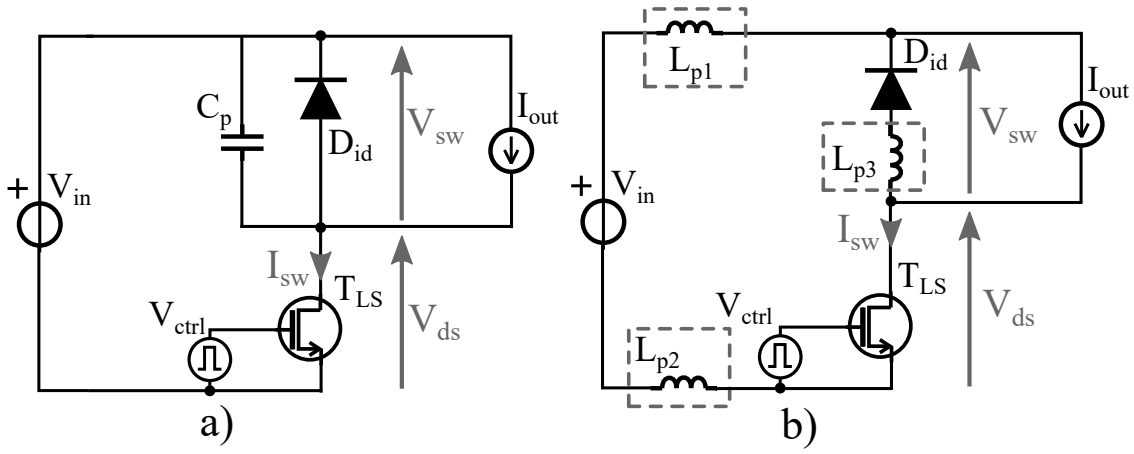

Figure 1.9: Simplified buck converter to analyze the switching waveform. In a) both the controlled switch and the diode have the parasitic capacitance. In b) the parasitic inductances L_{p1}, L_{p2} and L_{p3} are placed in the power loop.

The third step of this analysis consists of inserting in the considered circuit the last parasitic component which affects the transients behavior, the inductance. This element models the bond wires, the PCB traces, and it is distributed along all the power loop. For such a reason, several parasitic inductances are placed in

the power loop, as shown in Fig. 1.9(b), and the resulting waveforms are compared with the ones obtained from the analysis of the circuit shown in 1.9(a), the last one of the previous analysis.

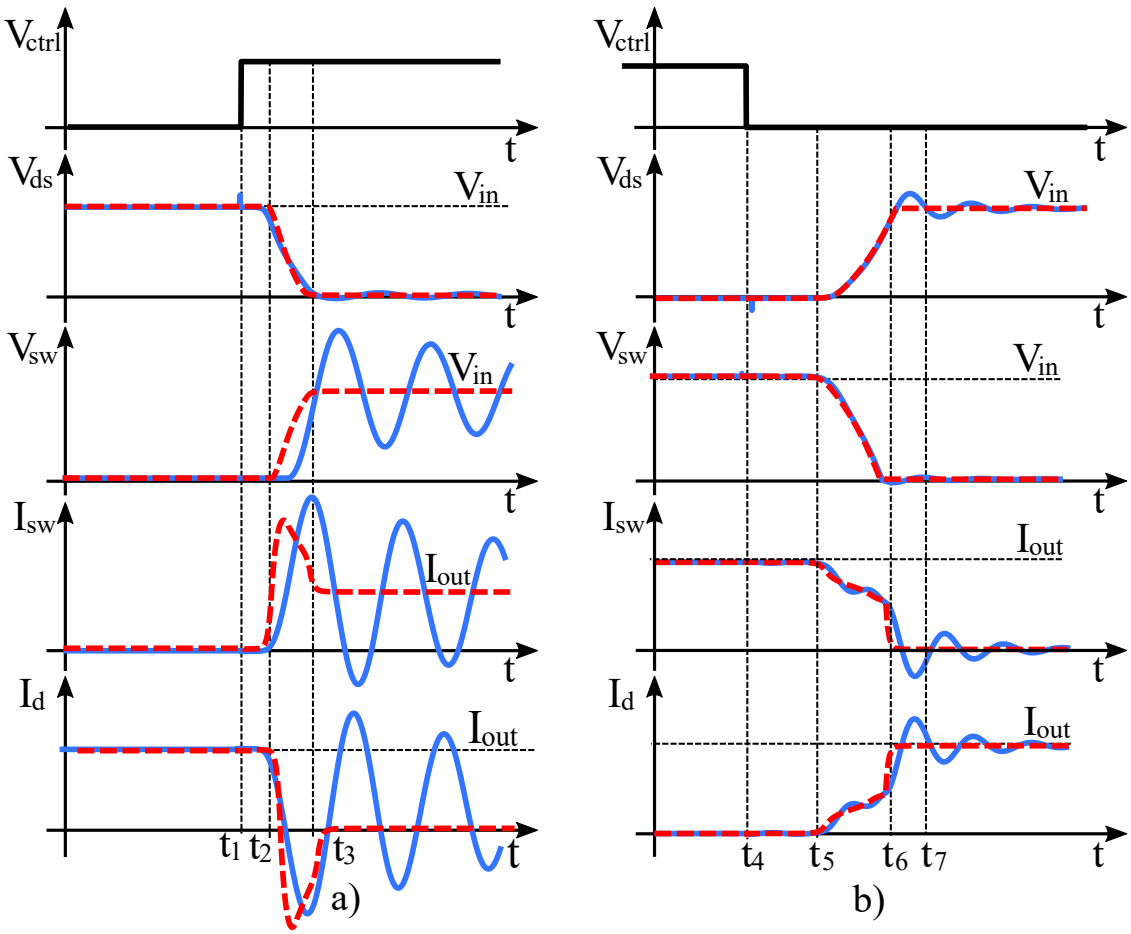

Figure 1.10: Comparison of the switching waveforms resulting from the analysis of the buck converter in Fig. 1.9(a) (dashed lines) and from the analysis of the same converter in which parasitic inductances are placed in the power loop 1.9(b). In a) the turn-on waveforms while in b) the turn-off ones.

By comparing the switching waveforms resulting from the analysis of these two circuits, several considerations can be made. The first refers to the turn-on, more precisely to the voltages V_{sw} and V_{ds} that are not more evenly distributed on the two switches during the transient, because there is a voltage drop on the inductances. The second point refers to the slope of the current I_{sw} which is limited by the inductances. Last but not least is the oscillating behavior that the waveforms assume and the overshoot on voltage V_{sw} 1.10(a).

At the turn-off the parasitic inductances have essentially two effects: the first is the overvoltage on T_{LS} caused by the charging of the inductances L_p and the

second is the oscillating behavior of the switching waveforms. The analysis of the

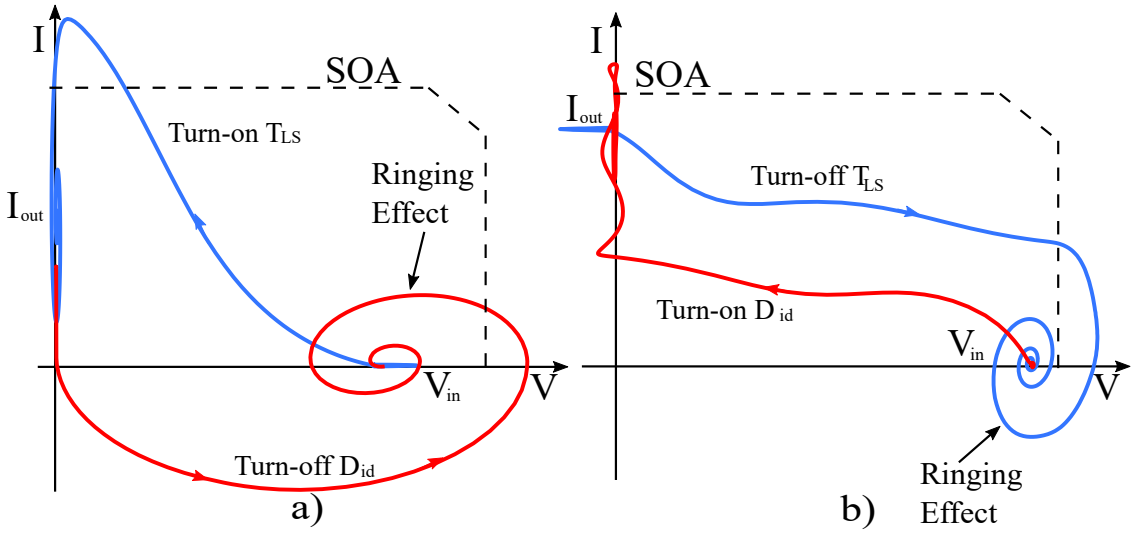

Figure 1.11: Switching characteristics of the transistor T_{LS} (blue lines) and of the diode D_{id} (red line) of the circuit in Fig. 1.9(b). In a) the trajectories refer to the T_{LS} turn-on, in b) to its turn-off.

switching characteristics in Fig. 1.11, shows all the already analyzed effects and also a positive effect that such inductances have on the turn on switching waveforms. More precisely, the voltage drop on these inductances reduces the stress on the switch T_{LS} at the turn on but, as already stated, increase it on the high side diode, on which it is possible to see a peak of voltage. It is worth noticing that the oscillations superimposed to the switching waveforms increase the stress on the power switches as well as the level of EMI, so it is a good practice to attenuate that with proper damping circuits.

1.3.1 Electromagnetic Interference

Switching circuits generate electromagnetic interference both in conducted and radiated forms [7]. The conducted EMI can be generated in differential mode or in common mode. The former depend on current slopes of the power switches, the latter on their voltage slopes and on the parasitic capacitances to ground. EMI generated with power converters depend on several factors, i.e., the switching frequencies, the voltage and current slopes, but also the impedance of the power supply and the length of the cables from the converter to the load. EMI level is strictly related to frequency spectrum of the switching voltages and currents. When ringing phenomena occurs, the frequency spectrum of the oscillating waveforms exhibits peaks that affect the EMI level, as shown in Fig. 1.12(b). These peaks depend on the oscillating behavior of the switching waveforms, thus unwanted oscillations

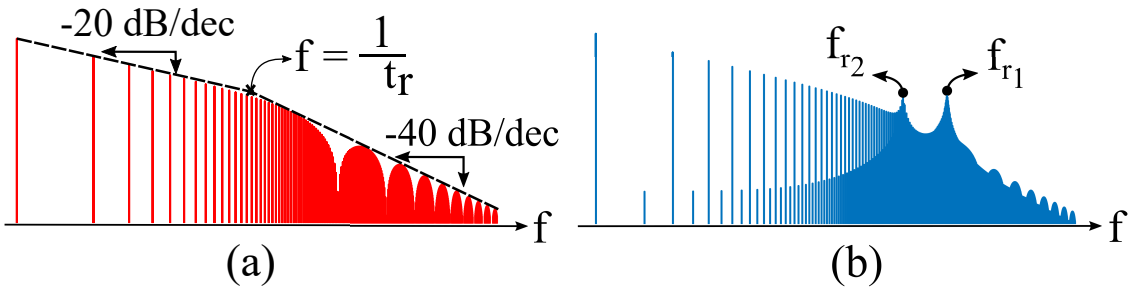

Figure 1.12: Frequency-domain representations of (a) an ideal trapezoidal, and (b) oscillating waveform.

have to be avoided. Snubbers are the most common solution to suppress oscillations and, in the next section, the most popular topologies will be introduced.

1.4 Snubber Circuits

One of the most common and simple solutions to attenuate the oscillations in a power converter consists of using snubber circuits. In [13], Severns provides a clear definition of a snubber circuit, describing it like *"a network that alters the voltage and/or current waveforms of a switch during its turn-on and/or turn-off"*. Although, this definition is correct, it is so general and does not give an overall picture about the importance of the snubbers in the switching circuit, because it does not highlight all the functions that a snubber plays in such circuits. The most important functions are to limit the peaks of current and/or voltage, and their time derivative. In this way, snubbers improve the converter reliability, reducing the electrical and/or thermal stresses of the device, shaping voltage and current in order to stay within the SOA boundaries of the device, and reducing the level of the EMI. In addition, snubbers can be used to balance the voltage sharing between series devices, and to distribute the current in parallel connected ones. These features all contribute to extend the lifetime of the switches, improving the reliability of the whole converter.

1.4.1 Snubber Classification

There are several types of snubber circuits, that can be simply categorized as follows [13]:

- Passive snubbers, that include only linear lumped elements, i.e. resistors, capacitors and/or inductors.
- Active lossy snubbers, which include in the passive network, also active devices like diodes or transistors. Such snubbers dissipate the great part of the

switching losses, avoiding that this energy is dissipated in the power device.

- Active low-loss snubbers, that recover the switching losses, delivering them to the input source or to the load.

An additional important aspect that must be considered when using a snubber is related to the compromises its usage requires. In fact, as stated in [13], each time a snubber is introduced in a circuit to attenuate one problem, new different stresses will be introduced for the switches. For such a reason, when the designer deals with these type of issues, it is common that he/she works to find the best compromise between the introduced issue, i.e. overvoltages and overcurrent, EMI and dissipated power.

1.4.2 RC snubber

An RC snubber, consisting of a series of a resistor and a capacitor, is the most common and cheaper snubber. Referring to the analysis presented in section 1.3, an RC snubber placed in parallel to the high side diode can damp the oscillations that take place after the turn-on of the low side switch, while an RC snubber placed in parallel with the low side switch can attenuate the oscillations related to the transistor turn-off. The components of an RC snubber can be sized following these

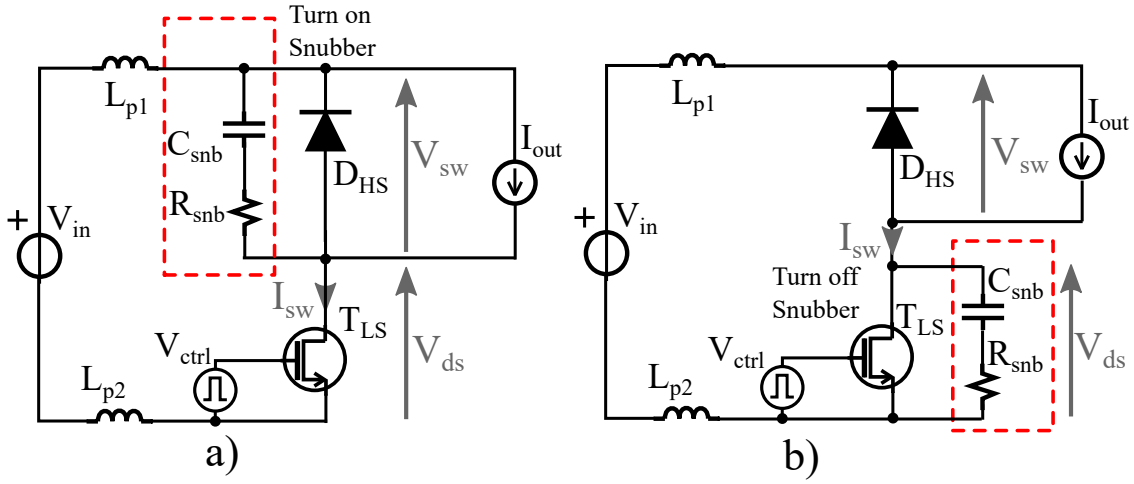

Figure 1.13: RC snubber circuits (a) for damping turn-on oscillations, and (b) for damping turn-off oscillations

steps [13]:

- Measure the resonant frequency (f_r) that should be damped.
- Place in parallel to the considered switch a test capacitance C_t and measure the new resonant frequency (f_{r_t}).

- Calculate the value of the parasitic capacitance acting on the considered node as:

$$C_{\mathrm{p}} = \frac{C_{\mathrm{t}}}{\left(\frac{f_{\mathrm{r}}}{f_{\mathrm{r_t}}}\right)^2 - 1} \tag{1.6}$$

- Calculate the value of the equivalent parasitic inductance ($\mathrm{L_p}$) that makes the resonant circuit as:

$$L_{\mathrm{p}} = \frac{1}{(2\pi f_{\mathrm{r}})^2 \cdot C_{\mathrm{p}}} \tag{1.7}$$

- Finally, the values of $\mathrm{C_{snb}}$ and $\mathrm{R_{snb}}$ can be calculate exploiting (1.8) as indicated in [14].

$$C_{\mathrm{snb}} = 4 \cdot C_{\mathrm{p}} \qquad R_{\mathrm{snb}} = 0.65 \cdot \sqrt{\frac{L_p}{C_p}}. \tag{1.8}$$

An RC snubber has not only positive effects, because the increase of the equivalent capacitance leads to have a higher peak of the current. In steady state, the capacitance of the snubber is charged to $\mathrm{V_{in}}$ or discharged to the ground voltage. The current in capacitance $\mathrm{C_{snb}}$ is a short and high amplitude pulse, which can stress or damage the snubber capacitor. The peak amplitude of such current depend on the value of $\mathrm{R_{snb}}$. More precisely, larger is the value of $\mathrm{R_{snb}}$, lower is the peak of this current. On the other side, by increasing too much the value of the resistance $\mathrm{R_{snb}}$ the effect of the $\mathrm{C_{snb}}$ is reduced and the oscillations superimposed to the switching waveforms will not be damped. Moreover, it is worth noticing that the snubber introduce switching losses according the equation 1.9, discussed in [13].

$$E_{snb} = C_{snb} \cdot V_{in}^2 \tag{1.9}$$

1.4.3 Dissipative RLC diode snubber

The RC snubber is very effective in reducing peak voltages and damping the oscillations at the cost of increasing the power losses. Sometimes this in not enough, because it could be necessary to reduce the switching losses or change the load line in order to remain in the boundaries of the device SOA [13]. In these situations RLC - diode snubbers are very helpful. An RC diode snubber, as the one shown in Fig.1.14(a), can be used to reduce the oscillation at the transistor turn-off. This snubber does not influence the peak power at the turn-on, but affect the peak current. The peak can be reduced increasing $\mathrm{R_{snb}}$, but this resistance should be small to discharge rapidly $\mathrm{C_{snb}}$.

Compared to the no-snubber case, these snubbers improves the load line trajectory, but this improvement increases stress during turn-on, as in an RC snubber. At the turn on, the RLC-diode snubber can be configured as shown Fig. 1.14(b). This snubber reduce the slopes of the current, reducing the peak of the $\mathrm{V_{ds}}$ voltage.

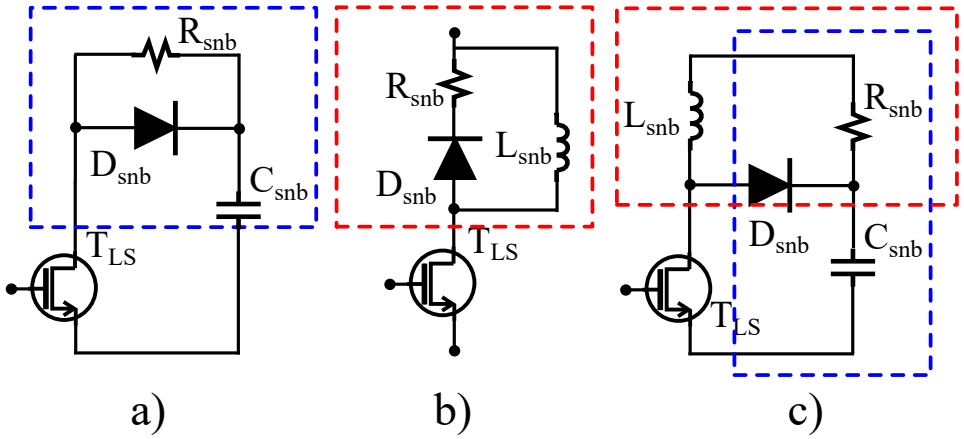

Figure 1.14: RLC diode snubber circuits a) for damping turn-off oscillations, b) for damping turn-on oscillations and c) combinations of the two circuits.

This two snubbers can be put together, making the circuit in Fig. 1.14(c). Besides, if the inductance is equal to zero such snubber is equivalent to an RCD one.

Chapter 2

Driving a Power Transistor

In the previous chapter the analysis of the switching behavior of a buck converter is proposed considering the parasitic elements that could affect the power loop, causing overvoltages, and/or overcurrents and leading these waveforms to oscillate increasing the level of the EMI and the probability that faults occur during the operation of the power module. The most common technique to attenuate such issues are introduced, with their advantages and disadvantages.

The proposed analysis was carried out considering an ideal driver which turns-on and off the power transistor, with the aim to analyze the effect of the driving on the switching waveforms separately. Indeed the power loop and the driving interact, changing the behavior of the switching waveforms. Moreover, the gate driver of a power transistor provides the designer a further degree of freedom for controlling the behavior of the switching waveforms, especially if an Active Gate Driver (AGD) is taken into account.

This chapter provides a brief analysis of the switching waveforms of a power converter, considering the transistor driven with a real gate driver, its effects on the switching waveforms, by including the most common parasitic components in the circuit. It is introduced how a gate driver can control the switching waveforms by referring to the most common topologies of AGD. This analysis lays the groundwork for explaining the technique for tuning the parameters of a generic AGD based on the mathematical model proposed in this thesis.

2.1 Switching Transients of a Power Transistor

As stated before, the switching behavior of a power transistor installed in a power converter does not depend only on the load and on the parasitic components included in the power loop, but also on gate driver strength and on the parasitic elements affecting the driving loop. In this section the waveforms resulting by the analysis of the circuits in Fig. 2.1 are proposed, providing an analytical and

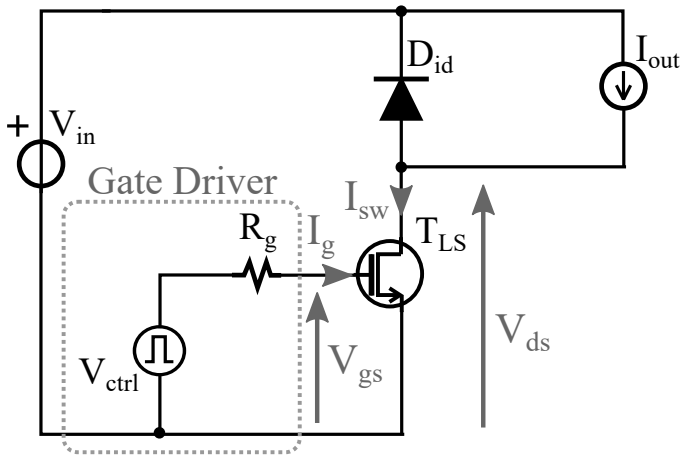

Figure 2.1: Ideal buck converter in which the power transistor is driven with the Thevenin equivalent model of a real gate driver.

qualitative analysis of the switching waveforms. Such an analysis is provided both for the turn on ad the turn off, modeling the gate driver with a Thevenin equivalent [11]. The circuit in Fig. 2.1 shows an ideal buck converter in which the power transistor is driven with the model of a real gate driver, with the aim to explain how the switching waveforms of such a transistor depend on gate resistance R_g. In this preliminary analysis the parasitic elements of the converter, introduced in Chapter 1, are not considered. The switching waveforms of the transistor T_{LS} are shown in Fig. 2.2(a) for the turn on and in Fig. 2.2(b) for the turn-off.

2.1.1 Turn-on Transient

Before being turned-on, in $t = t_0$, the power transistor is in the off state, because the control voltage V_{ctrl}, as well as, the V_{gs} voltage, are equal to zero. When V_{ctrl} goes up, the voltage V_{gs} starts to increase, charging the capacitance C_{gs}. Until this voltage is under the threshold of the transistor V_{th}, the device is still off and no current can flow through the power device. Thus, the V_{ds} remains equal to V_{in}. From t_0 to t_1 the value of the capacitance C_{gd} does not change because the voltage V_{ds} is constant, so the v_{GS} voltage an be expressed as:

$$V_{gs} = V_{ctrl}\left(1 - exp\left(\frac{-t}{R_g(C_{gs} + C_{gd})}\right)\right). \tag{2.1}$$

Once the gate voltage exceeds the V_{th}, in $t = t_1$, the current I_{sw} starts to increase according the following equation:

$$I_{sw} = \beta(V_{gs} - V_{th})^2(1 + \lambda V_{ds}), \tag{2.2}$$

where β and λ are two values depending on the technological parameters of the power switch. From t_1 to t_2 the current I_{sw} is rising, while the voltage V_{ds} is

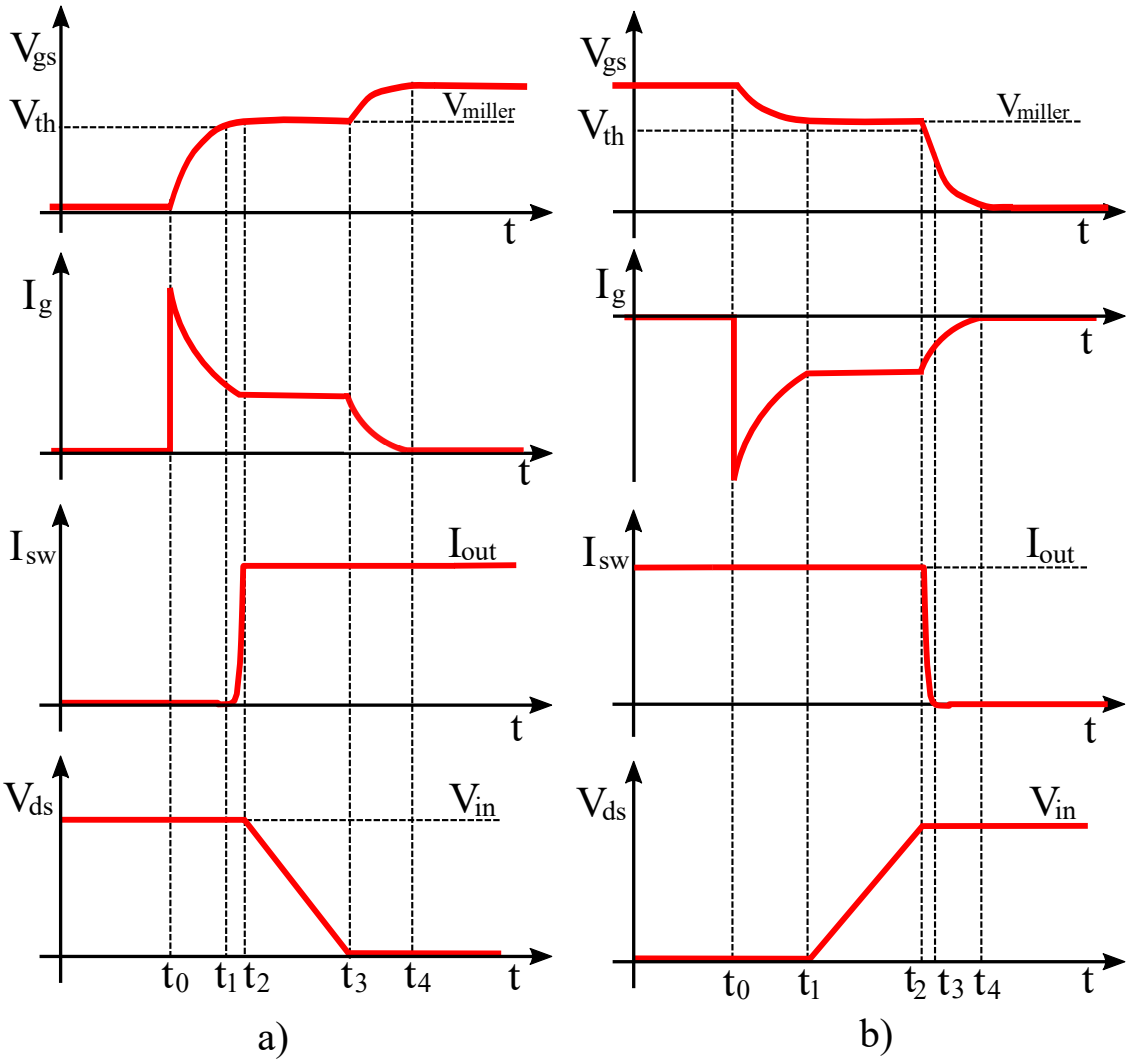

Figure 2.2: Switching waveform of a power transistor placed in an ideal buck converter. In a) the turn-on analysis while in b) the turn-off one.

still equal to V_{in} because the freewheeling diode is still conductive. Also in this case, since the drain voltage is constant, the C_{gd} does not change. The drain current increases until it becomes equal to the I_{out} in $t = t_2$, when the current flows completely in the power switch and the diode is able to sustain voltage. At this point, the voltage V_{ds} starts to decrease and the V_{gs} becomes almost constant and equal to the Miller voltage V_{Miller}, since the I_{sw} is constant. The V_{gs} is equal to V_{Miller} until the power transistor is in linear region, i.e., until the V_{ds} is higher than the overdrive voltage V_{od} that is:

$$V_{od} = V_{gs} - V_{th}. \tag{2.3}$$

As stated before, from t_2 to t_3 the V_{gs} voltage is constant, so the gate current I_g can be calculated as reported in 2.4, resulting in a constant value.

$$I_g = \frac{V_{ctrl} - V_{Miller}}{R_g} \tag{2.4}$$

Most of the I_g current flows through the C_{gd} capacitance, whose voltage drop changes linearly according to:

$$\frac{dV_{gd}}{dt} = -\frac{I_g}{C_{gd}}. \tag{2.5}$$

Therefore, also the V_{ds} voltage changes in the same way, and it can be approximated as:

$$V_{ds} = V_{in} - \frac{(V_{ctrl} - V_{miller})t}{R_g C_{gd}}. \tag{2.6}$$

When the V_{ds} becomes equal to V_{od}, in $t = t_3$, the V_{gs} starts to increase again exponentially until it reaches the steady state voltage V_{pwl}, in $t = t_4$. In this time interval, the V_{ds} reaches the $V_{ds,on}$ value, which depends on the value of the on resistance $R_{ds,on}$ when the transistor is in the ohmic region [11].

2.1.2 Turn-off Transient

When the transistor T_{LS} is in on state all the load current I_{out} flows in the power switch and the diode D_{id} is off. When V_{ctrl} goes down for turning off the device, the gate of the transistor is connected to its source through the R_g resistance and the C_{gs} starts to discharge. Nevertheless, the V_{ds} voltage and the current I_{sw} are still equal to $V_{ds,on}$ and to I_{out}, respectively until the V_{gs} reaches the Miller plateau. During this interval of time, from t_0 to t_1, the V_{gs} voltage decreases according to:

$$V_{gs} = V_{ctrl} \cdot exp\left(\frac{-t}{R_g(C_{gs} + C_{gd})}\right). \tag{2.7}$$

In $t = t_1$, even if the V_{ds} starts to increase, the current I_{sw} continues to be constant until the voltage V_{ds} exceeds the V_{in} by the threshold of the diode, when it becomes conductive. Since the current I_{sw} is constant, also the V_{gs} is constant between t_1 and t_2 and the the gate current can be approximated as:

$$i_g = \frac{V_{Miller}}{R_g}. \tag{2.8}$$

Similarly to the turn-on, also for the turn-off, all the gate current is used to discharge the C_{gd}, because the V_{gs} is constant, so the voltage variation across the C_{gd} capacitance is reflected on the C_{ds} according:

$$\frac{dV_{ds}}{dt} = \frac{dV_{gd}}{dt} = \frac{I_g}{C_{gd}}, \tag{2.9}$$

and the V_{ds} can be calculated as:

$$V_{ds} = R_{ds,on} \cdot I_{out} + \frac{V_{Miller}}{R_g C_{gd}} \cdot t. \tag{2.10}$$

At the end of the plateau, when the diode is on, the current starts to decrease according the eq. 2.2 and the V_{ds} voltage becomes equal to V_{in}. From t_2 to t_3 the current I_{sw} decreases, until the V_{gs} reaches the voltage V_{th} and the current I_{sw} becomes equal to zero, in $t = t_3$. Finally, from t_3 to t_4, the V_{gs} voltage decreases exponentially, until it reaches the zero level. The time constant of this discharging phase depends on the capacitance C_{gs} and the resistance R_g, as in the first phase of the turn-on.

2.1.3 Gate Resistance

The analysis presented so far shows the ideal switching waveforms of a buck converter. As deeply discussed in Chapter 1, the parasitic elements included in the power loop significantly affect the switching behavior of converters, making such equations not usable, especially for high speed devices, where the effect of parasitic components is more evident [10]. For instance, as shown in Fig. 1.10, the power loop parasitic inductance affects significantly the behavior of the I_{sw} current, by changing completely its trajectory if compared with the ideal one. Nevertheless, the Eqs. 2.6 and 2.10 gives the user the capability the control the switching waveform when the device is in the linear region by acting on resistance R_g, as suggested in [7]. More precisely, a higher value of R_g allows to decrease the dv/dt both for the turn-on and the turn off in order to reduce the overvoltages and/or the overcurrents that affect the power switches. A comparison between the switching waveforms of the circuit in Fig. 2.1 that includes its parasitic components, obtained by increasing the R_g is shown in Fig. 2.3. Such comparison shows that the increase of the gate resistance,reduce the slope of V_{ds}, and so reducing the peaks of voltages and current, but also the converter efficiency. For such a reason, a combination of a properly chosen gate resistance with a properly sized snubber are used in power converters to find the best trade off between losses, reliability and EM emissions.

2.1.4 Effect of parasitic distribution on the Gate Driving

In Chapter 1, the effect of the parasitic inductances on the switching waveforms was analyzed without considering the common source inductance [10], i.e., the parasitic inductance shared between the power loop and the driving loop, as shown in Fig. 2.4(a). As long as the distribution of the parasitic inductances does not affect the driving loop, as presented in Chapter 1, these components affect the switching waveform by altering the distribution between voltage V_{sw} and the voltage V_{ds}, without any effect on the transistor driving. As discussed in [15], the inductance

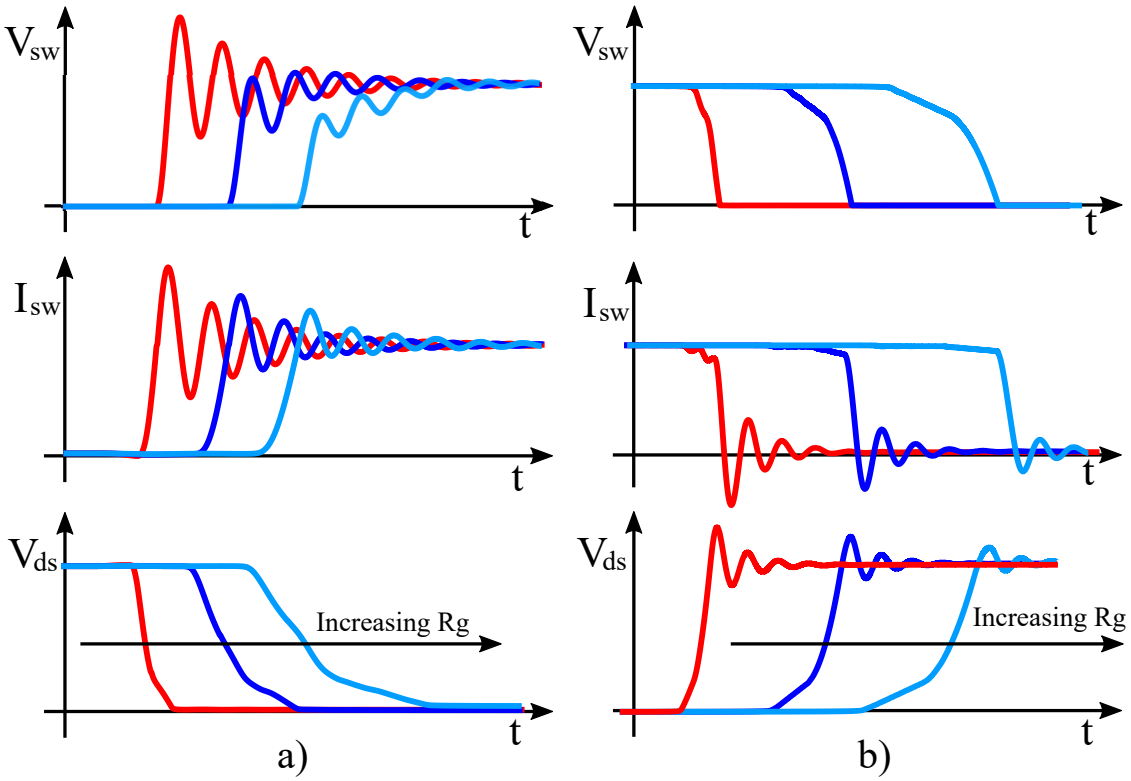

Figure 2.3: Buck converter including its parasitic elements.

L_s affects also the transistor driving. When the power switch is turned on, the increase of the current I_{sw} will induce a voltage drop on the L_s that reduces the level of the gate current I_g and so increases the time needed to completely charge the capacitance C_{gs}. During the variations of the current I_{sw} the gate current can be approximated as:

$$I_g = \frac{V_{ctrl} - V_{gs} - L_s \frac{dI_{sw}}{dt}}{R_g}. \tag{2.11}$$

The L_s increases the overall turn-on time, as well as the turn-on switching losses but, in extreme cases, can induce the self turn-off phenomenon [10], causing the converter damaging.

Similarly, at the turn-off, the current I_{sw} decreases with an high slew rate. This induces on the L_s a negative voltage drop, reducing the turn-off current and consequently increasing the switching losses. In this case, a high value of L_s inductance with a high di/dt can lead to the self turn-on phenomenon [15].

The gate inductance L_g is another parasitic element that affects the driving loop, as shown in Fig. 2.4(b). In the previous analysis the interaction of the power loop with the driving loop is analyzed by introducing the inductance L_s in the circuit. The inductance L_g has no interaction with the power loop, but with the L_s, the C_{gs}

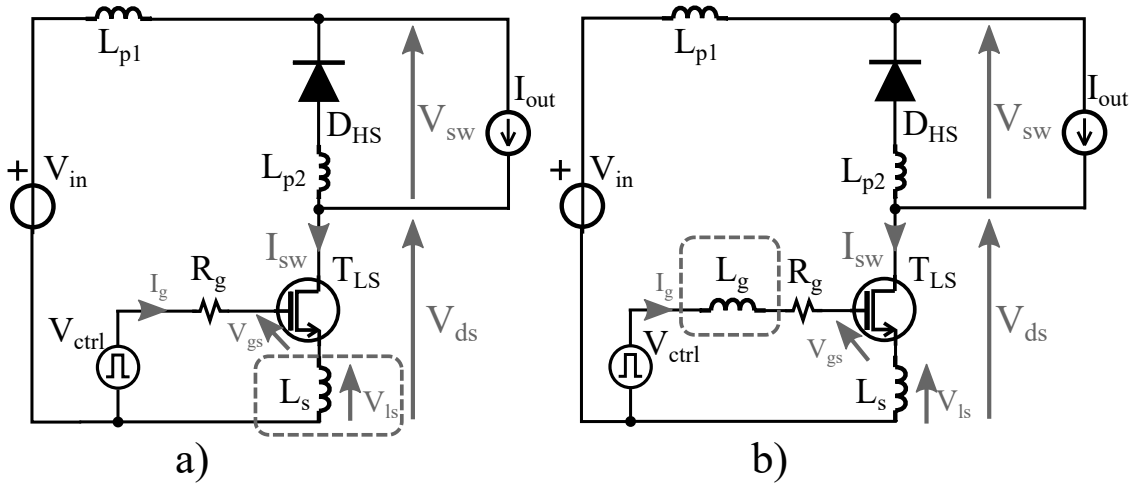

Figure 2.4: Buck converter with parasitic components. In a) the common source inductance L_s is shared between power loop and the input one. In b) the gate inductance is placed in the driving loop.

and R_g makes an RLC circuit that could lead the V_{gs} to oscillate. This phenomenon can occur both at the turn-on and at the turn-off. Such oscillations can lead the V_{gs} to exceed the maximum allowed by the device, causing it permanent damaging, but also to a phenomenon like the self turn-on and/or the self turn off. For such a reason, as discussed in [7, 16], a minimum value of R_g, calculated as reported in 2.12, is necessary to avoid such oscillations. It is worth noticing that the suppression of such oscillations does not ensure the damping of the power ringing related to the power loop, but only the good functionality of the driving loop.

$$R_g > 2\sqrt{\frac{L_s + L_g}{C_{gs} + C_{gd}}}. \tag{2.12}$$

2.2 Gate Driver

In a power converter, the gate drivers are the connection between the control and the power systems. Indeed, they represent the link between the control signals, generally generated with a microcontroller, and the power transistors. A good gate driver should control power devices taking into account their static and dynamic characteristics and considering the possibility that faults could occur, damaging the converter. More precisely, referring to static conditions, a good driver should keep the device on and off with very low power losses. In literature, several types of gate drivers can be found. One of most simple techniques to drive a power transistor is the asymmetric gate driver [17] whose simplified circuit is shown in Fig. 2.5(a). The diode allows the user to control with different resistances the turn-on and turn-off

rates. More precisely, when the V_{ctrl} is high, the diode is on and the current charges the gate source capacitance through the R_1 resistance, while when V_{ctrl} is low, the diode is off, and the C_{gs} is discharged through the resistance R_2. An alternative circuit to obtain the same results is shown in Fig. 2.5(b). The advantages of this circuit compared with the one presented before, is related to the dissipated power. In fact, the diode in the first circuit dissipates power for all the turn-on phase, while the one of the circuit in Fig. 2.5(b) is on only during the off transient of the power switches.

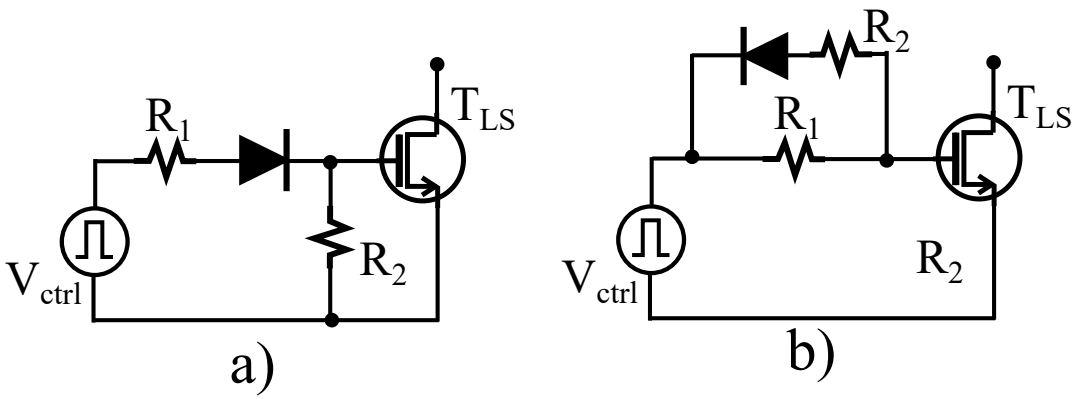

Figure 2.5: Schematic of asymmetrical gate drivers. a) with diode actve at turn-on and b) with diode active at the turn off.

The schematic of a more functional gate driver is shown in Fig. 2.6. In a hard switching topology, as introduced in Chapter 1, the V_{ds} overvoltage encountered at turn-off is a common issue that could lead to destroy the device, due to the avalanche effect [17]. Such overshoot, induced by the slope of the drain current, can be reduced by increasing the gate resistance, but the power losses will be higher. The gate driver shown in Fig. 2.6 can control the slope of the drain current and the slope of the V_{ds} voltage at the turn-off, without significantly affecting the power losses [17]. At the transistor turn-off, both M1 and M2 are turned on, to discharge the input capacitance of the transistor, but when the V_{ds} voltage reaches the breakdown voltage of the zener diode, current starts to flow through the capacitor C_1 in order to activate the triggering circuit that turns-off M1 for a short interval of time. This phenomenon increases the equivalent turn-off resistance and consequently reduces the falling current slope. Then, M1 is turned again on and the turn off continues rapidly. This driver, proposed in [18], can be considered a predecessor of several and more complicated AGD topologies.

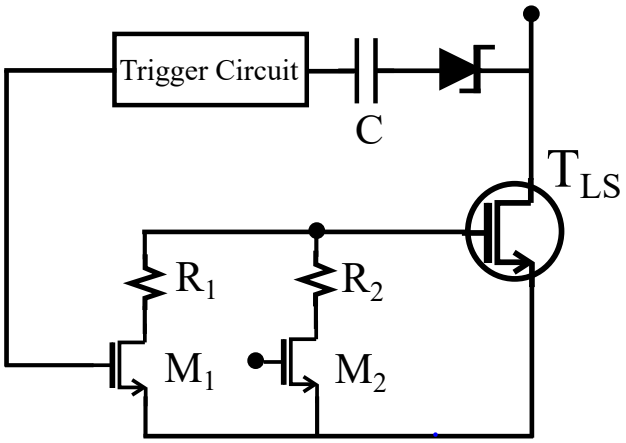

Figure 2.6: Schematic of a simple AGD.

2.2.1 Active Gate Driver

The main function of an Active Gate Driver (AGD) is to control the switching waveforms of a power device to keep it inside the limits of its SOA [19]. In order to accomplish their task, AGDs can adjust their driving strength, following a well defined shape (open loop) or adjusting their output as a function of a continuously monitored voltage and/or current (closed loop). In literature, it is possible to find several topologies of AGD that can be classified according their output type. More precisely, the AGDs can control the switching waveforms by changing dynamically their output resistance or regulating their output voltage or current. Whatever the different output topology, AGDs share the same purpose, i.e, to control the flow of the gate charge to obtain the faster, less dissipative and safest transients on power switches. Simplified schematics of all these topologies are shown in Fig. 2.7. More precisely, Fig. 2.7(a) shows a modulation resistance gate driver that, closing and/or opening dedicated switches, can change the equivalent resistance that links the gate with the on and the off gate driver voltages. Instead, the circuit shown in Fig. 2.7(b) can adjust the injected and sunk current by means of paralleled current sources and sinks. Finally, the circuit in Fig. 2.7(c) can regulate the V_{gs} voltage exploiting an operational amplifier and a variable voltage source. Generally, in all these topologies, the control signal comes from a Control Unit (CU).

Resistance Gate Modulation Driver

The modulation of the gate resistance is the most common approach for controlling the switching waveforms in a power converter [20, 21]. By adjusting dynamically the value of the gate resistance it is possible to change the dv/dt and the di/dt during the transient. Generally, according to the analysis proposed in section 2.1.3, a high value of gate resistance is used during the Miller plateau to reduce

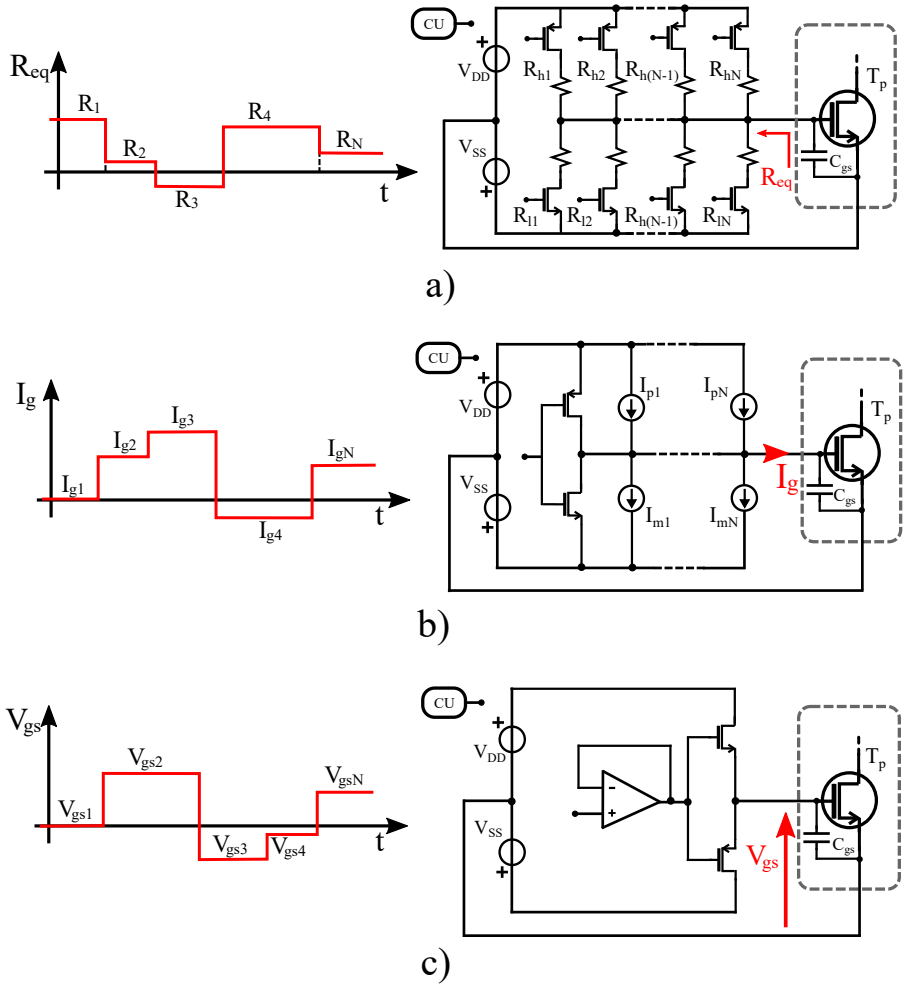

Figure 2.7: Simple schematics of Active Gate Drivers: a) resistance, b) current and c) voltage modulation topologies.

the slew rate while a low value resistance is used when the transistor gets out of the Miller region to avoid self turn-on and self turn-off [22]. By referring to the circuit in Fig. 2.7, the CU can choose what and how many resistances have to be connected to the gate of the power switch, giving the user the capability to turn-on and turn-off the device using several equivalent gate resistances, allowing to shape the switching waveforms. The equivalent resistance R_{eq} can be both positive and negative. This because such a resistance represent the equivalent one between the gate and the source of the driven power transistor. When this mosfet is in the off state, through the turn on of one or more low side transistor of the gate driver shown in Fig. 2.7(a), its V_{gs} is equal to -V_{SS}. When the power transistor must be turned on. the high side transistor of the driver are closed, while the low side ones are opened. This allow the C_{gs} to charging until to reach the voltage V_{CC},

with a positive current and so a positive R_{eq}. Similarly, at the turn off, the C_{gs} of the power transistor is discharged by means of the low side transistors of the gate driver, resultig in a negative current and so, in a negative resistance R_{eq}. The resistance modulation AGD exploiting these concepts, by combining extremely fast intervals of times, in which the low side and high side transistors of the AGD are on and/or off to obtain positive and or negative R_{eq} both during the turn-on and turnoff phases.

Gate Current Modulation Driver

This topology exploits paralleled current sources, as shown in Fig. 2.7(b) to change the level of the gate current that charge or discharge the C_{gs} capacitance. As proposed in [23, 24], a current mirror is a good solution to realize this type of AGD, while in [25, 26] alternative solutions that exploit the energy stored in inductors to charge the gate capacitance are proposed. Current source gate drivers are more complicated than the voltage source ones, but are less dissipative because they do not dissipate any energy in the gate resistance [27]. In these AGD topologies, positive and negative current values can be obtained with current mirror, capable to source and to sink current in/from the driven transistor T_p. An other technique, to obtain different constant current levels, consists of exploiting the Miller plateau of the driven transistor T_p, during the which, the voltage V_{gs} is about constant. In this way, driving the transistor with different voltage sources V_{ctrl} with a series resistance R_{ser}, it is possible to obtain different constant current level depending on V_{ctrl}, as highlighted in:

$$I_{g,i} = \frac{V_{ctrl,i} - V_{Miller}}{R_{ser}}. \tag{2.13}$$

The last proposed solution is an intermediate between a gate current modulation and a voltage modulation driver because exploits a voltage sources to obtain constant gate current levels.

Gate Voltage Modulation Driver

Gate voltage modulation drivers can adjust the V_{gs} voltage to control the trajectory of the switching waveforms at the turn-on and at the turn-off of power switches. This topology is more feasible than the others, because it is similar to the conventional driving method. The advantage of this methodology is related to the simplicity of its implementation [28]. The block diagram shown in Fig. 2.7(c) can model several topologies proposed in [19, 28, 29]. The desired voltage profile is generated with an Arbitrary Waveform Generator (AWG) and then it is amplified to control the power transistor. During the Miller plateau, the driver voltage is regulated to a certain value to control the slopes of the switching waveforms, then it is regulated at its normal on-off voltage.

Control Strategy for AGDs

As already mentioned an active gate driver can work in open loop or in closed loop. This last operation mode contains other two subcategories, i,e. the adaptive feedback control and the indirect model based control. In literature, it is possible to find several types of control strategies, with different optimization targets, i.e, the dissipated power, the EMI level or the junction temperature. Generally the target is chosen according the need of the specific application [30].

Independently from the topology, the open loop AGDs are always the simplest and the cheapest to design. In these AGDs, the modulation strength is established by means of trial and error procedures in an experimental setup or in a simulation environment and the control trajectory is saved in the microcontroller memory as proposed in [31]. The disadvantages related to these topologies depend essentially on the operating conditions of the device. In fact, as highlighted in [32], and also analyzed in this thesis, the operating conditions of the power converter affect the optimal driving pattern that should be changed to obtain the desired waveform trajectory. In literature, this issue is bypassed in [32], in which the microcontroller contains more than one modulation patterns that can be selected according to the operation conditions. This expedient is often cost-less because also without AGD the operating conditions in a converter are monitored for the control and the reliability of the circuit. Among closed loop solutions, the most effective are the real time ones that, by sensing the dv/dt and/or the di/dt, can change in real time the strength of the AGD [33]. This type of solutions are very complex to be implemented, especially in circuits in which the transitions are very fast. In fact, the sense circuit and the gate driver response should be much faster than the slope of the switching voltage and current in order to control them without incurring in frequency response issues. Simpler, but less effective, closed loop techniques are represented by the adaptive feedback solutions [34], in which some quantities are sensed and used as references to select a pre-established modulation pattern that will be used to drive the transistor in the succeeding cycle. The reference quantity could be a peak voltage and/or a peak current as in [35], but also a time instant as proposed in [36]. The last category of AGDs includes models and, in combination with sensed quantities, estimates the switching losses and changes the modulation patterns finding the best trade off between EMI, power dissipation, and junction temperature, as discussed in [37]. The performance of this last category strongly depends on the accuracy of the used models, that should be able to adjust the parameters also as a function of the temperature and humidity levels [34].

Chapter 3

The Optimal Switching Waveforms

The previous chapter ended with the analysis of the most common AGDs topologies and methodologies to drive the power transistors. Notwithstanding the effectiveness of AGDs, it is important to highlight that a model does not exist to predict what are the best switching waveforms and to derive the optimal gate current profile to obtain them. Indeed, in most of the analyzed gate drivers, the gate profile is obtained with experimental trial and error approaches, with the aim to find the best trade-off between switching speed, switching losses, and/or EMI emissions.

In [38] qualitative approaches are proposed in terms of driving profiles and techniques, without defining target switching waveforms. The aim of this chapter is to fill such a gap, proposing a model that allows the designer to obtain the optimal switching waveforms, i.e, the non-oscillating and less dissipative ones, by means of simulations and, in initially, without exploiting the AGD. In this way, the input loop and the power loop are analyzed separately and the obtained optimal switching waveforms can been used as a reference to build the optimal gate profile. Such waveforms, along with the parameters resulting from the proposed algorithm, are a step forward with respect to the trial-and-error or local optimization methods that can be found in literature. Indeed, the proposed approach provides the target output waveforms [39, 40], thus knowing in advance the best trade-off between power dissipation and switching speed. In this way, the designer can separate the analysis of the input and the output loop, reducing the complexity of the design flow.

3.1 Ringing Phenomenon in a Buck Converter

In this section the switching behavior of a power converter is analyzed to build-up a simplified circuit that allows one to derive a mathematical model describing

the turn-on and turn-off behavior of these circuits, with the aim to understand what parasitic components and what transients are responsible for the oscillations that take place after the turn on and the turn off of the power transistor. Figure 3.1 shows the circuit considered to carry out such an analysis.

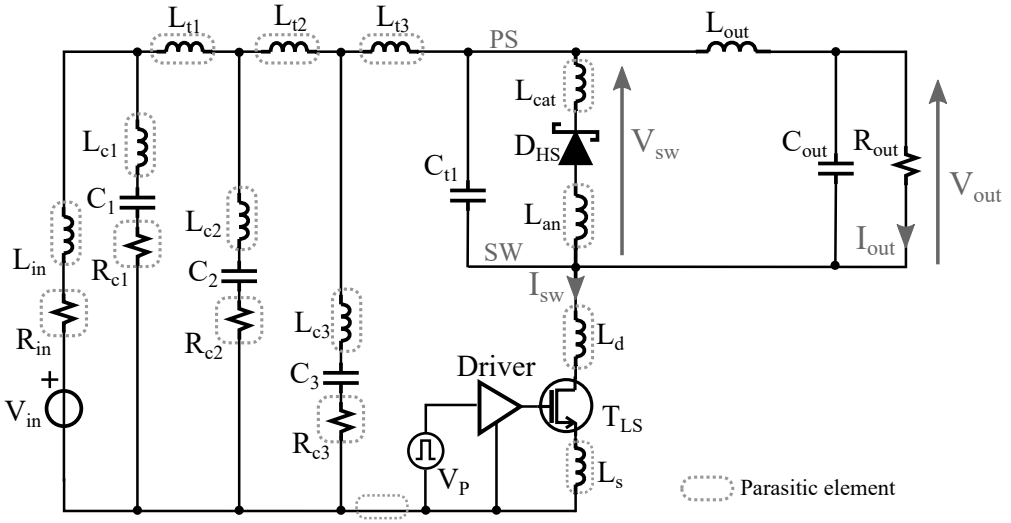

Figure 3.1: Buck converter including its parasitic elements.

The picture shows a low side buck converter that includes several parasitic components with the aim of modeling its high frequency behavior. The voltage V_{in} with the resistance R_{IN} and the inductance L_{IN} models the input power source and its output impedance, while the three capacitances C_1, C_2 and C_3 with the corresponding series resistances $R_{c_{1\text{-}3}}$, and inductances $L_{c_{1\text{-}3}}$, model the input capacitors of the DC link. These components provide the switching current I_{sw} that allow the buck converter to work properly, and reduce the unwanted voltage drop on the DC link related to the output impedance of V_{in}. The low side power transistor T_{LS} represents the controlled switch while the diode D_{HS} is the high side freewheeling switch of the power converter. This two components regulate the energy flow between the input and the output of the converter with the aim to adjust the voltage V_{out} on the load resistance R_{out}. The power inductance L_{out} ensures the continuity of the current provided to the load and, with the capacitance C_{out}, makes a second order low pass filter which attenuates the ripple affecting the output voltage V_{out}. The inductances $L_{t_{1\text{-}3}}$ and the capacitance C_{t_1} are parasitic elements related to the Printed Circuit Board (PCB). All such parasitic elements, along with the parasitic inductances (L_d, L_s, L_{cat}, L_{an}), and the parasitic capacitances (C_{gs}, C_{gd}, C_{ds}) of the power switches, contributes to create the resonant circuit responsible for the oscillation affecting the switching waveforms, after the turn-on and the turn-off of the power switch T_{LS}, as introduced in Chapter 1.

3.1.1 The Equivalent High Frequency Model

As already mentioned in Chapter 1, the oscillation superimposed to the switching waveforms are characterized by two different frequencies, because the parasitic elements, and therefore the resonant circuit, involved in such phenomena are not the same. More precisely, after the turn-on and after the turn-off of the power transistor T_{LS}, the parasitic elements responsible for the oscillations are different, as well as their triggering event.

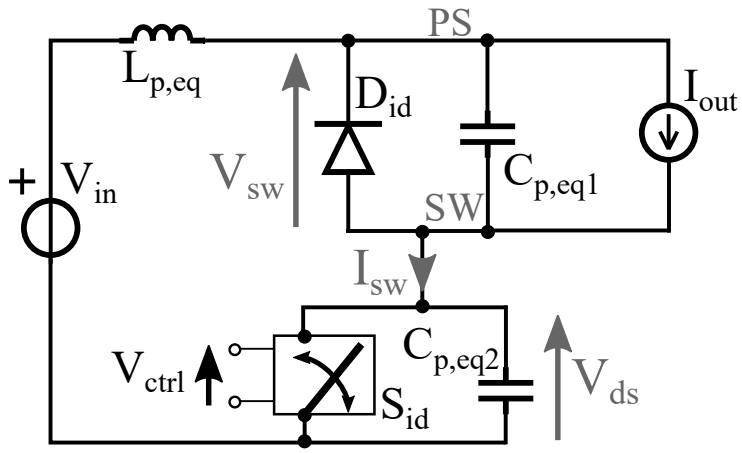

Figure 3.2: Simplified high frequency model of the buck converter.

In this subsection, a simplified circuit modeling the high frequency behavior of the real one is proposed. This circuit, shown in in Fig. 3.2, provides a simple way to establish which transition between voltage and current, causes the oscillations after the turn-on and after the turn-off of the power transistor T_{LS}. Furthermore, this circuit lets one identify which are the parasitic components responsible for the turn-on and turn-off oscillations and so, to develop a model and a method to minimize them. The power transistor T_{LS} and the freewheeling diode D_{HS} are replaced by the ideal switch S_{id} and by the ideal diode D_{id}, while the current sinker I_{out} models the load of the converter. The DC link is modeled with the ideal voltage source V_{in}, while all the parasitic elements are lumped in only three reactive components, two capacitances (C_{p,eq_1}, C_{p,eq_2}) and an inductance $L_{p,eq}$). The value of these three parasitic components can be calculated by means of simulations, exploiting the method proposed in [13] and discussed in Chapter 1, generally used for sizing the components of an RC snubber. More precisely, firstly the complete circuit shown in Fig. 3.1, is simulated in the time domain to obtain the value of the oscillation frequencies f_{r_1} and f_{r_2}, and then, after connecting a test capacitance C_t between the power node PS and the switching node SW, the simulation is repeated. This second simulation results in switching waveforms characterized by a different oscillation frequency after the turn on $f_{r_{1,t}}$, while the turn-off oscillations are at the same frequency of the ones resulting from the first simulation. This analysis

allow one to calculate the value of capacitance C_{p,eq_1} and of the inductance $L_{p,eq}$ by means of the Eqs. 3.1. Later, also the value of C_{p,eq_2} can be calculated using the Eq. in 3.2.

$$C_{p,eq1} = \frac{C_t}{\left(\frac{f_{r1}}{f_{r1,t}}\right)^2 - 1} \qquad L_{p,eq} = \frac{1}{(2\pi f_{r1})^2 \cdot C_{p,eq1}}. \tag{3.1}$$

$$C_{p,eq2} = \frac{1}{(2\pi f_{r2})^2 \cdot L_{p,eq}}. \tag{3.2}$$

The proposed circuit represents a powerful means to analyze the switching behavior of the converter because it is easy to study, but at the same time provides reasonable results, useful for the analysis of the complete circuit.

Figure 3.3 shows the switching waveforms resulting from the analysis of this circuit both for turn-on 3.3(a) and for the turn-off 3.3(b), highlighting for each transition the conduction state of the two switches.

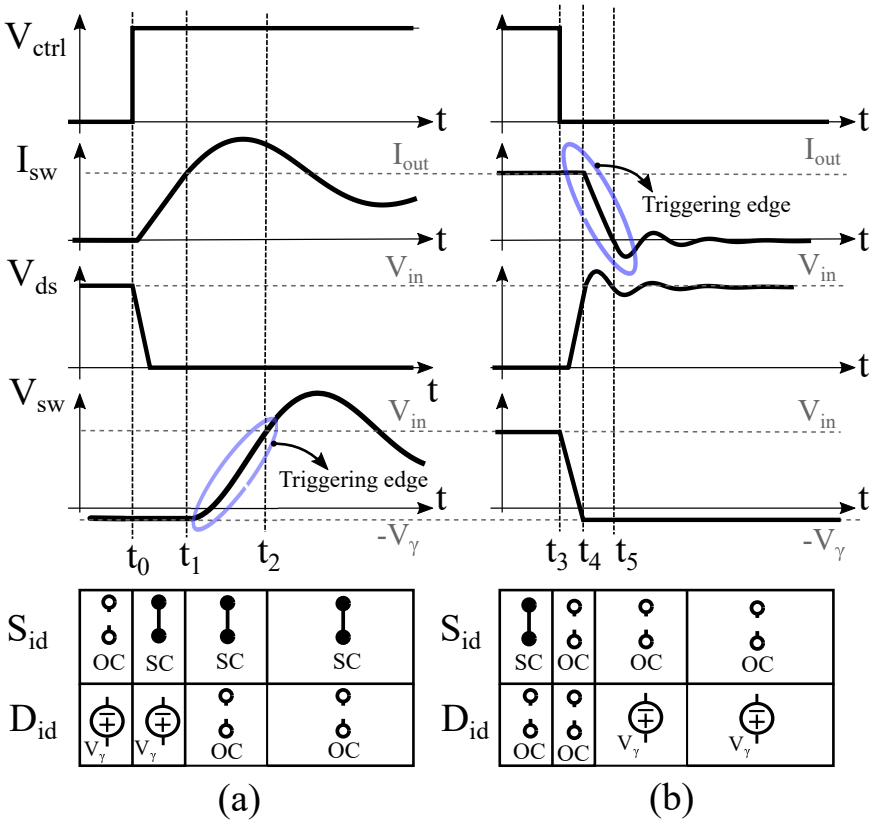

Figure 3.3: Ideal switching wavefoms at the turn-on (a) and at the turn-off (b).

3.1.2 Analysis of the turn-on oscillations

In this subsection a detailed analysis of the switching waveforms behavior after the turn-on of the controlled switch S_{id} is reported, referring to the Fig. 3.3(a). For $t < t_0$ the V_{ctrl} signal is low, so the ideal switch S_{id} is open and the V_{ds} voltage is equal to V_{in} as well as the current I_{sw} is equal to zero. In this time interval, the load current I_{out} flows completely in the ideal diode D_{id}, whose drop voltage is $-V_\gamma$. In $t = t_0$ the control signal V_{ctrl} closes the low side switch S_{id} and the voltage V_{ds} goes instantaneously to zero, discharging the capacitance C_{p,eq_2} on the on-resistance of the ideal switch. This happens because, in this time interval, the voltage drops on the parasitic inductances $L_{p,eq}$. At this point, when the switch S_{id} is closed, the current I_{sw} starts to increase linearly according the following equation:

$$I_{sw}(t) = L_{p,eq}\frac{I_{out}}{V_{in}}(t - t_0). \tag{3.3}$$

During this time interval the diode continues to be closed and load current is shared between the diode and the ideal switch. The equivalent circuit of the I_{sw} current transition at the turn-on is shown in Fig. 3.4(a). When the current I_{sw} becomes equal to I_{out}, at $t = t_1$, the diode D_{id} turns-off and it behaves like an open circuit allowing the charging of the capacitance C_{p,eq_1} and the rising of the voltage V_{sw}, that reaches the value V_{in} at $t = t_2$. The equivalent circuit of the transition of the voltage V_{sw} is shown in Fig. 3.4(b). This analysis allows one

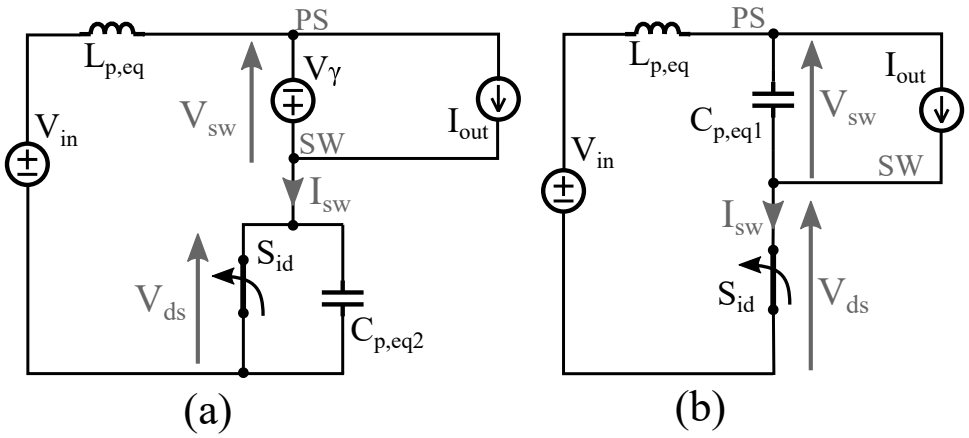

Figure 3.4: Equivalent circuit for the current transition (a) and for the voltage transition (b) after the turn-on of the ideal switch S_{id}.

to identify two interesting time intervals after the turn-on of the ideal switch S_{id}. The first one, from t_0 to t_1, in which the I_{sw} current transition takes place and the second, from t_1 to t_2 in which the V_{sw} voltage transition occurs. During the current transition both the capacitance C_{p,eq_1} and C_{p,eq_2} are kept to a constant voltage by

the corresponding parallel switch. More precisely, the diode D_{id} keeps the voltage across the capacitance C_{p,eq_1} to $-V_\gamma$, while the capacitance C_{p,eq_2} is kept to a low voltage by the switch S_{id}. So, during the transition of I_{sw} no resonant circuit can be excited and no oscillations can take place (Fig. 3.4(a)). Instead, during the V_{sw} transition, the voltage drop on the capacitance C_{p,eq_2} continues to be constant, while the capacitance C_{p,eq_1} can be charged by means of the current I_{sw} coming from the inductance $L_{p,eq}$. So the V_{sw} voltage transition can excite the resonant circuit comprising $L_{p,eq}$ and C_{p,eq_1}, causing oscillations at the frequency f_{r_1} (Fig. 3.4(b)). In addition, the time domain analysis of such equivalent circuit suggests that the higher is the slope of V_{sw}, the greater is the magnitude of its frequency spectrum at f_{r_1}, thus the resulting oscillation will be larger.

3.1.3 Analysis of the turn-off oscillations

The analysis of the turn-off switching waveforms is reported in this subsection referring to Fig. 3.3(b). In the time interval between t_2 and t_3 the switch S_{id} is closed and the current I_{sw} is equal to the load current I_{out}. The diode D_{id} is open and the voltage drop on the capacitance C_{p,eq_1} is equal to the input voltage ($V_{sw} = V_{in}$). At $t = t_3$ the signal V_{ctrl} turns-off the switch S_{id}, so the voltage V_{ds} increases rapidly, while the voltage V_{sw} decreases until the values V_{in} and $-V_\gamma$, respectively are reached at the time instant t_4. In this time interval, the current I_{sw} continues to be equal to I_{out} as well as the current flowing in the $L_{p,eq}$ inductance is almost constant. The equivalent circuit of the voltage transitions at the turn-off is shown in Fig. 3.5(a). At $t = t_4$, the diode D_{id} starts to provide current to

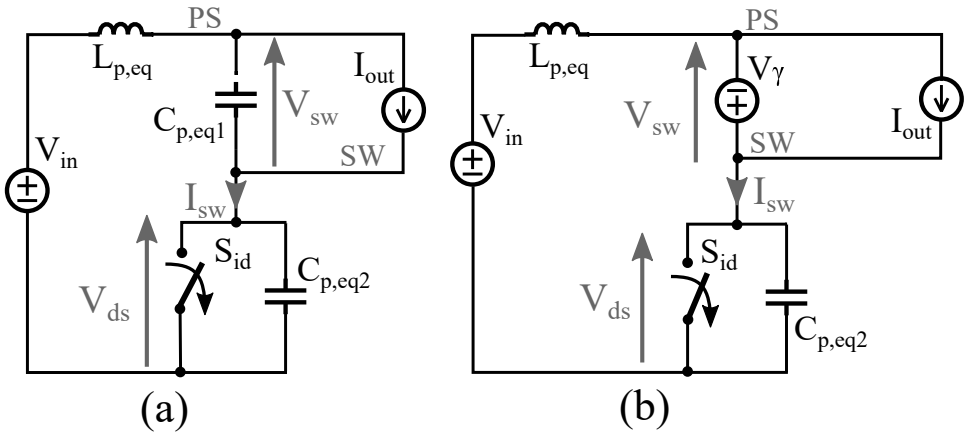

Figure 3.5: Equivalent circuit for the voltage transition (a) and for the current transition (b), after the turn-off of the ideal switch S_{id}.

the load, holding the voltage drop on C_{p,eq_1} at $-V_\gamma$. The current I_{sw} suddenly decreases until it reaches the value of 0 A at $t = t_5$. The equivalent circuit of

this current transition is shown in Fig. 3.5(b). Also during the turn-off, it is possible to identify two different intervals of time, the first one in which the voltage transition occurs, and the second in which the current one takes place. In such circuit, the voltage transitions cannot trigger any oscillations because the current flowing through the inductance $L_{p,eq}$ during this phase is almost constant and it is not subjected to any fast variation. Instead, the transitions of the current I_{sw} can excite the resonant circuit including the capacitance C_{p,eq_2} and the inductance $L_{p,eq}$ triggering the oscillations at the frequency f_{r_2}. In fact, during this transition the load current flows completely in the freewheeling diode and I_{sw} is free to oscillate. Differently from the turn-on, during the turn off voltage transition it may happen that the current I_{sw} slightly decreases because a portion of the current that charge $C_{p,eq2}$ is provided by $C_{p,eq1}$. However this small variation does not affect the validity of this analysis, except if $C_{p,eq1}$ is much larger than $C_{p,eq2}$.

3.2 The Optimal Switching Waveforms

The analysis presented so far explains in detail the causes of the oscillations occurring after the turn-on and and the turn-off of the low side switch S_{id}. More precisely, the former, dealing with the parasitic resonator made of $L_{p,eq}$ and C_{p,eq_1}, are triggered at the turn-on by the transition of the voltage V_{sw}, while those resulting at turn-off, are triggered by the transition of the switching current I_{sw}, and are related to the resonator that includes the $L_{p,eq}$ and the C_{p,eq_2} parasitic components. In order to prevent the triggering of the oscillations, the slope of these signals should be controlled dynamically, thus to avoid the excitation of the resonant frequencies f_{r_1} and f_{r_2}.

The approach presented in this thesis, proposes to include in the power loop two time variant components, the resistance $R_t(t)$, and the conductance $G_t(t)$, aiming to control the slope of V_{sw} and the slop of I_{sw} [39, 40]. More precisely, $R_t(t)$ is placed in series with the ideal switch S_{id} to control the slope of the voltage V_{sw}, while $G_t(t)$ is connected in parallel with S_{id}, to control the slope of the current I_{sw}, as shown in Fig. 3.6. Moreover, the $R_t(t)$ element should be effective only at the turn-on to avoid the worsen of the turn-off performance, whose oscillations are not affected by the transition of V_{sw}. Similarly, $G_t(t)$ is active only at the turn-off, because the transition of I_{sw} does not affect the oscillation related to the turn on, and this element would increase the turn-on losses unnecessarily. The $R_t(t)$ component is defined as:

$$R_t(t) = k_1 \frac{dV_{sw}(t)}{dt}, \tag{3.4}$$

while the $G_t(t)$ element as:

$$G_t(t) = k_2 \frac{dI_{sw}(t)}{dt}. \tag{3.5}$$

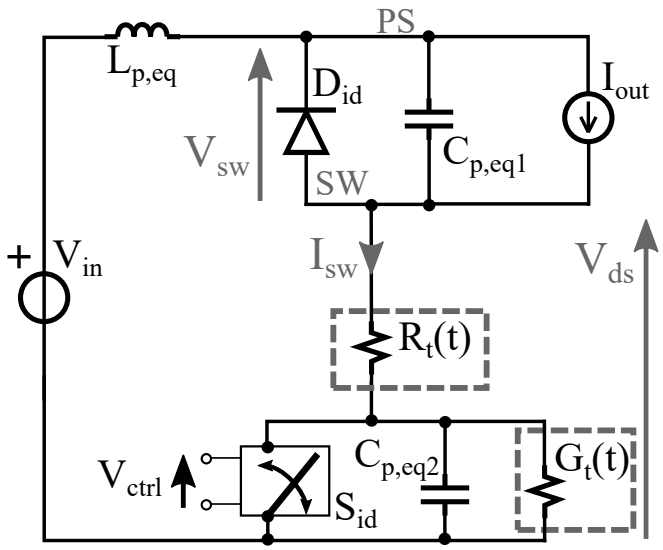

Figure 3.6: Equivalent circuit of the buck converter including the $R_t(t)$ and $G_t(t)$ elements.

The coefficients k_1 and k_2 have to be evaluated imposing the critically damped conditions in the equations resulting from the analysis of two equivalent circuits shown in Fig. 3.7, which refers to the V_{sw} voltage transition of the turn-on (3.7(a)) and to the I_{sw} current transition of the turn-off (3.7(b)), respectively.

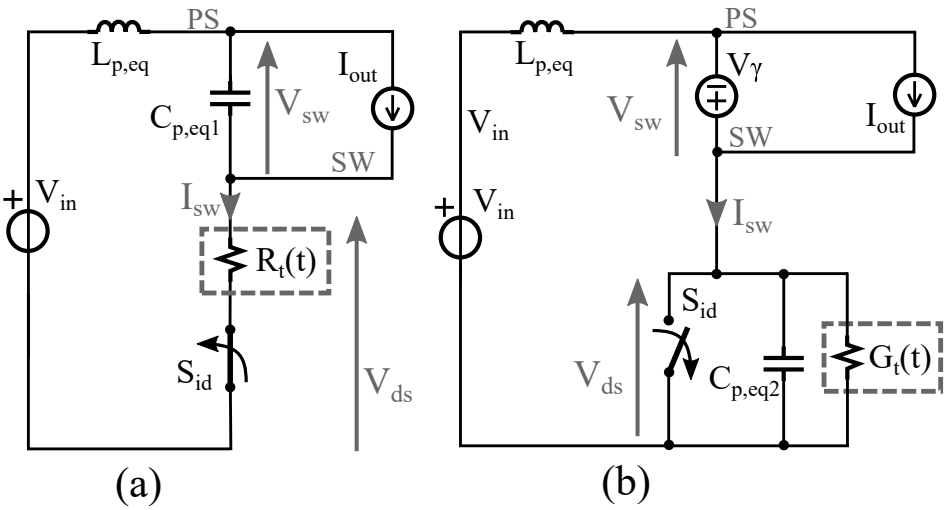

Figure 3.7: Equivalent circuit for the turn-on voltage transition (a) and for the turn-off current transition (b), including the $R_t(t)$ and $G_t(t)$ components.

3.2.1 The Evaluation of the k_1 coefficients

From the analysis of the circuit in Fig. 3.7(a) (3.6) is found. It describes the behavior of such resonant circuit.

$$V_{\text{in}} = L_{\text{p,eq}} C_{\text{p,eq1}} \frac{d^2 V_{\text{sw}}(t)}{dt^2} + V_{\text{sw}}(t) + R_{\text{t}}(t) \left(I_{\text{out}} + C_{\text{p,eq1}} \frac{dV_{\text{sw}}(t)}{dt} \right). \tag{3.6}$$

This differential equation cannot be solved explicitly, so the circuit was analyzed by means of the state space method [41], using as state variables the voltage on the capacitance $\text{C}_{\text{p,eq1}}$, V_{sw}, and the current flowing in the inductance $\text{L}_{\text{p,eq}}$, I_{sw}. This analysis allows to obtain the following system of equations:

$$\begin{cases} \dfrac{dV_{\text{sw}}}{dt} = \dfrac{I_{\text{sw}} - I_{\text{out}}}{C_{\text{p,eq1}}} \\ \dfrac{dI_{\text{sw}}}{dt} = \dfrac{V_{\text{in}} C_{\text{p,eq1}} - k_1 (I_{\text{sw}} - I_{\text{out}}) I_{\text{sw}} - C_{\text{p,eq1}} V_{\text{sw}}}{L_{\text{p,eq}} C_{\text{p,eq1}}}. \end{cases} \tag{3.7}$$

The equilibrium point (V_{SW}, I_{SW}) can be evaluated by equating the derivative of V_{sw} and I_{sw} to zero as shown below,

$$\begin{cases} \dfrac{I_{\text{sw}} - I_{\text{out}}}{C_{\text{p,eq1}}} = 0 \\ \dfrac{V_{\text{in}} C_{\text{p,eq1}} - k_1 (I_{\text{sw}} - I_{\text{out}}) I_{\text{sw}} - C_{\text{p,eq1}} V_{\text{sw}}}{L_{\text{p,eq}} C_{\text{p,eq1}}} = 0, \end{cases} \tag{3.8}$$

by obtaining

$$\begin{cases} I_{\text{SW}} = I_{\text{out}} \\ V_{\text{SW}} = V_{\text{in}}. \end{cases} \tag{3.9}$$

Based on that, the Jacobian of this system can be expressed as

$$J = \begin{bmatrix} \dfrac{dv'_{\text{sw}}}{dv_{\text{sw}}} & \dfrac{dv'_{\text{sw}}}{di_{\text{sw}}} \\ \dfrac{di'_{\text{sw}}}{dv_{\text{sw}}} & \dfrac{di'_{\text{sw}}}{di_{\text{sw}}} \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{1}{C_{\text{p,eq1}}} \\ -\dfrac{1}{L_{\text{p,eq}}} & -\dfrac{k_1}{L_{\text{p,eq}} C_{\text{p,eq1}}} i_{\text{out}} \end{bmatrix} \tag{3.10}$$

and the characteristic equation of the system can be written as

$$i''_{\text{sw}} + \frac{k_1 i_{\text{out}}}{C_{\text{p,eq1}} L_{\text{p,eq}}} i'_{\text{sw}} + \frac{1}{C_{\text{p,eq1}} L_{\text{p,eq}}} i_{\text{sw}} = 0. \tag{3.11}$$

The value of the resonance frequency f_{r1} and that of the damping factor α_1 can be obtained from (3.11) as:

$$f_{r1} = \frac{1}{2\pi\sqrt{L_{p,eq}C_{p,eq1}}} \quad \text{and} \quad \alpha_1 = \frac{k_1 I_{out}}{2L_{p,eq}C_{p,eq1}}. \tag{3.12}$$

Therefore, wanting to obtain a critically damped circuit, it needs to be $\alpha_1 = 2\pi f_{r1}$, thus the optimal value of k_1 can be calculated as:

$$k_1 = \frac{2\sqrt{C_{p,eq1}L_{p,eq}}}{I_{out}} = \frac{1}{\pi f_{r1} I_{out}}. \tag{3.13}$$

.

3.2.2 The Evaluation of the k_2 coefficients

Similarly to k_1, k_2 can be evaluated by analyzing the circuit in Fig. 3.7(b). Also in this case, the equation resulting from the analysis of this circuit cannot be explicitly solved, so the state space method is used, for the evaluation of k_2, that provides a critically damped circuit. In such a case, the state space variables chosen for the analysis, are the voltage on the capacitance C_{p,eq_2}, V_{ds} and the current I_{sw}, flowing in the inductance $L_{p,eq}$, again. The system of the equations, resulting from such analysis, is

$$\begin{cases} \dfrac{dV_{ds}}{dt} = \dfrac{I_{sw}}{C_{p,eq2}} + (V_{in} + V_\gamma - V_{ds})\dfrac{k_2}{L_{p,eq}C_{p,eq2}}V_{ds} \\ \dfrac{dI_{sw}}{dt} = \dfrac{V_{in} - V_{ds} + V_\gamma}{L_{p,eq}}. \end{cases} \tag{3.14}$$

The equilibrium point results

$$\begin{cases} I_{SW} = 0 \\ V_{DS} = V_{in} + V_\gamma, \end{cases} \tag{3.15}$$

thus, the system can be linearized as

$$J = \begin{bmatrix} \dfrac{dv'_{ds}}{dv_{ds}} & \dfrac{dv'_{ds}}{di_{sw}} \\ \dfrac{di'_{sw}}{dv_{ds}} & \dfrac{di'_{sw}}{di_{sw}} \end{bmatrix} = \begin{bmatrix} -\dfrac{k_2(V_{in} + V_\gamma)}{L_{p,eq}C_{peq,2}} & \dfrac{1}{C_{p,eq2}} \\ -\dfrac{1}{L_{p,eq}} & 0 \end{bmatrix} \tag{3.16}$$

and its characteristic equation can be expressed as

$$v''_{\mathrm{ds}} + \frac{k_2(V_{\mathrm{in}} + V_\gamma)}{L_{\mathrm{p,eq}} C_{\mathrm{p,eq2}}} v'_{\mathrm{ds}} + \frac{1}{L_{\mathrm{p,eq}} C_{\mathrm{p,eq2}}} v_{\mathrm{ds}} = 0, \tag{3.17}$$

where

$$f_{\mathrm{r2}} = \frac{1}{2\pi\sqrt{L_{\mathrm{p,eq}} C_{\mathrm{p,eq2}}}} \quad \text{and} \quad \alpha_2 = \frac{k_2(V_{\mathrm{in}} + V_\gamma)}{2 C_{\mathrm{p,eq2}} L_{\mathrm{p,eq}}}. \tag{3.18}$$

Therefore, the optimal value for k_2 can be expressed as

$$k_2 = -\frac{2\sqrt{L_{\mathrm{p,eq}} C_{\mathrm{p,eq2}}}}{V_{\mathrm{in}} + V_\gamma} = -\frac{1}{\pi f_{\mathrm{r2}} (V_{\mathrm{in}} + V_\gamma)}. \tag{3.19}$$

3.2.3 Assessment of the Optimal Switching Waveforms

In this section, the analysis presented so far is validated by referring to the buck converter shown in Fig. 3.1. The power switch chosen to perform this analysis is the GaN EPC2001C [42], while the diode is the STPS30100ST [43]. All the passive component that make up the circuit are listed in Table 3.1, as well as the parasitic elements.

Table 3.1: Parameter values of the analyzed converter.

Name	Value	Name	Value	Name	Value
C_1(x 2)	220 μF	L_{c1}	10 nH	R_{c1}	100 mΩ
C_2	22 μF	L_{c2}	5 nH	R_{c2}	50 mΩ
C_3(x 2)	2.2 μF	L_{c3}	2 nH	R_{c3}	10 mΩ
$L_{\mathrm{t1}}, L_{\mathrm{t2}}$	1 nH	$L_{\mathrm{d}}, L_{\mathrm{s}}$	1 nH	$L_{\mathrm{an}}, L_{\mathrm{cat}}$	1 nH
L_{t3}	100 pH	L_{in}	10 μH	C_{t1}	200 pF
L_{out}	33 μH	C_{out}	270 μF	R_{in}	730 $m\Omega$
V_{in}	48 V	V_{out}	12 V	I_{out}	16.5 A

The circuit was analyzed performing the time domain simulations exploiting the *spectre* simulator included in the Cadence Virtuoso environment [44]. The aim of this analysis is to obtain the parameters of the equivalent simplified high frequency model, shown in Fig. 3.2. The obtained parameters are reported in Table 3.2. Further details about the simulations, the netlists and the implementation of the $\mathrm{R_t}$ and $\mathrm{G_t}$ components are reported in th Appendix A.
The comparison between the $\mathrm{I_{sw}}$ current resulting by simulating the complete circuit and the proposed model are shown in Fig. 3.8. The frequencies of the oscillations are in good agreement, both after the turn-on and after the turn-off of the low side

Table 3.2: List of the oscillating waveforms parameters

Symbol	Description	Value
f_{r_1}	Turn-on oscillation frequency	116 MHz
f_{r_2}	Turn-off oscillation frequency	132 MHz
$C_{p,eq1}$	High side equivalent capacitance	638 pF
$C_{p,eq2}$	Low side equivalent capacitance	493 pF
$L_{p,eq}$	Equivalent inductance	2.95 nH

switch. It is worth noticing that the aim of the proposed model is to reproduce only the resonant and the steady state behavior of the circuit, by neglecting the information about the transients, which are strictly related to the distribution of the parasitic elements in the circuit.

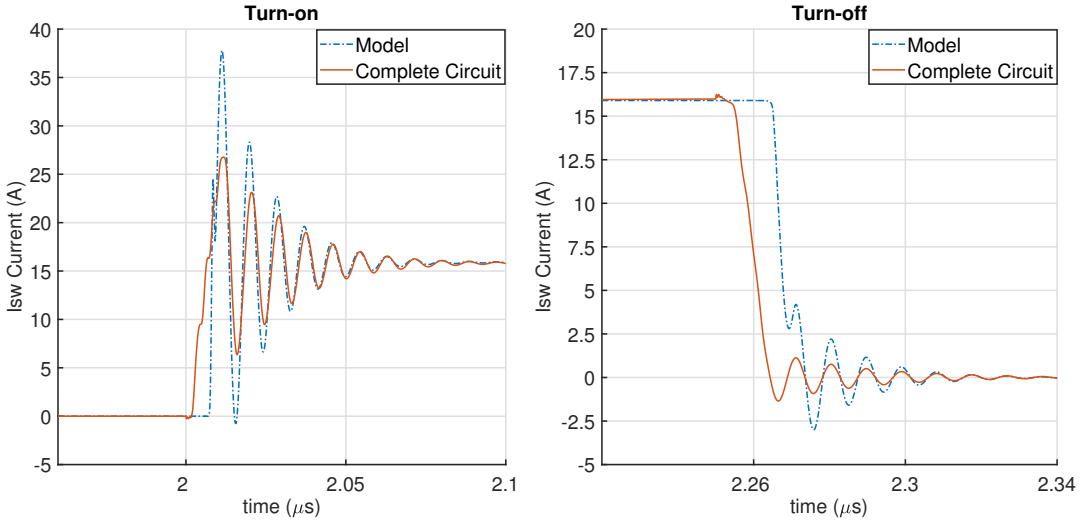

Figure 3.8: Comparison between the I_{sw} current resulting by a simulation of the complete circuit (continuous lines) and from the equivalent model (dotted lines), after the turn-on and after the turn-off of the low side switch.

The steady state condition of the converter and the frequencies of the oscillations, are used to evaluate the optimal values of k_1 and k_2 using the Eqs. 3.13 and 3.19. The optimal value of the coefficient k_1 is 165 ps/A while the optimal one of k_2 results to be -61 ps/V. Such parameters were used to analyze the equivalent circuits shown in 3.6, comprising the R(t) and G(t) elements that are modeled using the *Verilog-A* hardware description language. The code describing such components is reported in Appendix A. The voltages V_{sw} and the current I_{sw}, resulting by a simulation of such circuit, are plotted in Fig. 3.9 and and in Fig. 3.10 by

solid lines. The other waveforms shown in these figures, are obtained without

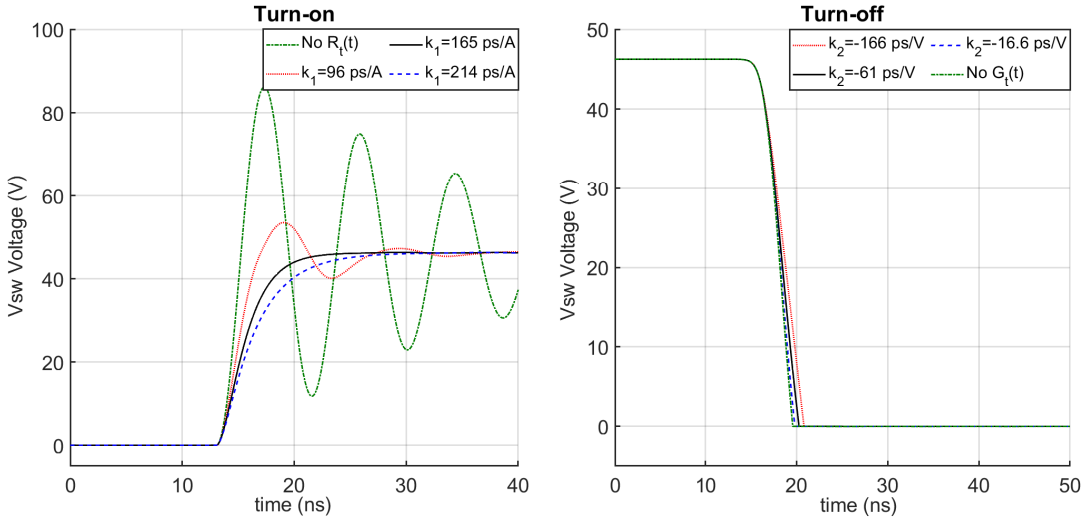

Figure 3.9: Switching voltage V_{sw} obtained from a parametric simulation of the coefficients k_1 and k_2 by simulating the circuit in Fig. 3.6. The coefficients steps from 0 (No R(t) and G(t)) to a value greater than the optimal one, resulting in an overdamped voltage.

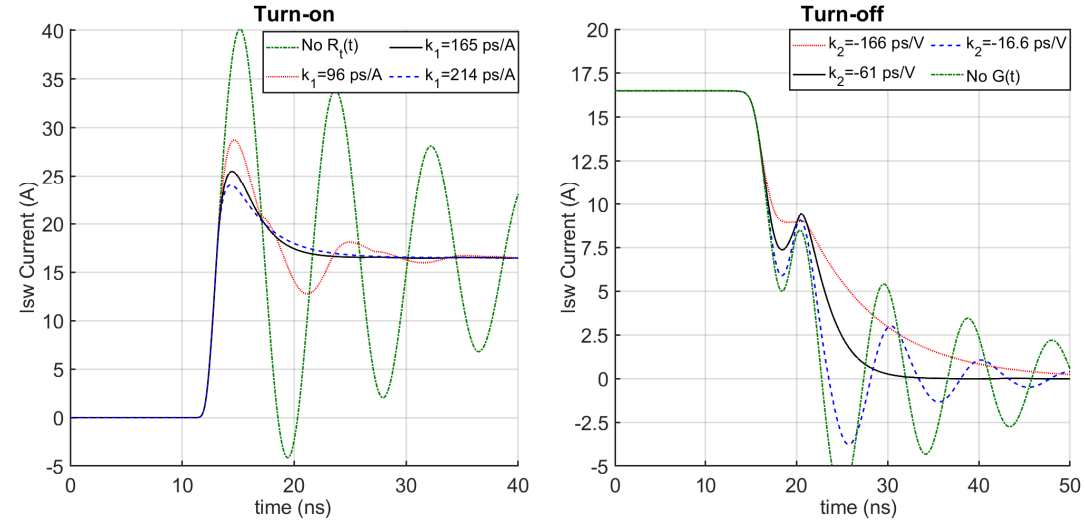

Figure 3.10: Switching Current I_{sw} obtained from a parametric simulation of the coefficients k_1 and k_2 by simulating the circuit in Fig. 3.6. The coefficients steps from 0 (No R(t) and G(t)) to a value greater than the optimal one, resulting in an overdamped current.

the proposed damping elements (dash-dotted lines) and with values of k_1 and k_2

greater (dotted lines) and lower (dashed lines) than the optimal values. The former are over damped waveforms, the latter are under damped ones, thus confirming the validity of the analysis presented so far. Referring to the optimal value of k_1 and k_2, in Fig. 3.11 is shown the comparison between the voltage V_{ds} obtained with and without the R(t) and G(t) components active. At the turn-on, when the R(t) is active, the voltage V_{ds} shows a parabolic behavior, due to which the oscillations superimposed on the voltage V_{sw} and on the current I_{sw} are avoided. On the other side, after the turn-off of the switch S_{id}, the V_{ds} voltage shows the lack of oscillations due to the G(t) elements, that sinks a piece of current that, otherwise will flow through the capacitance C_{p,eq_2}, triggering oscillation. This effect is clearer, by comparing also the optimal current with the no snubbered one, at the turn-off (Fig. 3.10). In fact, the former softly decreases compared to one obtained without G(t) and, this behavior allows one to obtain critically damped waveforms. The $R_t(t)$ and $G_t(t)$ behavior are validated for other circuit topologies in the Appendix B.

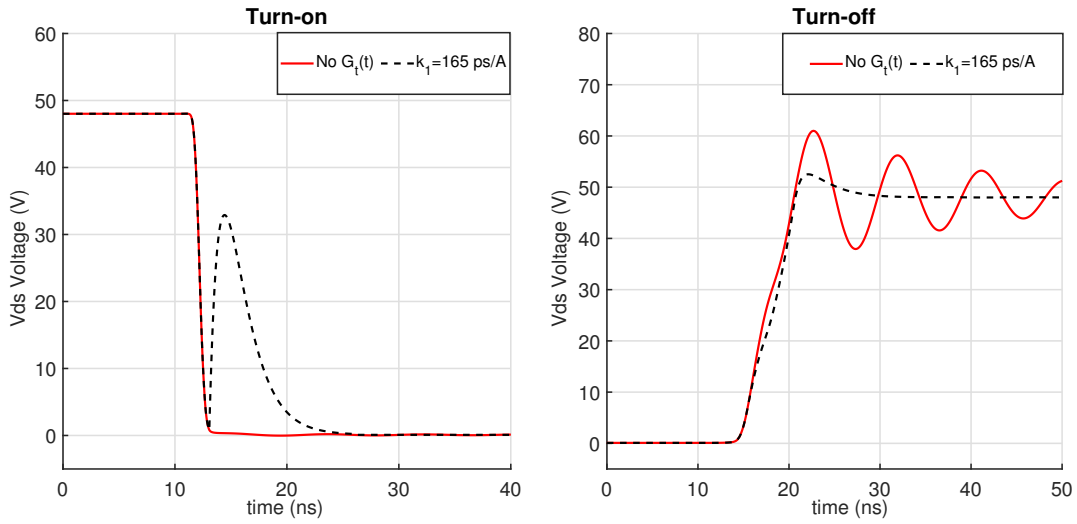

Figure 3.11: Comparison between the V_{ds} voltage obtained with k_1 and k_2 equal to zero (solid lines), with the ones resulting exploiting their optimal values (dashed lines).

3.3 Analysis of R_t and G_t Behavior

In the previous section, the time variant R_t and G_t components have been defined according the proposed analysis of the switching transients, which led to establish that the turn-on oscillations are triggered by the rising edge of the voltage V_{sw} while the turn-off ones are caused by the falling edge of the current I_{sw}. Due to these considerations, a mathematical analysis on the turn-on and on the turn-off equivalent circuits was performed, and the optimal value of the two coefficients k_1 and k_2, to obtain critically damped circuits, have been evaluated.

In this section, firstly a simulation analysis on the simplified buck converter was conducted, with the aim to understand how R_t and G_t components work if the operation conditions of the converter change. This analysis has highlighted some limitations in the definition of k_1 and k_2 allowing to improve them by means of an expedients which makes them more feasible. After these adjustments, mathematical equations of the energies associated to the turn-on commutation and to the turn-off one were derived. These equations have an important role, because they allow one to compare the effectiveness in terms of efficiency of the proposed technique with respect to the one of other widespread methods to dump the oscillations.

3.3.1 Load Current Variation

In this subsection the circuit shown in Fig. 3.6 is simulated by stepping the load current and analyzing the behavior of R_t and G_t, by exploiting the optimal values of k_1 and k_2 derived in section 3.2. The results of such simulations are shown in dashed lines in Fig. 3.12 both for the turn-on and the turn-off. The analysis of the turn-on waveforms highlights that less is the value of the load current, higher is the peak value that the voltage V_{ds} reaches when R_t is active. Besides, with the smallest currents, the trajectory of the current I_{sw} that charges the parasitic capacitance $C_{peq,1}$, is similar to the current that flows in an overdamped series RLC circuit. This suggest that the power dissipated by R_t at the turn-on is higher than the one needed to obtain a critically damped circuit. This effect is more evident with lower load current.

This behavior depends on the definition of k_1, more precisely on the value of I_{out} that appears in the denominator. When R_t is active, for each time steps, the value of the derivative of V_{sw} is multiplied by a constant k_1 inversely proportional to I_{out}, creating a time variant damping resistor. In practice, the value of the current flowing through R_t, when this component is active, is higher than I_{out} and is related to the value of the parasitic capacitance $C_{p,eq1}$. This means that a more effective definition of k_1 can be stated exploiting the value that the I_{sw} current assumes in each instant. This is equivalent to apply the state space method for all the time

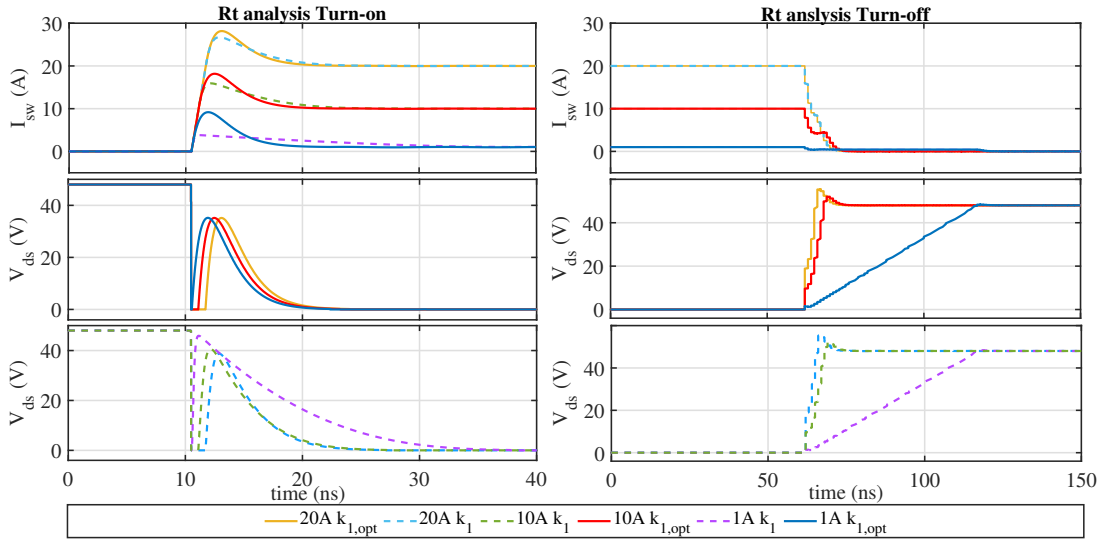

Figure 3.12: Comparison between the V_{ds} voltage and the I_{sw} current obtained with the constant k_1 (dashed lines) and the time variant one (solid lines).

instants in which the R_t and the G_t are active [41].

$$k_{1,\text{opt}} = \frac{1}{\pi f_{r1} I_{sw}(t)}. \tag{3.20}$$

The switching waveforms resulting by using $k_{1,opt}$ instead of the previously defined one, to calculate the optimal value of R_t are plotted in Fig. 3.12, with solid lines. These waveforms are all critically damped, in fact the peak of the Vds is the same for all the waveforms regardless of the value of the current I_{out}, and the trajectory of I_{sw} when the R_t is active, appears to be always the one of a critically damped circuit. By comparing the energy involved at the turn-on, shown in Fig. 3.13, using these two different types of R_t, it is possible to see that the use of $k_{1,opt}$ results to be less dissipative if compared with the constant k_1. Moreover as expected, the relative difference between these two energies is higher when the load current is lower, as highlighted in the bottom of Fig. 3.13. Besides, the R_t does not play no role at the turn-off. In fact, as shown in Fig. 3.12 (right side), the turn off switching waveforms are identical both with the k_1 and $k_{1,opt}$.

3.3.2 Power Supply Variation

Similar considerations can be made about the G_t component and the power supply voltage V_{in}. Indeed, at the turn-off, the k_2 coefficient depends on the value of V_{in} as shown in Eq. 3.19. More precisely, smaller is the value of V_{in}, and higher is the value of k_2, but as in the case of k_1 at the turn-on, this high value is not needed

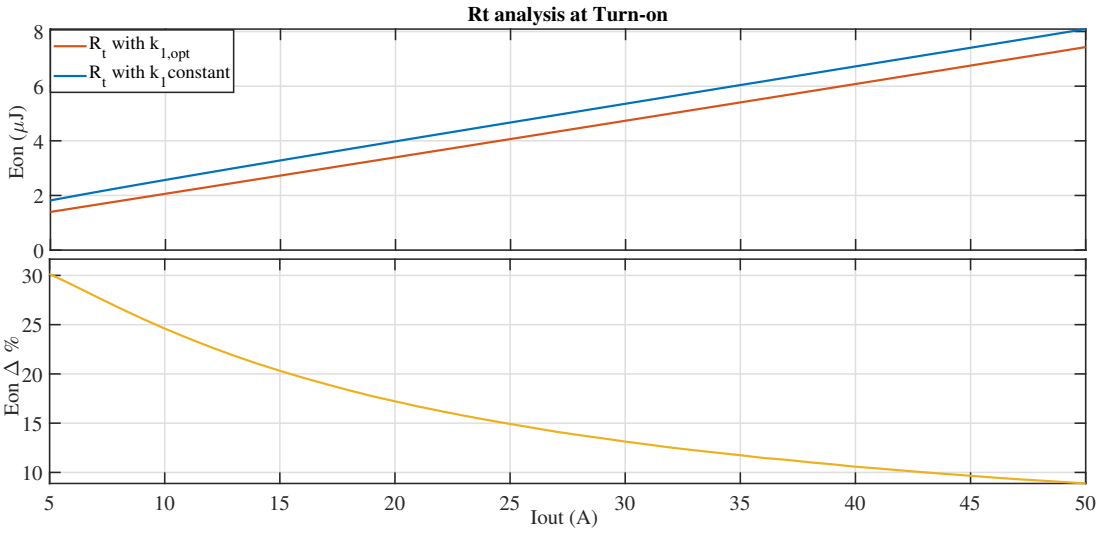

Figure 3.13: Comparison between the turn on energy as a function of the load current exploiting the constant k_1 and the optimal time variant one.

for all the duration of I_{sw} transition and it is possible to define a time variant $k_{2,opt}$ according to the following:

$$k_{2,\text{opt}} = \frac{1}{\pi f_{r2} V_{ds}(t)}. \tag{3.21}$$

The better performance obtained exploiting $k_{2,opt}$ can be seen in Fig. 3.14, especially by analyzing the V_{ds} waveforms. In fact, the smaller is the value of V_{in}, the higher is the difference between the V_{ds} obtained using the optimal $k_{2,opt}$ and the one obtained by using the constant k_2. Also in this case, the smaller is the value of the V_{in}, the greater is the advantage of using the time variant k coefficient with respect the constant one. The turn-on switching waveforms are not affected by the definition of the optimal $k_{2,opt}$, as well as the turn-off switching waveforms do not depend on the optimal $k_{1,opt}$ as expected by the equations in 3.4 and 3.5.

3.3.3 Turn on energy estimation

The analysis of the turn-on switching waveforms presented so far, has highlighted that, using the optimal k_1 coefficient, the trajectory of such waveforms is always the same as shown by solid lines in Fig 3.12. This behavior does not depend on the value of the load current I_{out} that affects only the steady state value of the I_{sw}. Such remarks allows one to write the current I_{sw} as:

$$I_{sw} = I_{out} + I_{C_{p,eq1}} \tag{3.22}$$

where $I_{C_{p,eq1}}$ is the current I_{sw} when I_{out} is equal to zero. By imposing this condition in the circuit shown in Fig. 3.6, it become possible to find an explicit solution of

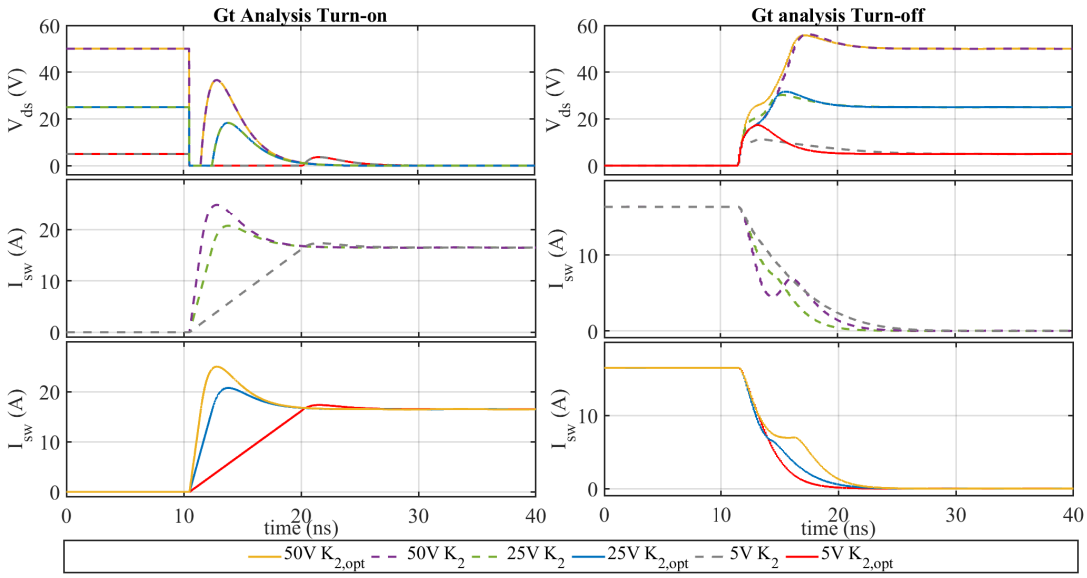

Figure 3.14: Comparison between the V_{ds} voltage and the I_{sw} current obtained with the constant k_2 (dashed lines) and the time variant one (solid lines).

the I_{sw}, that in this particular case, is the same current that flows through the capacitance $C_{p,eq1}$. The solutions of the resulting differential equation, in critically damped conditions, is derived, and I_{sw} can be expressed as:

$$I_{sw} = I_{out} + \frac{V_{in}}{L} \cdot t \cdot exp\Big(- \frac{t}{\sqrt{LC}}\Big). \tag{3.23}$$

In the same way, the voltage V_{ds} can be expressed as:

$$V_{ds} = 2\sqrt{\frac{L}{C}}\frac{V_{in}}{L} \cdot t \cdot exp\Big(- \frac{t}{\sqrt{LC}}\Big) \tag{3.24}$$

By knowing I_{sw} and V_{ds} it is possible to calculate the energy dissipated at the turn-on exploiting the following equation, where the instantaneous power is integrated as a function of the time:

$$E_{on,Rt} = \int_0^\infty (I_{sw} V_{ds}) dt \tag{3.25}$$

Such an integral, can be easily solved by individually solving the DC and the AC part of the instantaneous power:

$$E_{on,Rt} = \int_0^\infty (I_{out} V_{ds}) dt + \int_0^\infty (I_{C_{p,eq1}} V_{ds}) dt \tag{3.26}$$

The second term of the integral is the power dissipated to charge the capacitance, so it can be expressed as:

$$\int_0^\infty (I_{C_{p,eq1}} V_{ds}) dt = \frac{1}{2} C_{p,eq1} V_{in}^2 \tag{3.27}$$

while the first term can be solved and the total energy results:

$$E_{on,Rt} = 2I_{out}V_{in}\sqrt{C_{p,eq1}L_{p,eq}} + \frac{1}{2}C_{p,eq1}V_{in}^2 = \frac{I_{out}V_{in}}{\pi f_{r1}} + \frac{1}{2}C_{p,eq1}V_{in}^2 \tag{3.28}$$

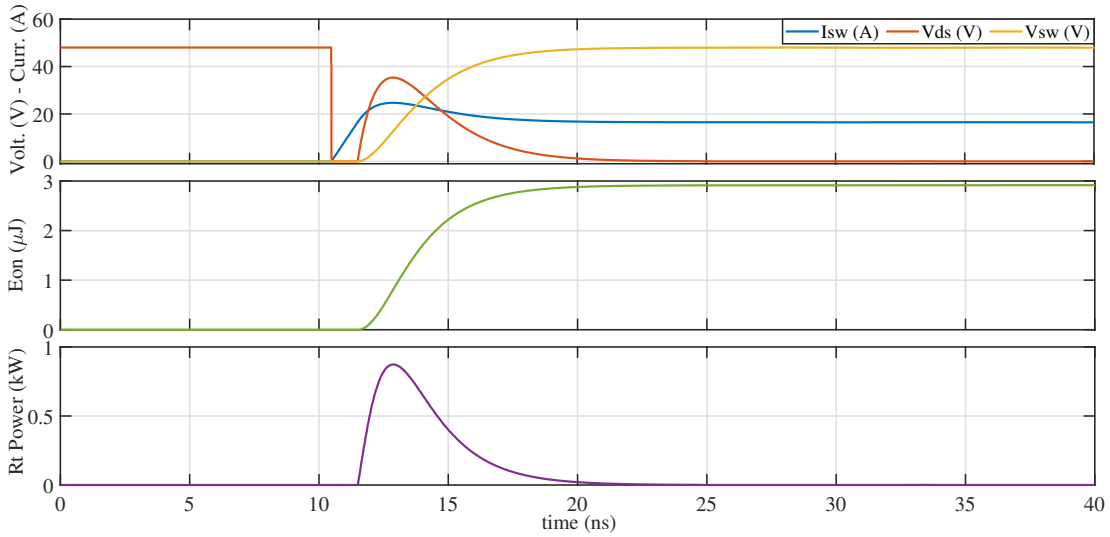

Figure 3.15: Optimal switching waveforms obtained using the optimal $k_{1,opt}$. The turn-on energy and and the instantaneous power are shown in green and violet lines, respectively.

The calculated turn-on energy exploiting the value of the parameters listed in Table 3.2 and the Eq. 3.28 is $2.9\,\mu J$, the same obtained by simulating the circuit in Fig. 3.6 and evaluating the energy dissipated at the turn-on. This can be seen in Fig. 3.15, in which the optimal switching waveforms of the circuit with the energy related to the turn-on are shown.

Comparison with the RC snubber solution

In this subsection, the turn-on energy dissipated by the R_t component is compared with the energy dissipated by means of the RC snubber topology. As stated in Chapter 1, an RC snubber can remove the oscillations superimposed to the switching waveforms if placed in parallel with the freewheeling diode and if it is properly sized, according the following equations:

$$C_{snb,hs} = 4C_{p,eq1} \qquad R_{snb,hs} = 2\sqrt{\frac{L_{p,eq}}{C_{p,eq1}}} \tag{3.29}$$

The energy dissipated at the turn-on using the snubber can be calculated as:

$$E_{on,snb} = \frac{5}{2} \cdot C_{p,eq1}V_{in}^2 \tag{3.30}$$

So, by equating the energy dissipated using the R_t $E_{on,Rt}$ with the energy dissipated by means of the RC snubber at the turn-on it is possible to carry out the relationship in 3.31, that represent a criterion for establishing what solution is most convenient, once it has been established the operating condition of the converter and the parasitic components that cause the oscillations after the turn-on of the switch. More precisely, the R_t solution is more effective if the following inequality is respected:

$$I_{out} < \sqrt{\frac{C_{p,eq1}}{L_{p,eq}}} \cdot V_{in} \tag{3.31}$$

This means that a lower value of the equivalent parasitic inductance and an higher value of the voltage power supply, result in a more convenient usage of the R_t if compared to the traditional snubber solution. As far as the variation the load current is concerned, the values of V_{in}, $C_{p,eq1}$ and $L_{p,eq}$ define the limit of I_{out}, under which the R_t dissipates less energy than the RC snubber, at about 22 A. Such relationship has been validated by means of a parametric simulations whose results are shown in Fig. 3.16. Different from I_{out} current variation, if the power supply voltage V_{in} changes, the relationship is slightly more complicated because the value of the capacitance $C_{peq,1}$ depends on the reverse voltage applied to the freewheeling diode when it is off, i,e., V_{in}. In this situation, is the higher value of $C_{peq,1}$ to establish if the R_t is more convenient than the snubber but, on the other side, the value of the snubber components are chosen according the worst oscillating conditions. This means that the snubber should be sized to damp the lowest oscillation frequency that could affect the switching waveforms. This happens with the highest value of

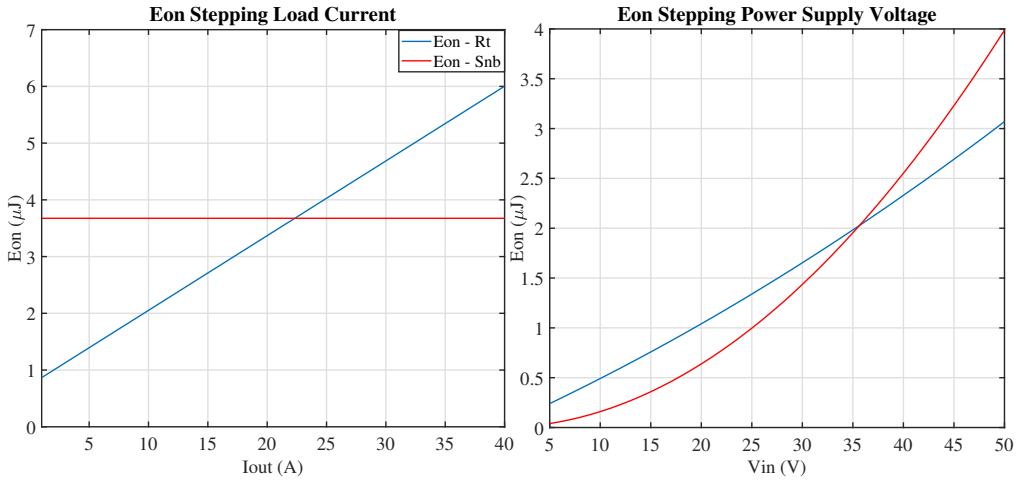

Figure 3.16: Comparison between the energy dissipated by the RC snubber and the R_t component at the turn-on, by stepping the load current I_{out} and the voltage V_{in}.

the capacitance $C_{peq,1}$ that should be used as reference to properly size the snubber components.

3.3.4 Turn-off Energy estimation

As stated before, the G_t component acts during the turn-off in a complementary way if compared with the R_t at the turn-on. For such a reason, in this case it is possible to write the V_{ds} voltage as follow,

$$V_{ds} = V_{in} + V_{C_{p,eq2}} \tag{3.32}$$

where $V_{C_{p,eq2}}$ is the voltage drop across the parasitic capacitance $C_{p,eq2}$ when V_{in} is equal to zero. The explicit solution of the circuit in Fig. 3.7 with the critically damped condition and V_{in} equal to zero is:

$$\begin{aligned} V_{ds} &= V_\gamma - V_\gamma \cdot exp\left(- \frac{t}{\sqrt{L_{p,eq}C_{p,eq2}}}\right) + \\ &+ \frac{t}{C_{p,eq2}} \cdot exp\left(- \frac{t}{\sqrt{L_{p,eq}C_{p,eq2}}}\right) \cdot \left(I_{out} - \sqrt{\frac{C_{p,eq2}}{L_{p,eq}}} \cdot V_\gamma \right) + V_{in} \end{aligned} \tag{3.33}$$

For a sake of simplicity, V_γ is placed equal to zero, since in a good converter the voltage V_{in} is always much larger than the forward voltage of the diode. So the equation 3.33 can be simplified as follow:

$$V_{ds} = \sqrt{I_{out}C_{p,eq,2}} \cdot t \cdot exp\left(- \frac{t}{\sqrt{L_{p,eq}C_{p,eq,2}}}\right) + V_{in}. \tag{3.34}$$

In the same manner, the current flowing through the G_t component can be calculated as:

$$I_{G_t} = 2\sqrt{\frac{C_{p,eq2}}{L_{p,eq}}\frac{I_{out}}{C_{p,eq2}}} \cdot exp\left(- \frac{t}{\sqrt{L_{p,eq2}C_{p,eq2}}}\right). \tag{3.35}$$

So the energy related to the turn off can be written as:

$$E_{on,Gt} = \int_0^\infty (I_{G_t}V_{in})dt + \int_0^\infty (I_{C_{p,eq2}}V_{ds})dt \tag{3.36}$$

In this case, the energy can be calculated as the sum of three terms, the first one is related to the charge of the capacitance $C_{peq,2}$ with the constant current I_{out}, the second terms is related the G_t component, while the last to the charge of the $L_{p,eq}$ inductance.

$$E_{off,Gt} = \frac{1}{2}C_{p,eq2}V_{in}^2 + \frac{1}{2}L_{p,eq}I_{out}^2 + 2 \cdot I_{out} \cdot V_{in}\sqrt{L_{p,eq}C_{p,eq2}} \tag{3.37}$$

In contrast with the turn-on energy estimation, in an asynchronous converter the Eq. 3.37 is an approximation because at the turn-off a portion of the energy stored in the capacitance $C_{peq,1}$ is recovered during the turn-off voltage transition. This relationship is more accurate when $C_{p,eq1}$ in much lower than $C_{p,eq2}$. In the considered case, a comparison between the results of the Eq. 3.37 and the dissipated energy evaluated by means of simulation is shown in Fig. 3.17.

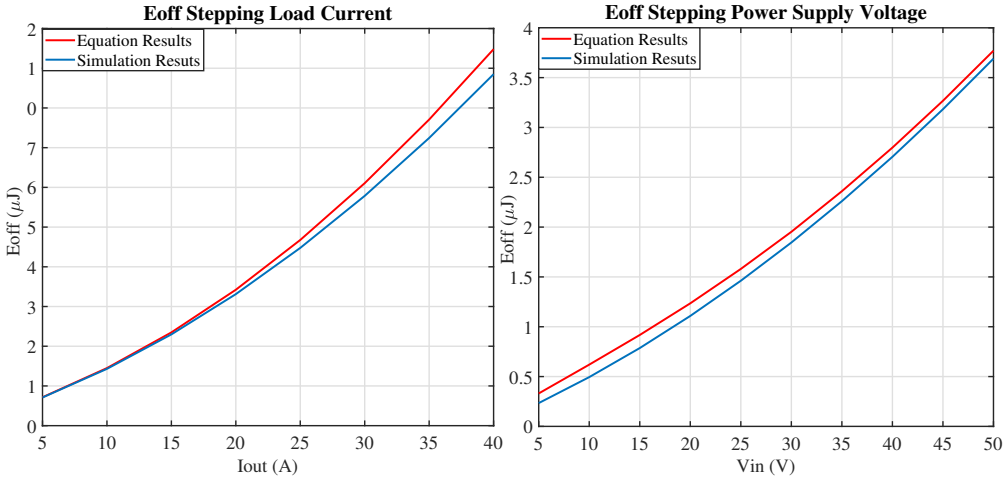

Figure 3.17: Comparison between the turn-off energy calculated exploiting the Eq. 3.37 (red lines) and the one evaluated by means of simulations (blue lines) by stepping the load current and the power supply voltage.

3.4 A Method to derive the gate current profile

The above presented analysis allows one to understand how it is possible to obtain critically damped waveforms from the commutations of a power converter, providing a mathematical model based on two auxiliary elements, a time variant resistance R_t and a time variant conductance G_t, placed inside the power loop. There are several aspects that must be taken into account by referring to the proposed model; the first is just about the R_t and G_t elements. Such components cannot be physically deployed, in fact their purpose is to provide guidelines about the switching trajectories to reproduce, for avoiding oscillations superimposed to the switching waveforms. A further consideration is about the controlled switch. In the proposed model it is used an ideal one but, in a real converter, this function is performed by a power transistor. These considerations suggest to exploit the power transistor itself to reproduce the optimal switching waveforms, resulting from the analysis presented so far driving it with an AGD. As a consequence, the study goes on, referring to the circuit shown in Fig. 3.18.

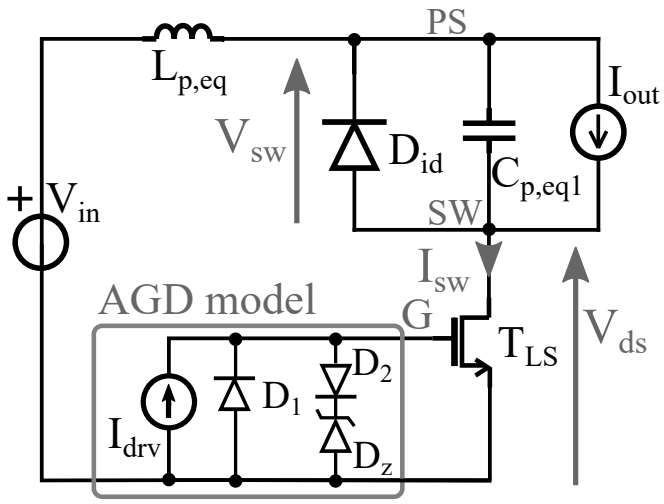

Figure 3.18: Proposed model in which the ideal switch and the capacitance C_{p,eq_2} are replaced with the power transistor, driven by an ideal driver.

In this circuit the ideal switch S_{id} and the capacitance C_{p,eq_2} are replaced with a power transistor. More precisely, it is considered the same GaN device used in the complete circuit shown in Fig. 3.1, the *EPC2001C*. In this way, the equivalent parasitic capacitance of the power transistor, in the same operating condition, assumes the same value of C_{p,eq_2}, without affecting the value of the frequency f_{r_2} after the transistor turn-off. The transistor is driven by means of an ideal current AGD with in parallel the diode D_1 and the couple of diodes D_2 and D_z needed to avoid the input voltage, exceeding the minimum voltages bearable by the power device, between gate and source. The optimal switching waveforms obtained due to the R_t and the G_t time-variant components, can be reproduced driving properly the power transistor T_{LS}. In order to explain how to drive T_{LS} to reproduce the power loop optimal switching waveforms, one should refer to the switching characteristic of a generic power transistor reported in Chapter 2, and to the optimal switching waveforms shown in Fig. 3.19. This figure reports the switching current I_{sw} and the voltage V_{ds} resulting from the undamped circuit (dashed lines) and those resulting exploiting R(t) and G(t) with the optimal values of k_1 and k_2 (continuous lines). Fig. 3.6 gives important information about such waveforms. More precisely, during the turn on transient the current I_{sw} and the voltage V_{ds} are the current that flows through R(t) and the voltage that drops on it, respectively. Furthermore, at the turn-off, these are the electrical waves that characterize the G(t) component. For these reasons, in order to obtain a critically damped circuit, these should be the voltages and the currents that will characterize the power transistor T_{LS} during its turn-on and turn-off transients.

At the turn-on, the trajectory of the voltage V_{ds} results of particular interest for reproducing the optimal switching waveforms. More precisely, when the $R_t(t)$ is

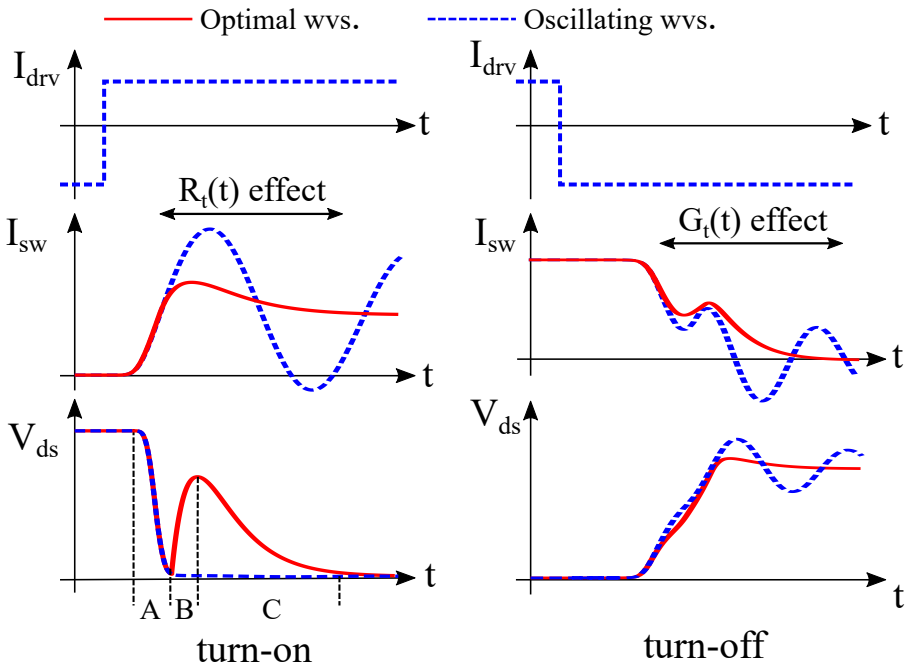

Figure 3.19: Effect of $R_t(t)$ and $G_t(t)$ on the switching waveforms at the turn-on and at the turn-off. The oscillating waveforms are shown by dashed dot lines, the ones with $R_t(t)$ and $G_t(t)$ are plotted by continuous lines.

active, the V_{ds} firstly increases, and later decreases rapidly, allowing to dissipate the energy that, otherwise, will trigger the oscillations. In other words, by controlling the behavior of the V_{ds} voltage, it is possible to control the current that charges the parasitic capacitance C_{p,eq_1}, allowing to the V_{sw} and I_{sw} to reach the steady state at the same time, and avoiding that the oscillations take place. This behavior can be reproduced with the power transistor exploiting the Miller's effect. More precisely, keeping the transistor in linear region, it is possible to change linearly its V_{ds} voltage drop, by injecting or sinking in the gate a constant piecewise current. So, the optimal turn-on behavior can be theoretically reproduced by means of a three level gate current, as the one shown in Fig. 3.20.

Referring to the Fig. 3.20, the three phases of the turn-on can be summarized as follows [39, 40]:

- The first level $I_{A,on}$ is positive, turns-on the switch pulling down the V_{ds}, and let the I_{sw} to reach its nominal value for the first time.
- The second level $I_{B,on}$ is negative and occurs when the power device is in linear region. It allows the V_{ds} voltage to increase linearly and to follows the optimal one shown in Fig. 3.20.
- Finally,the third level $I_{C,on}$ is positive again, to turn on definitely the power

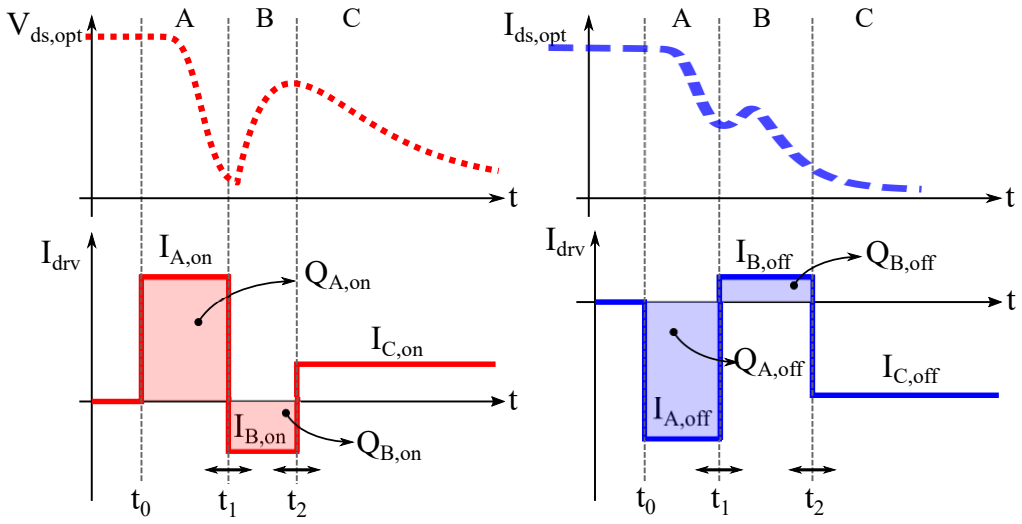

Figure 3.20: Gate current to reproduce the optimal switching waveforms at the turn-on and at the turn-off of the power transistor.

transistor, whose V_{ds} continues to follow the trajectory of the optimal one.

Similarly, in order to obtain the optimal turn-off, avoiding the oscillations, a dual three level gate driver current can be exploited. In such case, the three levels ca be summarized as follows:

- The first level $I_{A,off}$ is negative and allows the turn-off the power switch. In this way the voltage V_{ds} reaches the value V_{in} and the V_{sw} becomes zero.
- The second level $I_{B,off}$ is positive and it is necessary to limit the slope of the current I_{sw}, avoiding the triggering of the ringing phenomenon.
- The last level $I_{C,off}$ is negative again and leads softly the current I_{sw} to zero, keeping the waveforms free from oscillations.

3.4.1 The Alghortim to Derive the Optimal Gate Current Profiles

The analysis presented so far allows one to obtain the optimal switching waveforms through a single time-domain simulation of the power circuit including in the simulation environment the R_t and G_t components, whiose coefficients k_1 and k_2 depend on the oscillation frequencies and on the operating conditions of the power converter. In the previous section, a general idea about the driving technique for reproducing the optimal switching waveforms is provided in order to introduce the proposed algorithm to derive the gate current profile, based on parametric simulations. In this subsection, the algorithm for extrapolating the optimal gate current profile is described, referring to the flow chart shown in Fig. 3.21.

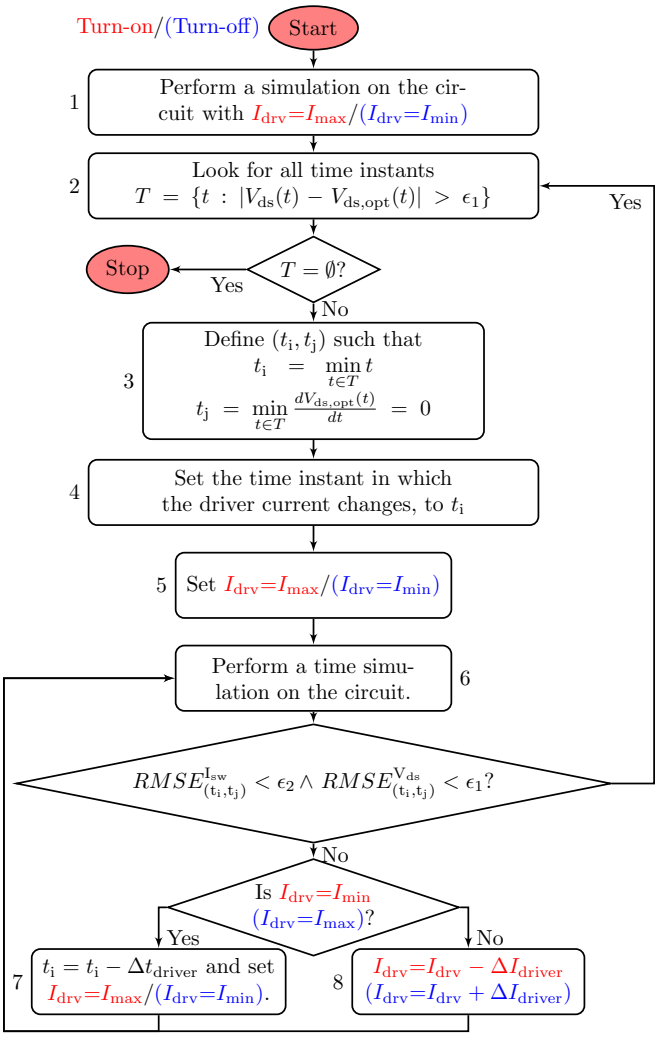

Figure 3.21: Flowchart of the proposed tuning algorithm.

The proposed algorithm is explained by referring to the simplified circuit shown in Fig. 3.18. As previously reported, the low-side transistor T_{LS} driven with an ideal driver, replaces the switch S_{id} in Fig. 3.2. The current source I_{drv} represents the AGD output stage and models its main features, like the maximum and the minimum bearable current, the time, and the current resolutions. I_{drv} can source and sink the maximum and minimum programmable currents (I_{max} and I_{min}), adjust the current level every Δt_{driver} (time resolution) and can change the output current level (current resolution) in steps of ΔI_{driver}. Therefore, in order to quantify the goodness of the selected driver parameters during the algorithm iteration, the root mean squared error, defined accordingly to (3.38) and (3.39), is exploited. In the time interval (t_a, t_b) the root mean squared error, hereafter called $RMSE$, is

evaluated on the base of all the N samples belonging to such time interval, as

$$RMSE^{\mathrm{I_{sw}}}_{(\mathrm{t_a},\mathrm{t_b})} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(I_{\mathrm{sw}}(i) - I_{\mathrm{sw,opt}}(i))^2}, \tag{3.38}$$

$$RMSE^{\mathrm{V_{ds}}}_{(\mathrm{t_a},\mathrm{t_b})} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(V_{\mathrm{ds}}(i) - V_{\mathrm{ds,opt}}(i))^2}. \tag{3.39}$$

The proposed algorithm aims to determine the number of current steps, as well as the corresponding levels and time duration, while keeping the aforementioned errors, during the turn-on and turn-off transients, below two given thresholds, i.e. ϵ_1 and ϵ_2 for the V_{ds} and the I_{sw}, respectively. The proposed algorithm is made up of eight steps, which are highlighted in Fig. 3.21. The procedure has to be executed two times, since the turn-on and turn-off transients are analyzed separately. Therefore, the simulation time covers a single transient, meaning that the switching waveforms have to be clipped from the turn-on and turn-off triggering event until the voltages current reach their steady state.

Algorithm for the optimal turn-on

The converter shown in Fig. 3.18 is simulated, turning-on the low side transistor $\mathrm{T_{LS}}$ with the maximum current that $\mathrm{I_{drv}}$ can source. This simulation allows the

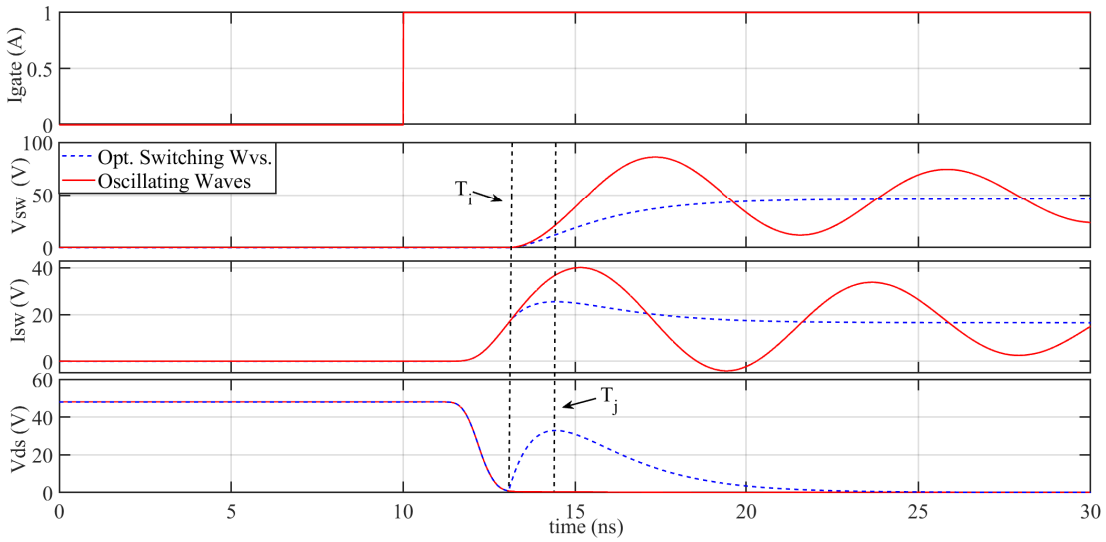

Figure 3.22: Step 1 of the proposed algorithm. The optimal switching waveforms are shown in dotted lines, while the oscillating ones resulting by the turn-on of the transistor with all the available gate current are shown solid lines.

designer to obtain the turn-on oscillating waveforms, shown in Fig. 3.22 in solid

lines, and to calculate the value of the coefficient k_1. Now, the circuit can be configured as shown in Fig. 3.6, to obtain the optimal switching waveforms by means of a single transient simulation, also performed with $I_{drv} = I_{max}$ (step 1). These waveforms are shown in Fig. 3.22, by dashed lines.

The obtained optimal switching waveforms, named $I_{sw,opt}$, $V_{sw,opt}$ and $V_{ds,opt}$ hereafter, will be the target for tuning the parameters of the gate driver in what follows. With reference to Fig. 3.22, it can be noticed that the $V_{ds,opt}$ is not monotonic at the turn-on, but it promptly decreases, then it increases up to reach a local maximum, and finally it slowly decreases to zero. The latter two stages, as stated before, are caused by R_t, since its resistance value increases to avoid the oscillations from being excited by the rise of the voltage V_{sw}. Detecting the interval of time in which the R_t is active, means to perform the step 2 of the proposed algorithm.

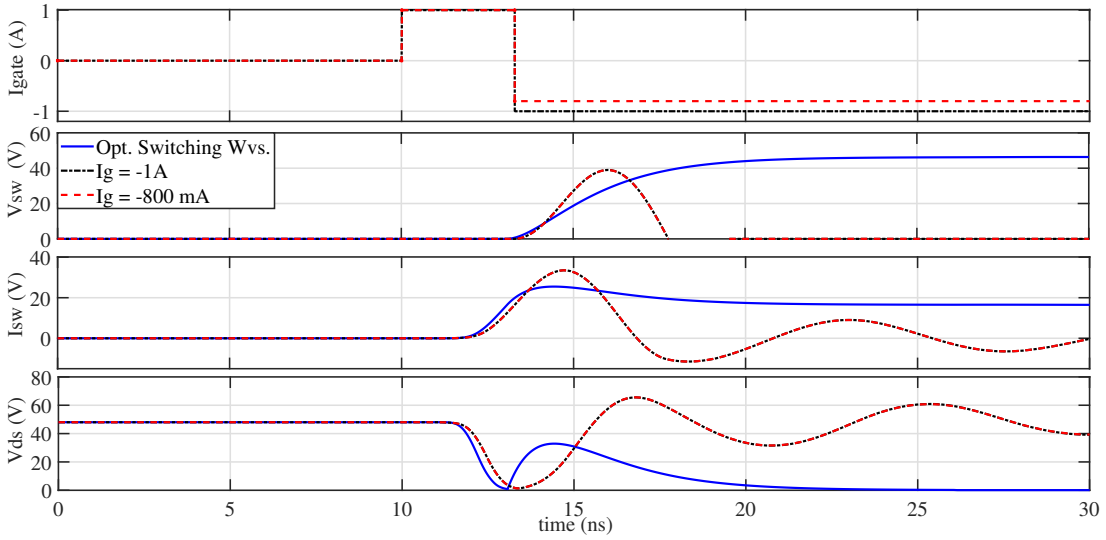

Figure 3.23: From step 6 to 7 of the proposed algorithm. Parametric simulation of the current level $I_{B,on}$. The comparison of the waveforms highlights that there is no matching between the optimal waves and the driver resulting ones.

At this point, by comparing V_{ds} against $V_{ds,opt}$, the step 3 of the algorithm can be executed, by detecting the first interval (t_i, t_j). More precisely, t_i is the first point in which the difference between $V_{ds,opt}$ and V_{ds} is greater than ϵ_1 and t_j is the first point in which the derivative of $V_{ds,opt}$ changes its sign. Accordingly, in step 4, the driver is set to change its output current at t_i, and the driver current is set to its maximum value as indicated in step 5.

Since the RMSEs can not be met whatever is the value of $I_{B,on}$ (step 6 and step 7), as shown in Fig. 3.23, t_i has to be brought backward as indicated in step 8. Figure 3.24 shows parametric simulations on t_i keeping constant the gate current, that corresponds to execute the loop from steps 6-8 several times. The

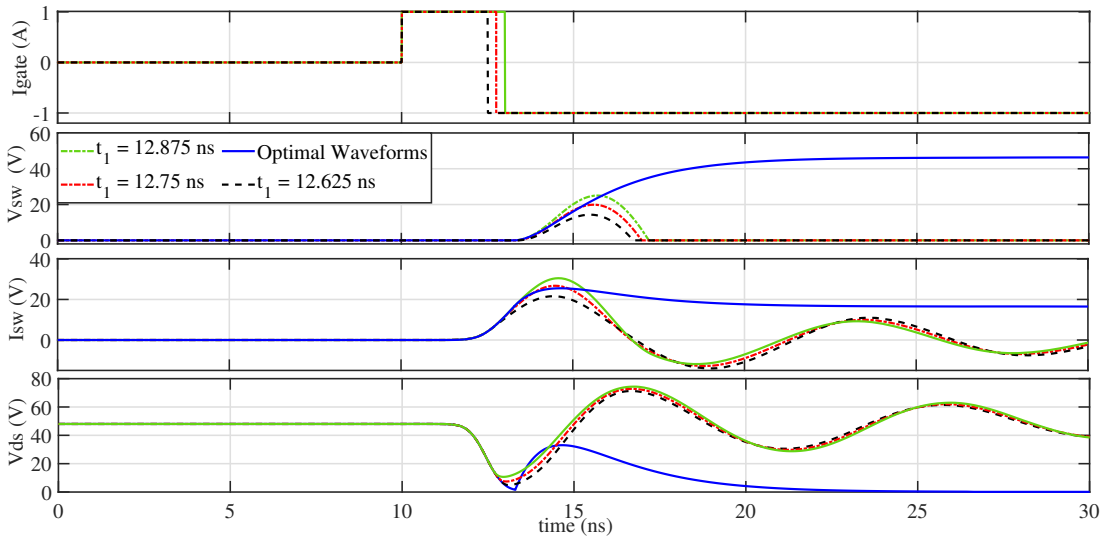

Figure 3.24: Step 8 of the proposed algorithm. Optimal switching waveforms (blue lines), compared with the ones resulting by simulations bringing forward the time instant t_1.

strategy of decreasing t_i allows one to reduce the RMSE, and the value of $t_1 = t_i$ and $I_{drv} = I_{B,on}$ satisfying the error criterion, can be found, eventually. Once that the (t_i, t_j) time interval is matched, the algorithm comes back to step 2, and a new time interval (t_i, t_j) is defined accordingly to step 3, as shown in Fig. 3.25.

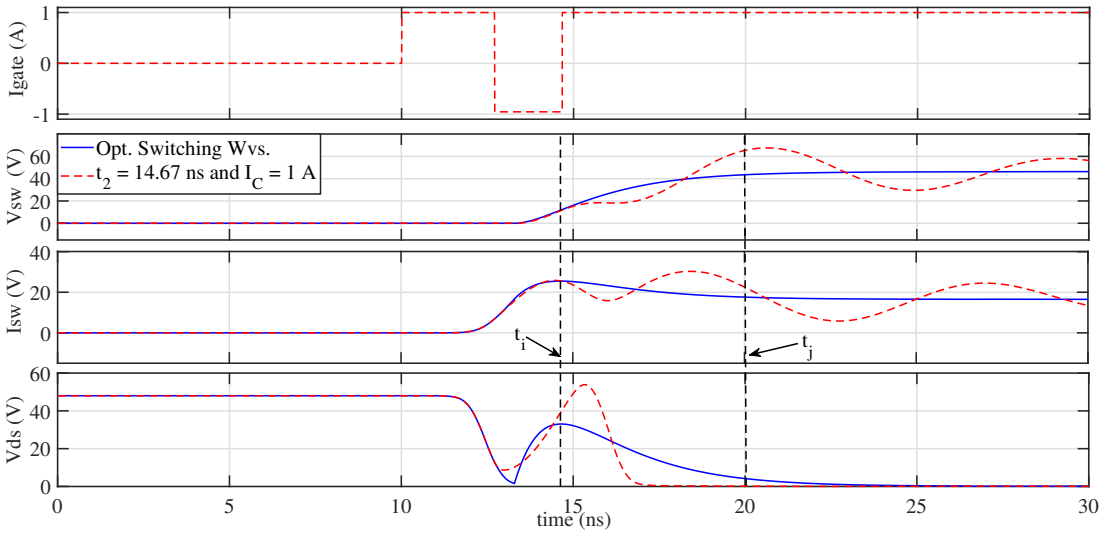

Figure 3.25: Steps 2 to 3 after the matching of the first time interval. The waveforms are in good agreement, until the V_{ds} derivative becomes negative again.

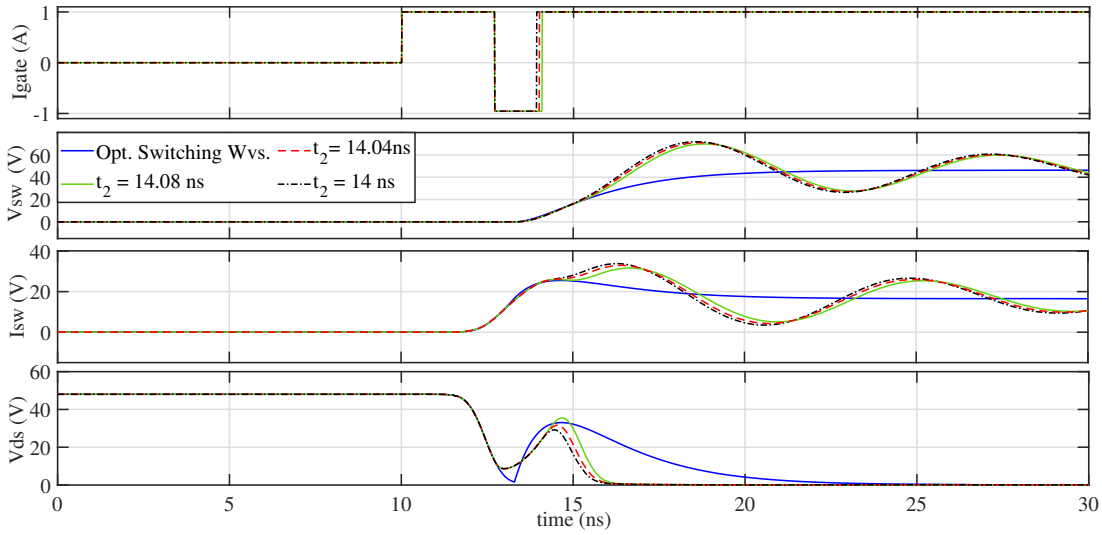

Figure 3.26: Effect of $R_t(t)$ and $G_t(t)$ on the switching waveforms at the turn-on and at the turn-off. The oscillating waveforms are shown by dashed dot lines, the ones with $R_t(t)$ and $G_t(t)$ are plotted by continuous lines.

By repeating the loop from step 6 to 7 several times, no suitable value of I_{drv} can be found to reduce enough the RMSE, thus, also in this case t_i has to be modified, as shown in Fig. 3.26. By executing steps 6-8, a proper pair of $I_{drv} = I_{C,on}$ and $t_i = t_2$ can be found, as shown in Fig. 3.27.

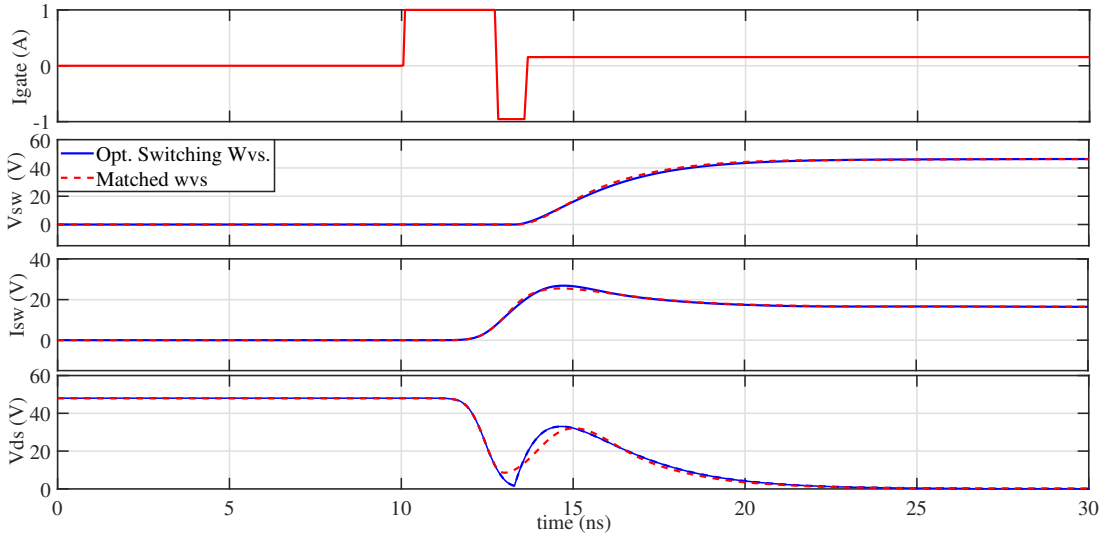

Figure 3.27: Step 6 to 7 of the algorithm. Looking for the time instant t_2.

An additional information regarding the current level $I_{A,on}$ results from (3.3). Since the slope of the rising I_{sw} current is not significantly affected by $I_{A,on}$, it

Table 3.3: Gate driver parameters for the turn-on and turn-off, equivalent model.

	Turn-on			**Turn-off**
	3-levels	4-levels (Case A)	4-levels (Case B)	3-levels
I_{A}	1 A	1 A	1 A	−1 A
$t_{1,1}$	//	12.35 ns	12.35 ns	//
I_{A1}	//	100 mA	100 mA	//
t_1	12.83 ns	12.83 ns	12.9 ns	17 ns
I_{B}	−800 mA	−533 mA	−800 mA	100 mA
t_2	13.88 ns	13.61 ns	13.47 ns	22 ns
I_{C}	133 mA	123 mA	133 mA	−43 mA

is possible to split the interval (t_0, t_1) into $(t_0, t_{1,1}), (t_{1,1}, t_1)$, where the current levels are $I_{\mathrm{A,on}}$ and $I_{\mathrm{A1,on}}$, respectively. Such approach, in which a four level gate driver is exploited, allows to increase the degree of freedom on the gate driver parameters. For instance, using $I_{\mathrm{A1,on}} < I_{\mathrm{A,on}}$ and keeping the same duration for the interval (t_0, t_1), the level $I_{\mathrm{B,on}}$ can be significantly reduced. Otherwise, if the level $I_{\mathrm{B,on}}$ is kept high, the interval (t_0, t_1) can be extended. The proposed gate current profiles, whose parameters are listed in Table 3.3, suggest that the optimal switching waveforms can be matched exploiting several shapes of gate current.

Algorithm for the optimal Turn-off

The turn-off gate current profile can be extrapolated using a similar approach to the one used for the turn-on. As stated in step 1 of the flowchart, the driver current

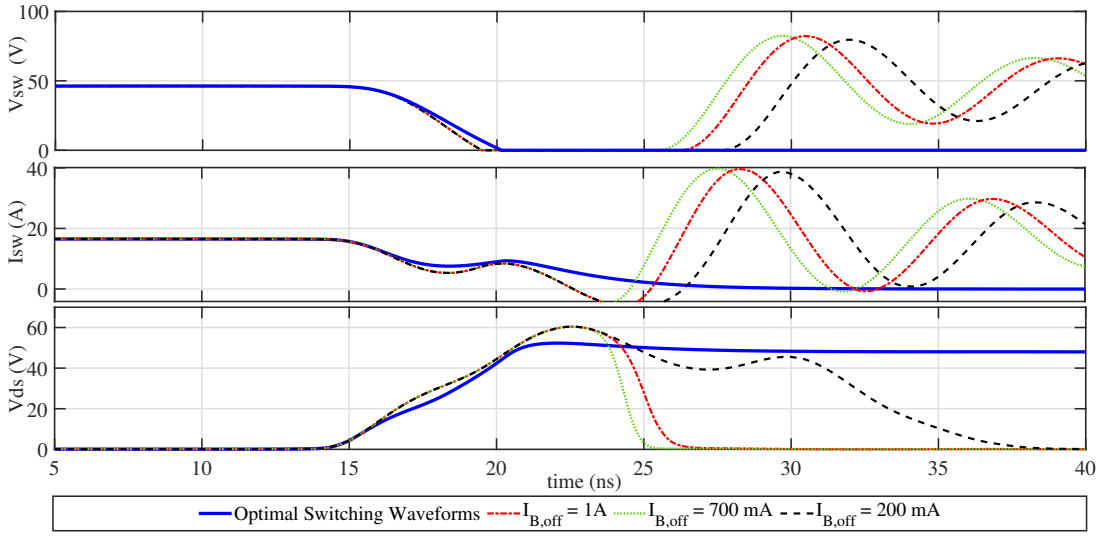

Figure 3.28: Turn-off algorithm: parametric simulation on the current $\mathrm{I_{B,off}}$.

is initially set to I_{min}, leading the V_{sw} to reach the negative threshold voltage of the diode (V_γ) promptly. Similarly to the turn-on, once the first time interval is defined, Fig. 3.28 shows that it is impossible to respect the error criterion modifying only the level $I_{B,off}$ of gate current, without bring forward the instant of time in which it is necessary to re-inject current in the power transistor.

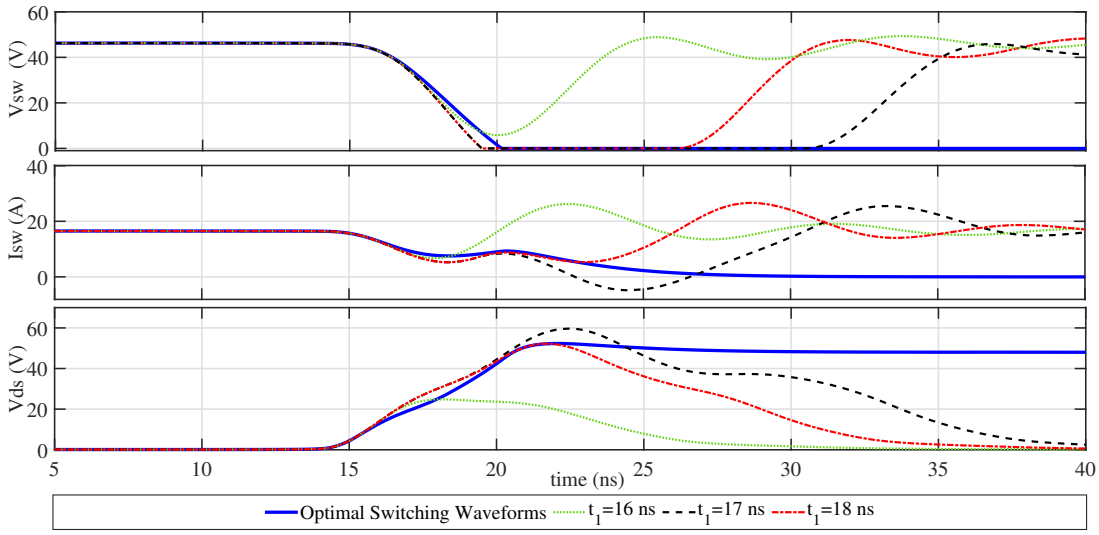

Figure 3.29: Turn-off algorithm: parametric simulations on the t_1.

By repeating steps the steps 6, 7 and 8 of the proposed algorithm, it is possible to find the proper values for t_1 and $I_{B,off}$ as shown in Fig. 3.29, in which the waveforms with $t_1 = 17$ns respect the error criterion. For such waveform, the value of the optimal $I_{B,off}$ is 100 mA.

Once the values of $I_{B,off}$ and t_1 has been established, it is possible to return to the step 2 of the algorithm, and subsequently to define the parameters t_2 and $I_{C,off}$ by changing the value of the third level of the gate driver (step 6 and 7). The resulting matched turn-off waveform are shown in Fig. 3.30 and the obtained driving parameters are listed in Tab. 3.3.

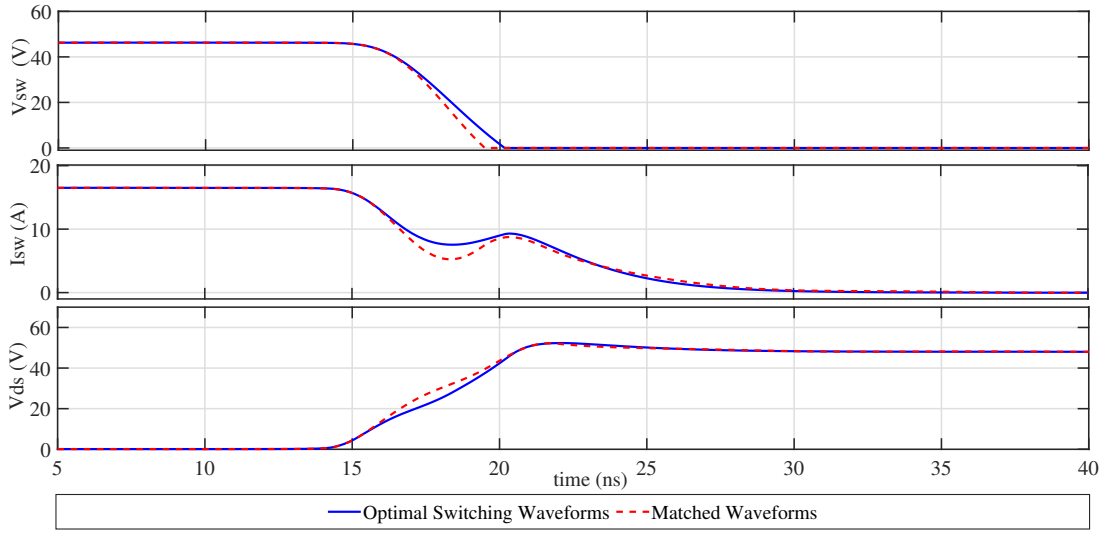

Figure 3.30: Turn-off algorithm: matched waveforms.

3.4.2 R_t and G_t in the complete circuit

The derived gate current profile exploiting the model of the real circuit cannot be used to reproduce the optimal switching waveforms on the complete circuit because, as deeply discussed in Chapters 1 and 2, the distribution of parasitic components in the circuit affects both the behavior of the power loop and the behavior of driving loop. Nevertheless, the R_t and G_t components, and the proposed algorithm for tuning the gate driver parameters can be used in the same way in the complete circuit for obtaining the optimal switching waveforms of the complete circuits and the parameters of the driver. In this situation the R_t and the G_t components are placed in series and in parallel to the real power switch respectively. In the complete circuit, with the real power transistor, it could happen that the R_t starts to work before that the V_{ds} has reached the zero level, so the optimal V_{ds} is partitioned between the transistor and the R_t. A similar consideration can be made for the optimal current at the turn-off. For such a reason, it is useful to define an equivalent power switch as the one shown in Fig. 3.31. The optimal $V_{ds,opt}$ at the turn on can be written as in Eq. 3.40 while the optimal $I_{sw,opt}$ at the turn off as in Eq. 3.41.

$$V_{ds,opt} = V_{ds} + V_{R_t} \tag{3.40}$$

$$I_{ds,opt} = I_{sw} + I_{G_t} \tag{3.41}$$

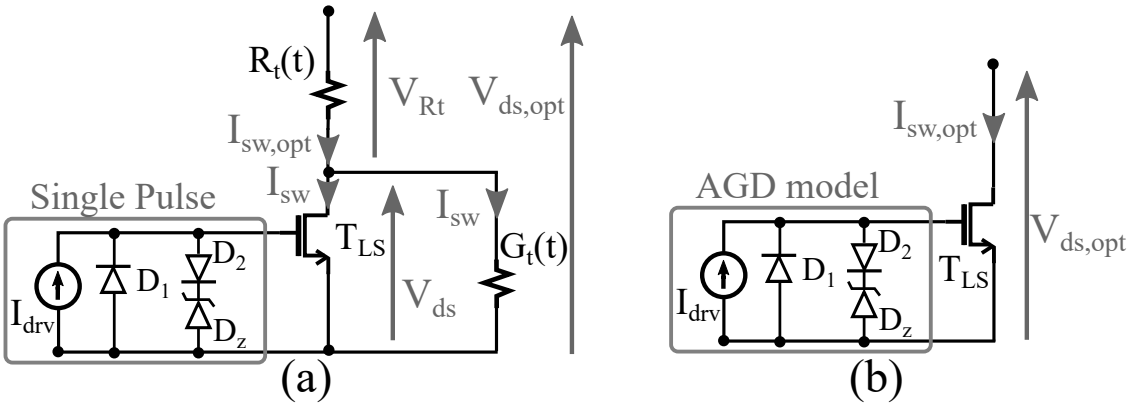

Figure 3.31: a) Equivalent transistor with R_t and G_t. b) Power transistor driven with the AGD for reproducing the optimal switching waveforms.

3.5 Analysys of the Real Circuit

Aiming to check the correctness of the proposed approach, the R_t and G_t elements ar placed is series and in parallel respectively, to the power transistor of the complete circuit shown in Fig. 3.1. As long as the low side switch is driven sharply, the resulting switching waveforms, i.e., I_{sw}, V_{sw}, V_{ds}, are affected by unwanted oscillations as shown by the dashed lines in Fig. 3.32 both after the turn-on and the turn-off. The oscillation frequencies at the turn on and turn off as well as the load current are the same of the equivalent circuit used to derive the mathematical analysis, but the optimal switching waveforms are not the same of the equivalent circuit because the distribution of the parasitic elements affects their behavior. Indeed, the complete circuit shows a higher order frequency response that affects the behavior of the circuit during the transients. Based on that, the optimal waveforms were derived from the analysis of the circuit comprising the additional elements R_t and G_t as discussed in section 3.4.2. Then, the tuning algorithm, presented before, was executed for the turn-on and for turn-off, resulting in the AGD parameters listed in Table 3.4. The corresponding switching waveforms are shown in Fig. 3.33

Table 3.4: Gate driver parameters of the complete circuit.

	t_0(ns)	I_0(A)	t_1(ns)	I_1(A)	t_2(ns)	I_2(mA)	t_3(ns)	I_3(mA)
Turn on	10	1	13.78	−0.9	15.63	291	17	427
Turn off	10	−1	17.25	0.1	21.58	−10	//	//

(dashed-dot lines) along with the optimal ones (continuous lines) and with the current levels and the time instants obtained from the proposed algorithm. The obtained results are in good agreement with the optimal switching waveforms.

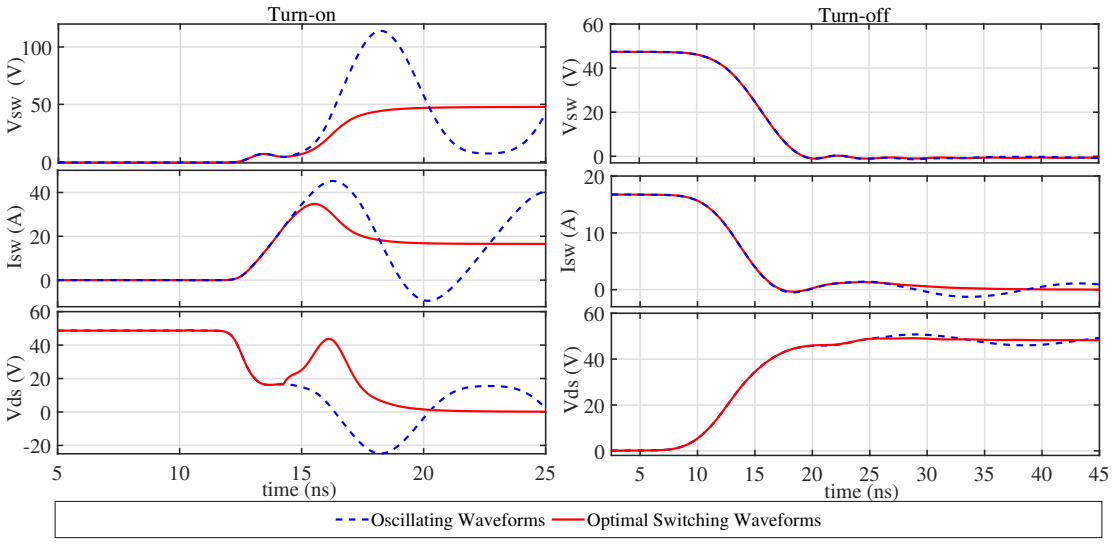

Figure 3.32: Comparison between the oscillating waveforms resulting by simulating the complete circuit (dashed lines) and the ones resulting by exploiting the R_t and the G_t.

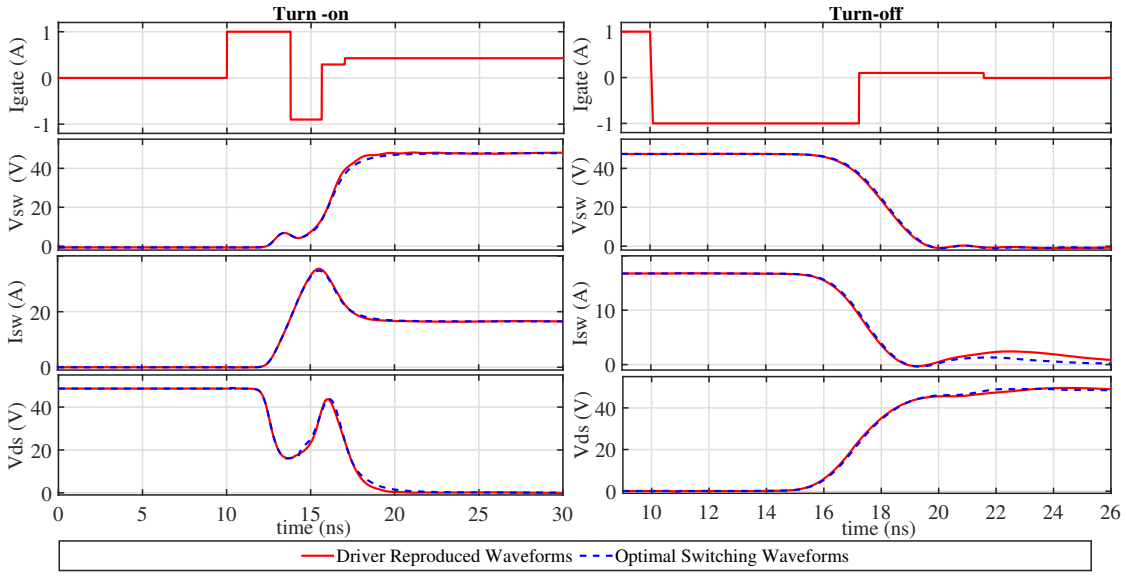

Figure 3.33: Comparison between the optimal switching waveforms at the turn-on and the turn-off with the ones resulting exploiting the AGD parameters reported in Tab. 3.4.

3.5.1 Sensitivity Analysis

To investigate the impact of the driver parameters on the switching waveforms, parametric simulations were carried out referring to the parameters listed in Table

3.4. The variation of the current levels $I_{A,on}, I_{B,on}, I_{C,on}, I_{D,on}$ by $\pm 2.5\,\%$ resulted in

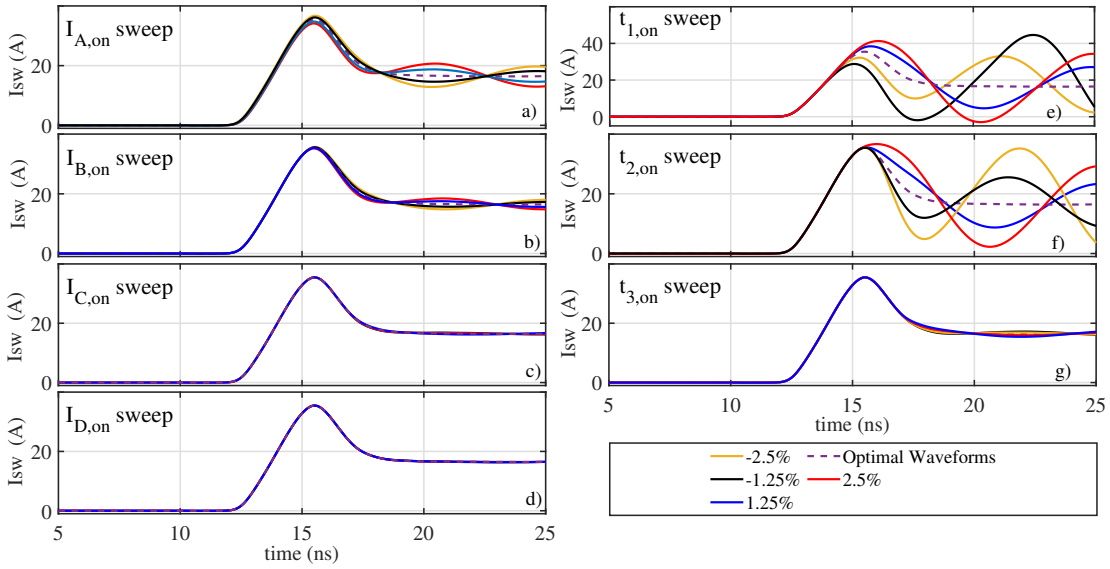

Figure 3.34: Sensitivity Turn-on analysis: (a) parametric simulations on the $I_{A,on}$, (b) on $I_{B,on}$, (c) on $I_{C,on}$, (d) on $I_{D,on}$, (e) on t_1, (f) on t_2 (g) on t_3.

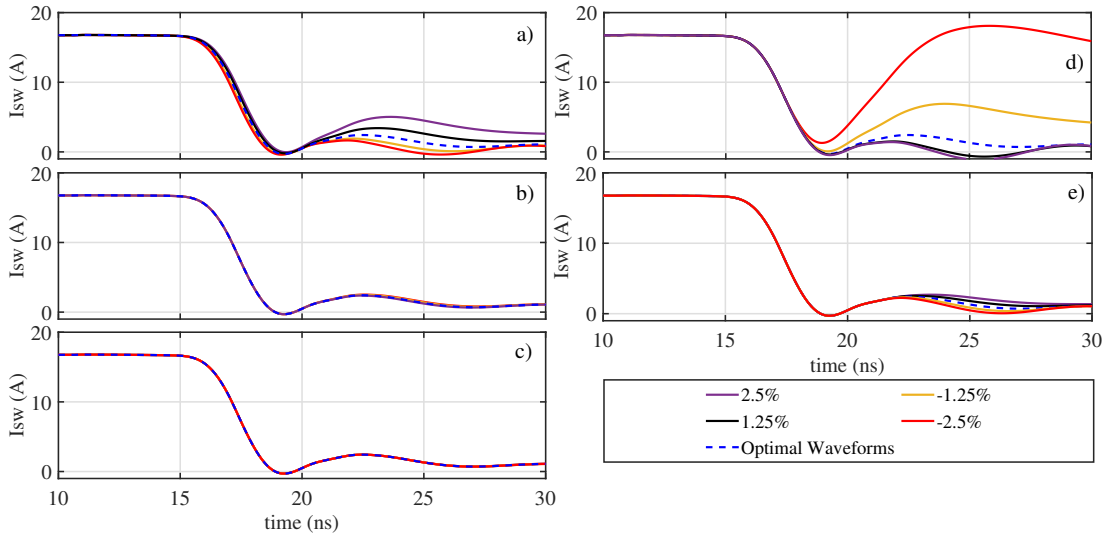

Figure 3.35: Sensitivity Turn-off analysis: (a) parametric simulations on $I_{A,off}$, (b) on $I_{B,off}$, (c) on $I_{C,off}$, (d) on the t_1, (e) on the t_2.

oscillations as sketched in Fig. 3.34(a,b,c,d). Furthermore, it is worth mentioning that the first current level is the most critical, since it causes wider oscillations. Similarly, the plots in Fig. 3.34(d,e,f) show the impact of $\pm 2.5\,\%$ variation of

$t_{1,on}, t_{2,on}, t_{3,on}$ on the switching waveforms. It can be noticed that the switching waveforms are more affected by the variations of $t_{1,on}$ and $t_{2,on}$. Sensitivity analysis was also performed at the turn off obtaining similar results, shown in Fig. 3.35. As a consequence, such strong dependence on the driver parameters points out again the benefits of a methodology to tune of such values; thus, the trial-and-error process should be definitely avoided. Furthermore, it has been found that the time instant variations affect more the switching waveforms than the current level variations. This is highlighted by the plots shown in Fig. 3.34(e) ($t_{1,on}$ variation) and Fig. 3.34(f). Indeed, the variation of the first time instant affects both the charge $Q_{A,on}$ and $Q_{B,on}$, i.e., both the charge injected into and sunk from the gate terminal, whereas the variation of $I_{A,on}$ or $I_{B,on}$ affects only one of them.

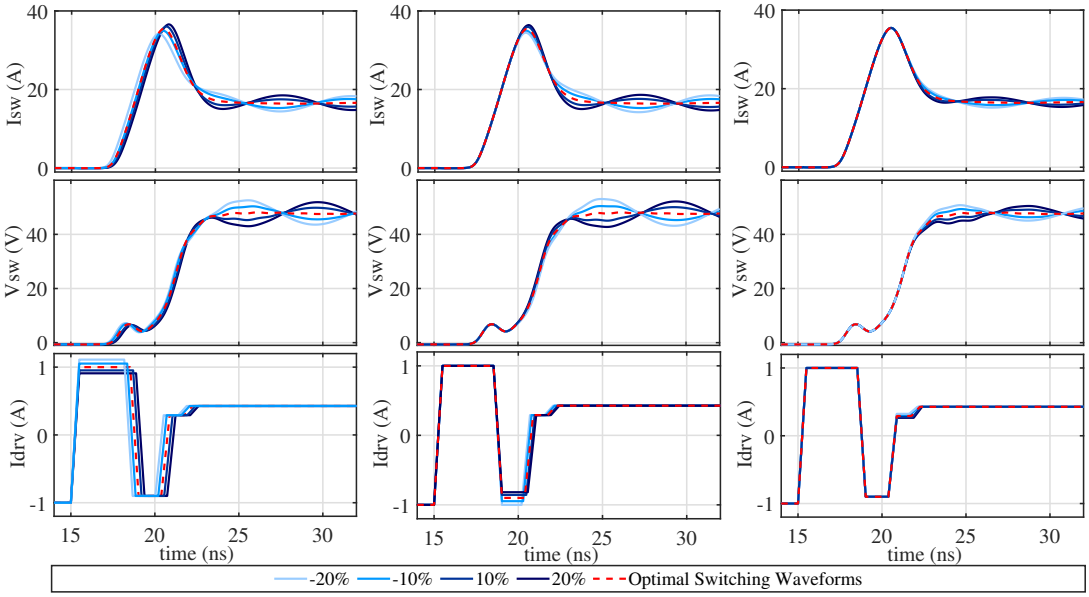

Figure 3.36: Parametric simulation keeping constant the level of the charges $Q_{A,on}$, $Q_{B,on}$ and $Q_{C,on}$.

Based on that, the sensitivity of the switching waveforms to the variation of gate current profile was investigated keeping the charge injected (sunk) into (from) the gate $Q_{A,on}$ ($Q_{B,on}$) at the turn on. The analysis provided the results shown in Fig. 3.36 and in Fig. 3.37. In particular, the plots in Fig. 3.36(a) have been obtained with a variation of $I_{A,on}$ and $t_{1,on}$ of $\pm 20\%$ around their respective nominal values, Fig. 3.36(b) by varying $I_{B,on}$ and $t_{2,on}$, Fig. 3.36(c) with the variation of $I_{C,on}$ and $t_{3,on}$. In all these cases, the ringing amplitude is lower than in the case of a time variation only, as shown in Fig. 3.34(d,e,f). Also a simultaneous variation of all the aforementioned parameters has been simulated, as shown in Fig. 3.37(a). This points out that a relation between the switching waveforms and the amount of injected (sinked) charge in (from) the gate exists, resulting in some degree of

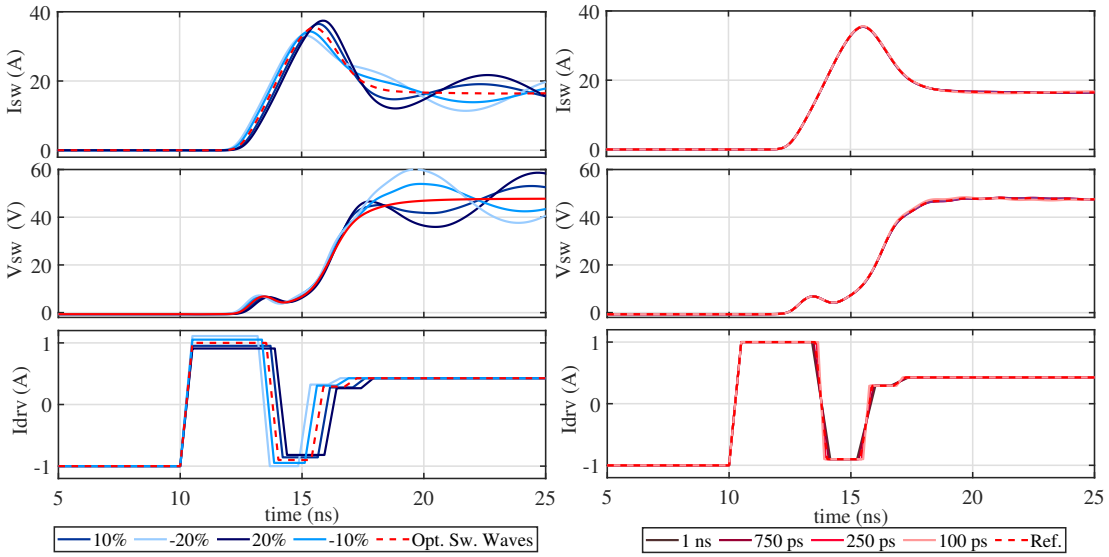

Figure 3.37: Parametric simulation changing all the charge values and the slopes of the gate current.

freedom on the current driver profile.

Finally, the case of a non-zero slope in the driver current profile has been considered, as shown in Fig. 3.37(a), where the rise and fall time have been changed from 100 ps to 1 ns. As a results, the switching waveforms have been negligibly affected, assessing the effectiveness of the proposed methodology when a non-ideal AGD will be exploited. This last analysis is in agreement with the the one reported in [40], in which the optimal switching waveforms are reproduced at the turn-on exploiting saw-tooth gate current waveforms, that can be seen as square waves with very slow slopes.

3.5.2 Comparison with Standard Solution

In order to assess the advantages of the proposed methodology in terms of ringing suppression and power loss reduction, a comparison with undamped and traditional solutions was carried out. As far as the complete converter shown in Fig. 3.1 is concerned, the switching waveforms, corresponding to the turn-on of the high side transistor driven sharply, are shown in Fig. 3.32(a) by dashed lines. It is worth noticing that the oscillations leads the power transistor to conduct reversely and increase the level of the electromagnetic emission delivered by the converter, therefore a damping technique is required. In order to address such issue, the standard solution consists in the use of snubbers. Thus, a low side RC snubber, in parallel to the free-wheeling diode, and a high side RC snubber, in parallel to the power switch, were later included with the aim to suppress the oscillations at the

turn-on and at the turn-off as introduced in Chapter 1. The snubber components, are $C_{\text{snub}-\text{l}} = 4\,\text{nF}$ and $R_{\text{snub}-\text{l}} = 1.5\,\Omega$ and $C_{\text{snub}-\text{h}} = 4\,\text{nF}$ and $R_{\text{snub}-\text{h}} = 2\,\Omega$. The results of the simulations of the buck converter comprising the snubbers and a gate driver output resistance of $R_{\text{g}} = 18\,\Omega$, are shown in Fig. 3.38 by dashed-dot. The

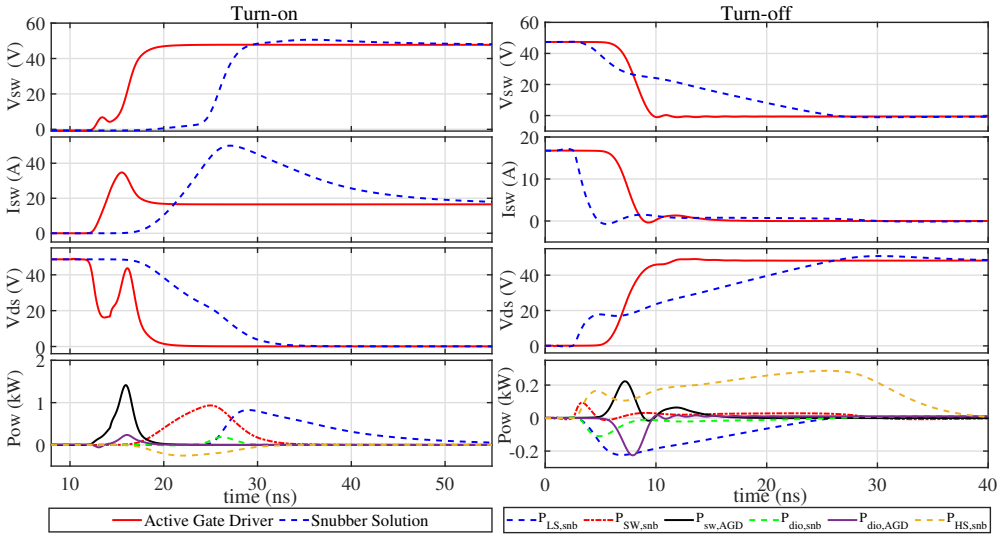

Figure 3.38: Comparison between the switching waveforms resulting by using the snubber and the proposed driving technique.

continuous lines were obtained from the analysis of the same circuit driven by the tuned AGD. In both cases the oscillations were found to be damped effectively, but those obtained with the RC snubbers show longer switching time and higher power losses. Similar results were obtained at the turn-off, since the tuned AGD solution outperformed the snubbered ones in terms of both power dissipation and switching time. By comparing only the power dissipated by the transistor, it results that the AGD solutions seems to be more dissipative than the snubber solution, but it is important to consider that there are also the power dissipated in the snubbers, that make the snubber solution more dissipative than the AGD one. The figures of merit shown in Table 3.5 highlight the best performance of the AGD solution. The following parameters are considered: the power dissipated by the high side switch (P_{sw}), by the low side diode (P_{diode}), by the snubbers ($P_{\text{lsnb}}, P_{\text{hsnb}}$) and the sum of them ($P_{\text{tot}}$). Furthermore, the peak values of the switching waveforms (V_{sw_p}, V_{ds_p}, I_{sw_p}) were also considered, as well as the conversion efficiency (η) of the circuit. The results obtained from the analysis carried out for the two solutions, along with the oscillating case, are listed in Table 3.5. In the case of undamped waveforms (Table 3.5(a)), the total power dissipation is the lowest, however, it should be noticed that the converter is not of any practical interest because of the self-turn-off phenomenon occurring during the turn-on. Comparing the last three solutions in Table 3.5, it comes out that both (b) and (c) dissipate more power than the AGD

Table 3.5: Comparison between (a) oscillating, (b) snubber with $R_g = 18\,\Omega$ and (c) proposed technique.

	P_{sw}	P_{diode}	P_{lsnb}	P_{hsnb}	P_{tot}	V_{swp}	V_{dsp}	I_{swp}	η
(a)	1.11 W	7.7 W	//	//	8.8 W	115 V	53.8 V	45.2 A	92.2%
(b)	7.65 W	7 W	5.5 W	4.8 W	24.95 W	53 V	51 V	50 A	83.5 %
(c)	4.6 W	7.3 W	//	//	11.8 W	47.7 V	49 V	34.7 A	91.5%

driven solution (d). From their comparison it results that the total power dissipated by the circuit based on the AGD driven to provide the output with the optimal switching waveforms is about 50% less. Similarly, also the conversion efficiency of the buck converter benefits from the tuned AGD, since it increases of more than 5 % with respect to the snubbered solutions.

3.5.3 Load Current Variation

The previous results assess the proposed method both in terms of oscillation damping and reduction of switching losses with respect to traditional solutions. In this subsection, a parametric simulation on the load current has been performed with the aim to check if the tuned gate driver parameters can still reproduce the optimal switching waveforms. Figure 3.39 shows how the V_{sw} behavior changes,

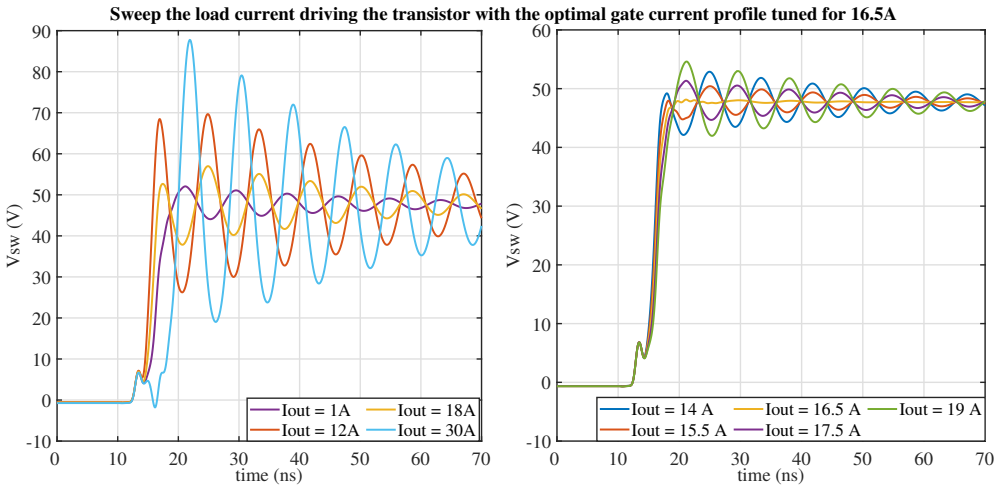

Figure 3.39: Voltage V_{sw} resulting by stepping the load current. The power transistor is driven exploiting the optimal parameters tuned for 16.5 A.

resulting in oscillating waveforms. More precisely, the amplitude of the oscillations increases with larger variations of the load current with respect to 16.5 A, the reference value used to tune the parameters of the gate driver.

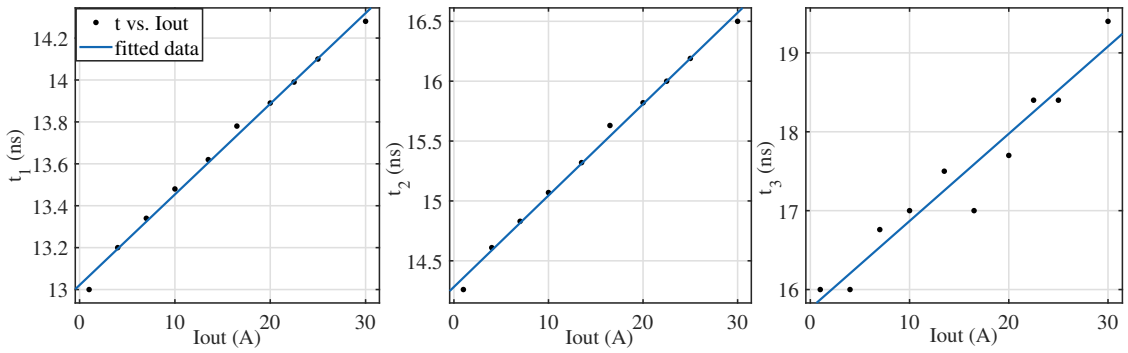

Figure 3.40: Optimal time parameters obtained by using the algorithm for different load current levels (black dot) and the best fitting waveforms (blue solid lines).

At this point, the optimal switching waveforms were evaluated for different load current value, and the tuning algorithm was applied to identify the optimal parameters for all such conditions. This analysis was performed keeping the value of the currents $I_{A,on}$, $I_{B,on}$, $I_{C,on}$ and $I_{D,on}$ equal to the ones obtained in the nominal case, for all the load currents. The optimal parameters are shown in Fig. 3.40 by black dots. This time values can be approximated with a linear function as shown by the solid lines in Fig. 3.40. The resulting expressions for $t_{1,on}$, $t_{2,on}$, and $t_{3,on}$

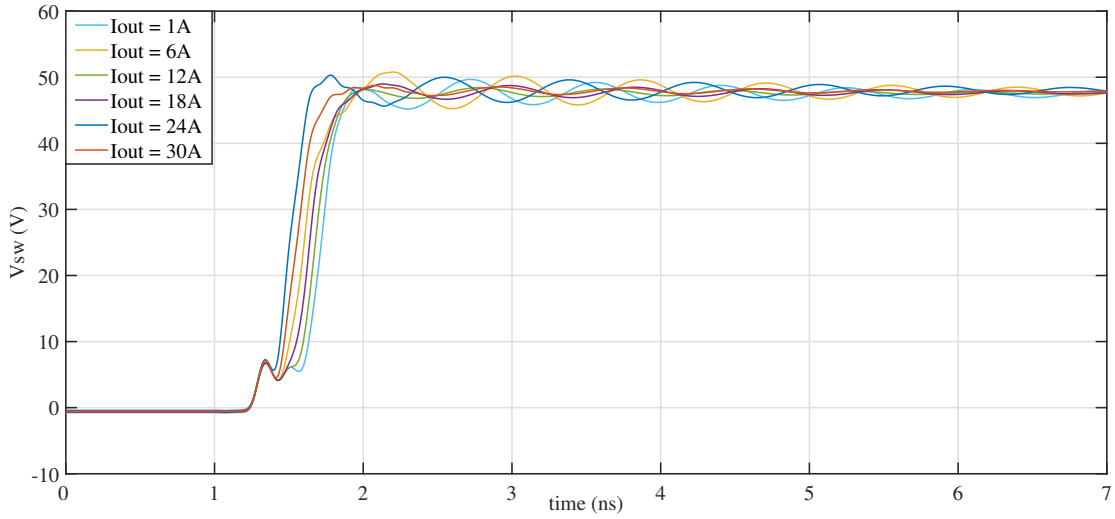

Figure 3.41: Voltege V_{sw} resulting by stepping the load current. The transistor is driven by exploiting time parameters resulting by the equations in 3.42.

are reported in 3.42 and the voltage V_{sw} resulting by stepping the load current from 1 A to 30 A with the gate driver time parameters regulated exploiting such

equations are shown in Fig. 3.41.

$$\begin{aligned} t_{1,on} &= 43.26\,ps/A \cdot I_{out} + 13.02\,ns \\ t_{2,on} &= 76.32\,ps/A \cdot I_{out} + 14.28\,ns \\ t_{3,on} &= 110.7\,ps/A \cdot I_{out} + 15.76\,ns \end{aligned} \tag{3.42}$$

It is worth to be noticed that the amplitude of the oscillations are significantly reduced if compared with the ones shown in Fig. 3.39, in which the gate driver parameters were the optimal found for the load current 16.5 A.

Chapter 4

Experimental validation

In this chapter, the methodology proposed in section 3 is validated by means of an experimental setup, analyzing its pros and the cons, and highlighting the challenges that have been addressed during the implementation of such technique, exploiting a real AGD. A low side buck converter was considered as case of study. Firstly, a simplified model of this converter was derived by means of experimental measurements in order to obtain a circuit on which to apply the proposed technique, and then the optimal switching waveforms have been evaluated by means of a time domain simulation of the circuit that includes the R_t component. At this point, using an ideal current source, the optimal gate current profile was derived by means of the proposed algorithm, and then, after the characterization of the AGD, this current profile was reproduced with the real AGD and used to drive the low side transistor of the real buck converter, validating the proposed methodology. In order to deepen and further investigate the obtained results, a comparison of the measured switching waveforms with the ones obtained by means of simulations is carried out, highlighting the negative effects that a model mismatch could produce when using this technique, but also proposing a method to overcome these issues.

Once that the optimal gate current profile was picked out, the proposed technique is compared with the traditional RC snubber solution to confirm that, with the resulting equivalent parasitic components and the proposed chosen operating conditions, the AGD allows to dissipate less power than the RC snubber solution, resulting in the best compromise between oscillation and dissipated power. Finally, a parametric analysis of the sensitivity on the time parameters of the AGD is performed, as well as on the load of the buck converter, assessing the simulation obtained results.

4.1 Analysis of the Prototype

The prototype used to check the effectiveness of the proposed methodology is a low side buck converter, whose schematic is shown in Fig. 4.1. This converter

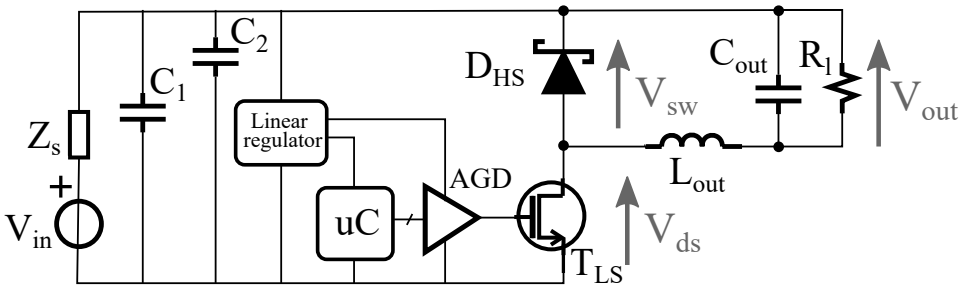

Figure 4.1: Schematic of the buck converter used to assess the effectiveness of the proposed technique.

works at 100 kHz with a fixed duty cycle, because no control on the output voltage is required for the purposes of this thesis. The converter is designed to properly work when the input voltage V_{in} changes in a range between 20 V and 50 V and, to provide the load with a minimum current of 0.1 A and a maximum current of 5 A. A picture of this converter is shown in Fig. 4.2.

Since the aims of this work are to check the effectiveness of the proposed method to tune the parameters of an AGD and to verify the correctness of the proposed mathematical model on a real circuit, for the sake of simplicity, a low side buck converter is used. In fact, this topology makes it easier for the user the design and the control of the gate driver, because it is possible to avoid the use of level-shifters or optocouplers, that otherwise would be required for an high side traditional topology. Moreover, in order to avoid synchronization issues, a power diode is used as high side switch. These two choices do not affect the proposed analysis, because the optimal switching waveforms do not depend neither on the topology of the converter, nor on the type of freewheeling switch, but only on the distribution of the parasitic components and on their values. In fact, the optimal waveforms ca be obtained also using an enhancement switch, without using a sophisticated driving technique, but also exploiting a simple turn-on/turnoff of the device in parallel with the load.

An other important point concerns the AGD mounted on the board, that includes only discrete components, thus it is not characterized by a high speed and its performance is not comparable with the one offered by an integrated AGD like the one proposed in [31]. For such a reason, both the freewheeling diode and the low side enhancement transistor have been chosen paying particular attention to the value of their parasitic capacitances. More precisely, these components have been selected with a high value of parasitic capacitances. In this way, the discrete AGD

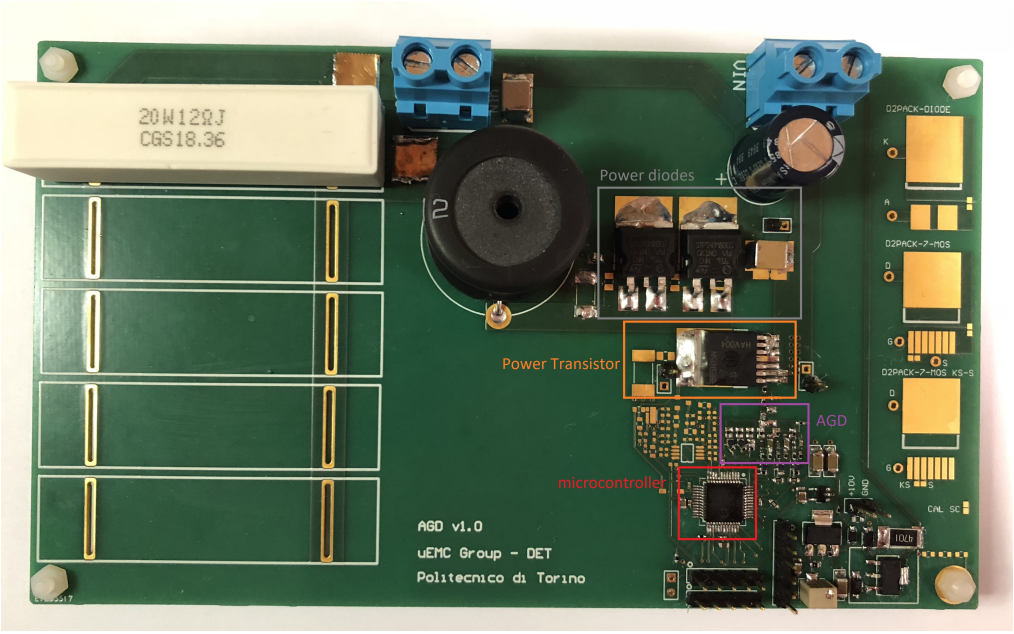

Figure 4.2: A picture of the buck converter used for the experimental validation of the proposed technique. In the red rectangle is shown the microcontroller, in the grey one the power diodes, while in the orange and violet ones, the power transistor and the AGD, respectively.

used to test the effectiveness of the proposed approach, is fast enough to control the switching waveforms of the analyzed converter, without encountering frequency response issues.

This approach is sustained by the simulation analysis reported in Chapter 3, in which is demonstrated that the optimal switching waveforms do not depend on the transistor speed. In fact, the R_t and G_t approaches are validated exploiting ideal switches, but for shaping their trajectory an high performance AGD should be used. In the case of study, the limited speed performance of the proposed AGD has led to test the discussed technique on slow devices, but with a better AGD, it would have been possible to use in the same way the proposed approach on faster devices.

4.2 Building the equivalent model of the circuit

The layout of the board used to assess the effectiveness of the method is shown in Fig. 4.3. As can be seen, this layout does not comply with the traditional rules to reduce the EMI, because the board was designed with the aim to obtain oscillations superimposed to the ideal switching waveforms and with a well designed geometry, in order to simplify the detection and the evaluation of each parasitic

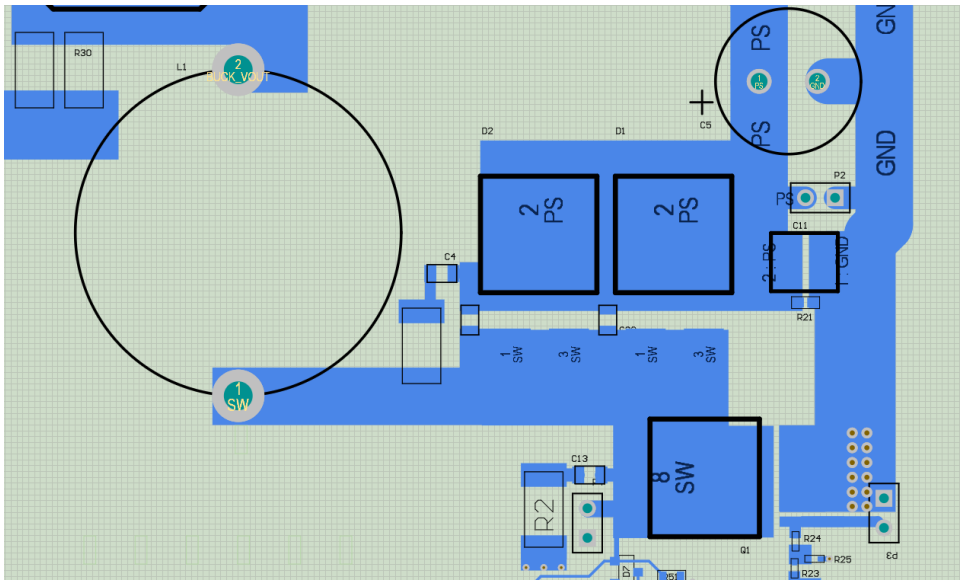

Figure 4.3: Layout of the buck converter focused of the power loop.

contribution. Indeed, all the components of the circuit are placed on the top of board to avoid the use of vias, and the power loop is drawn with a simple rectangular geometry and with properly located pads that allow the user to take measurements of the power loop impedance by means of a network analyzer. More precisely, in order to simplify the model implementation, all the components, except the power transistor, are placed on the board and the power loop impedance was measured between the drain and the source pads of the board with the diode biased to the voltage V_{in}. The results of such measurement is shown in Fig. 4.4. The measurement results evidence a capacitive behavior of the power loop for frequencies lower than 10 MHz and an inductive behavior for frequencies higher then 40 MHz. A resonant peak can be observed when the frequencies is equal to 31.5 MHz. The low frequency results can be used to calculate the values of the capacitance $C_{p,eq1}$ while the resonant frequency allows the user to evaluate the value of the parasitic inductance $L_{p,eq}$. More precisely, it is possible to calculate the value of $C_{p,eq1}$ a low frequency point where the admittance behavior is mainly capacitive, exploiting the following equation:

$$C_{p,eq1} = \frac{|Y(j2\pi f_{low})|}{2\pi f_{low}}. \tag{4.1}$$

Furthermore, the value of $L_{p,eq}$ can be evaluated exploiting the measured resonant frequency f_{res} by means of Eq:

$$L_{peq1} = \frac{1}{4\pi^2 f_{res}^2 C_{peq1}}. \tag{4.2}$$

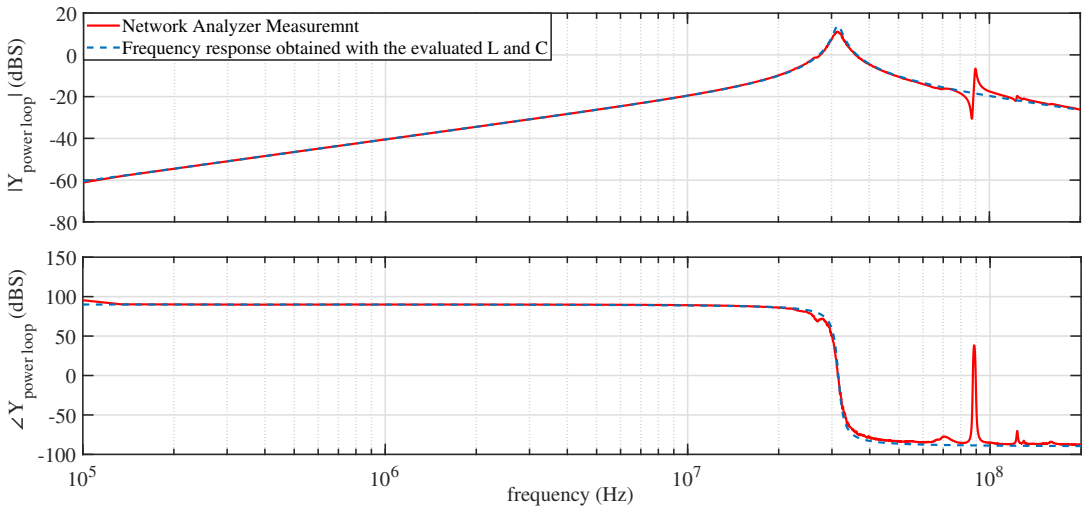

Figure 4.4: Power loop admittance of the board obtained with a network analyzer characterization.

For the analyzed board, the value of $C_{p,eq1}$ is approximately 1.5 nF while $L_{p,eq}$ is about 16.7 nH, since f_{res} results to be 31.5 MHz. The dashed line in Fig. 4.4 represents the admittance trend obtained placing in series these two elements, showing a good agreement between the measurements and model results.

At this point, the converter was completely mounted, and the turn-on switching waveforms are acquired, with the aim of matching them with the ones resulting from simulations. In this preliminary phase, the AGD, whose schematic is shown in Fig. 4.7, is used as a common gate driver exploiting only one of its three legs. Detailed information about the AGD circuits will be provided in Section 4.3. Table 4.1 reports all the information about the components which make up the converter and its operating conditions.

Table 4.1: Component values of the designed converter.

Parameter	Value	Parameter	Value	Parameter	Value
C_1	100 μF	V_{out}	6 V	V_{in}	24 V
C_2	2.2 μF	R_l	12 Ω	L_{out}	220 μH
T_{LS}	[45]	D_{HS}	[46]	M_1, M_2, M_5, M_6	[47]
M_3, M_4	[48]	R_{p1}	20 Ω	R_{p2}	28 Ω
R_{p3}	39 Ω	R_{p4}	56 Ω	R_{on1}, R_{on3}	4.7 Ω
R_{on2}, R_{off1}	0 Ω	$V_{dd,drv}$	10 V	R_g	0.5 Ω

At this point, the complete model of the analyzed converter is build in simulation environment with the aim of matching the measured oscillating switching waveform with the ones resulting from measurements. In such a way, after that, the optimal

switching waveforms have been evaluated, exploiting the R_t component, the tuning algorithm can be applied, making the chances of success much better. In order to

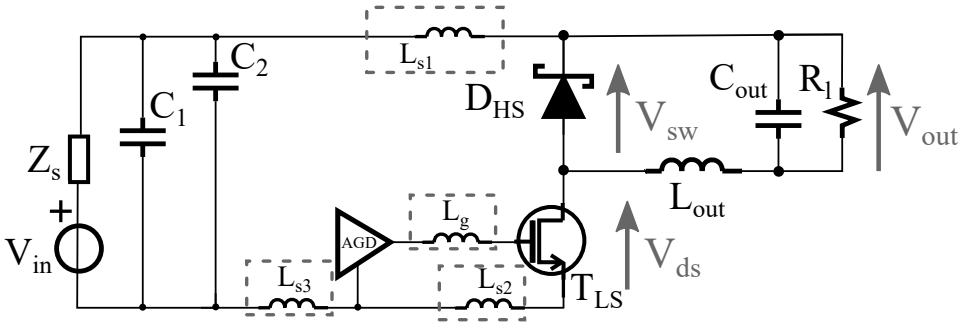

Figure 4.5: Schematic of the buck converter with the distributed parasitic inductances

perform such operation, the V_{ds} and the V_{gs} are measured on the prototype and the parasitic $L_{p,eq}$ has been distributed in the power loop taking into account the inductive contribute of the DC link capacitors and the portions of source, drain and gate inductances yet included in the transistor model. The inductance $L_{p,eq}$ is distributed as shown in Fig. 4.5 and parametric simulations on the values of such components are performed to obtain the best matching between the measured and simulated waveforms.

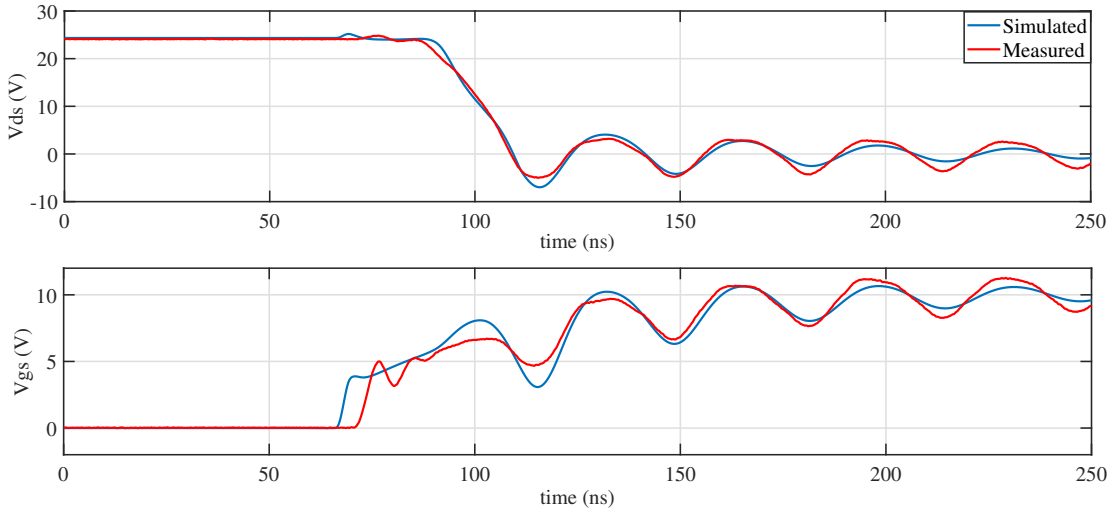

Figure 4.6: Comparison between the oscillating waveforms (V_{ds} and V_{gs}) obtained with measurements (red lines) and simulations (blu lines).

The simulations are performed by keeping constant and equal to 17.6 nH the value of the total inductance. The comparison between the well matched obtained waveforms are shown in Fig. 4.6. These waveforms have been obtained

with $L_{s1} = 9.3\,\text{nH}$, $L_{s2} = 2\,\text{nH}$ and $L_{s3} = 3.5\,\text{nH}$. The others 2.8 nH are inside the model of the power switch, more precisely 1 nH in series with the drain and 1.8 nH with the source. On the gate of the device, in addition to the 4 nH already existing in the model, further 5 nH were placed between the gate and the driver to match the waveforms.

4.3 Active Gate Driver

In this section, a description of the designed AGD is provided. This driver includes only discrete components and can source and sink three different levels of positive and negative current. The proposed AGD is not a current modulation driver, but it allows to change the gate resistance during the transition of the switching waveforms. The choice of this topology is based both on the straightforwardness of the design with respect to a current modulation one, and to validate the effectiveness and the practicability of the proposed technique exploiting any type of AGD. Further it should be kept in mind that, during the Miller plateau, the gate voltage is approximately constant, so the current injected/sunk in/from the gate of the transistor can be considered constant also using a resistance modulation driver. For the sake of simplicity, in this thesis only the turn on of the T_{LS} transistor is experimentally validated using the proposed gate driver, whose schematic is shown in Fig. 4.7. As stated before, the proposed gate driver allows

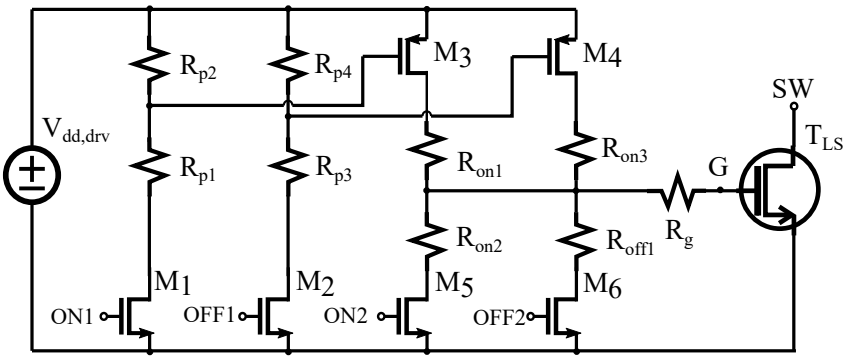

Figure 4.7: Schematic of the proposed gate driver.

the user to turn-on the power transistor using only one of its legs, so as a traditional gate driver with a series gate resistor, but also exploiting all the legs with a sequence of three pulses, the first and the third ones positive, while the second one negative. All the transistors that make up the driver are used as switches, so they could be opened or closed. More precisely, the low side transistors M1 and M2 control the high side p-mos transistors M3 and M4 capable to connect the gate to driver power source through the two resistances $R_{on,1}$ and $R_{on,2}$ respectively, while M5 and M6 can connect the gate of the power transistor to ground through

the resistances $R_{off,1}$ and $R_{off,2}$. The control signals ON_1, ON_2, OFF_1 and OFF_2 are provided by a microcontroller. This means that these signals can be modeled with a PWL that can switch between $0\,V$ and $3.3\,V$ with an output resistance of about $100\,\Omega$. The characteristics of the PWL signal allow to define the first set of specifications for the low side transistors of the driver. The threshold voltage must be lower than 2 V and the device should be in deep triode with V_{gs} equal to 3.3 V. Furthermore, in order to keep the propagation delay lower than 10 ns, and to have a fast turn on, the capacitance should be lower than 100 pF. These specifications can be met only using GaN transistors, because there are not n-mos devices capable to comply with these needs. Instead, for the high side device, p-mos transistors are chosen because p-channel GaN device are not commercially available. Luckily, p-mos devices are faster than their n-type counterpart. The value of the resistances R_{on1}, R_{on2} and R_{off1} are chosen according the current levels obtained as the output of the algorithm, while R_{p1}, R_{p2}, and R_{p3}, R_{p4} are sized to speed up the turn-off of M3 and M4 when the signals ON1 and ON2 are down and, at the same time, to limit the current in M1 and M2 when these two devices are on.

4.3.1 Gate Driver Characterization

The first prototype of the AGD has been characterized in order to evaluate its performance. More precisely, the proposed AGD shows some delay between the instant of time in which the microcontroller sends a command and its output response. Such delays should be measured in order to consider their effects when the tuning algorithm will be applied exploiting the ideal driver. In other words, the ideal optimal parameters provided by the tuning algorithm have to be adjusted considering the time delays obtained by means of such characterization. In order to

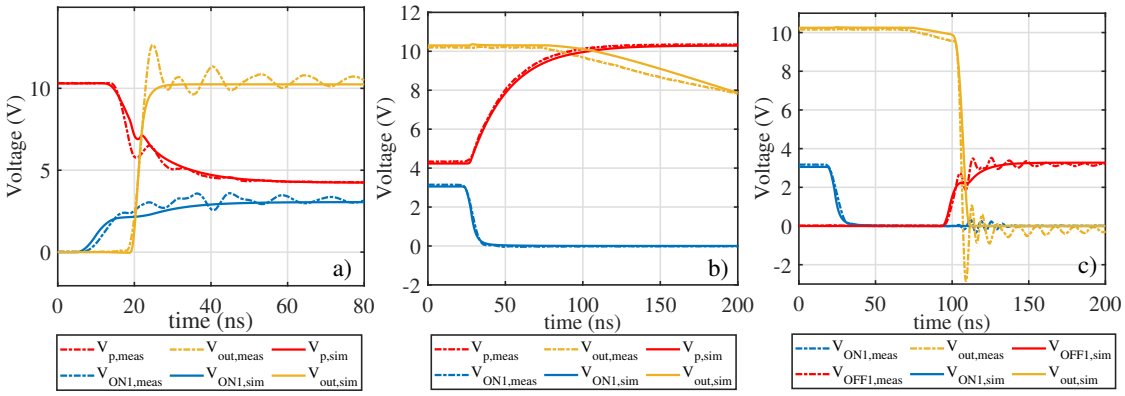

Figure 4.8: Comparison between the gate driver measured waveforms with the ones obtained by means of simulations.

measure these delays, the output of the gate driver is loaded with a $10\,k\Omega$ resistor.

Figure 4.8 shows the waveforms related to the first leg of the gate driver, that includes M1 and M3. This leg can be used both to completely turn-on the power transistor with a single command and to inject the first positive pulse when the three level AGD is used.

When the ON1 command (blue line) in Fig. 4.8(a) reaches the threshold of M1, the voltage V_p (red line), starts to decrease because M1 is closing. When the V_{sg} voltage of the p-mos transistor M3 exceeds its threshold voltage, also this one turns-on and the output of the driver (gold line) starts to rise, in order to reach the power voltage of the driver ($V_{dd,drv}$). Similarly, when the control signal ON1 goes down, turning off the power transistor M1, the voltage V_p increases and reaches $V_{dd,drv}$, turning off M3 and consequently the output voltage starts to decrease, discharging the parasitic capacitances of M5 and M6 on the 10 kΩ resistance. The third leg of the gate driver is used to remove the charge from the power transistor in order to create the negative current level of the proposed driving technique. When the transistor M5 is turned on with the OFF1 signal (red lines) in Fig. 4.8(c), after the turn off of M1 (blue lines), the output voltage reaches rapidly the zero level as shown in Fig.4.8(c) (gold lines). Fig 4.8, as well as showing the experimental results related to the gate driver characterization, also shows the comparison of such waveforms with the ones obtained by means of simulations of the same gate drivers, resulting in good agreement. Such AGD model will be used in the last part of the chapter in order to discuss the obtained results.

Gate driver delays

As already stated and highlighted in Fig. 4.8, there are delays between the PWL command and the instant in which the output of the gate driver changes its state. These delays need to be considered when the user defines the timing of the control signals to reproduce the optimal gate current profile. Such delays are defined between the 10% and 90% of the gate voltage of the nmos transistor of the driver, which is driven by the microcontroller, and the output voltage of the driver. The estimated delays, are:

- $\Delta_{1,on} = 9.5$ ns, that represents the turn on delay of the leg controlled by ON1, used for the first positive pulse.
- $\Delta_{1,off} = 35$ ns, that represents the turn off delay of the leg controlled by ON1, used for the first positive pulse.
- $\Delta_{2,on} = 6.2$ ns, that represents the turn on delay of the leg controlled by OFF1, used for the negative current pulse.
- $\Delta_{2,off} = 5.9$ ns, that represents the turn off delay of the leg controlled by OFF1, used for the negative current pulse.

- $\Delta_{3,\text{on}} = 10\,\text{ns}$, that represents the turn on delay of the leg controlled by ON2, used to turn-on definitely the device.
- $\Delta_{3,\text{off}} = 54\,\text{ns}$, that represents the turn off delay of the leg controlled by ON2, used to turn-on definitely the device.

4.3.2 Microcontroller and Timing

The microcontroller chosen to generate the PWM signals to drive the AGD is the dsPIC33CH128MP205 [49], because it is characterized by optimal timing characteristics. Indeed, this device allows the user to control up to 12 PWM channels with 250 ps of resolution. The PWM timing can be defined according Fig. 4.9 where ON1, ON2, OFF1 and OFF2 are the signals that control the legs of the gate driver. The ON1, ON2 and OFF1 signals are used to turn-on the power transistor

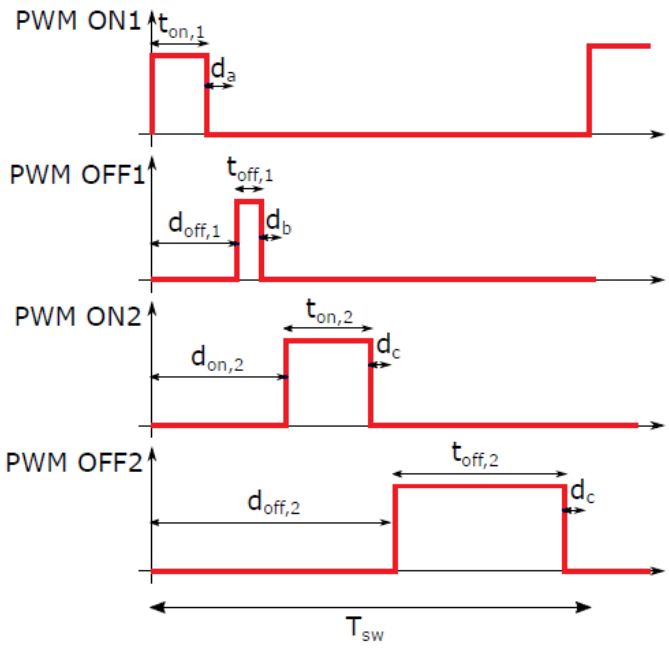

Figure 4.9: Timing to control the AGD imposed by the microcontroller.

according the proposed technique, while OFF2 is used to simply turn off the device during its off phase. Besides, the ON1 signal is used by the microcontroller to trigger the further signals. All the PWM signals are characterized by the same period T_{sw}, i.e. the switching period of the converter, but they have different duty cycle and different delay with respect the ON1 rising edge. It is worth noticing that a constant time delay of $\Delta\mu = 15\,\text{ns}$ between the ON2, ON3, OFF1 rising edge and the corresponding rising edge of their trigger signals exists. Such a delay has to

be considered in the evaluation of the AGD optimal parameters, together with the AGD time delays previously measured. The parameters that must be evaluated in order to drive the AGD are $t_{on,1}$, $d_{off,1}$, $t_{off,1}$ and $d_{on,2}$ whose equations are reported in 4.3.

$$t_{on_1} = t_1 - \Delta_{1,on} \tag{4.3}$$
$$d_{off_1} = t_1 + \Delta_{1,on} - \Delta_{2,on} - \Delta\mu \tag{4.4}$$
$$t_{off_1} = t_2 - t_1 + t_f + \Delta_{1,on} - \Delta_{3,off} \tag{4.5}$$
$$d_{on_2} = t_2 + \Delta_{1,on} - \Delta_{3,on} - \Delta\mu \tag{4.6}$$

The parameters t_1, t_2 and are the output of the proposed algorithm, as shown in Fig. 3.20 and allow the user to define the parameters for the microcontroller.

4.4 Optimal Parameters for the Gate Driver

After the matching of the waveforms resulting from measurements on the converter with the ones obtained exploiting simulations (Fig. 4.6) and the characterization of the proposed AGD (Fig. 4.8), in order to assess the validity of the proposed technique on the real circuit, the R_t is placed in series with the power mosfet and a single simulation was performed. In this situation the power transistor was driven exploiting a single pulse of an ideal driver. Once obtained the optimal switching waveforms, the tuning algorithm for evaluating the optimal gate current profile was applied on the circuit resulting in the waveforms shown in Fig. 4.10. In order to obtain such waveforms the rise time and the fall time of I_{gate} is set to 7 ns.

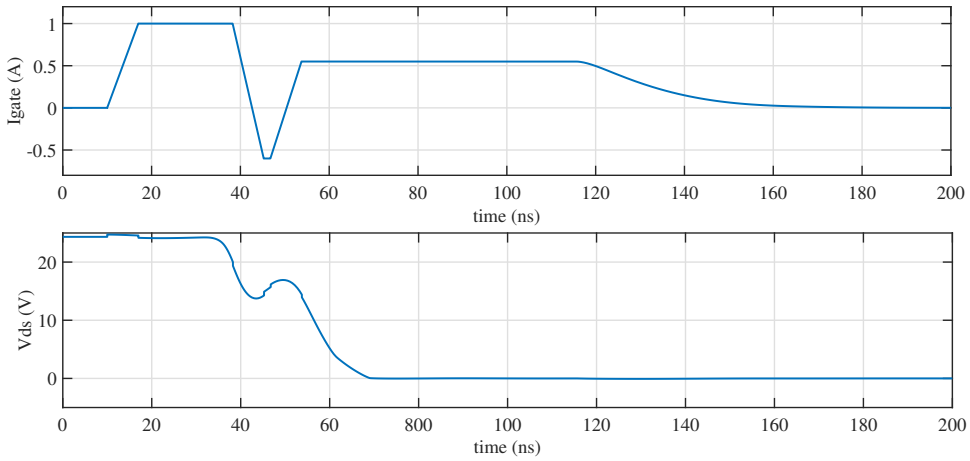

Figure 4.10: Optimal gate current profile obtained with the tuning algorithm and the resulting optimal V_{ds} (simulation results).

The timing values resulting from the algorithm are $t_1 = 28\,\text{ns}$ and $t_2 = 37\,\text{ns}$. At this point, by referring to the Eqs. 4.3 the values of the parameters for the PWM signals are calculated resulting in the value listed in Tab. 4.3.

Table 4.2: Gate driver parameters obtained from the proposed algorithm.

t_1	t_2	$I_{on,1}$	$I_{on,2}$	$I_{on,3}$
28 ns	37 ns	1 A	−0.6 A	0.55 A

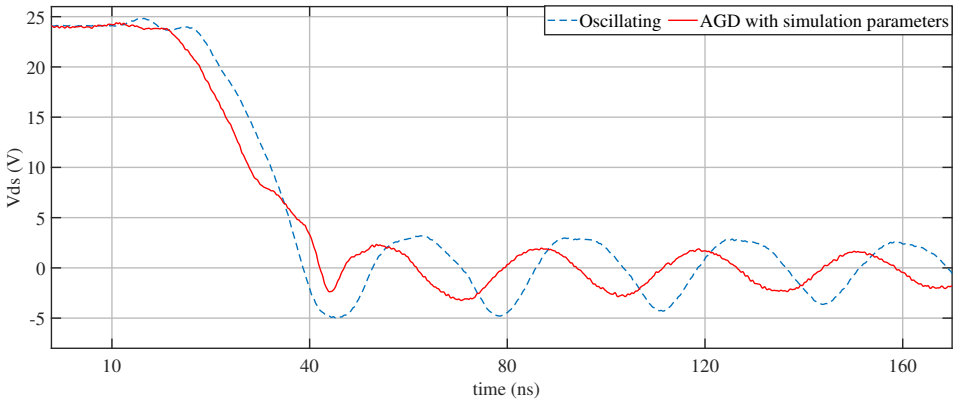

Figure 4.11: Comparison between the oscillating V_{ds} obtained driving the power transistor with a single positive pulse (dashed line) and the one resulting exploiting the parameters obtained with the proposed algorithm (solid line).

These values are stored in the memory of the microcontroller and used to drive the power transistor resulting in the waveforms shown in Fig. 4.11.

As shown in this figure, the oscillations are reduced, but they are not completely damped and the V_{ds} is not equal to the optimal ones resulting exploiting the R_t. By analyzing the V_{ds} waveforms, by exploiting this driving parameters the rise of the voltage V_{ds} related to the negative gate current starts when this voltage reaches approximately $7\,V$. On the other side, the optimal V_{ds} obtained by means of simulations with the R_t and so with the tuning algorithm shows that the rising behavior occurs when this voltage is about $13\,V$. This suggest that there are issues on the timing parameters related the negative gate current levels, more precisely on d_{off1} and t_{off1}.

So the experimental setup shown in Fig. 4.12 is implemented to perform parametric measurement on these two parameters of the driving signal exploiting a MATLAB script. More precisely, this script can program the microcontroller, exploiting the UART interface and the PC stores the switching waveforms measured with the oscilloscope for each configuration of the driving signals. A photo of the

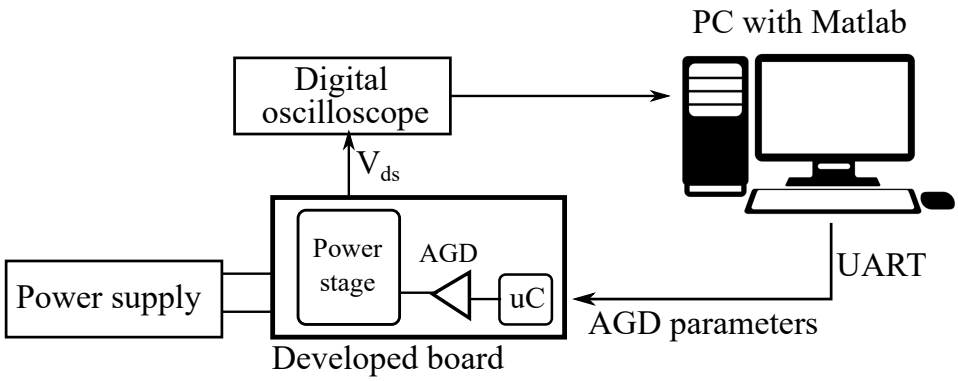

Figure 4.12: Experimental setup to perform the experimental characterization.

proposed experimental setup is shown in Fig. 4.13.

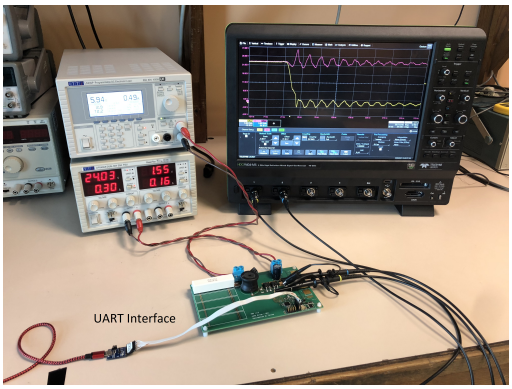

Figure 4.13: A picture of the experimental setup.

After the proposed finer tuning of the driving parameters, two optimal solutions were found that are free of oscillations and that are in optimal matching with the optimal switching waveforms. The optimal driving parameters are also listed in Tab. 4.3 and the comparison of the measured waveforms with the optimal ones is shown in Fig. 4.14, resulting in a good agreement. Fig. 4.14 also shows the waveforms resulting by simulating the model of the converter, exploiting the model of the real driver whose outputs are driven with the parameters listed in Tab. 4.3. In this situation the V_{ds} results to be equal to the optimal one assessing the goodness of the algorithm, but highlighting some mismatch between model and real converter, more precisely between the parasitic capacitance of the power transistor that appear to be higher in the model if compared with the ones of the real transistor. In fact, to obtain the same optimal V_{ds} in simulation, the first pulse results to be longer as can be seen also by comparing the V_{gs}.

The conducted experimental validation allows to make two important considerations. The first refers to the power loop and the optimal switching waveform which

Table 4.3: Timing parameters for the AGD.

time	Simul. Params.	Opt. Sol A	Opt. Sol B
$t_{on,1}$	18.5 ns	18.5 ns	18.5 ns
$d_{off,1}$	16.3 ns	11.25 ns	10 ns
$t_{off,1}$	16.3 ns	16.25 ns	15.25 ns
$d_{on,2}$	22 ns	22 ns	22 ns

are completely in agreement between simulations and experimental worlds, by assessing the goodness of the method based on the auxiliary R_t component, while the second refers to the tuning algorithm of the driving parameters. More precisely, the parameters obtained exploiting the proposed algorithm can be considered as starting points to drive the power transistor and to reproduce the optimal waveforms. In fact, a small mismatch between the model and the experimental setup can results in oscillating waveforms. This phenomenon legitimates the sensitivity analysis performed in Section 3.5.1.

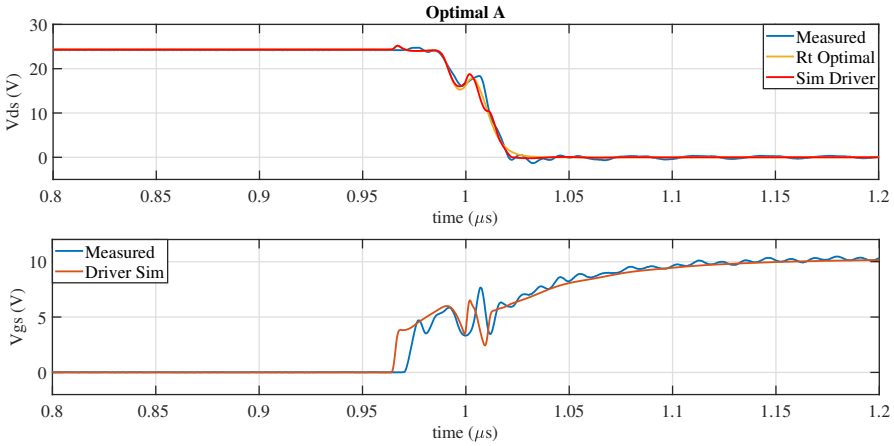

Figure 4.14: Comparison of the optimal switching waveforms resulting from experimental measurements and simulations.

4.5 Comparison with the snubber solution

With the aim of comparing the proposed solution with a traditional one in terms of ringing suppression and power loss reduction, an high side RC snubber was placed in parallel to the freewheeling diode. The values of the RC components that make up the snubber have been calculated according to the method discussed

Table 4.4: Switching energy.

	$E_{\mathrm{T_{LS}}}$	$E_{snubber}$	$E_{\mathrm{D_{HS}}}$	E_{tot}
Oscillating	213 nJ	-	625 nJ	838 nJ
Tuned AGD	1.13 μJ	-	594 nJ	1.72 μJ
RC Snubber	215 nJ	3.28 μJ	626 nJ	4.12 μJ

in Chapter 1, exploiting the following equations:

$$C_{snb,h} = 6C_p = 10\,nF \qquad R_{snb,h} = 1.5\sqrt{\frac{L_p}{C_p}} = 4.7\,\Omega \tag{4.7}$$

The V_{ds} switching waveform resulting from the converter with the snubber is shown

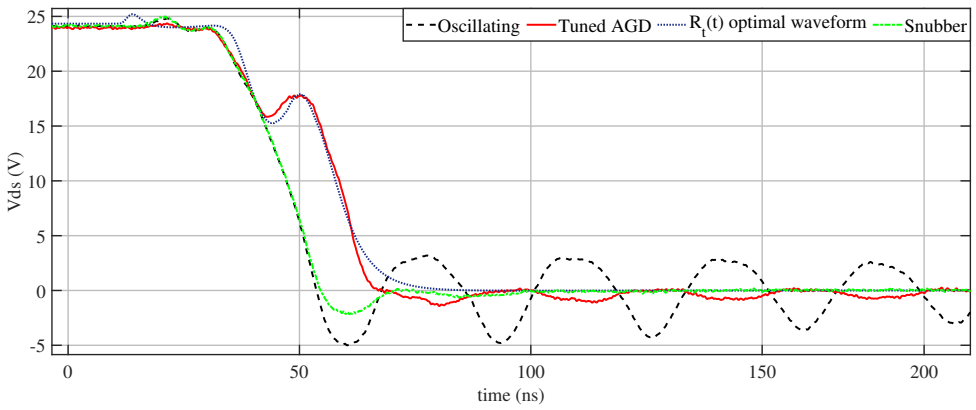

Figure 4.15: Comparison of the optimal switching waveforms resulting from experimental measurements and simulations.

in Fig. 4.15, as well as the the oscillating, the optimal one obtained exploiting the R_t and the one resulting driving the transistor with the optimal driving profile. The comparison shows that the oscillations results to be completely damped both using the snubber and the AGD. On the other hand, if the power losses are concerned, the beneficial effects of using the AGD solution instead of snubbers, stand out. The oscillating case shows the highest efficiency due to the fastest transients during the commutations of the power switches, but the important result is about the highest efficiency of the AGD solution if compared with the snubber one. With the aim of deepening such a point, the switching energy related to each component was obtained from time-domain simulations in the three cases and listed in the Table 4.4. The switching energy of the power transistor is highest in the case of the tuned AGD, since it is exploited to dissipate the energy that otherwise would bounce

between the parasitic inductance and capacitance, causing oscillations. Instead, such an energy is about the same for the oscillating case and the snubbered one, because the switching speed in these situations is approximately the same. Indeed, the switching energy associated to the high-side power diode is not affected by how TLS is driven, resulting in the RC snubber case to be the less efficient because of the switching energy related to R_{snb} to be equal to $3.28\mu J$.

4.5.1 Impact of timing parameters

In this subsection a sensitivity analysis on the optimal time parameters is performed with the aim to understand their impact on the switching waveforms in an experimental setup. Such a sweep is performed by considering of $\pm 5\,ns$ around the optimal values of the tuned parameters reported in Table 4.3. The variable used as reference to compare the switching waveforms is the peak of the V_{ds} undershoot which is plotted in Fig. 4.16 as a function of the time parameters. The central point in the central plot is the optimal value corresponding to the previously matched parameters As can be seen in the figure the measured undershoot reaches about $7\,V$ in the worst conditions, highlighting the importance to have some reference values when performing the tuning of an AGD. In fact, the nominal optimal parameters, obtained by means o the tuning algorithm, allow to have intervals of time in which looking for the true optimal parameters. This allows the user to avoid a the completely trial and error approach, with the risk to have high overshoots and/or undershoots on the power devices.

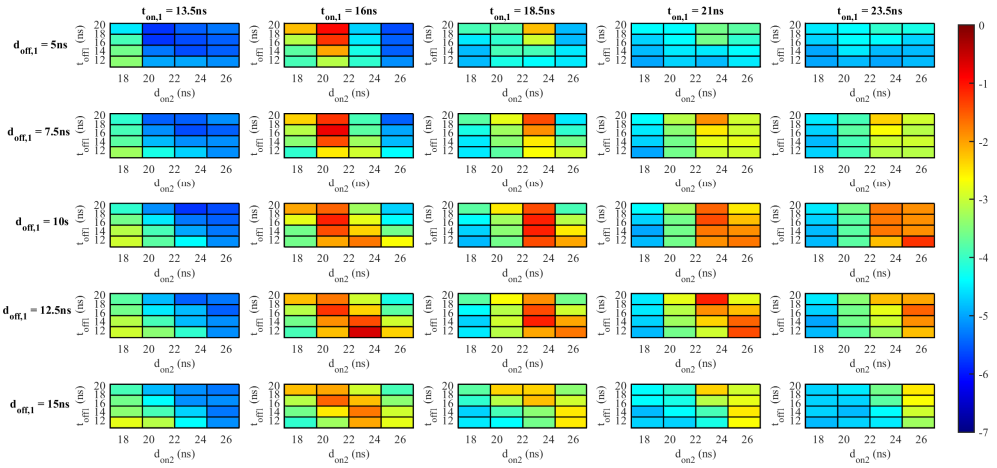

Figure 4.16: Parametric analyses obtained sweeping the optimal timing values reported in Tab. 4.3) of $\pm 5\,ns$. The undershoot of the V_{ds} is acquired and considered as a figure of merit to compare all the switching waveformss.

Chapter 5

Testing of Heatsinks Mounted on Power Transistor

In this chapter the focus of the thesis moves from the efficiency of power transistors, related to overvoltages and overcurrents, to the analysis and the management of their junction temperature (T_j), which represent a critical issue in the design of power converters [50]. In fact, the high switching frequencies, the high voltages and the high currents, to which power transistors are subjected, generate heat that must be dissipated to avoid failures or damages of the power transistor itself or, in the worst case, of the whole system that includes the power converter [51].

A mismanagement of the thermal aspect of a power device does not necessary lead to an immediate malfunction, but could accelerate the aging effect of a system, increasing the cost of the management and reducing the lifetime of the device and consequently, the time between two consecutive services [52]. Most of the heat generated in a power converter depends on the power switches that can reach very high temperature. For this reason, the power transistors which compose a power converter are often supplemented with passive heatsinks mounted on their surface. In most critical applications these type of heatsinks could be complemented with other cooling systems, like fans or with a system of a refrigerant fluid that circulates around the power module. Moreover, it is not uncommon that more transistors share the same heatsink [53].

Passive heatsinks are composed of an opaque metal surface designed to rapidly diffuse the heat produced by the transistor and in general, their reliability depend on how they are mounted on the power device, and on their state of wear [54]. The heatsink mounting phase is often underestimated in industrial applications, but a wrong assembly of these devices can lead to a considerable increase of the temperatures in the semiconductor devices. For example, the heatsink can move away from the power device due to the continuous small movements caused by vibrations of the system. Other external factors may affect the in-field operation of the heat sink, for instance, heatsinks can be clogged with dust or dirt reducing

their capability to dissipate the heat.

Referring to the existing test strategies, several approaches can be found in literature to cover electrical faults of power systems [55–57], but it results very difficult to find test strategies for checking the capability of a heatsink to propagate the heat. Indeed, in actual tests the heatsink mounting is checked only with an optical inspection that assures the presence of the heatsink, without asserting its effective capability dissipate the heat. For such a reason, it is important to introduce some tests that allow the monitoring of the heatsink capability to dissipate the heat, by referring to the different phases of the life of a generic converter. More precisely, in order to reduce the risk of faults, the estimation of the performance of the heatsinks mounted on a power transistor should be evaluated at the end of the production of the board, and also during its normal operation.

In this thesis, only passive heatsinks directly mounted on a single power transistor will be analyzed, with the aim of proposing an *End-of-Manufacturing Test* strategy, that, exploiting an Automatic Test Equipment (ATE) and the *Thermal fault* concept, allows to establish if an heatsink works properly. The proposed test technique lays the groundwork for the development of an *online* test strategy to check the heatsink status during the normal operation of the converter [58]. More precisely, in the first part of this chapter, an end-of-manufactury test strategy for checking the capability of an heatsink mounted on a power transistor to dissipate the heat is proposed. For this type of test, two different situations will be considered, the first in which the user can control the duration of the on and of the off phases of the transistors, the second in which the degrees of freedom of the user are reduced, and he/she can apply to the converter only input stimuli, monitoring well defined quantities, and without having the possibility to control the duty cycle of the transistors which compose the power module. The aim of the proposed technique is to provide an estimation of the thermal resistance and so of the junction temperature by means of an electrical measurement, exploiting Thermal Sensitive Parameters (TSEPs) [59]. In these way, when a converter is tested to check its performance and to establish its correct behavior, it is possible to identify defects that could affect the dissipation system without performing temperature measurements. The proposed analysis is complemented both with experimental and simulation results.

In the second part of this chapter the proposed methodology is conceptually extended, in order to perform an online monitoring of the heatsink capability to dissipate the heat, i.e., when the converter is working inside a system and there is not the possibility of using an ATE for checking the status of the converter dissipation system.

5.1 Thermal effects on Power Transistor

The maximum T_j of a power transistor affects significantly its performance and reliability, in particular a high T_j accelerates the failure mechanisms, reducing the lifetime of the device [60]. It is worth noticing that the failure mechanisms are not related only to electrical issues, but depend also on mechanical stresses caused by temperature fluctuations. In fact, all the materials that make up a power transistor are characterized by different thermal coefficients, so the temperature changes can physically damage the device, especially the solder connections and the wire bonds [60]. Moreover, the junction temperature affects also electrical characteristics of power transistor [60]. For instance, the on resistance of a power MOSFET rises up if the T_j increases [16, 61], while its threshold voltage goes down if the T_j goes up [16]. The dependence of the electrical features of a components is exploited by researchers and practitioners to have an estimation of the device junction temperature. All the Thermal Sensitive Parameters are classified as TSEP and each of them is characterized by pros and cons when it is used for estimating the temperature of a device. The most common TSEPs are deeply discussed in [62, 63]. In this thesis only the $R_{ds,on}$ as a T_j function is considered.

5.2 End of Manufacturing Tests

In this section some basic information about the most common test methodologies implemented at the of the production of a device are provided. At the end of manufacturing, each device or system is tested to asses the correctness of their functionalities. As far as tests on systems are concerned, it is important to highlights that more than 75% of manufacturing defects occur during the assembly of the PCB while only the remaining 25% can be associated to malfunctions of the components that make up the system. The main test strategies used at the end of production to test PCB can be distinguished in *functional tests* and *in circuit tests* [64–67]. Other common test strategies used to test system architectures are the *Built-In Self Test* (BIST) and the Boundary Scan (BS) [67]. BIST techniques consist in the capability of a system to test itself and looking for hardware defects. Often circuits in which such technique is implemented, include spare parts that automatically substitute the damaged parts. The BS is a technique for testing the interconnections on a PCB [67]. The BS test technique does not require test probes, but exploits test cells connected to each pins of the devices for checking its functionality. This technique is common in circuits with a large number of pins, that often cannot be reached with test probes.

5.2.1 In Circuit Test

The in-circuit tests are performed on fully assembled PCBs to check that all the devices are correctly mounted on the board, to check the correctness of electrical connections and to verify the response of each components to electrical stimuli. Such tests are performed by means of ATE that, by contacting some pins of electronic devices can establish if a system works according to its specifications. Generally, the electrical contact operation can be performed in two different ways, by means of bed of nails or by means of flying probes, as discussed in [66]. Using the former approach, the board is placed on the ATE needles to create the electrical contact, and the DUT board is moved to create the electrical contact. Instead, when a flying probe test machine is considered, the DUT is in a certain position while a robotic arm move the needles to make the electrical contacts on the PCB. The contacts can be performed on the welding of the component to be tested, or by means of specific test points, that are pads on the PCB used to measure a certain quantity or to apply a test signal. By means of probes contacted on the PCB, electrical stimuli are applied to the circuit and its response is measured in terms of voltage or current. The obtained results are compared with the ones expected and in this way the ATE can discard or certify the tested circuit.

Performing an in-circuit test on a PCB can lead to the propagation of the stimuli through unwanted paths. This phenomenon can make such test ineffective and, in the worst cases, it can damage the PCB components. In these situations, the addition of *guard probes* can solve such an issue [66]. The guard probes are ground connections that decouple the DUT from the rest of the circuit. The use of guard probes is widespread in the industrial environment, as discussed in [66] and it is also common in power circuits [66].

5.2.2 Functional Test

A *functional test* checks the correct working of a complex circuit by observing only its steady state outputs, as a function of some input stimuli. This type of functional tests is called *base functional tests* and can be improved, to increase their reliability and their faults coverage. The *timely enhanced functional test* extends the base functional test, monitoring the outputs, also during the transients, while the *observability enhanced functional test* improving the observability of the test by increasing the number of the output variables and combining functional test and in circuit test methodologies.

As previously introduced, in this work only an in circuit test methodology and a functional one have been developed to test the correctness of the heatsinks mounted on power transistors.

5.3 Thermal model

In this section the concept of thermal model is introduced. The heat propagation in a system can take place in three different ways, by means of convection, radiation and conduction. In a electronic circuit assembled on a PCB the heat propagates mainly through the conduction phenomenon [60]. A thermal model can be built considering the analogies between the heat propagation and the charge distribution in an electrical circuit as discussed in [16, 60, 68].

The thermal resistance R_{th} can be defined as the opposition that the heat meet when crossing a material. For instance, Fig. 5.1 shows all the resistances that the heat finds when it goes from the junction of a transistor encapsulated in a TO220 package to the external environment. In this particular case, three resistances,

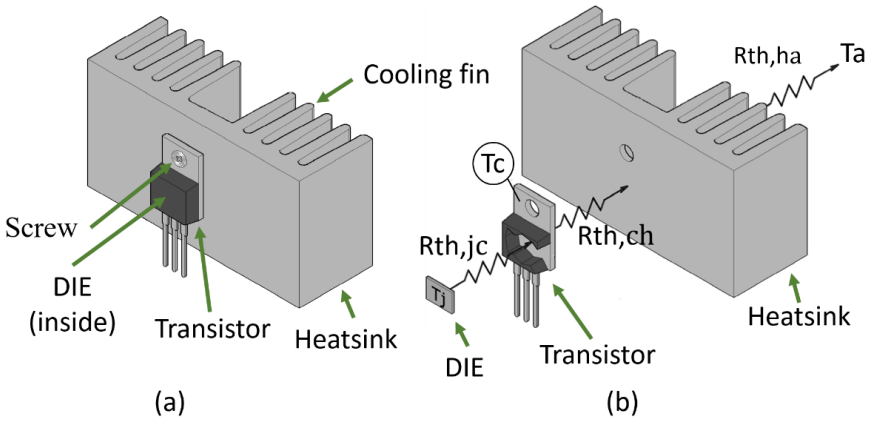

Figure 5.1: Thermal resistance model of a power transistor in TO220 package with an heatsink mounted on its tab pad. a) Physical system. b) Thermal resistance model.

i.e., $R_{th,jc}$, $R_{th,cd}$ and $R_{th,ja}$ can be identified, which are the thermal resistance between the junction and the case of the transistor, the thermal resistance between the case and the heatsink and the one between the heatsink and the ambient. Generally, the value of $R_{th,jc}$ is provided by the manufacturer, while $R_{th,cd}$ depend on how the heatsink is mounted on the device, more precisely on the size of the surface contact and on its goodness. The value of this resistance depends also on presence or the absence of Thermal Interface Material (TIM). The value of the last resistance $R_{th,da}$ depends on the heatsink and on the environmental conditions. The described model is only an approximation, because there are a lot of other things that affect the dissipation capability of a system. In fact, this model assumes that the heat propagation is unidirectional from the die to the heatsink but, in a real case, such a propagation occurs in all the directions, preferring the low resistances path. Another fundamental characteristics of the thermal dissipation refers to the

environmental conditions. Indeed, the ambient temperature (T_a) and the other heat sources near to the device, affect the heat propagation, making more difficult the development of an accurate thermal model.

The complex analysis needed to analyze a thermal system can be bypassed by approximating the whole thermal resistance with its equivalent steady state value $R_{th,ja}$, exploiting:

$$R_{th,ja} = \frac{T_j - T_a}{P_{dis}} \tag{5.1}$$

where $R_{th,ja}$ is the thermal resistance between the junction and the ambient, T_j is the junction temperature, while T_a is the temperature of the external environment. Finally, P_{dis} is the power dissipated by the transistor.

A thermal model can be complemented with thermal capacitances C_{th_i}. These components refer to the amount of heat that a given material can store and can be calculated as:

$$C_{th} = C \cdot M \tag{5.2}$$

where M is the mass quantitiy, while C is the specific heat of the considered material. The value of the thermal capacitance affects the thermal transient response.

5.3.1 Cauer and Foster thermal networks

In the previous subsection, the thermal resistance and capacitance concepts have been introduced. In this subsection, the most common thermal models, the Cauer one and the Foster one, will be discussed. The Cauer approach allows one to build the thermal model exploiting the physical characteristics of the system [69]. In particular, both the thermal resistance and the thermal capacitance of each component of which the system is composed, are evaluated, and included in Cauer network as shown in Fig. 5.2. As far as a simple geometry is concerned,

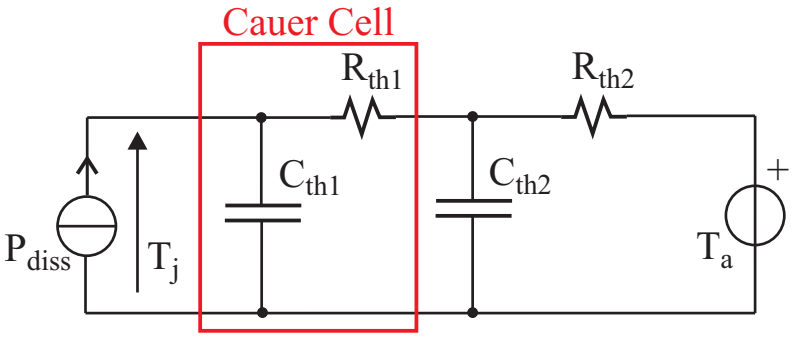

Figure 5.2: Cauer thermal network modeling a system with two time constant.

like the rectangular one shown in Fig. 5.3, the use of Cauer network allows to build a thermal model which is strictly related to the real dissipation behavior of

the system. Indeed, in this case the thermal resistance and capacitance can be calculated referring to (5.3).

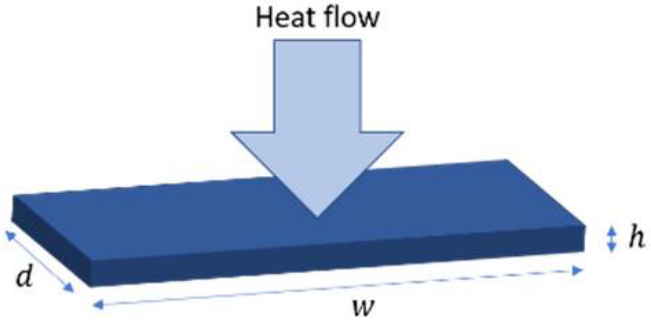

Figure 5.3: Rectangular geometry to explain the Cauer model.

$$R_{th} = \frac{h}{d \cdot w} \cdot \frac{1}{\lambda_{th}} \qquad c \cdot \rho \cdot d \cdot w \cdot h. \tag{5.3}$$

Despite its conceptual simplicity, the Cauer approach needs an excellent knowledge of the material composition and of the geometry of the system which needs the thermal model. Indeed, the geometry of a system is often not so regular to allow the use of simple formulae to evaluate the value of the thermal resistances and capacitances.

The Foster network can solve this issue, giving the user the capability to build the thermal-electrical model by exploiting experimental measurements [69]. It is worth noticing, that the RC Foster network, shown in Fig. 5.4, has no relationship with the geometry of the system, but it is an equivalent electrical model that reproduces the same time response of the real thermal transient.

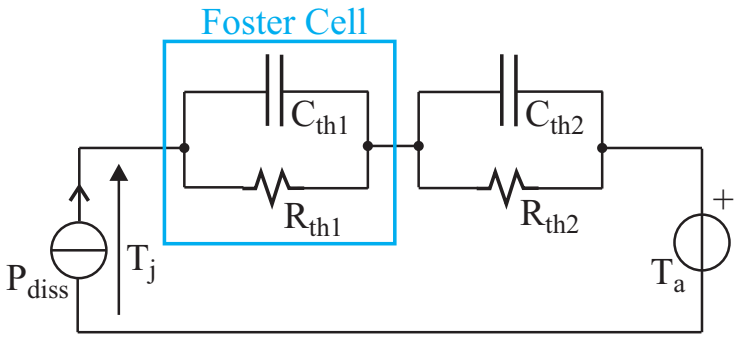

Figure 5.4: Foster thermal network modeling a system with two time constants.

5.4 The proposed Approach

After the introduction of the thermal models' basis, and the discussion on the most common TSEPs, in this section the concept of the *thermal fault* is introduced and the proposed methodologies to execute the in-circuit test to check the correctness of the heatsink mounted on the power transistor and for monitoring its capability to dissipate the heat while the power converter is in normal operating conditions.

5.4.1 Thermal Faults Definitions

A thermal fault is defined as a reduction of the capability of a heatsink to propagate the heat from the power device to the external environment, causing an unwanted increase of the device junction temperature [70]. In accordance with the steady state thermal models, presented in section 5.3, a thermal fault consists in an increase of the equivalent thermal resistance, that could depend on a physical degradation of the materials which compose the dissipation system or on a simple displacement of the heatsink from the power transistor, that could be caused by vibrations of the converter. The value of the maximum thermal fault resistance can be calculated considering the maximum temperature that the transistor junction can reach according the Eq. 5.4.

$$R_{th,f} = \frac{T_{j,max} - T_a}{P_{diss}} - R_{th,jc} - R_{th,ca}. \tag{5.4}$$

It is worth noticing that a thermal fault is a steady state concept and that in this analysis are not taken into account the junction thermal stresses related to the switching transients.

5.4.2 Power Transistor TSEP characterization

In this work the chosen TSEP for evaluating the transistor temperature is the on state resistance ($R_{ds,on}$) of the power MOSFET. It is worth noticing that the proposed technique can be applied only on power converters whose switches belong to the power MOSFET category. For other types of switches other TSEPs should be used because the linear relationship between the R_{on} and the junction temperature cannot be ensured. In this work, two calibration procedures are proposed. The first one is based on the circuit shown in Fig. 5.5. This procedure is one of the most popular and requires to adjust and control the junction temperature T_j exploiting the external environment. More precisely, the DUT temperature is regulated by putting the device in a controlled temperature environment. Generally this operation is performed exploiting a controlled temperature heatsink or putting

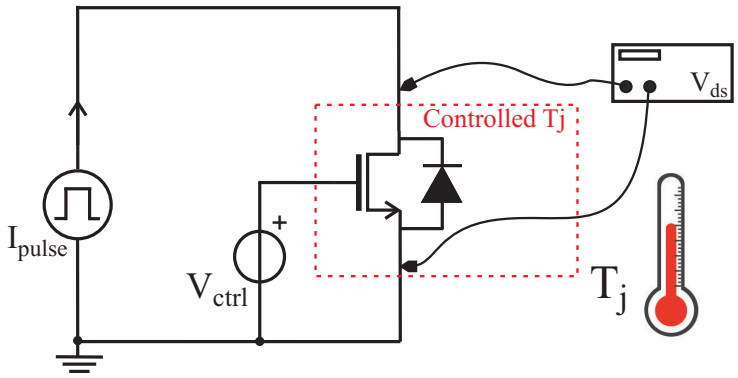

Figure 5.5: First calibration setup. The junction temperature is controlled exploiting the external environment.

the device in a oven. When the DUT is off, the T_j is equal to the external temperature T_a. In this situation the internal heat source is off, and once the steady state is reached, the internal junction temperature is equal to T_a. After the steady state is reached, the transistor is turned on by means of V_{ctrl} and a series of properly time spaced and different amplitudes current pulses are applied to the DUT. At the same time, the drain source voltage V_{ds} is measured by means of a multimeter. The voltage V_{ctrl} is high enough for drive the transistor in the ohmic region, but the pulse duration should be short enough to avoid the that the transistor causes the self-heating, but also long to have the transistor in steady state [71]. The operation has to be repeated for different temperatures in order to populate the relationship between the junction temperature (T_j) and the on resistance (R_{on}).

Another method for evaluating the relationship between T_j and R_{on} exploits the circuit shown in Fig. 5.6. In contrast with the first approach, this technique

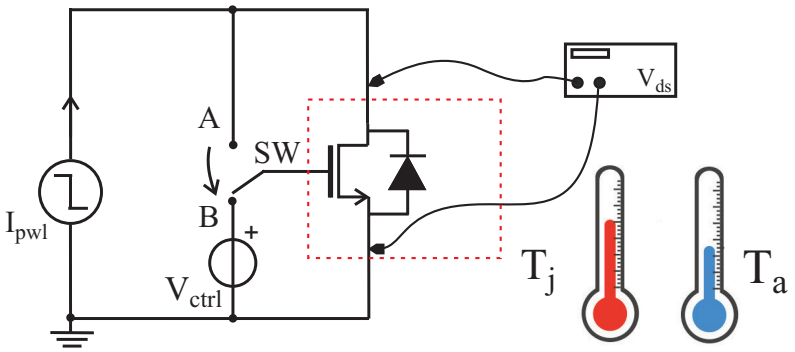

Figure 5.6: Second calibration setup. The junction temperature is increased exploiting the transistor self-heating.

does not need to control the external temperature, but a thermometer is necessary to measure the junction temperature. Such type of calibration needs to connect

the device in diode configuration, i.e, with the drain connected to the gate. In this way the device is in linear region and dissipates a lot of power, causing self-heating. When the DUT temperature reaches the maximum allowed, the switch SW biases the device in ohmic region starting the cooling phase. During this time interval the drain source voltage is monitored as well as the tab temperature. During the cooling time interval, the difference between the tab temperature and case temperature becomes smaller and smaller. This is because, in the cooling phase all the parts of the device come to the steady state value, which is the ambient temperature. This analysis can be extended also to junction temperature, since there is a low thermal resistance between the case and the tab. So the approximation of the junction temperature with the tab one is a right choice as discussed in [54].

5.4.3 End-of-Production Test

As stated in the introduction, two different methodologies of end-of-production tests have been proposed and analyzed. The first one is more general and belongs to the category of the *in-circuit* tests, because it is necessary to have different access points on the transistor on which is mounted the heatsink to test, while the second one is a *functional test*, specific for heatsinks mounted on power transistors included in hard switching power converters topologies.

In Circuit Test

This type of test needs that the turn-on and the turn-off phases of the power transistor on which is mounted the heatsink to test can be fully controlled by means of the ATE. In addition, each possible load connected in parallel with the transistor must be disconnected or protected by means of guard probes. This test requires the monitoring of the ambient temperature. The test procedure can be summarized as

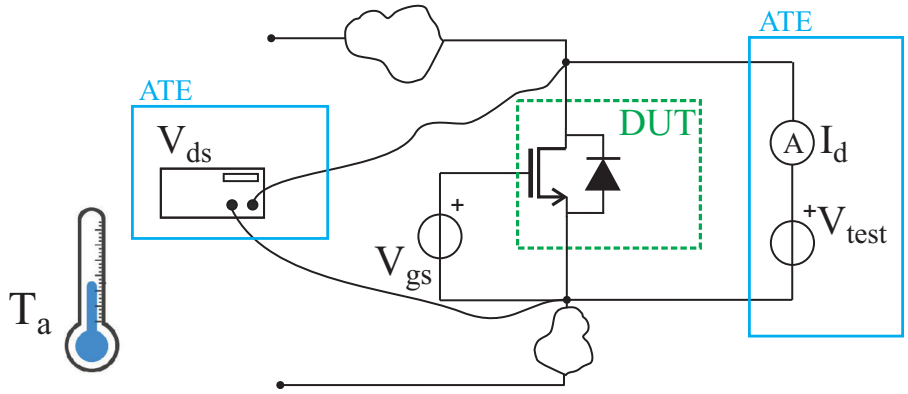

Figure 5.7: ATE configuration to test the heatsink mounted on the power transistor.

follows, by referring to schematic shown Fig. 5.7:

- By knowing the nominal power dissipated by the transistor during its normal working (P_{dis}) and its nominal drain source on resistance (R_{on}), it is possible to calculate the value of the voltage V_{test} to apply between the drain and the source terminals of the device during the test in order to heat-up the device, according to (5.5).

$$V_{test} = \sqrt{\frac{P_{dis}}{2} R_{ds,on}} \tag{5.5}$$

  The power used to calculate V_{test} is an half of the total nominal power so, if the heatsink is not correctly assembled on the transistor, the probability of destroying it is reduced.

- The ATE sets the V_{gs} voltage in order to turn-on the transistor leading it in deep triode. Such operation can be done both with the gate driver or bypassing it exploiting guard probes.

- The ATE forces the calculated V_{test} voltage between the drain and the source of the device, so a drain current I_d can flow through the power transistor. At the same time, both the V_{ds} and the I_d are continuously monitored.

- When the ratio between V_{ds} and I_d reaches the steady state, and thus the thermal equilibrium, the R_{on} can be evaluated, as well as the T_j exploiting the $T_j(R_{on})$ calibration curve.

- At this point, exploiting the Eq. 5.3, the $R_{tj,ja}$ thermal resistance can be evaluated and compared with the expected one.

- If the measured value is larger than the maximum declared in the specifications, a thermal fault is detected.

Functional Test

In contrast with the previously discussed in-circuit test, the proposed functional test can be applied on power MOSFETs installed in hard switching converters, in which it is not possible to control with an ATE the duration of the transistor on phase.

The proposed test can be executed at the end of the circuit production with a proper test configuration. This test does not need any specific circuit mounted on the board because both the voltage V_{ds} and the current I_{sw} are acquired by means of the ATE. As far as a hard switching topology is concerned, the average current flowing through the transistor can be estimated by means of a DC current measurement. In fact the current that must be measured is related to the topology of the converter. This means that the ammeter should be placed at the input or at the output port as a function of the converter topology. For instance, in a step

down converter, the ammeter should be connected in series with the output, while in a step up converter the ammeter connection should be in series with the power supply [16].

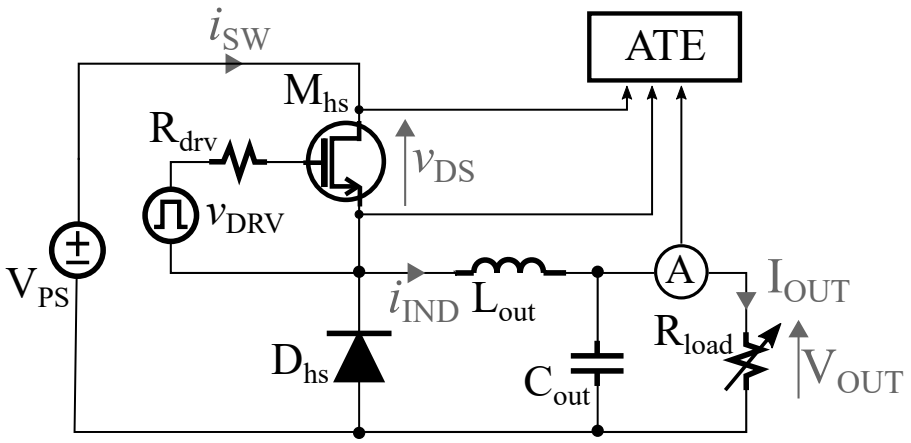

Figure 5.8: Test setup for the end-of-production functional test in a buck converter.

In this thesis a step down converter, shown in Fig. 5.8, is considered as reference to discuss the proposed technique, and to perform the experimental validation of the proposed technique. The device under test is the high side power MOSFET M_{hs}, whose duty cycle regulates the output voltage of the converter. By assuming that the converter works properly, the output voltage V_{out} and the output current I_{out} can be considered almost constant. During the on phase of the power transistor, the current flowing inside it is the same that flows through the power inductor L_{out}, whose average value is exactly the output current, as shown in Fig. 5.9.
For this reason, at the half of the conduction time, I_{sw} is equal to I_{out} [16]. Thus, by monitoring the voltage V_{ds} at the half of the conduction time, it is possible to approximate the $R_{ds,on}$ as:

$$R_{on} = \frac{V_{ds}(t_{on}/2)}{I_{out}}. \tag{5.6}$$

In order to perform the proposed end of manufactury functional test, it is required to perform the following procedure:

- The power converter is supplied with a compliant functional stimulus, V_{ps}, by means of the ATE. At the same time, a resistance R_{out}, whose value has been calculated to sink the maximum output current of the converter, when V_{out} assumes its nominal value, is used to load the converter output. In such a way the power transistor can reach its maximum temperature as well as the V_{ds} voltage, that reaches its maximum value. As a consequence, the measurement of this voltage results to be easier, as well as the estimation of the thermal resistance $R_{th,ja}$.

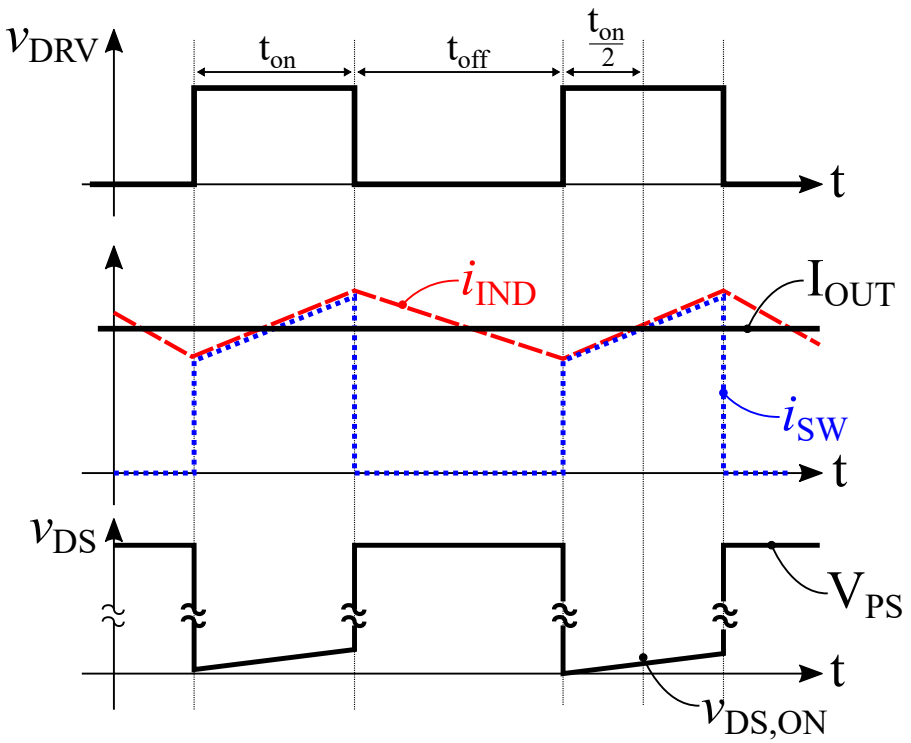

Figure 5.9: Switching currents and voltages for a generic buck converter.

- Before performing the voltage and current measurements, it is needed to wait for the end of the thermal transient. In fact, if all the thermal capacitances are not fully charged to the steady state value, the measured V_{ds} will result in a wrong value and consequently, also the thermal resistance will be wrong.
- During the test, the ambient temperature T_a should be continuously monitored. Such measurement does not require sophisticated thermometer because such test generally are performed in temperature controlled environments, so that a measurement could be cost-free.
- At this point, the junction to ambient resistance can be evaluated as:

$$R_{th,ja} = \frac{T_j - T_a}{P_M} \tag{5.7}$$

  where P_M is the power dissipated by the transistor. In this type of test, the power dissipated by the transistor consists of two different contributions, the conduction one and the switching one.
- As a result, if the measured value of the thermal resistance $R_{th,ja}$ is higher than the expected one, means that the test has detected a fault in the heatsink mounting.

5.4.4 Analysis of the measurement uncertainty

In this subsection the $R_{th,ja}$ uncertainty is analyzed with the aim to calculate the best value of the current I_{out} and of the power dissipation P_M to increase the accuracy on the evaluation of the thermal resistance $R_{th,ja}$. In order to perform such analysis, the junction temperature T_j is approximated as:

$$T_j \approx \alpha R_{ds,on} \tag{5.8}$$

where α is the angular coefficient derived from the calibration procedure. Such an approximation allows one to write the thermal resistance as:

$$R_{th,ja} = \frac{\alpha R_{ds,on} - T_a}{P_M} \tag{5.9}$$

where the total dissipated P_M includes the contribution of the conduction losses (P_{on}) and the one depending on the switching losses (P_{sw}), as reported in (5.10).

$$P_M = P_{on} + P_{sw} = D \cdot R_{ds,on} \cdot I_{out}^2 + \frac{1}{2} f_{sw}(t_r + t_f) V_{ps} I_{out}. \tag{5.10}$$

In this equation D represents the *duty cycle*, f_{sw} the *switching frequency* while t_r and t_f are the rise and the fall time of the V_{ds} voltage.

For the sake of simplicity, the analysis was performed by considering two different cases, the first in which the P_{on} is much larger than P_{sw} and the second in which the dominant power contribution is given by P_{sw}. So, in the first case the thermal resistance can be written as:

$$R_{th,ja} \approx \frac{\alpha V_{ds,on} - T_\alpha I_{out}}{D \cdot V_{ds,on} I_{out}} \tag{5.11}$$

and the absolute uncertainty ($\Delta R_{th,ja}$) results to be:

$$\Delta R_{th,ja} = \frac{\Delta\alpha}{D I_{out}^2} + \frac{2\alpha\epsilon_{I_{out}}}{D I_{out}} + \frac{\Delta T_a}{P_{on}} + \frac{T_a \epsilon_{V_{ds}}}{P_{on}} + \frac{T_a \epsilon_{I_{out}}}{P_{on}}. \tag{5.12}$$

On the other hand, by considering the situation in which the switching losses are larger than the conduction ones, the thermal resistance can be expressed as:

$$R_{th,ja} = \frac{\dfrac{\alpha V_{ds,on}}{I_{out}} - T_a}{\dfrac{1}{2} f_{sw}(t_r + t_f) V_{ps} I_{out}}, \tag{5.13}$$

thus the uncertainty can be calculated as:

$$\Delta R_{th,ja} = \frac{R_{on}\Delta\alpha}{P_{sw}} + \frac{\alpha \Delta V_{ds}}{P_{sw} I_{out}} + \frac{2\alpha R_{on}\epsilon_{I_{out}}}{P_{sw}} + \frac{\Delta T_a}{P_{sw}} + \frac{T_a \epsilon_{I_{out}}}{P_{sw}}. \tag{5.14}$$

In both the analyzed situations, by increasing the current I_{out}, and so the power dissipated by the transistor, the uncertainty on the evaluated thermal resistance can be reduced, increasing the accuracy on the evaluated $R_{th,ja}$. This means that, for obtaining a meaningful evaluation of the R_{th}, it is necessary to perform the measurement with the device that dissipates a lot of power to reach an high value of the junction temperature.

5.4.5 Functional In-Field Test

The proposed approach can be extended to the *online in-field test* [58, 72–74]. This type of test is generally used in safety critical applications, with the aim to check the correct working of the circuit. The in-field test often needs a dedicated circuitry that monitors periodically or continuously certain quantities in the circuit. This test extension needs to include in the power module two sensing circuits, the first for monitoring the V_{ds} and the second one for measuring the current I_{sw}. For the first measurement, it is possible to refer to the circuit developed in [58], while for the current monitoring it is possible to exploit a simple shunt resistance in series with the power transistor. The measured quantities can be acquired by means of an Analog-to-digital converter (ADC). The circuit proposed in [58] for monitoring the V_{ds} when the transistor is on, consists of an instrumentation amplifier connected between the drain and the source of the DUT. In order to decouple the input of the instrumentation amplifier from the DUT when it is off and consequently with a very high voltage drop, two diode polarized with a very low current, are placed in series with the amplifier inputs. In such a way when the DUT is on the instrumentation amplifier measures the $V_{ds,on}$, while when the DUT is off the amplifier is disconnected from the DUT. In our work, the experimental measurements related to this test are validated with an oscilloscope, as shown in Fig. 5.18.

For the online monitoring of the thermal resistance it is required also the measurement of the environment temperature. In this situation, a temperature sensor can be placed far from the main heating sources or the one provided by an external system can be exploited. For instance, in a vehicle the environment temperature can be provided by the central unit exploiting the CAN bus interface.

During this test, the V_{ds} voltage and the current I_{sw} are continuously monitored and the $R_{ds,on}$ is evaluated in the same manner of the in-circuit test. At this point, by exploiting the relationship obtained with the calibration procedure that relates the junction temperature to the drain source resistance $T(R_{on})$, the T_j is estimated, and then, by exploiting the value of the ambient temperature, the R_{th} is estimated exploiting (5.7). If the thermal resistance is higher than the expected value saved in the memory of the microcontroller, the system generates a signal fault, and the module goes in safety mode. The pseudocode of the proposed in-field test is shown in Fig. 5.10.

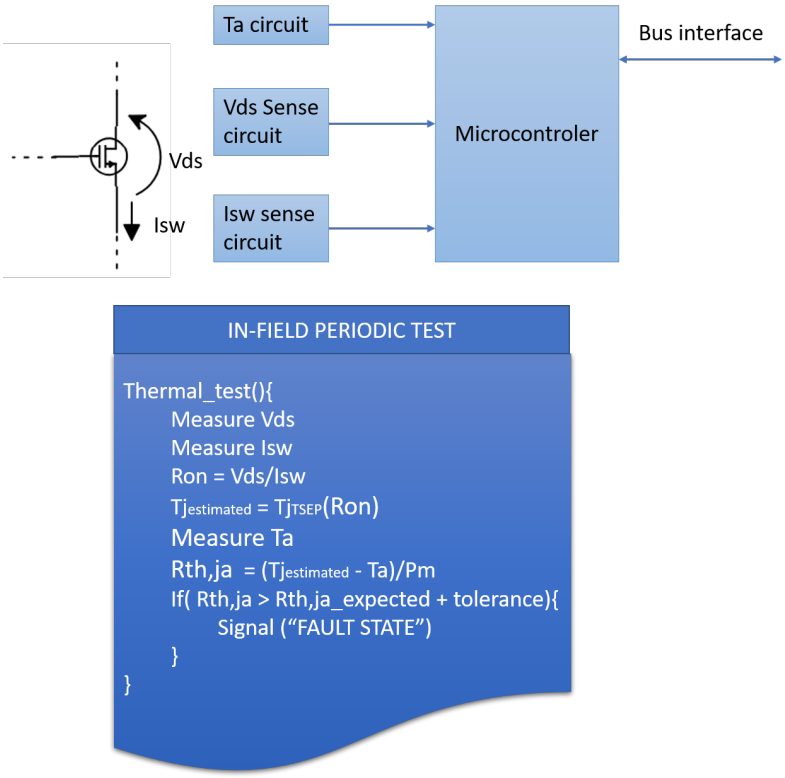

Figure 5.10: Pseudocode for the functional In-Field Test.

5.5 Experimental Results

In this section, the effectiveness of the proposed heatsink test methodologies are evaluated by means of experimental results. The transistor used to perform such validation is the SPP07N60C3, device encapsulated in a TO220 package. In the first part of the experimental validation the transistor is configured as proposed in section 5.4.2, in order to perform the calibration procedure that relates T_j to the R_{on} values, exploiting the transistor self-heating when it is in the saturation region.

After the calibration procedure has been performed, the in-circuit test methodology has been evaluated considering a rectangular heatsink as reference for the optimal dissipation for the analyzed transistor. Then, some defects have been introduced between the transistor and the heatsink, in order to check the capability of the proposed in circuit test to identify the introduced thermal faults.

At the end of this preliminary analysis, the same power transistor has been mounted in a high side buck converter, and the effectiveness of the functional test has been evaluated considering three different heatsink mounted on the transistor with three different defects inserted between the transistor and the considered heatsink. Also in this case, the capability of the method to identify the dissipation defects is assessed with the results of the measurements.

5.5.1 Calibration Procedure

The power transistor has been configured as shown in Fig. 5.6 and the calibration curve has been evaluated considering different values of drain current. The transistor current is regulated by means of the active current load, while the tab temperature is monitored with a directly contacted thermocouple. As introduced in section 5.4.2, the calibration procedure needs that the V_{ds} voltage is monitored during the cooling phase of the transistor. In the specific case, this voltage has been monitored with a multimeter. Fig. 5.11 shows the temperature behavior in the time domain during the two phases of the calibration procedure. More precisely up to 120 s the switch SW keeps the transistor in saturation region, thus the device dissipates a lot of power, and the temperature rise up very quickly. When the transistor temperature has reached a predefined value, in this case 160° C, the switch SW goes in position B, as shown in Fig. 5.6, and the cooling phase can take place. The drain source voltage behavior during this time interval, with the drain

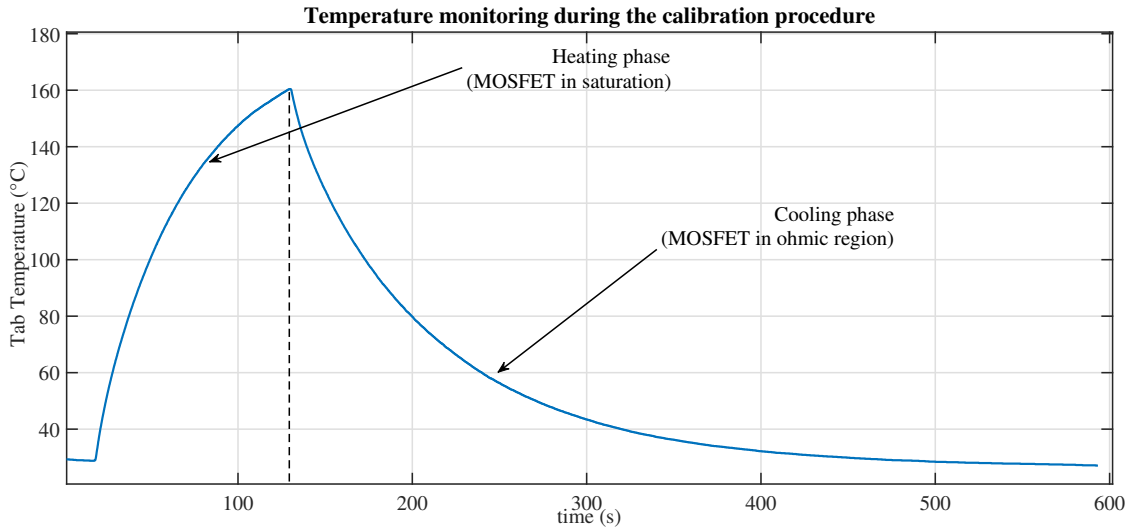

Figure 5.11: Temperature behavior of the tab transistor during the heating and the cooling phase of the calibration procedure.

current equal to 100 mA, is shown in Fig. 5.12. Due to a time to time association of the measured $R_{ds,on}$ with the temperature acquired during the cooling phase it is defined the calibration curve that relates the junction temperature to drain source resistance. This characterization is performed for five different current levels, without and with heatsink. All the experiments highlight that the relationship is significantly not influenced by the power level and by the dissipating conditions, as shown in Fig. 5.13. The resulting data have been used to estimate the temperature as a function of the $R_{ds,on}$.

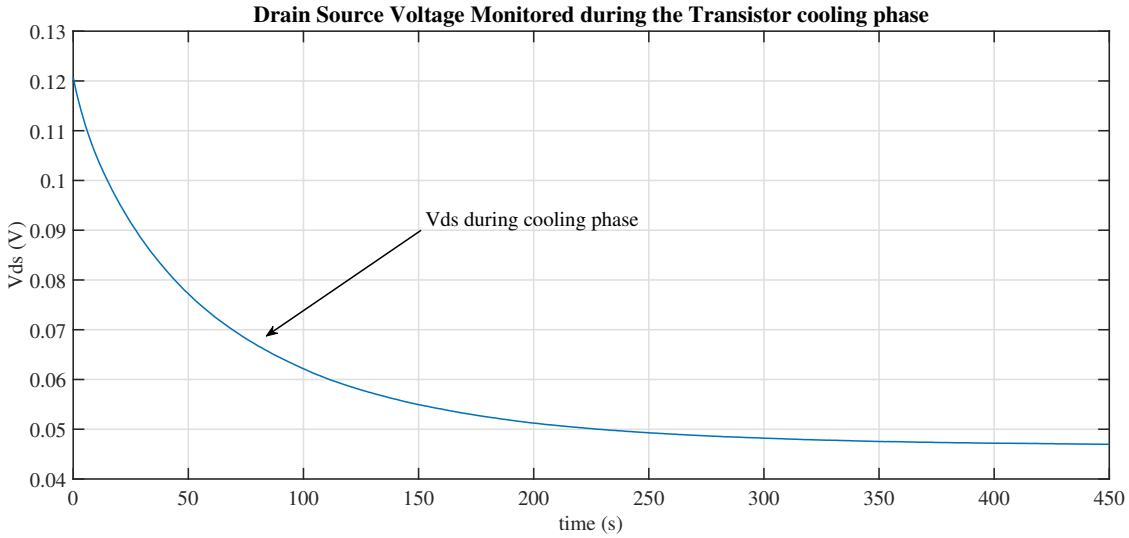

Figure 5.12: V_{ds} behavior during the cooling phase of the calibration procedure.

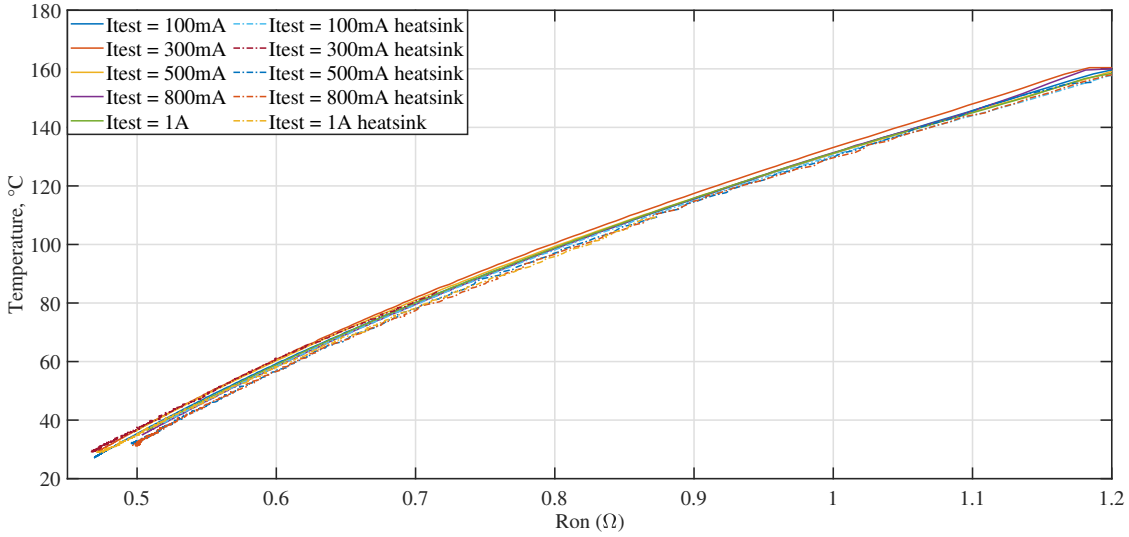

Figure 5.13: Junction temperature as function of R_{on} with several current test and with and without heatsink.

5.5.2 In-Circuit Test Validation

At this point the transistor is configured as shown in Fig. 5.7, with the aim to test the effectiveness of the method.

Firstly, the transistor with the optimal mounting of the heatsink was tested at four different power levels. In such conditions, the average value of $R_{th,ja}$ measured with the thermocouple is 25.22 °C/W while the average value evaluated with the proposed approach is 26.17 °C/W. In this analysis, six different faults are consid-

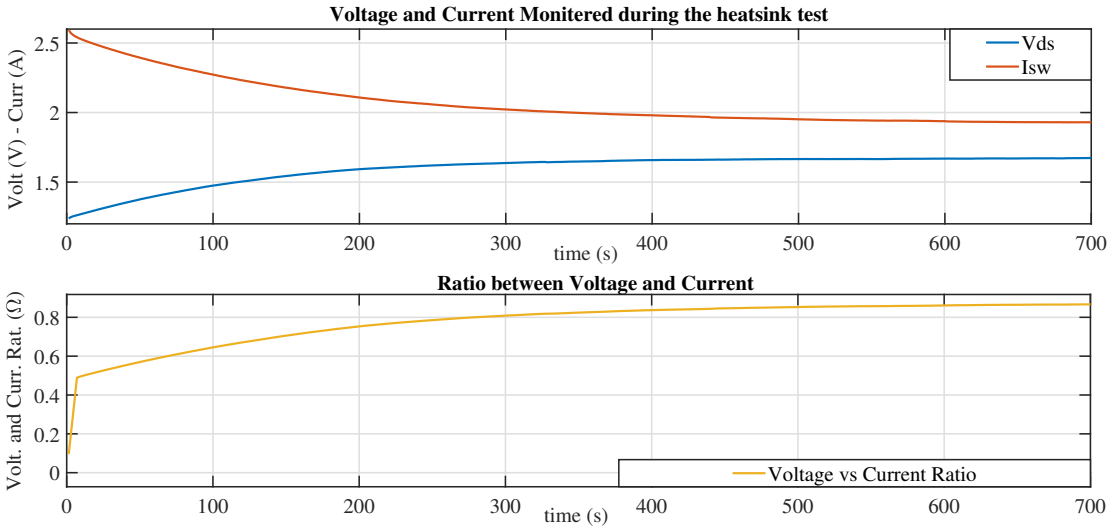

Figure 5.14: Drain source voltage and drain current during the in-circuit test.

ered. In each case an obstacle to the heat propagation is introduced exploiting some mechanical parts. The six faults introduced between the heatsink and the transistor reduce the heat conductibility. More precisely, Case 1 refers to a metal washer placed between the tab of the transistor and the heatsink, to reduce the surface contact. In Case 2, the metal washer is replaced with a plastic one to further reduce the thermal conductivity. In Case 3, the metal screw used for mounting the heatsink is replaced with a plastic one because of the lower thermal conductibility of the plastic materials if compared with metal while, in Case 4 the heatsink is again mounted with the metal screw, but with a reduced torque. Finally, in Case 5 a piece of paper is placed between the heatsink and the tab of the transistor covering all the contact surface, while in Case 6 the piece of paper covers only one half of the contact surface. This defects introduce an obstacles to the heat propagation. As shown in Table 5.1 all the performed measurement, both the one

Table 5.1: Results obtained with the In-Circuit test.

Case	Vtest (V)	Vds (V)	Ids (A)	Ron (mΩ)	Pdiss (W)	Tj (°C)	Tj (Ron) (°C)	Ta (°C)	Rthja (°C/W)	Rthja (Ron) (°C/W)
Optimal Dissipation	1.86	1.67	1.93	865	3.22	104.8	110.1	23.1	25.34	26.99
	1.09	0.94	1.52	623	1.44	62.9	63.2	23.2	27.55	27.75
	0.634	0.53	1.04	510	0.55	37.6	37.6	23.6	25.35	25.35
	2.59	2.38	2.10	1130	4.99	137.2	147	24.0	22.65	24.61
Case 1	1.16	1.01	1.51	675	1.52	73.8	74.2	23.9	32.69	32.95
	0.635	0.53	1.02	523	0.54	43.6	40.0	24.1	35.87	29.24
	1.81	1.63	1.76	926	2.86	112.2	119.2	24.2	30.75	33.19
	2.62	2.43	1.91	1270	4.64	155.2	160.0	24.3	28.20	29.24
Case 2	1.22	1.08	1.44	750	1.55	88.1	89.1	24.1	41.15	41.78
	1.82	1.66	1.62	1020	2.69	127.9	133.3	25.2	38.19	40.20
Case 3	1.33	1.18	1.46	808	1.72	96.4	99.5	25.3	41.27	43.06
	1.82	1.66	1.62	1020	2.69	127.9	133.3	25.2	38.19	40.20
Case 4	1.27	1.11	1.6	693	1.77	75.8	78.1	25.3	28.43	29.72
Case 5	1.28	1.12	1.62	694	1.82	76.1	79.0	25.0	28.03	29.62
Case 6	1.20	1.06	1.52	695	1.60	77.2	79.5	25.0	32.52	33.95

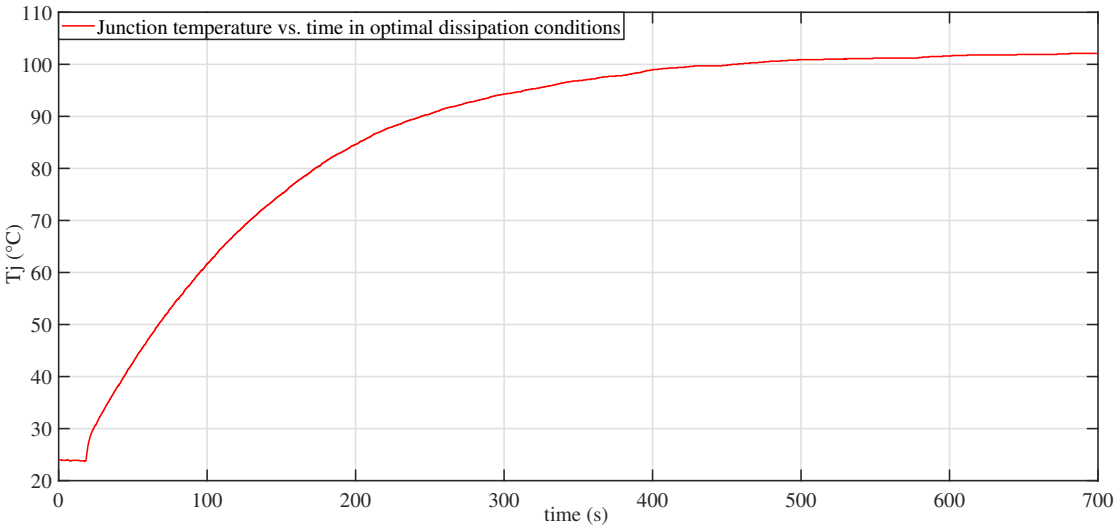

Figure 5.15: Drain source voltage and drain current during the in-circuit test.

obtained exploiting the TSEP and the one obtained with the thermometer are in good agreement. Besides, with the proposed technique all the introduced faults can be well distinguished from the measurement of the thermal resistance of the optimal mounted heatsink. This can be seen in Fig. 5.16, in which all the measurements of the considered faults are compared with the optimal mounted heatsink.

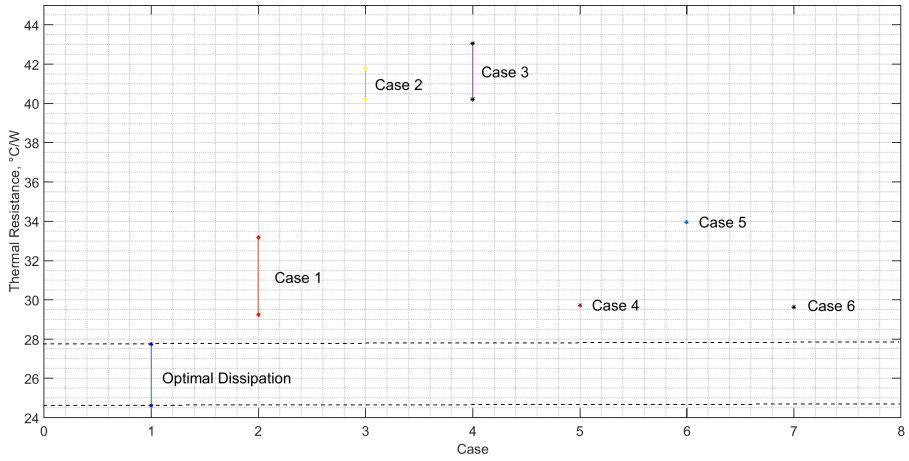

Figure 5.16: Measurement intervals for all the introduced faults. All the considered thermal faults are out of the band of the optimal dissipation.

5.5.3 Functional Test Validation

After the validation of the in-circuit test methodology, the same transistor was installed in the high side DC-DC converter shown in Fig. 5.17. This converter was

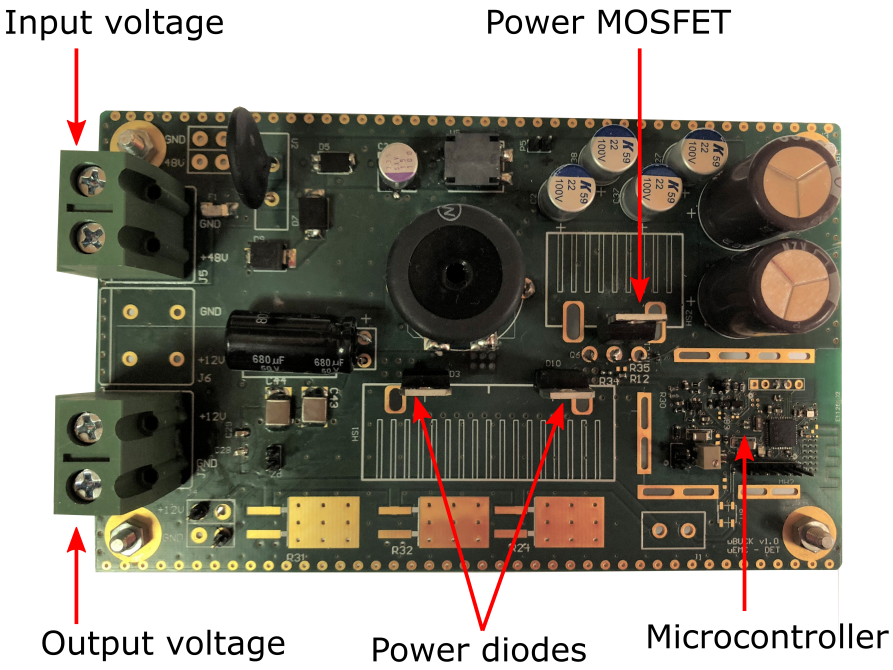

Figure 5.17: Buck converter used to assess the proposed functional test.

designed to step down a 24V input voltage (V_{ps}) to a 6V output voltage (V_{out}), working in closed loop. The maximum output current that it can provide to the load is 2 A. The high side transistor works with a 150 kHz switching frequencies. When the transistor M_{HS} is on, the current flows through the power inductor and, in this period of time, it is necessary to monitor the V_{ds} to validate the proposed functional test. At this point, the experimental setup shown in Fig. 5.18 is built up in order to emulate the behavior of an ATE for validating the proposed end of production method. The input of the buck converter was connected to a power supply while the resistive load is emulated with an active load. A digital oscilloscope, is used to acquire the V_{ds} voltage of the power transistor. The oscilloscope was configured in average mode to increase the accuracy of the measurements, and regulated to identify the rising and the falling edge of the V_{ds} voltage. In this way it is possible to acquire the average of the $V_{ds,on}$ voltage in one half of the conduction time. Besides, such rising and falling time are used to evaluate the contribution of the switching power to estimate the value of the thermal resistance $R_{th,ja}$. The output current is monitored with the internal ammeter of the active load while the tab temperature is continuously acquired by means of a thermocouple connected to the tab of the transistor.

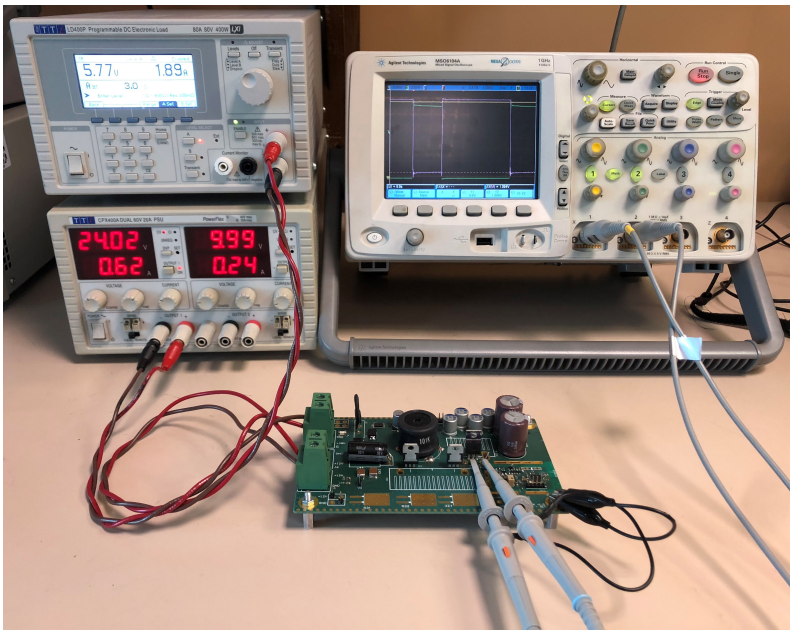

Figure 5.18: Experimental setup.

During this analysis, three different heatsinks and two different induced faults have been considered in order to assess the proposed method under different dissipation conditions. The considered heatsinks, named A, B and C, if properly mounted on the power transistor, are characterized by thermal resistances values of 40 °C/W, 35 °C/W and 25 °C/W respectively. Also during this analysis, a metal washer and a plastic one are considered to emulate the thermal faults. The acquired V_{ds} and I_{out} were used to calculate the value of the on resistance $R_{ds,on}$, which was exploited to estimate the junction temperature T_j. Fig. 5.19 shows the acquired data for the three heatsinks in the three different considered conditions, that are the optimal dissipation (circle markers), metal washer (diamond markers) and plastic washer (cross marker). As shown in these plots, the estimated T_j is in good agreement with the measured one, and the steady state value of T_j can be used for evaluating the thermal resistance.

Analysis of the results

Once the junction temperature was estimated and its values are compared with the one obtained by means of the thermocouple measurement, the values of the thermal resistances $R_{th,ja}$ were evaluated according the Eq. 5.7 and reported in Table 5.2.

In the first column are reported the values of the thermal resistances obtained exploiting the temperature estimated by means of the R_{on} measurements, while in the second one are reported the data obtained exploiting the junction temperature

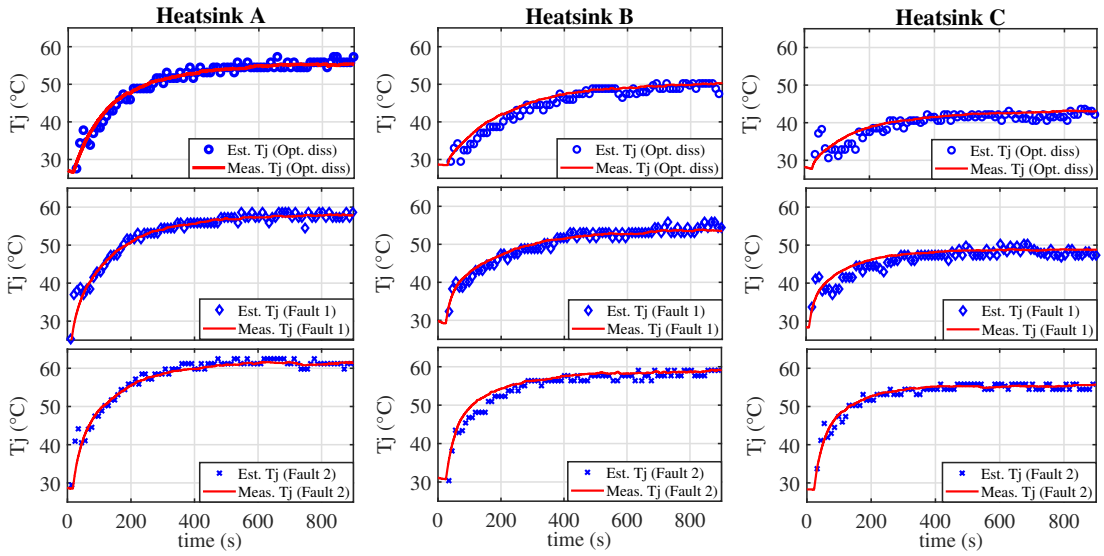

Figure 5.19: Estimated junction temperature when the heatsink is properly mounted (circle markers), with a metal washer inserted (diamond markers) and with a plastic washer (cross markers).

Table 5.2: Estimated $R_{th,ja}$ for all the heatsinks and defects

	Est. Rth,ja with Ron	Meas.Rth,ja (ther)
Heatsink A		
Optimal diss.	43.59°C/W	43.21°C/W
Metal washer	45.85°C/W	46.40°C/W
Plastic washer	49.47°C/W	50.13°C/W
Heatsink B		
Optimal diss.	36.42°C/W	37.19°C/W
Metal washer	42.05°C/W	42.60°C/W
Plastic washer	46.67°C/W	47.29°C/W
Heatsink C		
Optimal diss.	26.91°C/W	28.21°C/W
Metal washer	34.16°C/W	35.56°C/W
Plastic washer	42.97°C/W	43.80°C/W

measured with the thermocouple. It can be noticed that all the results are in good agreement and that the maximum error is equal to 1.4° C/W. Besides, for all the heatsinks the presence of the washer increases the value of the thermal resistance.

In order to asses the presence of a thermal fault, the value of the thermal resistance obtained with the proposed methodology are compared with the reference

value of the heatsink properly mounted. So, for each heatsinks and for each thermal defects, the difference between the measured $R_{th,ja}$ with the reference value are calculated and reported in Table 5.3. These data are compared with the measurement uncertainty calculated using 5.12, which is equal to 3.9 °/W. As a result, the proposed method can identify all the introduced thermal faults, except for when the metal washer is inserted between the power transistor and the heatsink A.

Table 5.3: Difference between the measured and expected $R_{th,ja}$.

	Iout=1.9A	
	Metal	Plastic
Heatsink A	2.26°C/W	5.88°C/W
Heatsink B	5.63°C/W	10.25°C/W
Heatsink C	7.25°C/W	16.06°C/W

Chapter 6

Conclusion

In this thesis the reliability of power switches, which hard switching power converters are made of, is discussed in terms of overvoltages, overcurrent, efficiency, EMI and thermal management. In the first part of the thesis the switching behavior of power converters is investigated, considering the effect of the parasitic elements that affect the ideal switching behavior. This analysis has allowed to identify and define mathematically the optimal switching waveforms, i.e., the fastest waveforms featuring the minimum level of oscillations and of switching losses in certain conditions. Due to the optimal switching waveforms definitions it has been possible to develop an algorithm to tune the parameters of a generic AGD, by knowing its features and providing the designer a powerful tool to save time and resources in searching for the right parameters to obtain the best switching waveforms of a power converter. The proposed algorithm is based on a piecewise constant gate current which drives the power transistor with the aim to reproduce the optimal switching waveforms obtained exploiting two auxiliary components placed in the power loop, the time variant resistance R_t and the time variant conductance G_t. The former controls the trajectory of the voltage V_{ds} at the turn-on while the latter shapes the trajectory of the current I_{sw} at the turn-off of the power transistor, avoiding the oscillations to take place.

Firstly, such technique is validated in a simulation environment, also performing a sensitivity analysis on the optimal gate driver parameters which highlights the high dependence of the switching waveforms on the driving parameters, especially on the time instants in which the gate current changes its level, but also that the optimal switching waveforms can be reproduced exploiting several current profiles. In fact the waveforms behavior depend on gate charge injected or removed from the device in the different phases of the driving.

Then the proposed technique is also experimentally validated on a buck converter, whose power transistor was driven with a resistance modulated AGD. The PCB was experimentally characterized to extract the value of the parasitic components and the measured turn-on oscillating switching waveforms are matched with

the one resulting from its equivalent circuit, in a simulation environment. Then the R_t was inserted in the power loop to find the optimal switching waveforms and the algorithm was applied to find the optimal driving parameters. After a further adjustment of the driving parameters, the resulting measured waveforms were in good agreement with optimal one and free from oscillations. In the last part of such analysis, the switching waveforms obtained exploiting the AGD are compared with those damped by means of an RC snubber. Even though the waveforms result to be damped with both the solutions, the proposed active gate driver solution results to be 60% less dissipative than the traditional one.

By referring to the last part of the thesis, two techniques for testing the correctness of the heatsinks mounted on power transistors are proposed. Both of them are based on the concept of *thermal fault*. The first in test circuit technique needs to access to the gate of the device to control the duration of its on phase, while the proposed functional test exploits only measurement performed on the input and the output port of a hard switch converter. The experimental results demonstrate the effectiveness of both the proposed techniques, which allows to estimate accurately the capability of an heatsink mounted on a power converter to propagate the heat by performing only electrical measurements.

Appendix A

Some Details on Simulations

This appendix provides some details about the simulations performed in the *Cadence Virtuoso* environment, exploiting the *spectre* simulator. Figure A.1 shows the schematic of the circuit implemented in Cadence, to simulate the buck converter proposed in Fig. 3.1.

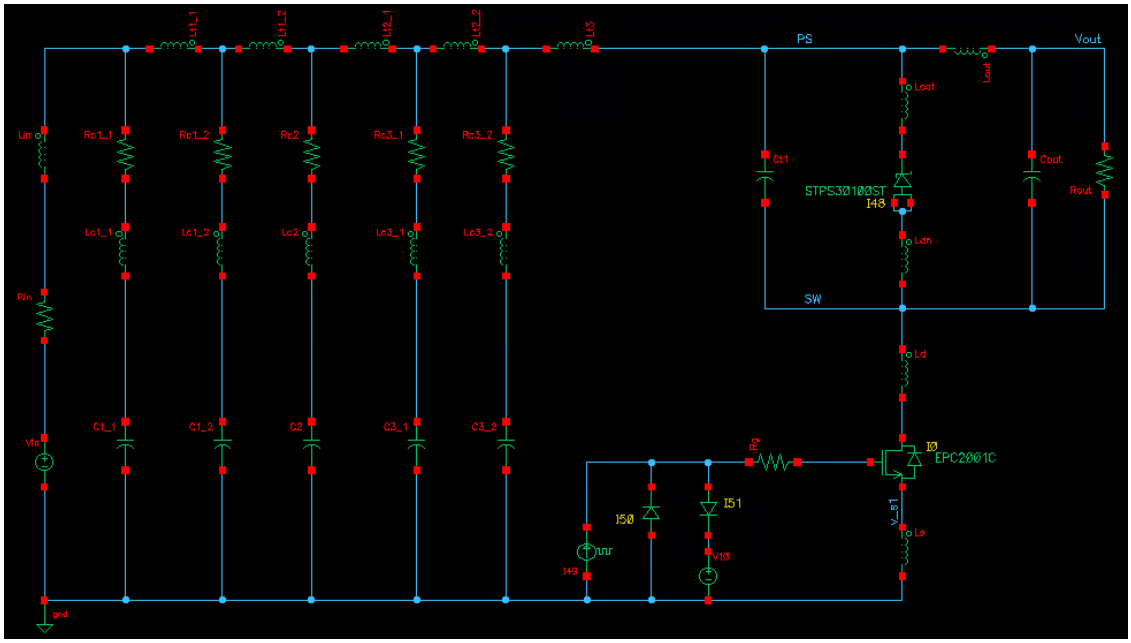

Figure A.1: Cadence Virtuso schematic of the circuit proposed in Section 3.1 (Fig. 3.1).

The netlist generated with the ADE environment from this schematic is reported below, and each of its parts is explained to allow the readers to better understand their functions. The netlist can be essentially divided in three part.

- The first part of the netlist contains the *Library Comments* prefixed by the

symbols "//" and the simulator language definition, in this case *spectre*. The next two lines define the reference node of the circuit and the list of the used parameters.

```
// Generated for: spectre
// Design library name: BuckConverterAGD
// Design cell name: BuckConverterSchematic
// Design view name: schematic
simulator lang=spectre
global 0
parameters Vout=12 Iout=16.5 Vin=48 per=1u Rg=18 TotCycle=10
Ncycle=50 Rout=Vout/Iout Dutycycle=Vout/Vin*per
```

• The body of the netlist includes all the components of the circuit with their values. For this schematic the components values are listed in Table 3.1. All the components with a *pspice* netlist need to be included in the simulation environment by importing the netlist provided by the manufacturers. In this particular case, the *pspice* model of the ECP2021C and of the STPS30100ST diode are included in the simulation environment.

```
// Library name: BuckConverterAGD
// Cell name: BuckConverterSchematic
// View name: schematic
I48 (net12 net33 net12) STPS30100ST
Lt3 (PS net6) inductor l=100p
Ld (SW net34) inductor l=1n
Lt2_2 (net6 net5) inductor l=1n
Lt1_2 (net4 net3) inductor l=1n
Lt2_1 (net5 net4) inductor l=1n
Lt1_1 (net3 net2) inductor l=1n
Lin (net2 net18) inductor l=10u
.
.
C1_2 (net24 0) capacitor c=220u
Cout (Vout SW) capacitor c=270u
Rout (SW Vout) resistor r=Rout
Rc2 (net4 net25) resistor r=50m
I51 (net7 net32) IdealDiode2
I50 (0 net7) IdealDiode2
I0 (net017 net34 v_s1) EPC2001C
```

• The last part of the netlist includes the simulator options, with the simulation type parameters, in this case, a transient simulation. This last part includes also the inclusion files, and the save options, that provide information about the data

to store.

```
simulatorOptions {list of options}
tran tran stop=Tsim {list of simulation parameters}
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save I0:drainin
saveOptions options save=allpub
pspice_include "/home/design/pspice_files/DRB238NS100.lib"
pspice_include "/home/design/STPS30100ST/design.pspice"
include "/home/design/IdealDiode2/spectreText/spectre.scs"
include "/home/design/EPC2001C/spectreText/spectre.scs"
```

Figure A.2 shows the schematic implemented in the *Cadence* environment, to simulate the simplified circuit proposed in Fig. 3.2. All the components that makes up the circuit belong to *AnalogLib* library of the software.

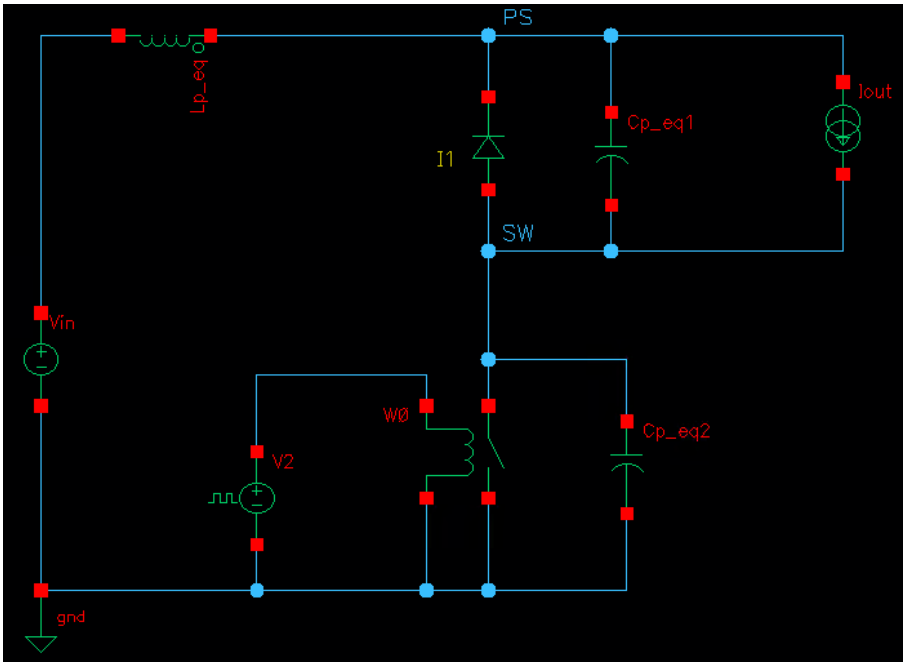

Figure A.2: Cadence Virtuso schematic of the circuit proposed in Section 3.1 (Fig. 3.2).

The netlist of this circuit has brought below:

```
// Generated for: spectre
// Design library name: BuckConverterAGD
// Design cell name: BuckConverterSimpleSchematic
// Design view name: schematic
simulator lang=spectre
global 0

// Library name: BuckConverterAGD
// Cell name: // Design cell name: BuckConverterSimpleSchematic
// View name: schematic
W0 (SW 0 net4 0) relay vt1=2.4 vt2=2.6 ropen=1T rclosed=1m
I1 (SW PS) IdealDiode2
Vin (net06 0) vsource dc=48 type=dc
Iout (PS SW) isource dc=16.5 type=dc
V2 (net4 0) vsource dc=5 type=pulse val0=5 val1=0 period=100u
Cp_eq2 (SW 0) capacitor c=493p
Cp_eq1 (PS SW) capacitor c=638p
Lp_eq (PS net06) inductor l=2.95n
simulatorOptions options {list of options}
```

By simulating the circuit shown in Fig. A.1 and in Fig.A.2, the switching currents reported in Fig. 3.8 are obtained. More precisely, the former returns the waveforms plotted in red, while the latter returns the blue waveforms.

R_t and G_t implementation

In the simulation environment, the R_t and G_t components are implemented by exploiting the *Verilog-A* language, as introduced in Section 3.2.3. Figure A.3 shows the structure and the symbols proposed for these components.

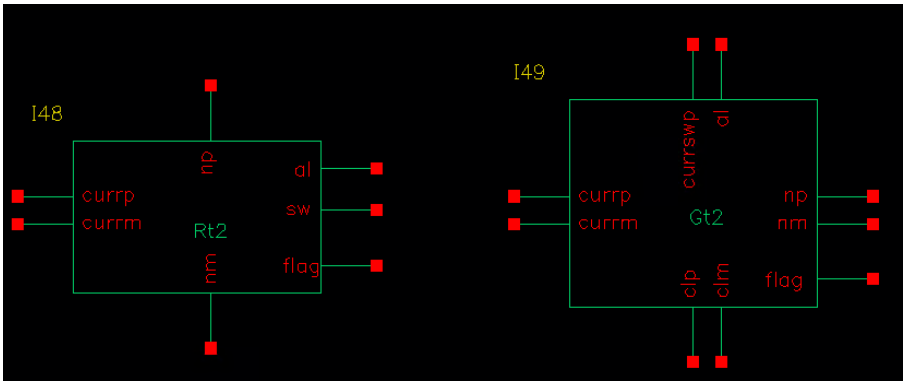

Figure A.3: Cadence Virtuso symbols of R_t and G_t components.

By referring to the R_t, it includes 7 terminals:

- *al* that senses the voltage V_{in}.
- *np,nm* that represent the nodes of the time variant resistance.
- *currp,currm* that monitor the current flowing in the freewheeling diode.
- *sw* that senses the voltage of the switching node.
- *flag* that provides the user with an output that indicates when the R_t is active.

The code of the R_t component is listed below:

```
 1 `include "constants.vams"
 2`include "disciplines.vams"
 3 module Rt2(np, nm, sw, al, currp, currm, flag);
 4 inout np, nm;
 5 input sw, al, currp;
 6 output currm, flag;
 7 electrical np, nm, sw, al, currp, currm, flag;
 8 real tmp, res, fl;
 9 parameter real fr1 = 116.71e6;
10 parameter real perc = 0.1;
11 parameter real Iout = 0;
12 analog begin
13 @ (initial_step) begin
14 res = 1p;
15 tmp = 1p;
16 end
17 tmp = 1/(I(np,nm)*3.14*alpha)*ddt(V(al,sw)); //Iout
18 res = 1p;
19 if  (I(currp,currm)<=1n && I(np,nm)>=1n &&
20 V(al,sw)<(V(al)-V(al)*perc/100)) res =tmp;
21 if (res<=0) res=1p;
22 fl = 1;
23 if (res == 1p) fl = 0;
24 V(np,nm)<+ res*I(np,nm);
25 V(flag)<+ fl;
26 end
27 endmodule
```

This component calculates for each instant of time the R_t value, storing it inside the variable *tmp*. The *if statement* in line 18 allows to establish if the turn-on voltage transitions is occurring, by monitoring the currents flowing through the

switch, through the diode and its voltage drop. In this condition the R_t behaves as indicated in (3.4), otherwise it assume the value of 1pΩ.
The G_t includes 9 terminal:

- the *al* node, that monitors the voltage V_{in}.
- the *np* and the *nm* terminals that are the nodes of the time variant resistance.
- the node *currswp* to monitor the current I_{sw}.
- the nodes *currp* and *currn* for monitoring the diode current.
- *clp* and *clm* to sense the load current
- *flag* that sends an output that advises the user about the G_t activity.

The *VerilogA code* for this component is listed below:

```
 1 `include "constants.vams"
 2 `include "disciplines.vams"
 3 module Gt2(np, nm, al, currp, currm, currswp, clp, clm, flag);
 4 inout np, nm;
 5 input al, currp, currswp, clp;
 6 output currm, clm, flag;
 7 electrical np, nm, al, currp, currm, currswp, clp, clm, flag;
 8 real tmp, g, fl;
 9 parameter real fr2 = 107.9e6;
10 parameter real perc = 0.1;
11 analog begin
12 @ (initial_step) begin
13 g = 1n;
14 tmp = 1n;
15 end
16 tmp = -1/(V(np,nm)*3.14*fr2)*ddt(I(currswp,np));//; al
17 g = 1n;
18 if  (I(currp,currm)<=I(clp,clm)-I(clp,clm)/100*perc &&
19 V(nm)<V(al)-0.1 && I(currswp,np)<I(clp,clm)) g = tmp;
20 fl = 0;
21 if (g == tmp) fl = 1;
22 I(np,nm)<+ g*V(np,nm);
23 V(flag) <+ fl;
24 end
25 endmodule
```

The G_t component works in complementarity with the R_t. In this case the *if statement* in line 18 and 19 allows to establish if the turn-off current transient is occurring. In this case, the conductance G_t assumes the value defined in (3.5) otherwise it is 1nS.

These two components, placed in series and in parallel with the power switch, allow to obtain the switching waveforms shown in Fig. 3.9 and in Fig. 3.10. The parametric waveforms can be obtained by sweeping the values of $f_{r,1}$ and $f_{r,2}$ in order to change the k values. The R_t and the G_t components, combined with the power switch, have been used also to obtain the optimal switching waveforms in the complete circuit, as discussed in section 3.5 and shown in Fig. 3.32.

Appendix B

R_t and G_t in other topologies

In this Appendix the possibility to obtain the optimal switching waveforms in other converter topologies, and consequently to have reference waveforms to obtain the AGD parameters, is assessed by means of simulations. Firstly, a high side buck converter and a synchronous one are analyzed, and finally the proposed technique is validated on boost (step-up) converter with the same proposed methodology. The aim of this analysis is to establish if it is possible to obtain the optimal switching waveforms, exploiting the R_t and the G_t in all types of hard switching converters.

B.1 High side buck converter

Fig. B.1 shows a comparison of a low side buck converter with a high side one, highlighting that the definition of the switching waveforms can remain exactly the same. In fact, the simulations of these two circuits returns the same switching

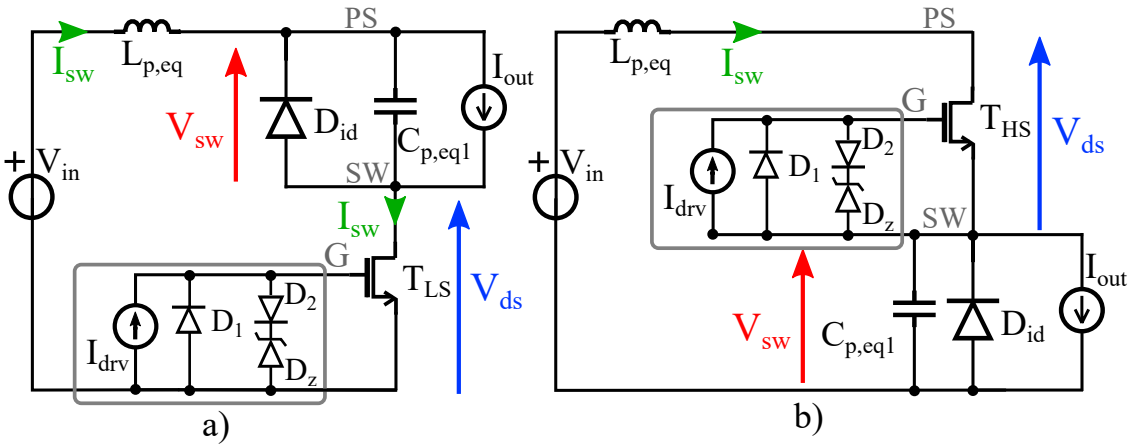

Figure B.1: a) Low side buck converter and b) high side buck converter. The same state variables are shown with the same color.

waveforms, as shown in Fig. B.2, by red and yellow lines. This is essentially because the current flowing in the parasitic inductance $L_{p,eq}$ is the same in both the circuit, and because the power transistor is driven in the same way in both the circuits. The possibility to define the state variables of the high side converter in same way of the low side one, allows to perform on such circuit the same mathematical analysis carried out in Section 3.2, and so, of exploiting the R_t and the G_t components in the same manner. The optimal switching, obtained by placing the R_t and the G_t

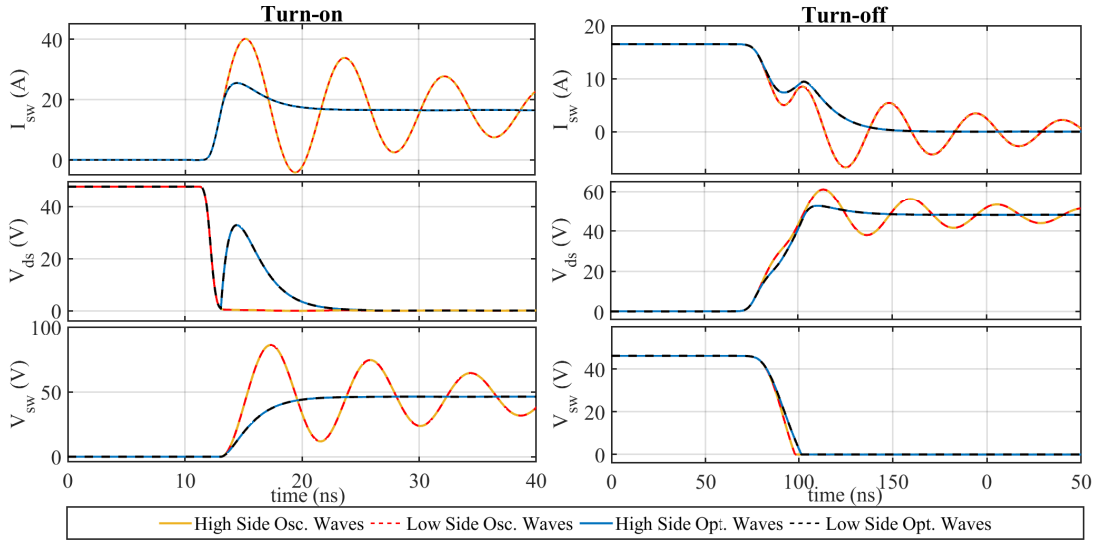

Figure B.2: Switching waveforms in low side and high side buck converters.

components in series and in parallel to the power transistor respectively, are shown in Fig. B.2 (blue ad red lines). The comparison of such waveforms highlights that the two circuits behaves in the same way, allowing the designer to use exactly the same optimal switching waveforms to find the power transistor driving parameters. Also the ideal driving parameters returned by the tuning algorithm are the same, but in a real case some difference can result, if the high side and the low side AGD have different features. This first analysis allows to establish that it is possible to find and use the optimal switching waveforms both in low side and high side converters.

B.2 Synchronous buck converter

In this section the R_t and G_t behavior is validated in a synchronous buck converter, in which the freewheeling diode is substituted with a enhancement power transistor. Also in this case the R_t and the G_t allow to obtain switching waveforms free of oscillations, but it is necessary to drive also the freewheeling transistor. It is important to highlight that the new transistor does not need no particular driving

waveforms, but also that it is turned on and/or off in the right instant of time. Fig. B.3(a) shows a synchronous low side converter while Fig. B.3(b) an high side one. Both the circuits include the R_t and the G_t components.

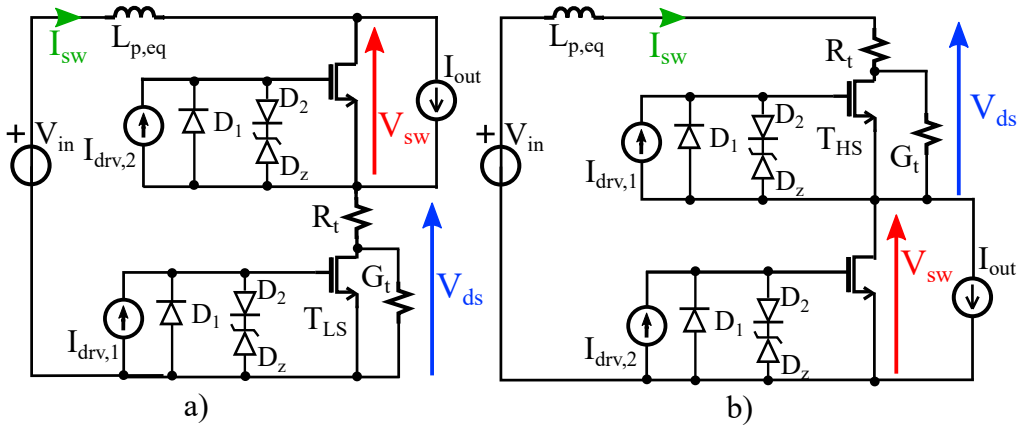

Figure B.3: a) Low side *synchronous* buck converter and b) high side *synchronous* buck converter. The same state variables are shown with the same color.

More precisely, by referring to a low side synchronous buck converter, it is possible to obtain the optimal switching waveforms firstly turning-on the low side transistor, and than turning-off the high side one immediately after that the current I_{sw} has reached the nominal I_{out} value, when the R_t starts to work. In this way the high side transistor works like it was the freewheeling diode. This behavior can be seen in Fig. B.4 (left side), in which are highlighted the trigger signal for the turn-on and the turn-off of the two transistors.

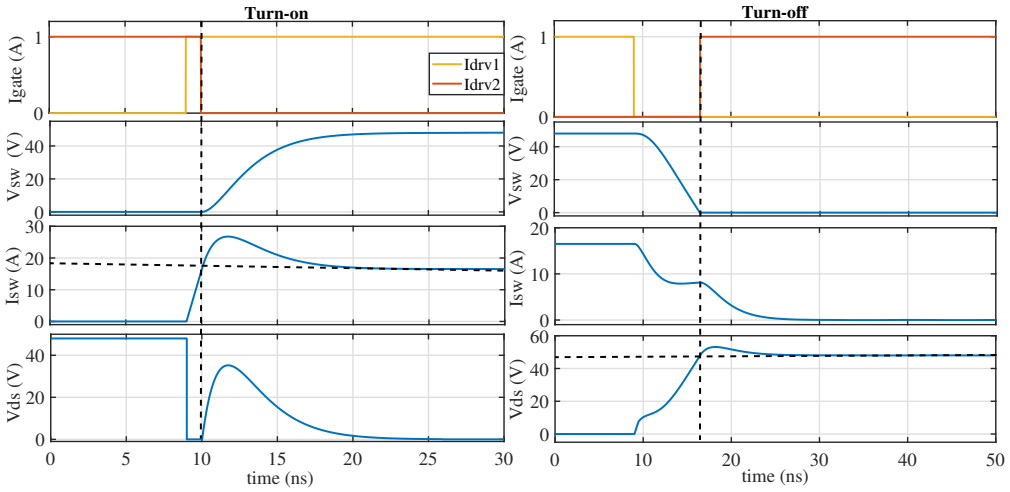

Figure B.4: Turn-on and turn-off optimal switching waveforms in high side and low side synchronous buck converter.

Instead, at the turn off, the G_t can work normally if the high side transistor is turned-on after that the low side one is turned-off. More precisely, the trigger to turn-on the high side transistor must be send after that the voltage V_{ds} has reached its nominal value V_{in}. At this point, the current I_{sw} starts to decrease and the G_t can work normally, to damp the oscillations. This behavior is shown in Fig. B.4 (right side), in which the trigger signals of the two transistors are highlighted. The proposed analysis allows to generalize the use of R_t and G_t to all the converter topologies that exploit an *half-leg* of transistors to convert voltages and currents.

B.3 Optimal switching waves in a boost converter

In this section, the proposed analysis is validated in a boost converter. Fig. B.5(a) shows the high frequency model of a generic boost converter, that can be derived in the same way proposed in Section 3.2.3 for a buck converter.

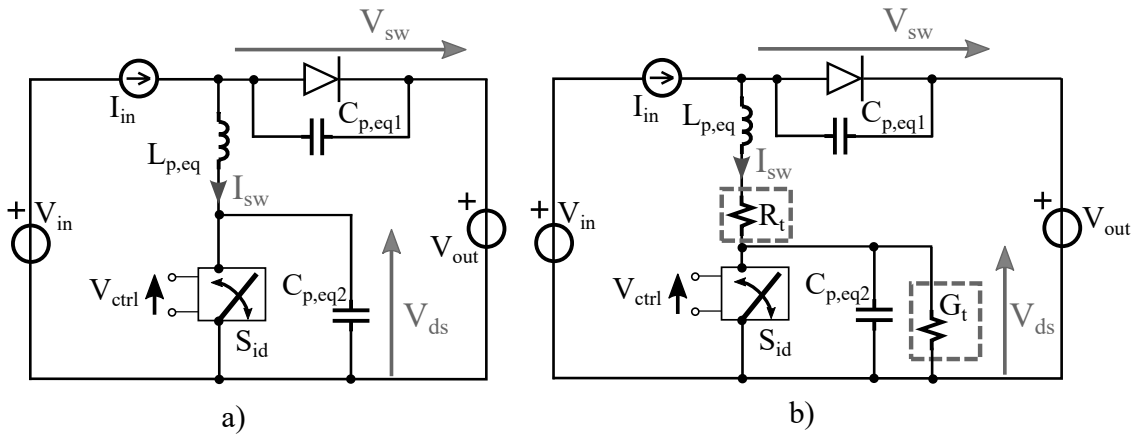

Figure B.5: a) High frequency model of a boost converter and b) high frequency model of a boost converter including R_t and G_t.

Similarly to the buck converter, at the turn-on of the transistor S_{id}, the voltage V_{ds} decreases rapidly, and the current I_{sw} and the voltage V_{sw} starts to increases only when the freewheeling diode is completely off. This means that, also in this case, the oscillations are triggered by the transition of the voltage V_{sw}, so the $R_t(t)$ can be used in the same way of the buck converter. The only difference is that the switched current is the input one instead of the output one. Similar considerations can be done for the turn-off, that allow to use the G_t like in a buck converter. In fact in this situation, the oscillation are triggered by the I_{sw} current transition. For the boost converter, the only difference is that the switched voltage is V_{out}, while in the buck converter is V_{in}. Detailed switching waveform obtained by simulating a boost converter are shown in Fig. B.6. The oscillating waveforms are plotted by red line, while the ones obtained exploiting the R_t and the G_t components are

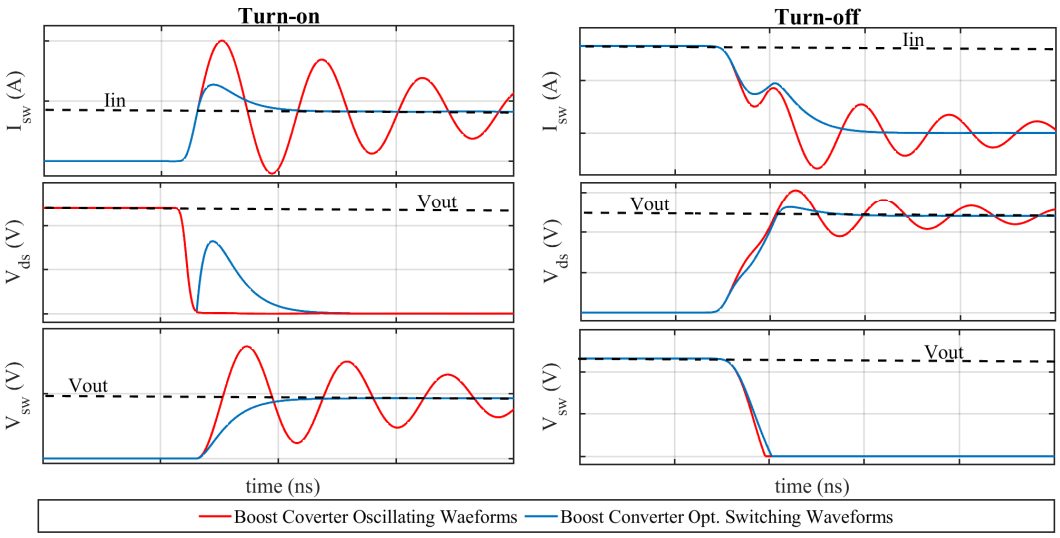

Figure B.6: Turn-on and turn-off switching waveforms in a boost converter. In red the oscillating waveforms while in blue the optimal switching ones.

plotted with blues lines. Also in this case, the waveforms result to be completely free of oscillations.

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