First Measurements on the Timespot1 ASIC: a Fast-Timing, High-Rate Pixel-Matrix Front-End

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First Measurements on the Timespot1 ASIC: a Fast-Timing, High-Rate Pixel-Matrix Front-End

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Abstract: This work presents the first measurements performed on the Timespot1 ASIC. As the second prototype developed for the TimeSPOT project, the ASIC features a 32×32 channels hybrid-pixel matrix. Targeted to space-time tracking applications in High Energy Physics experiments, the system aims to achieve a time resolution of 30 ps or better at a maximum event rate of 3 MHz/channel with a Data Driven interface. Power consumption can be programmed to range between 1.2 W/cm^2 and 2.6 W/cm^2. The presented results include a description of the ASIC operation and a first characterization of its performance in terms of time resolution.

Keywords: Hybrid detectors, Particle tracking detectors, Timing detectors, Front-end electronics for detector readout, VLSI circuits, Analogue electronic circuits, Digital electronic circuits.

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1 Introduction

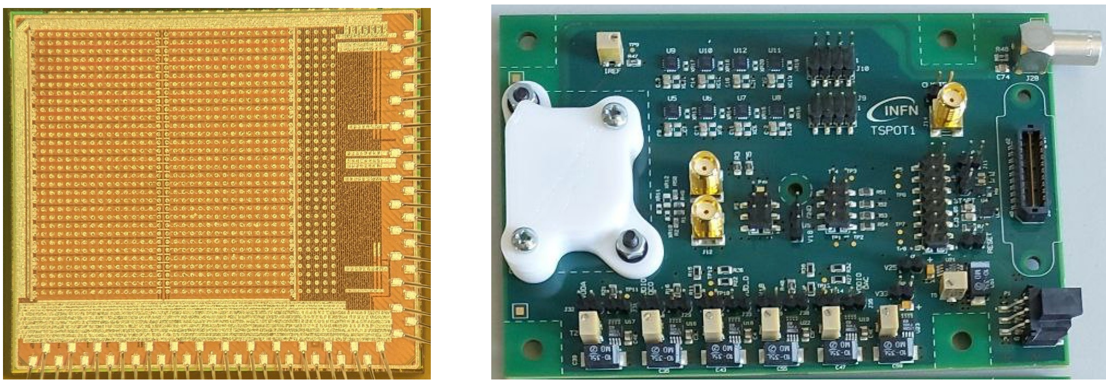
Future upgrades on High Energy Physics experiments aim to improve their capability to detect rare events by increasing the beam luminosity [1]. When operating in high luminosity regimes, current tracking techniques will no longer be sufficient to efficiently reconstruct the event. A proposed solution to this problem is adding a fine time measurement to the position information [2][3][4]. The TimeSPOT project [5] aims to build a small scale telescope demonstrator suitable for future experiments. The activity of the projects consists in both designing and testing of the whole detector including its sensors, front-end ASIC and readout electronics.

This article presents the first results from electrical tests on the Timespot1 ASIC. This front-end chip was designed to cope with a required timing resolution of 50 ps per single hit with an event rate per unit area larger than 11.6 GHz/cm^2. These requirements must also be met while keeping the power consumption per unit area below 1.5 W/cm^2 in order to be compatible with cooling. Furthermore, the candidate TimeSPOT 3D-Silicon sensor has experimentally proven to be capable of reaching a intrinsic time resolution better than 20 ps [6][7], establishing a new challenge for the FE electronics. In section 2 the ASIC architecture is briefly described. Pixel performance measurements are illustrated from the point of view of the time resolution of both the Time to Digital converter (TDC) in section 3 and the Analog Front-End electronics (AFE) in section 4.

2 Chip Architecture

A picture of Timespot1 is shown in figure 1a. The 2.6 mm $\times$ 2.3 mm chip is manufactured in a 28 nm CMOS commercial technology. This prototype is bump-bondable to sensors with a 32 $\times$ 32 pixel matrix with a pixel pitch of 55 µm. Five more columns of 32 dummy pixels are inserted to ensure mechanical stability. Input-Output signals and supply voltages are delivered through wire-bonding. The wire-bond pads are located on two adjacent sides of the chip making it two-side tileable. The ASIC has a data-driven interface.

The pixel matrix is organized in two symmetrical blocks of 16 $\times$ 32 pixels. Each block includes two service columns: a digital one for pixel generated data distribution and pixel programming,



(a) Timespot1 ASIC.
Chip size: 2.6 mm × 2.3 mm.

(b) TSPOT1 PCB. Board size: 8 cm × 12 cm. The ASIC is mounted on the left side under the white removable cover.

Figure 1.

and an analog one incorporating four independent service DACs, a band-gap and a programmable cell used to perform a fine setting of power consumption of the AFE components. Analog and digital circuits have independent power and ground nets in order to prevent cross talk, these nets are also included in the respective columns. For the same reason all the analog circuit has been realized inside dedicated triple-n-wells. All the nets are then redistributed by a repeated double row configuration of 16 × 2 pixels. Each pixel has a reduced pitch of 50 µm in the horizontal direction compared to the bond-pad matrix. In this way every 16 pixel 75 µm can be reserved to host the lateral service columns, making the design indefinitely repeatable.

The pixel architecture is presented in figure 2. Every pixel includes the AFE directly connected to the sensor pad as well as its dedicated TDC. The AFE chain is comprised of an input and inverter based Charge Sensitive Amplifier (CSA) with DC current compensation and a Leading Edge Discriminator (LED) with discrete-time Offset Compensation (OC). The TDC is based on a Vernier architecture with its two Digital Controlled Oscillators (DCO) clocked around 1 GHz. Every channel generates a 24 bit word which is then transmitted serially at 160 MHz. A charge injection capacitance is also included in every channel for testing purpose.

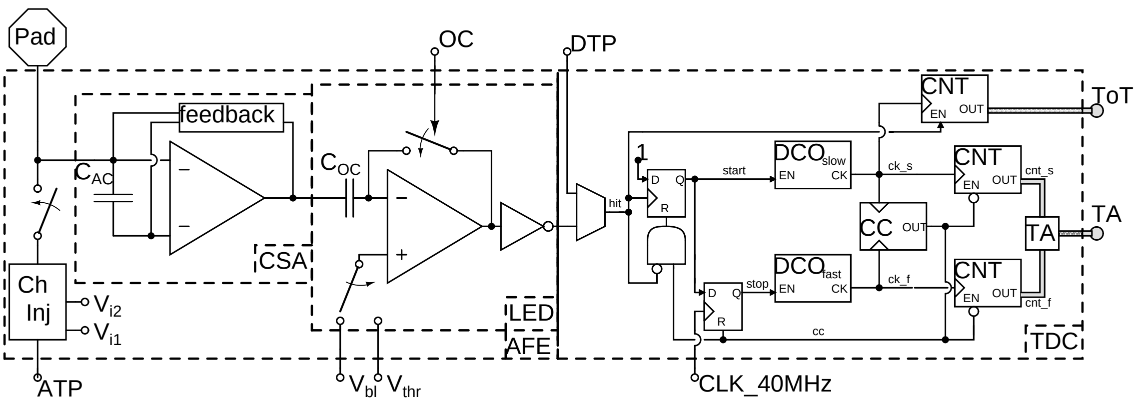


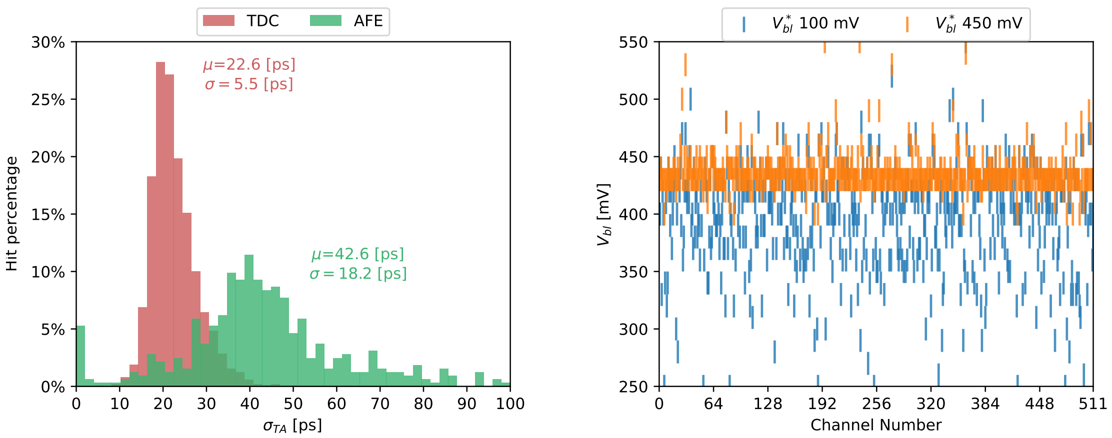
Figure 2. Schematic representation of the pixel architecture.

Data generated at pixel level are then redistributed to the chip periphery using four independent Read Out Trees (ROT). Each of these combinational blocks connects one fourth of the matrix to two multiplexed output links after a proper de-randomization by mean of a FIFO layer. The ASIC has in total 8 LVDS output drivers at 1.28 Gb/s each. Configuration is provided by an I^2C interface. Additionally an LVDS receiver is used to provide the system clock and a CMOS input is used as a Start signal providing absolute time reference.

The TSPOT1 PCB (in figure 1b) was designed both for chip standalone testing and as part of the final demonstrator. It provides ASIC grounding and power supplies using on-board LDOs as well as sensor biasing. The board also interfaces the ASIC with FPGA via QTH connector for data IO and provides the system clock via SMA connectors.

3 TDC Measurements

The TDC measures the phase between the input signal and the 40 MHz reference clock with a resolution dependent on the frequency difference of its two DCOs. The input signal triggers the activation of the slower DCO while the next 40 MHz clock rising edge, providing the stop signal, activates the faster DCO. Every period the phase between the two oscillators shrinks until it reverts. The count of the number of periods when this condition arises encodes the timing measurement. This kind of measurement will be referred to as Time of Arrival (TA). The TDC will simultaneously measure the Time over Threshold (ToT) of a signal. Due to the higher jitter associated with this parameter, a lower resolution is required for this measure: it is performed by directly counting the number of DCO period between the rising and falling edges of the pulse. DCOs calibration is crucial to extrapolate a reliable measure. This calibration is automatically operated by a per pixel self procedure.



(a) Red histograms: σ_{TA} on 100 repeated DTP across 1024 channels and 7 phases. Green histogram: σ_{TA} on 100 repeated ATP across 512 channels for a 2 fC input signal (MIP), the TDC contribution has been square subtracted.

(b) Baseline values obtained from threshold scan on 512 channels. The desired baseline is V^*_{bl}. At 100 mV OC fails to bringing V_{bl} to uncompensated higher values. At 450 mV the OC is working properly for most of channels.

Figure 3.

From the point of view of the self-test capability a Digital Test Pulse (DTP) can be injected. The signal can be programmed by changing its phase to 7 different sub-reference values and its width to 32 values. In order to measure the timing resolution the same measure has been repeated multiple times, the standard deviation on this measure is then used to quantify the resolution. This analysis can be repeated for different parameters in order to study dependencies. This communication focuses on measurement on TA resolution since its constitutes the most critical measurement for timing. The ToT measurement has exhibited an overall time resolution of 0.6 ns which is adequate to measure the intended signal. TA measurements have been repeated 100 times for each channel and for all the 7 input phases. Standard deviation of TA (σ_{TA}) is computed for each case, the results are collected in the histogram figure 3a. In this condition the TDC consumes 25 µW of power.

4 Analog FE Measurements

The AFE adapts the sensor current signal into a digital pulse to be processed by the TDC. The CSA produces a steep voltage signal with amplitude proportional to the input integrated charge. This charge is collected on the parasitic feedback capacitance and discharged with a constant current. In this way the signal ToT is proportional to the input charge enabling its measurement. Corrections based on ToT measurements can be used to reduce the effect of the time walk. LED offset compensation is operated by firstly saving the desired baseline voltage V_{bl}^* on the memory capacitance C_{OC} and then rising the threshold to V_{thr}. This operation is performed by switching between two voltages provided by dedicated DACs.

The AFE can be tested by injecting an Analog Test Pulse (ATP) by switching between two voltages. In this way a charge up to 7 fC can be injected. The ATP is always injected synchronously with the next reference clock rising edge, its TA represents the systematic propagation delay of the AFE. The signal is then directly measured by the pixel TDC. CSA signals can be characterized by threshold reconstruction on repeated signals. In order to quantify AFE contribution to the total σ_{TA}, the TDC contribution can be square subtracted from it. The total is computed from ATP, while the TDC contribution from DTP.

The AFE resolution is presented in figure 3a. In this condition the circuit consumes 15 µW of power. An issue with OC was found: the circuit is unable to set the base line to low values. This behaviour can be attributed to an unexpected voltage value across C_{OC} before compensation. The default voltage of this node is closer to V_{DD} compared to the one indicated by simulation, making the compensation time insufficient to move actual V_{bl} to the lower values. This behaviour is presented in figure 3b. The OC issue forces the setting of V_{bl}^* to 450 mV ($V_{DD}/2$) or higher. In this regime the P-type input differential cell of LDE limits its bias currents resulting in a loss of bandwidth and therefore slew-rate. By correlating V_{bl} position with σ_{TA} it is possible to understand this behaviour as presented in the plots of figure 4. This analysis shows that the actual CSA performance is masked by the LED issue and the TDC resolution. The CSA is capable to produce signal with a timing resolution better than 20 ps. It is noted that the OC compensation issue is not an intrinsic problem of the LDE design and therefore it can be solved with minor adjustments on the scheme.

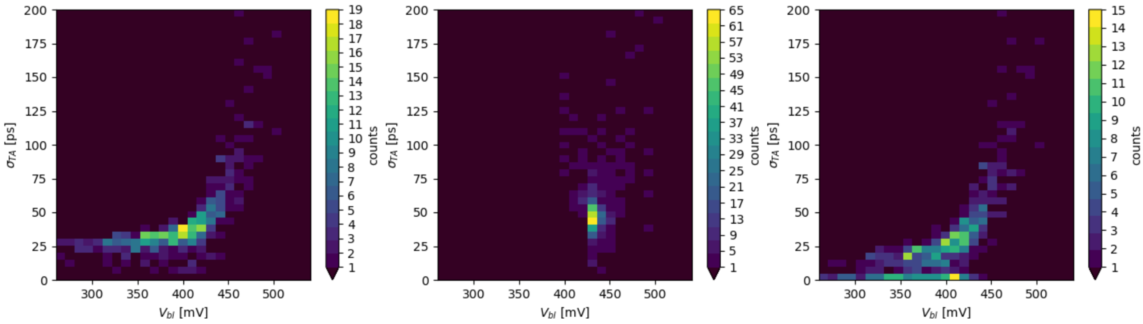


Figure 4. Correlation between measured σ_{TA} and V_{bl}. From left to right: V_{bl}^{*} 100 mV (case of OC failure), OC at V_{bl}^{*} 450 mV and V_{bl}^{*} 100 mV with TDC contribution removed. AFE total resolution is affected by LED baseline position. Channels with low V_{bl} shows CSA intrinsic resolution.

5 Conclusions

The Timespot1 ASIC has been tested in standalone configuration.The TDC resolution is below 50 ps, with an average of 23 ps. From the point of view of the AFE the resolution has been quantified to be under 100 ps with an average of 43 ps. All measures have been performed within the specified power consumption constraint of 40 µW per pixel. The tests illustrated in the present paper show the possibility of improving the performance of the proposed architecture with minor corrections. Measurements with the actual sensor matrix and particle generated signals will be performed in the near future.

Acknowledgments

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