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Metal and dielectric based materials for power semiconductor performance improvements

By

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Declaration

I hereby declare the contents and organization of this dissertation constitute my own original work and does not compromise in any way the rights of third parties, including those relating to the security of personal data.

Roberta Busca

2021

* This dissertation is presented in partial fulfillment of the requirements for **Ph.D. degree** in the Graduate School of Politecnico di Torino (ScuDo).

A Davide

che ha vissuto questo percorso insieme a me,

da collega, amico e compagno.

E ai miei genitori

che mi hanno sostenuto in questi anni universitari.

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I am grateful to the Department of Applied Science and Technology of the Polytechnic University of Turin and to Vishay Semiconductors Italiana S.P.A. Manufacturing and Assembly Departments, Reliability Laboratory and Failure Analysis Laboratory, for their kind support and the resources invested in this work.

I would like to thank all the colleagues from Vishay Semiconductors Italiana S.P.A. and the Polytechnic University of Turin, for their valuable advices and dedication on the topic.

As this four-year long commitment comes to a close, I move towards a new adventure with a heaped and valuable wealth of experience. A significant amount of these skills is because of Giovanni Richieri, mentor and supervisor, and his deep knowledge in this sector, as well as his passion in teaching future generations.

In this appreciation I would like to mention Rossano Carta, R&D Director, to have encouraged my progression and boosted my career with high level requirements.

While employing and continuing improving these competences, in a new position, as Manufacturing Process Engineer, I would like to thank the Borgaro Power Modules Group, for this opportunity and the trust placed in me.

To me, doctoral studies were not meant to obtain just a title, but they were the opportunity for a learning period. And in this perspective, I feel grateful because I have earned both.

During this time, I grew up personally as well as professionally, because of all the interactions, the friendships and respectful relationships I have cultivated in this journey, and I hope to carry on in the future. Among all, I would like to thank Davide Cimmino for his support as colleague, friend and partner. We shared part of the path in this Ph.D., collaborating in projects and publications, and we created enjoyable moments with other colleagues also, in the forms of travels, meetings and celebrations. These moments enriched this experience, and I give them a weight close to the other mentioned for my professional development.

In conclusion I am grateful to my parents, Anna Maria and Pierpaolo, and to my family for their support during all the university years, and their drive in believe in myself.

Abstract

Reliability is the key to match automotive sector needs. Innovation is exploded providing new opportunities and introducing new challenges, but robustness is still the most important feature above the others.

For this reason, power devices need to match AEC-Q101 global standards, and in some cases go beyond.

In parallel, higher device reliability is becoming a common requirement in industrial and consumer applications. Humidity robustness reached strong attention since power modules, commonly adopted for these purposes, are required to be operating outdoor as indoor.

When humidity diffuses through the package, a variety of deteriorating mechanisms initiates and a progressive reduction of the electrical performance lead to a failure.

The ability to combine optimal design and most efficient materials results in extended lifetime and improved resistance of devices in harsh working conditions.

This study is developed with a test-and-model systematic approach to obtain a full explanation of phenomena behind the principal failure modes and achieve the best structure.

Commonly, power semiconductor devices can be described with two main sections: active area and termination. Current capability and dynamic performances are determined by active area. On the other hand, termination plays a dominant role in controlling the rated blocking voltage value, combining ad-hoc design structure and multi-layer passivation schemes

Both the regions influence the electrical field distribution, but its shape is significantly modulated by termination layout and composition. Furthermore, recent approaches consider design and passivation materials as an integrated ensemble that should be optimized simultaneously.

A typical passivation scheme includes a semi-resistive and dielectric layer framework made of inorganic and organic materials.

In this thesis work a high-voltage temperature humidity bias (HV-THB) test is adopted to investigate interaction and synergy between the various above-mentioned materials.

This test consists in three different simultaneous stressors applied to the devices:

- High voltage, corresponding to 80% of the nominal voltage Vnom
- High operating temperature (85°C)
- High relative humidity environment (RH 85%).

Their concurrent action can trigger specific device failures. These failure modes are successively examined in order to understand the different degradation mechanisms involved.

The principal effects observed are:

- aluminum erosion
- dendrite formation on silicon resistive layer
- bubble formation in organic film passivation.

Several studies report HV-THB tests on high-power silicon devices. These investigations highlight direct connection between passivation layer degradation and high electric field presence in specific regions of the device. Moreover, the presence of humidity acts as catalyst for chemical–physical deterioration processes.

Principal degradation reactions affect:

- solder and contact metals
- amorphous silicon resistive layer
- dielectric layers such as silicon oxide and silicon nitride.

A model for each of them is proposed in this thesis and a complete description of the context is fulfilled.

Summarizing the results and conclusions of this study, the interactions between different materials constituting the termination structure of power diodes devices have been investigated, while a process optimization and layout improvement have been accomplished.

The combination of high voltage, temperature and relative humidity has appeared to be the most stressful one for the devices, and HV-THB's capability to trigger failure modes has been employed to analyze the principal degradation phenomena. Furthermore, a full description of the involved chemical physical mechanisms has been proposed.

Eventually, thanks to the integration of TCAD simulations, this research contributed to validate new device designs with optimized passivation structure and superior reliability performances.

Prefazione

Durante questo Dottorato in Scienze dei materiali svolto presso il Politecnico di Torino, in collaborazione con Vishay Intertechnology, ho visto da vicino tutto il flusso di lavorazione di wafer di silicio, per arrivare alla produzione di diodi di potenza. Combinando il mio lavoro da Process Engineer e Scienziata dei materiali ho partecipato a progetti di ricerca, sviluppo e qualifica di processi.

I principali materiali che ho utilizzato appartengono a queste tre categorie: ossidi, dielettrici e metalli, che rappresentano una parte importante dello spettro delle proprietà della materia e possono essere suddivisi tra isolanti o conduttori. La loro combinazione ottimale su semiconduttori a base silicio è fondamentale al fine di produrre i dispositivi elettronici comunemente utilizzati.

Questo lavoro di tesi è stato incentrato sull'analisi delle proprietà e delle caratteristiche di questi materiali e di come influenzano i processi, quindi il risultato.

La struttura di questa tesi rispecchia da un lato il lavoro che ho effettuato come Scienziata dei materiali, dall'altra quello da Process Engineer, e presenta una parte iniziale dedicata allo sviluppo e al controllo dei processi (Capitoli 1 e 2), ed una successiva dedicata ai materiali divisi per categorie di appartenenza: conduttori (alluminio e nickel, Capitolo 4) e isolanti (silicio amorfo e nitruro di silicio, Capitolo 5).

Contents

Chapter 1

Process engineering

1.1 Aspects of Process Development, Improvement and Optimization

This thesis work starts with a description of the principal approaches to process analysis. The impact these strategies had on the entire project is evident and represents the headlight which has driven the objectives during this three-year long period. In effect, since this Ph.D. has been developed in collaboration with a company, producing and applying effective solutions to business processes has constituted an essential aspect of the research work. Thus, the aim has been not only obtaining results about materials general properties, but also using this knowledge to create, adapt and better the final assembled products through industrial process development, improvement and optimization.

Process development is used to establish a specific manufacturing process. It ensures a product can be routinely made and meet specifications before manufacturing at scale. These first aspects are required to obtain quality, affordability, and reproducibility [1].

Process development (PD) activities should lead to the establishment of what is termed the “design space”, which represents the combination of variables and parameters that have been demonstrated to assure the required quality. In general, process development studies provide the basis for process improvement, validation and control [2]. The aim is to identify any critical and key aspect that needs to be monitored and controlled because it could affect the product critical characteristics, performance or yield.

Process optimization is usually introduced consequently, and its goals are minimizing cost and maximizing throughput. If optimization follow improvement, the produced changes are extremely more efficient [3].

In any case, optimization and improvement are very different activities. Optimization is about playing within the known constraints as best one can. On the other hand, improvement is about breaking through these constraints to reach a much higher level of performance.

Optimization usually involves an empirical test and validate method and different cycles to be obtained. Moreover, it requires a solid base to be implemented on. There is no optimization without a Definition of metrics to be optimized, a complete evaluation of the Measuring ability of these metrics and an Analysis of obtained data. Using the Lean Six Sigma methodology these are the first three phases of DMAIC flow.

In this context errors, issues and problems represent chances for improvement.

On the other hand, unsolved problems act as fuels for another fundamental dimension as well, that can radically shift markets and produces impacts far more significant than improvement and optimization. This dimension is innovation.

Differently from the others two, innovation not always needs a solid platform to start, but it surely expects a need to be satisfied.

Joseph Schumpeter is often thought of as the first economist to draw attention to innovation. He defined five types of innovation in the 1930s [4]:

- Introduction of a new product or a qualitative change in an existing product.
- Introduce a process new to an industry.
- The opening of a new market.
- Development of new sources of supply for raw materials.
- Changes in industrial organization.

The second point of this list stresses the role processes have in the industrial sector, and more in general, when a large-scale production is implemented. Their importance is at the same level of the creation of a new product. For this reason, researching on them is to be considered equally remarkable and effective.

1.2 The importance of Process control

When a process, no matter if innovative or not, is defined and introduced in production it requires to be controlled.

The complexity of semiconductor-based devices has led to a tight relationship between processes and manufacturing problems to be solved. In particular, these last ones seems to be a constant presence whenever a new process is introduced.

For this reason, management has recognized the importance process control plays in manufacturing environment since 90s to prevent and immediately identify any drift in process trends [5]. Moreover, economic reasons, besides technical ones, press to have an ever-better characterization of both individual steps and overall processes [6] [7]. Since a single wafer could contain thousands of good products, the damage could be significant in terms of profits. Thus, any materials, equipment or process anomaly need to be detected before it cause yield losses or reliability failures.

More in detail, process control has three goals:

1. assuring that a process is operating properly
2. if this is not, assuring to obtain the information necessary to activate corrective actions

3. facilitating the introduction of new products in a production with high yield standards

In electronics manufacturing, process control often is associated with statistics, so the complete name is statistical process control (SPC). The word “statistical” means great number of data and the ability to analyze them in search of conclusions and solutions [8].

In this context, the terms “process” may sound too extensive, because it could assume many different meaning. Maintaining a general approach, a process is a set of conditions which act mutually to produce a result. In operations they usually consist of a series of fabrication steps [9]. When process control is introduced it is important to define what are the key parameters or causes it will be operate on. So the process might be:

- a single tool/ machine or just an element of it,
- a single human being or a single motion he/she performs,
- a method of testing, measuring or processing,
- a combination of the three above,
- a mental activity or any related intangible human elements such as motivations, soft skills…

Clearly a common agreement on this aspect is fundamental in an organization.

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Chapter 2

Materials and processes

2.1 Processes in semiconductor manufacturing

In semiconductor device fabrication, the various processing steps fall into four general categories: Deposition, Removal, Patterning, and Modification of electrical properties [1].

Deposition is any process that grows, coats, or transfers a material onto the wafer. In this group, sputtering techniques represent one of the principal methods to produce thin metal layers, as well as evaporation. Chemical vapor deposition, both plasma enhanced (PECVD) or not (CVD), is adopted for monocrystalline, polycrystalline, amorphous, epitaxial materials which may include: silicon (dioxide, nitride, oxynitride), carbon (fiber, diamond and graphene), titanium nitride and various high-k dielectrics.

Removal processes are any that remove material from the wafer either in bulk or selective form and consist primarily of etch processes, both wet and dry. In this context, different approaches can be adopted. For deposited materials, the use of these processes is necessary to create a structure on wafer and obtain a good contact or adhesion. For crystalline silicon substrate, removal etch is used to reduce residual stress and thickness instead.

Patterning covers the series of processes that are required to mask and shape (in combination with etch) the deposited materials and is generally referred to as lithography.
Modification of electrical properties has historically consisted of doping materials by diffusion furnaces and later by ion implantation. These doping processes are followed by furnace anneal or in advanced devices, by rapid thermal anneal (RTA) which serve to activate the implanted dopants [2].

2.2 Materials and processes in this Thesis

In this thesis work different materials have been studied and applied to the state of art of power semiconductors to test their properties and robustness. In all these cases a strong influence of the adopted process has been found.
This is not surprising, considering the new available tool technologies which present numerous variables a process engineer can operate on. If on one hand, this progress has significantly contributed to the resolution of several issues, on the other hand it has incremented necessary steps for process development.
A focus on the impact of process on materials and vice versa has led to a full characterization of the layers. Moreover, these results have contributed to the explanation of the different failure modes encountered during reliability stress tests.
To discuss data and conclusions, one material at time will be investigated, following the layer by layer approach adopted during the experimentations. Here a general introduction is proposed, before dedicated Chapters are presented.

2.2.1 Metals

Metals discussed in this thesis have been deposited via sputtering. Process development started with the evaluation of the impact of deposition power, temperature and atmosphere on layer characteristics. In effect, temperature influences significantly grain dimension for aluminium [3], and power could

introduce more residual stress in nickel [4]. Gas adopted for plasma can modify their structure producing new compounds. Nickel sputtered in nitrogen atmosphere, for example, generates nitrides which result in completely new properties in terms of stress and morphological aspects, evident by XRD analysis..

2.2.2 Oxides

Oxides are adopted in electronics for many reasons: to passivate devices, to prevent conduction paths between metallization layers and to mask the substrate during doping.

There are several oxides used in electronics: hafnium oxide (HfO_2), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), aluminium oxide (Al_2O_3) and many others (Table 2.1). Their unique properties in term of dielectric constant, modulable band gap and physical interface make these materials truly versatile. However due to its stable equilibrium with its precursor, silicon dioxide is still on the most studied and implemented candidate [5].

Table 2. 1. Property comparison for selected high-k candidates. Key: mono. = monoclinic; tetrag. = tetragonal. Table from Wallace, Dielectric Materials For Microelectronics, 2017 [5].

Material	Dielectric constant (k)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO_2	3.9	8.9–9.0	3.2–3.5[b]	Amorphous
Si_3N_4	7	4.8[a] – 5.3	2.4[b]	Amorphous
Al_2O_3	9	6.7[h] – 8.7	2.1[a] – 2.8[b]	Amorphous*
Y_2O_3	11[d] – 15	5.6–6.1[d]	2.3[b]	Cubic
Sc_2O_3	13[d]	6.0[d]		Cubic
ZrO_2	22[d]	5.5[a] – 5.8[d]	1.2[a] – 1.4[b]	Mono., tetrag., cubic
HfO_2	22[d]	5.5[d] – 6.0	1.5[b] – 1.9[c]	Mono., tetrag., cubic
La_2O_3	30	6.0	2.3[b]	Hexagonal, cubic
Ta_2O_5	26	4.6[a]	0.3[a,b]	Orthorhombic
TiO_2	80	3.05–3.3	≈ 0.05[b]	Tetrag. (rutile, anatase)
$ZrSiO_4$	12[d]	6[d] – 6.5	1.5[b]	Tetrag.
$HfSiO_4$	12	6.5	1.5[b]	Tetrag.
$YAlO_3$	16 – 17[d]	7.5[d]		**
$HfAlO_3$	10[e] – 18[g]	5.5–6.4[f]	2–2.3[f]	**
$LaAlO_3$	25[d]	5.7[d]		**
$SrZrO_3$	30[d]	5.5[d]		**
HfSiON	12–17[i,j]	6.9[k]	2.9[k]	Amorphous

Silicon oxides can be growth and deposited but they also form a thin uniform layer under air exposition on native silicon. Depending on how they are produced these oxides can be divided in:

- Native oxides
- Thermal oxides
- Deposited oxides or Low thermal oxides

The first one is a consequence of chemical thermodynamic equilibrium of silicon with atmospheric O_2. For this reason, if no further treatments are performed on the substrate, the surface is composed by a thin (12 to 20 angstroms) layer of SiO_2. This film is usually removed with an HF treatment, to prevent bad contact areas. After cleaning, hydrogen atoms complex the dangling bonds and prevent oxidation for some hours [3].

Oxides thermally grown are the purest and are usually preferrable in power semiconductor devices, due to their excellent electrical characteristics. However deposited ones are likewise adopted as second layer and densified via thermal anneal to uniform their properties. Low temperature oxides have various

advantages. The first one is a demotion time, significantly shorter than the growth ones. Another benefit is the relative low temperature required for their deposition which allow them to be used when materials sensible to thermal variations are present [6].

Oxides used in microelectronics are exclusively amorphous. With a slight lower density compared to crystalline oxide (2.20 g/cm^3 Vs 2.65 g/cm3), amorphous SiO_2 presents an “open structure” (Figure 2.1) [7]. For this reasons this material is permeable to impurities. This permeability is usually attributed to non-covalent oxide as well.

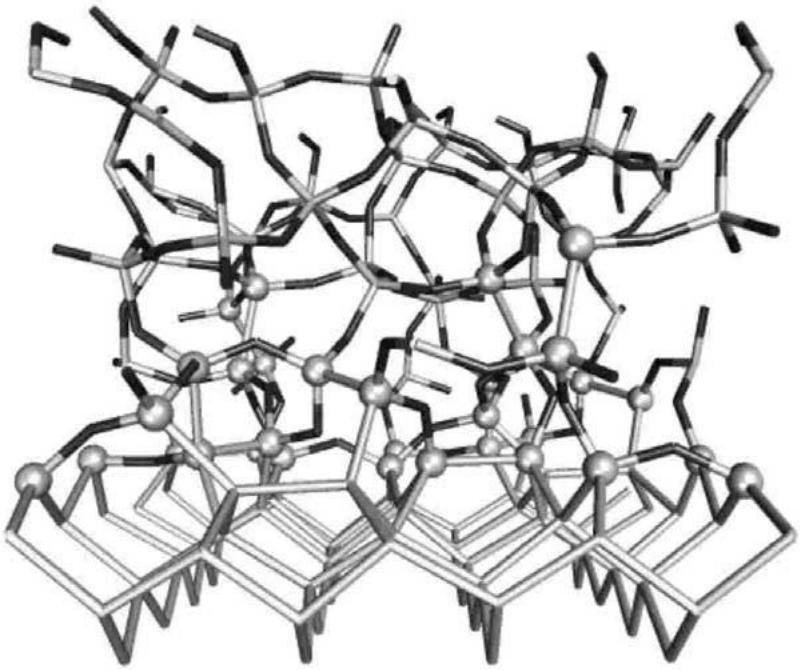

Figure 2. 1. Ball and stick representation of a model interface between Si (001) and amorphous oxide. Figure from A. Bongiorno et al., Mater. Sci. Eng. B (2002) [7].

In this work, contact angle measurements have been used to evaluate humidity and impurity penetrations varying low thermal oxide precursors and doping [8] [9]. These evaluations helped to validate failure mode mechanisms of devices working in high voltage, high temperature and high humidity conditions.

2.2.3 Dielectrics and resistive layers

Dielectrics are an important class of thin-film materials for microelectronics. In power semiconductors when referred to dielectrics, usually High-k dielectrics are intended. More in detail, this term generally refers to materials which exhibit dielectric constants higher than the SiON films (k≥7). In this group, due to their exceptional strength and insulating properties, silicon nitride is one of the most adopted solutions [10]. Figure 2.2 shows different SiON species in relation to their stability at different temperatures and oxygen relative pressures.

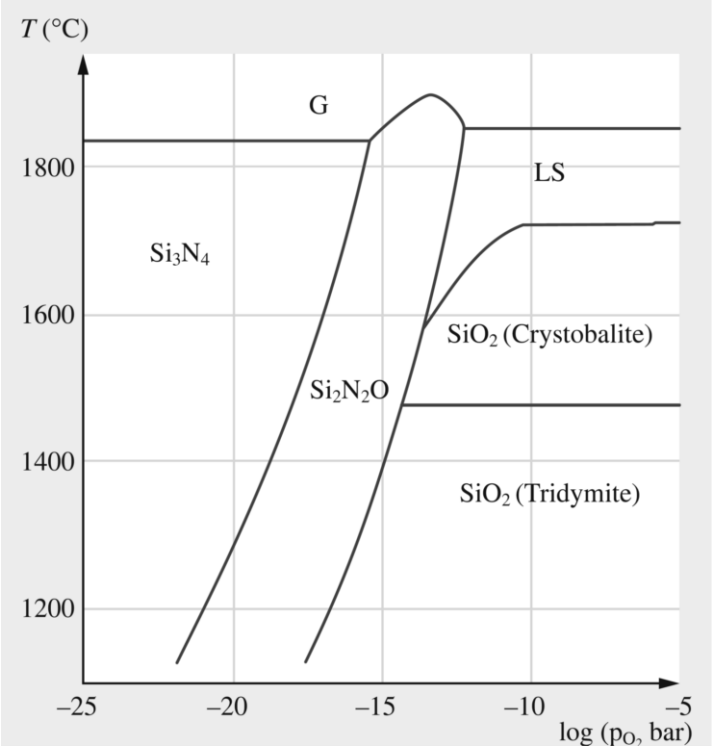

Figure 2. 2. Phase diagram of SiON species varying temperature and oxygen relative pressure [5].

Silicon nitride can be found in two crystalline structures. The α-Si_3N_4 phase is hexagonal, with each nitrogen atom bonded to three silicon atoms in a distorted trigonal planar configuration and each silicon atom tetrahedrally bonded to four nitrogen atoms [11]. The more common phase, β-Si_3N_4, has the phenacite structure consisting of a trigonal arrangement of silicon atoms tetrahedrally bonded to nitrogen atoms as shown in Figure 2.3. When viewed along the c-axis looking down onto the basal plane, a hexagonal arrangement of void channels is visible.

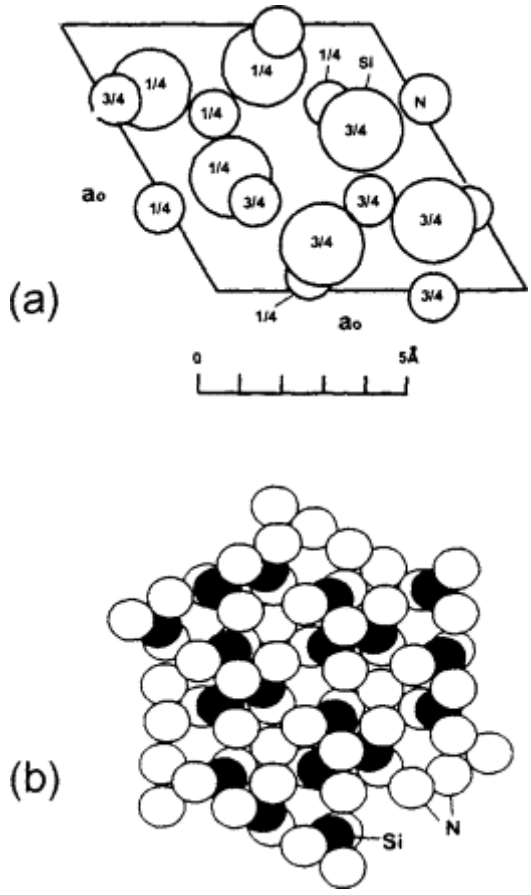

Figure 2. 3. (a) Atomic positions within the β-Si_3N_4 unit cell and (b) top view onto the basal plane showing a hexagonal arrangement of open channels.

Films presented in this thesis have been prepared by Plasma Enhanced Chemical Vapor Deposition (PECVD). This technique provides non-stoichiometric Si_3N_4. This type of layer is classified as SiN_xH_y and is also called plasma silicon nitride films and the hydrogen content can be as high as 35 atomic percent.
Silicon nitride has been used in combination of silicon resistive layers to improve device performance, producing an effective barrier against humidity [12] [13].
Silicon resistive layers are usually produced with Semi-Insulating Polycrystalline-Silicon (SIPOS) or with amorphous silicon. This last one is normally prepared by LPCVD, PECVD or PVD techniques and could be doped n-type (usually with phosphorus) and p-type (usually with boron). Doping changes the resistivity of amorphous silicon by more than seven and six orders of magnitude for n- and p-type doping, respectively. This characteristic may vary due to hydrogen content as well [14] [15].

2.3 How this work approaches material analysis

Today the semiconductor business exceeds $200 billion with about 10% of the revenue derived from power semiconductor devices and smart power integrated circuits [16]. Power semiconductors are recognized as a key component for all power electronic systems and it is estimated that at least 50% of the electricity used in the world is controlled with them. Moreover, considering the widespread use of these technologies in the consumer, industrial and transportation sectors, power devices own a major impact on the economy because they determine the cost and efficiency of systems [17].
Efficiency and reliability are becoming two essential requirements, determine our success in current challenges such as smart electrical mobility and renewable energy, which require to reduce losses, maintenance and waste [18]. For this reason, besides the analysis of materials, in this work a great attention has been paid to improve device robustness and performances.

In effect, recent studies consider design and materials as an integrated ensemble that should be optimized simultaneously, since their combination results in extended lifetime and improved resistance.

In a power diode complete structure, materials could be many. A layer by layer investigation and optimization is therefore necessary. This study is developed with a test-and-model systematic approach to obtain a full explanation of phenomena behind the materials response to stress and to achieve optimized structures.

A high-voltage temperature humidity bias (HV-THB) test has been adopted to investigate interaction and synergy between the various materials.

This test consists of three different simultaneous stressors applied to the devices:

- High voltage, corresponding to 80% of the nominal voltage V_{nom}
- High operating temperature (85°C)
- High relative humidity environment (RH 85%).

Their concurrent action can trigger specific device failures [19]. These failure modes are successively examined to understand the degradation mechanisms involved.

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Chapter 3

Principal parameters and tests

3.1 . Physical parameters

3.1.1 Film stress

Stress measurement, using substrate bowing, is a valuable resource in the definition and control of production processes. It is a cheap, fast and non-destructive technique that can be adopted in process stability monitoring. Samples composed by silicon monitor substrates are measured before and after film deposition. The variation of their warpage is proportional to stress induced by the analyzed layer.

Even if stress data acquisition is simple, its interpretation can be challenging since the final value depends on different parameters. Moreover, its effects on a completed wafer, where different types of films are applied, may vary significantly from expectations.

Stress depends on the thermal expansion characteristic of the involved materials, and it is possible to link stress response to various structural modifications, such as phase transitions and material transport along grain boundaries.

The total thin film stress σ_f is defined as the algebraic sum of the intrinsic stress (σ_i) and the extrinsic or thermal stress $\sigma(T)$

$$\sigma_f = \sigma_i + \sigma(T)$$

The intrinsic one is characteristic of a material and depends on its internal structure or on the conditions to which it has been exposed (e.g. during deposition). On the other hand, the extrinsic or thermal one is strictly related to the thermal expansion of the involved material. Thus, the equation can be expanded as

$$\sigma_f = \frac{1}{6}\frac{E_s h_s^2}{(1-v_s)h_f}\left(\frac{1}{R_2}-\frac{1}{R_1}\right) - (\alpha_s - \alpha_f)(T-T_0)\frac{E_f}{1-v_f}$$

Where α_s and α_f are the coefficient of thermal expansion of the substrate and the film respectively, $(T-T_0)$ is the temperature difference between the deposition temperature and the measure temperature, E_f is the Young's module of the film and E_s is the Young's module of the substrate. With the same nomenclature, v_f is the Poisson's ratio of the film and v_s of the substrate, h_f is the thickness of the film and h_s of the substrate. R_2 and R_1 are the curvature after and before the film deposition.

Considering the intrinsic contribute, two different type of responses are possible (Figure 3.1):

- Compressive (negative values)
- Tensile (positive values).

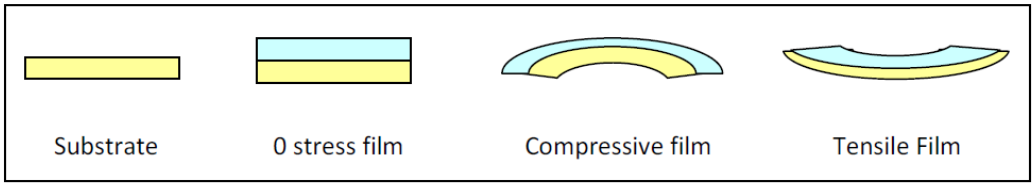
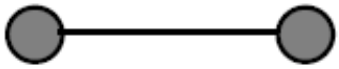


Figure 3. 1. Scheme of substrate reaction to different types of films.

To understand how film-induced stress affects a substrate, a description of the involved interactions is necessary.

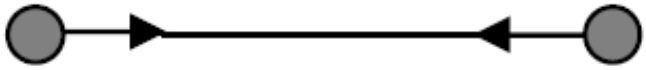
In a zero-stress material, the atoms are *averagely* positioned at the equilibrium, in a potential well. For this reason, they will not tend to increase or lower their distance, and this results in no force applied.



In a compressive stress state, atoms are positioned at a lower distance compared to their equilibrium. Thus, they tend to move away each other, producing a force responsible of a negative bowing.

Compressive stress involves high energies. Most deposited films, which requires highly energetic sources, such as with Sputter or PECVD, present this behavior [1] [2].

In a tensile state, atoms are positioned at a greater distance compared to their equilibrium. For this reason, they tend to move toward each other producing a bowing with a positive value.



Tensile stress is typical of crystallization and reticular bonding formation, but also very low-density materials may present it.

Considering a Lennard Jones surface, tensile and compressive stress can be represented as two opposite forces acting to repristinate the lowest potential state.

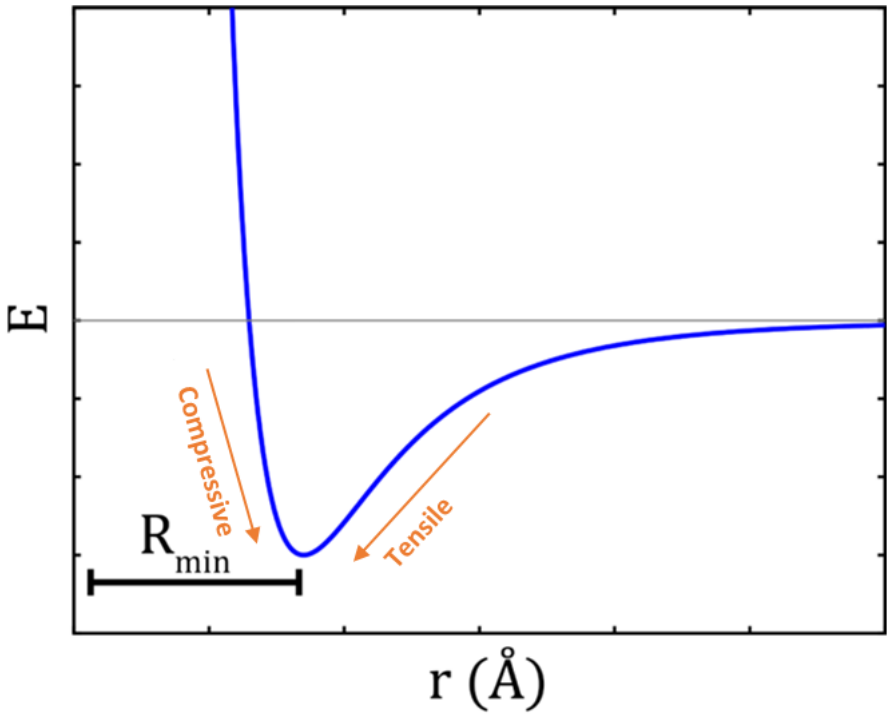


Figure 3. 2. Lennard Jones curve with details on compressive/tensile stress induced forces. The Lennard-Jones potential models interactions between two particles: they repel each other at very close distance, attract each other at moderate distance, and do not interact at infinite distance. In the graph, potential energy is represented as a function of the distance of the pair of particles. The potential minimum is at R_{min}, where compressive and tensile forces are balanced, and particles are at equilibrium distance. E represents the difference between energy zero at infinite distance and energy at R_{min}.

On the other hand, the thermal contribution is easy to understand, and related the thermal expansion coefficient of the two coupled material (film and substrate).

If the deposited one is characterized by a larger expansion, it will produce a tensile stress during cooling, and this is the case of aluminum on silicon.
On the contrary, if it has a smaller expansion coefficient, it will result in compressive stress. Example of this behavior are silicon oxides on silicon interfaces [3].

Table 3. 1. Sum up of the principal responses to external factors in the creation of compressive or tensile stress types.

TENSILE STRESS	COMPRESSIVE STRESS
Cooling a material with higher thermal expansion coefficient compared to the substrate	Cooling a material with lower thermal expansion coefficient compared to the substrate
Crystallization of a material with higher density on solid state compared to liquid state (exception for materials with very strong covalent bonding such as silicon and germanium)	Crystallization of a material with lower density solid state compared to liquid state
	Formation of grain structures or compounds
	Void or impurity inclusion

3.1.2 Sheet resistance

Surface resistivity or sheet resistance (Sres) is the measurement of resistance across the surface of a material in contact with electrodes. Figure 3.3 shows a simple configuration adopted in this type of analysis. Measuring Sres is a fast, non-destructive method to determine the electrical resistivity of flat materials. Thus, its applications the semiconductor industries are extensive.

To avoid confusion with volume resistance (which is expressed in the unit of ohm), sheet resistance is expressed in ohms per square (Ω/□).

In the method represented in Figure 3.3, the surface resistivity ρ is calculated from the relation:

$$\rho = R\frac{l}{W}$$

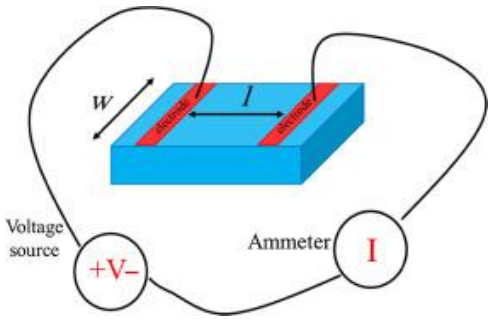


Figure 3. 3. Simple method for measuring surface resistivity.

where l is the distance between the two electrodes, R is the measured resistance, and W is the width of the sample.

The primary technique for measuring sheet resistance is the four-probe method (also known as the Kelvin technique), which is performed using a four-point probe. This tool consists of four electrical probes in a line, with equal spacing between each other as shown in Figure 3.4.

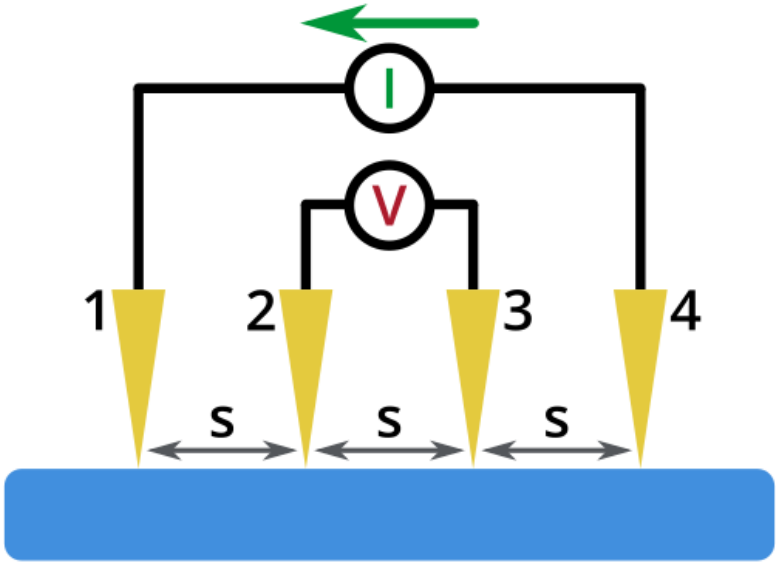


Figure 3. 4. schematic diagram of a four-point probe. The four probes have equal spacing (s) and are shown in contact with a surface. A current (I) is injected through probe 1 and collected through probe 4, whilst the voltage is measured between probes 2 and 3.

It operates by applying a current (I) on the outer two probes and measuring the resultant voltage drop between the inner two. The sheet resistance can then be calculated using the equation:

$$R_s = \frac{\pi}{\ln(2)} \frac{\Delta V}{I} = 4.53236 \frac{\Delta V}{I}$$

3.2 Electrical and reliability tests

3.1.2 High Voltage Temperature Humidity Bias Test (THB)

High Voltage Temperature Humidity Bias Test (THB-HV) is currently the state of the art test method for reliability evaluation of power devices in high humidity environments at high voltage. These conditions have become especially significant in the case of power modules for the automotive industry and other

applications in harsh environments. The current standard automotive THB test (H3TRB) sets the conditions of the test at 85 °C, 85% relative humidity (R.H.), and a maximum reverse bias of 100 V, with a no failure requirement of 1000 h for product qualification [4]. Several works on THB-HV testing [5] [6] [7] [8] highlight the importance of raising the voltage level, in some cases up to 90% of the device nominal voltage, in order to accelerate the test and evaluate the DUTs ruggedness against the presence of the previously described failure modes.

Moreover, the management of the test itself can introduce stress factors in addition to the main ones, so standardizing the test methodology becomes fundamental in order to get as much information as possible from the test.

For this research work, a custom system for active monitoring of THB-HV testing has been developed, in order to intercept device degradation in real time and allow for a controlled and more accurate failure analysis of the DUTs [9].

DUTs are positioned in the climatic chamber, which is then ramped up to 85 °C and 85% R.H. conditions. After waiting for 30 min, the voltage ramp is applied with a duration of 30 min. When the ramp reaches the selected voltage level, the test is officially started, and the regime conditions are shown in Table 3.2.

Table 3. 2. Set of stressors applied during the test.

PARAMETRES	**VALUES**
Temperature	85°C
Relative humidity	85%
Voltage	80% V_{nom}

At selected time steps of 168, 500, 1000 h (or more if needed) all DUTs are removed from the chamber, and after 12 h of rest at room conditions, a curvetracer measurement is performed. This process is repeated at each time step until a device exceeds the selected threshold criteria, or the test is deemed as over.

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Chapter 4

Conductors

4.1 Metals

In semiconductor devices fabrication, metals are adopted to create a junction with the silicon substrate. Depending on the junction final properties, a Schottky barrier or an ohmic contact can be obtained.

These physical characteristics are particularly important when comparing metals in terms of interaction with the substrate. With AlSi alloy a very high barrier height (over 1eV) can be measured [note that nominally pure aluminum has a φ_{bn} (Schottky barrier on n type silicon) of 0.7eV. The corresponding φ_{bp} (Schottky barrier on p type substrates) is 1.15eV - 0.7eV = 0.45eV (bandgap of silicon - φ_{bn}= φ_{bp})].

To create a good and stable junction between metal and silicon, a lot of process parameters must be considered. Depending on thermal treatments, surface preparation, aging time before metal deposition, the system behavior may change [1].

In any case, metals can play different roles on wafer, resulting in products for various applications. Two principal categories are solderable and bondable die to be assembled respectively in discrete and module devices. In this thesis work,

adopted metals can be divided in two ensembles depending on their function: contact metals and solder metals. The first group is responsible for the ohmic contact and the wire bonding process. Among others, aluminum is the principal candidate. The second ones assure a correct adhesion of the solder paste during assembly and they are usually made of a three metal layer structure with chromium or titanium, nickel and silver on top.

The first part of this work has been dedicated to assure an in-control process of each metal layer forming the structure on wafer. Thickness and uniformity are two of the principal aspects to be settled to match design structure and assure a durable and robust soldering process when assembled. Nevertheless, higher blocking voltage and current capability usually prefers thicker metalization, for these reasons reflectivity and surface morphology could become crucial parameters as well.

After an evaluation of parameters influencing uniformity and reflectivity, both related to materials physical characteristics and deposition process, a detailed study of metals behavior under stress conditions has been performed.

Since this work started with aluminum process evaluation and control, this thesis is following the same order, dividing the discussion by metal type. Paragraphs from 4.2.0 to 4.2.8 are dedicated to aluminum, the next ones, from 4.3.0 to 4.3.5, to nickel alloys.

4.2 Aluminum

Aluminum is a soft, non-magnetic and ductile material, with lower density if compared with other common metals. Chemically, being part of the boron group tends to form compounds in the +3 oxidation state. The strong affinity towards oxygen leads to the formation of a protective layer Al_2O_3, named alumina. This very superficial film protects the bulk from further oxidation and represents a powerful shield against chemical and physical attacks.

In the context of power semiconductors devices, the importance of aluminum behavior increases in specific zones, Figure 4.1 reassumes these differences.

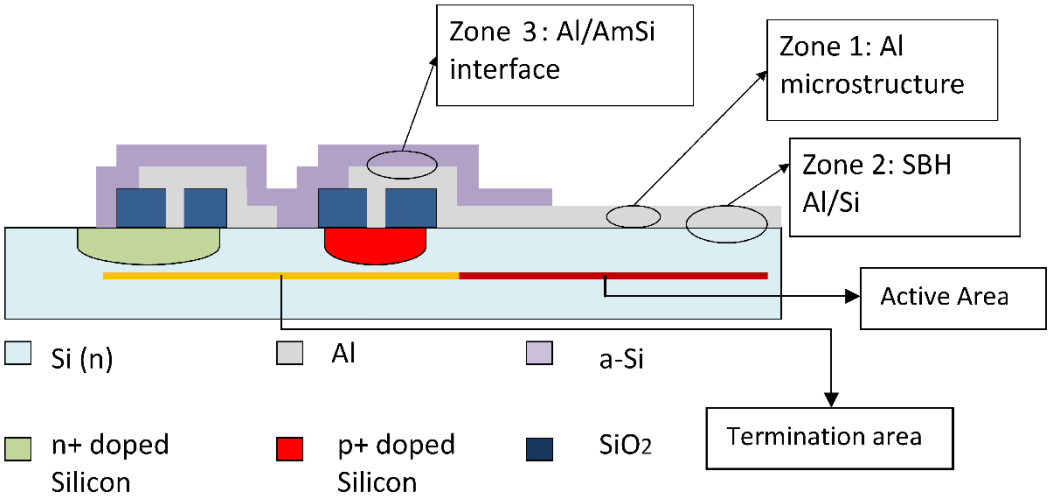


Figure 4. 1. Schematic representation of a power diode with detail on aluminum characteristics.

We can distinguish two main regions: the termination and the active area. In planar diodes the active area (AA) is mainly responsible for the conduction characteristics of the device, such as forward voltage drop. On the other hand, the efficiency of termination is important to reach the maximum breakdown voltage (V_z) determined by the epitaxial layer thickness. In this region, the electric field should be accompanied and distributed, avoiding surface peaks. Thus, terminations could assume different designs such as field limiting ring (FLR) structure or junction termination extension (JTE).

In order to assure a good electrical field dispersion, metal conformity and adhesion are far more important in the termination region, while aluminum microstructure and interface play a dominant role in active area, where a good ohmic contact is required to avoid any parasitic voltage drop.

In this thesis, aluminum has been deposited in alloy with a small percentage of silicon, for this reason, when specific process or layer characteristics are

discussed, the acronym AlSi is adopted, while when referred to general chemical-physical characteristic of the element, the name aluminum (Al) is used.

4.2.1 AlSi microstructure

Depending on the adopted process, AlSi layers may present different visual aspects (Figure 4.3 summarizes this variability). Grain structure, surface roughness and cubic formations are some features to consider in this type of analysis.

These effects can influence not only cosmetic appearance but also mechanical and electrical characteristics. For this reason, understanding aluminum microstructure and how it is influenced by deposition parameters is a key to obtain stable results, as well as predictable production processes.

Microstructure should be distinguished from crystal structure, since it is related to grain distribution (size, shape, orientation) and surface topology, instead of describing the relationship between unit cells and spacing. Microstructure ranges between nanometers and centimeters, while crystal structure plays at the atomic level (angstrom). Both are fundamental in the explanation of material properties.

On a macroscopic scale, microstructure is responsible for the opacity of a surface, as well as for the uniformity of its visual appearance. This becomes particularly important when dealing with automatic tools, where visual inspection or pattern recognition are involved. To avoid false signals or scraps a fine tuning of the process is essential.

Aluminum microstructure could be influenced by several variables:

- sputtering temperature,
- substrate preclean and native oxide
- sintering temperature

All these parameters affect the interface between the silicon and the AlSi layer.

On silicon, two different interfaces are possible, Figure 4.2 shows them respectively with and without silicon native oxide formation.

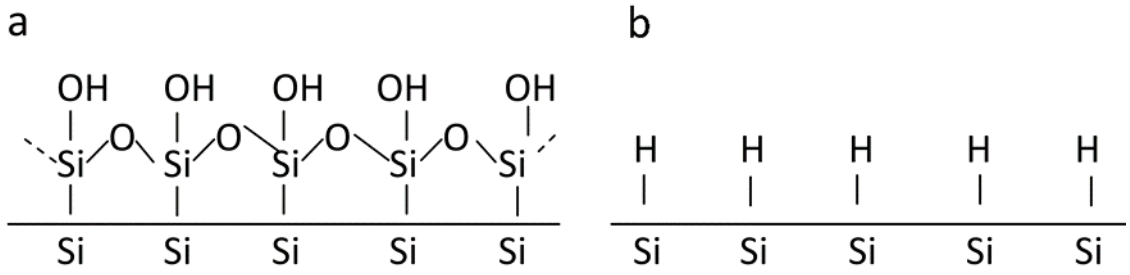


Figure 4. 2. Possible silicon surface terminations, depending on treatment: (a) native surface resulting from air exposure or oxidizing chemicals. (b) H passivated surface resulting from DHF treatment.

The silicon surface when exposed to air, humidity or to oxidizing chemicals forms SiO_2. The silicon-oxygen bond involves valence electrons, producing a strong and stable molecular orbital, where silicon lone electron pairs are shared with oxygen vacant orbitals [2].

When the above-mentioned silicon unpaired electrons are donated to hydrogen forming Si-H, as when the surface is treated with diluted hydrofluoric acid (DHF), the surface results in a steady state. The H passivation inhibits the formation of native oxide, it is possible to process wafers without risks of having a bad contact.

As already proved [1], the presence or the absence of oxygen strongly affects the metal layer growth during deposition. Process temperature impacts microstructure significantly only when the underlying surface is OH terminated.

More in details, if an amorphous silicon oxide layer is present, as the one forming spontaneously in an oxidating environment, the film does not tend to generate a preferential orientation. On the other hand, if the surface is passivated with H, the aluminum film uses the substrate as a template generating a film that is almost monocrystalline with a 45° tilt.

These two types of formations release stress caused by temperature in different ways. Non orientated material relaxes creating grains. On the contrary, on H

terminated layers, Al nucleates forming larger crystals which do not need to rearrange.

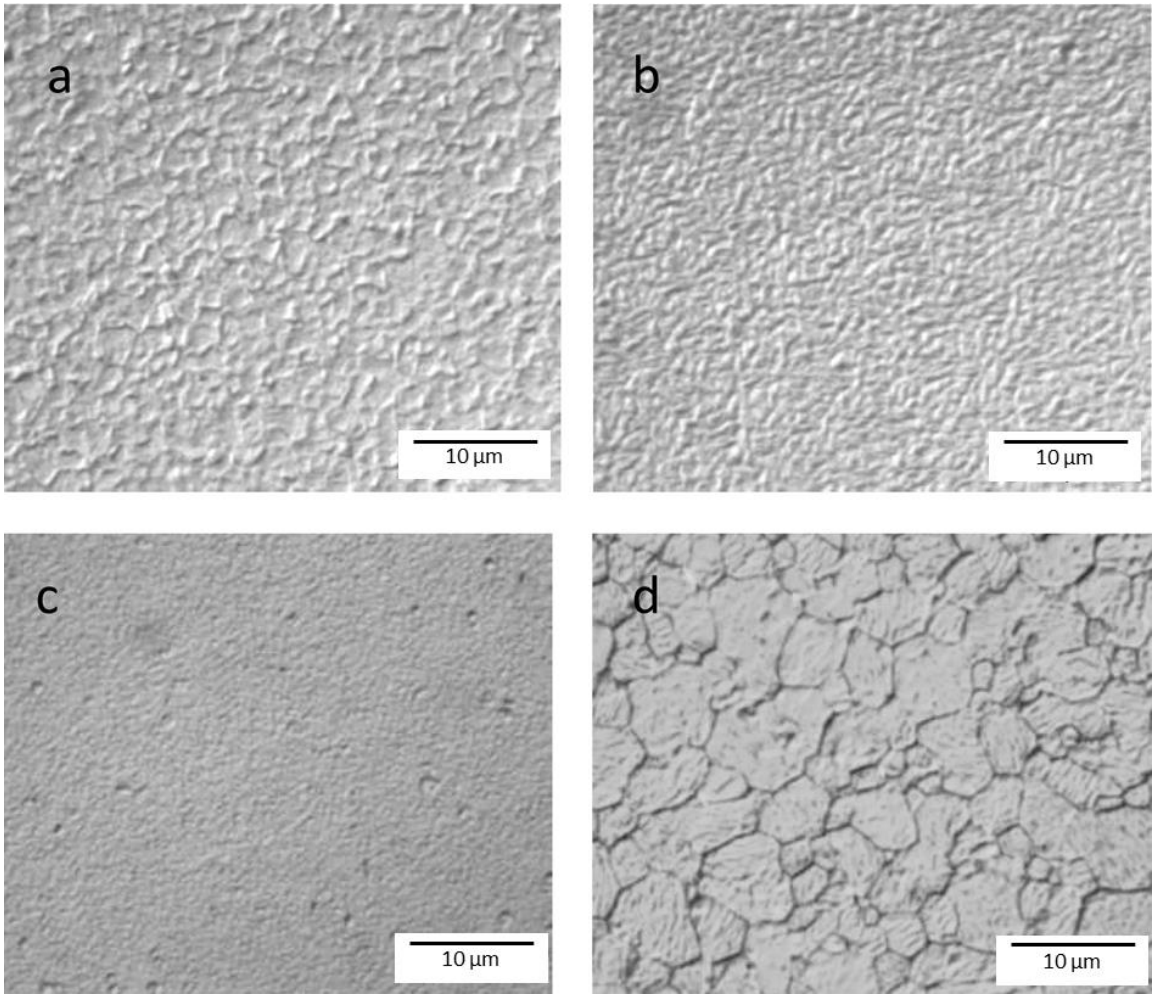


Figure 4. 3. SEM imaging of various AlSi sputtered samples: (a) DHF treated surface, with sputtering process at room temperature. (b) Surface with oxidizing preclean and sputtering process at room temperature. (c) DHF treated surface, with sputtering process at 160°C. (d) Surface with oxidizing preclean and sputtering process at 160°C.

Deposition may influence microstructure as well. Figure 4.3 shows that with low temperature deposition no grain structure is visible, while a mosaic structure

becomes visible starting above 160°C for OH terminated samples. In next paragraphs further investigations on this aspect are described, considering only OH terminated surface since, wafer preclean normally adopted in wafer manufacturing, presents a slightly oxidizing behavior.

4.2.2 Experimental set up

Aluminum silicon alloy (1% Si content) layers have been deposited using a DC magnetron sputter (Varian 3290). In this technology four steps occur in succession: the first one is a preliminary heating of the wafer, while the next three ones are dedicated to the aluminum sputtering process, depositing the desired thickness, one third at a time, at a pre-settled temperature.

Preheat process is performed for 73 seconds in argon atmosphere at a fixed power of 75%, for 75 seconds, to obtain a 4μm thick AlSi layer. Deposition can be executed with or without additional cooling argon flux.

As substrate, CZ silicon wafers with [100] orientation have been used. Before the deposition the surface is prepared using a mixture of NH_4OH:H_2O_2:H_2O 1:5:25, in a 10 minutes bath at 60°C. This mixture is expected to produce an OH terminated surface.

Wafers subjected to sintering process have been heated in a fast-ramping furnace (ATV PEO-601) at 400°C for 30 minutes.

A preliminary investigation of the samples was performed by optical microscopy using a Nikon Eclipse LV150, and further inspections by a multi-beam field-effect scanning electron microscope (AURIGA, ZEISS, probe current range of 1 pA–29 nA and HV range of 2–30 kV). Reflectance measures have been obtained with Nanospec AFT 210 (Nanometrics) with objective lenses 20x, five points per wafer. For sheet resistance Remap 273 Four Point Probe (CDE) has been used.

4.2.3 Experiment description

After cleaning, wafers are subjected to three different heat sources in three following steps. The first one is in the preheat station, where this thermic treatment eliminates humidity eventually adsorbed of the surface, which can modify aluminum adhesion and represent a catalyst for degradation. The second one is in the deposition chambers, before wafers are subjected to a last thermic treatment, taking place during the sintering process. While preheat and deposition occur in the same DC magnetron sputtering chamber (Varian 3290), sintering is performed in a dedicated furnace (PEO-601).

Increasing preheat and deposition temperature, a reflectivity enhancement is expected, as aluminum surface morphology shows bigger grain formations (Figure 4.3 above). Sintering process may play a role in structure stress release mechanisms, so half of the first group samples have been processed in furnace to evaluate changes in morphology.

Next tables summarize experimental structure then covered in detail in the following paragraph.

Step 1: evaluation of preheat and sinter process effects on morphology.

Preheat has been increased from 100 to 380°C, maintaining deposition temperature fixed to 60°C. Each group has been splitted between sintered and as-deposited ones. Deposition has been performed in absence of additional cooling argon flux in chamber. Note this tool is equipped with thermocouples only on the wafer backside, thus it can not measure the frontside temperature during process.

Table 4. 1. Step 1 experiment summary, see Figure 4.4.

Sample	*Preheat (°C)*	*Deposition (°C)*	*Sinter*	*Figure*
AlSi_100_60_S	100	60	Yes	1.a.
AlSi_100_60	100	60	No	1.b.
AlSi_200_60_S	200	60	Yes	2.a.
AlSi_200_60	200	60	No	2.b.
AlSi_380_60_S	380	60	Yes	3.a.
AlSi_380_60	380	60	No	3.b.

Step 2: evaluation of deposition temperature on AlSi grain size.

Preheat fixed to 350 or 380 °C to assure complete removal of humidity from wafer surface, deposition temperature is increased from 160 up to 350 °C and argon flux is present. Each group has been sintered after process.

Table 4. 2. Step 2 experiment summary, see Figure 4.5.

Sample	*Preheat (°C)*	*Deposition(°C)*	*Figure*
AlSi_300_160	300	160	1.a.
AlSi_350_160	350	160	2.a.
AlSi_350_200	350	200	2.b.
AlSi_350_350	350	350	3.a.

Step 3: evaluation of the impact of argon flux on heat accumulation

Table 4. 3. Step 3 experiment summary, see Figure 4.6.

Sample	*Deposition(°C)*	*Argon flux*	*Figure*
AlSi_200_Ar	200	Yes	a
AlSi_200_noAr	200	No	b

4.2.4 Results and discussion

Step 1 investigates the influence of preheat and sintering process on microstructure. After optical microscope inspection all samples present a similar microstructure with smooth surface and small grain formation (around 5 to 8 μm) with edges slightly pronounced (Figure. 4.4).

This microstructure with lump plate formations is consistent with an OH terminated surface.

Since no difference arises between sintered and non-sintered samples, this treatment can be considered irrelevant for microstructure modification. Step 1 also demonstrates no significant influence of preheat and sintering process on microstructure modification.

However, since performing a sinterization of the AlSi layer on the silicon substrate assures a good ohmic contact, samples of step 2 have been all thermally processed in the furnace. In addition to promote a complete evaporation of humidity preheat is settled to 300 °C-350°C.

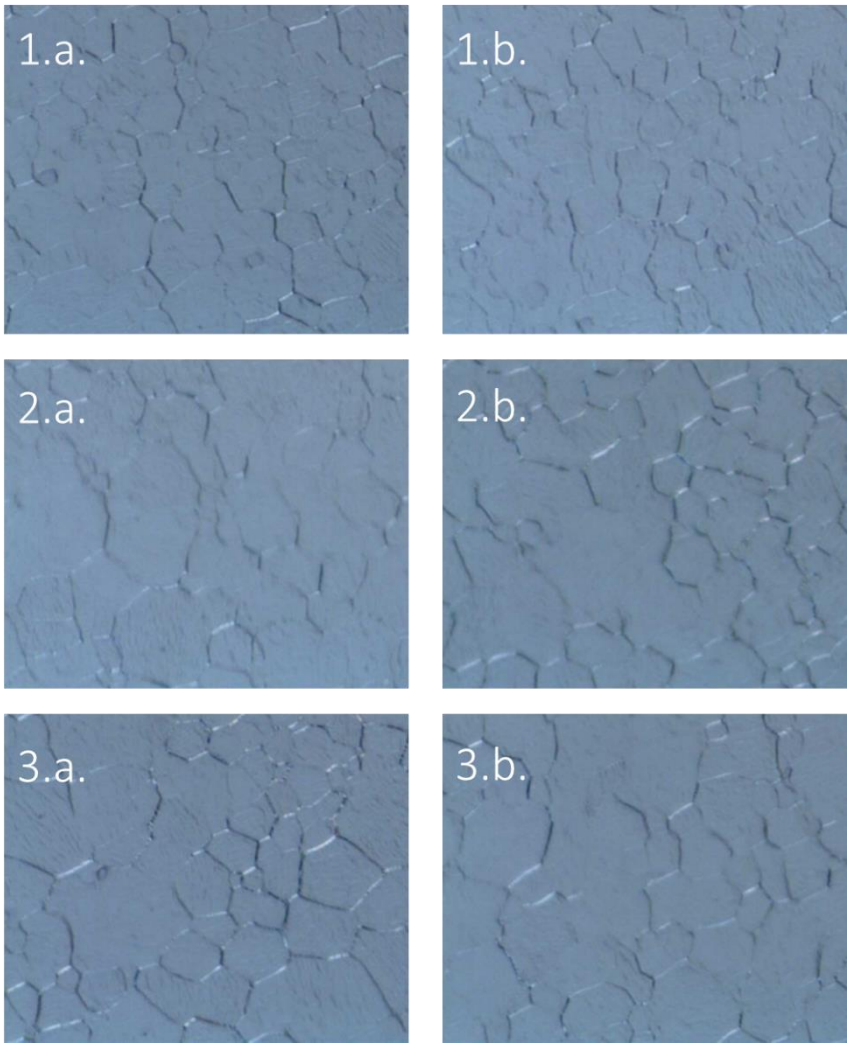


Figure 4. 4. Optical inspection, 100x magnification of Step 1 samples for the evaluation of preheat and sinter process effects on morphology (see Table 4.1.). All samples have been sputtered at 60°C. The number refers to preclean temperatures, the letter to the sintering process. (1a) Preheat 100°C, sinter at 400°C. (1b) Preheat 100°C, no sinter. (2a) Preheat 200°C, sinter at 400°C. (2b) Preheat 200°C, no sinter. (3a) Preheat 300°C, sinter at 400°C. (3b) Preheat 200°C, no sinter.

Step 2 analyzes the effects of deposition recipe on layer microstructure. Deposition temperature varies from 160 to 350 °C to evaluate the impact of a significant increment of heat. Moreover, to reduce process time, a compromise between high preheat temperatures and low deposition temperatures is required. When higher preheat temperature are applied, more time is required to cool down the wafer before deposition start. For this reason, argon flux has been applied.

Optical microscope inspection highlights a change in surface morphology with the increment of deposition temperature. Figure 4.5.1.a and 4.5.2.a confirm no significant impact of preheat even when higher deposition temperatures are involved. As appear from Figure 4.5.3.a. aluminum microstructure degrades forming grains above 350°C during deposition.

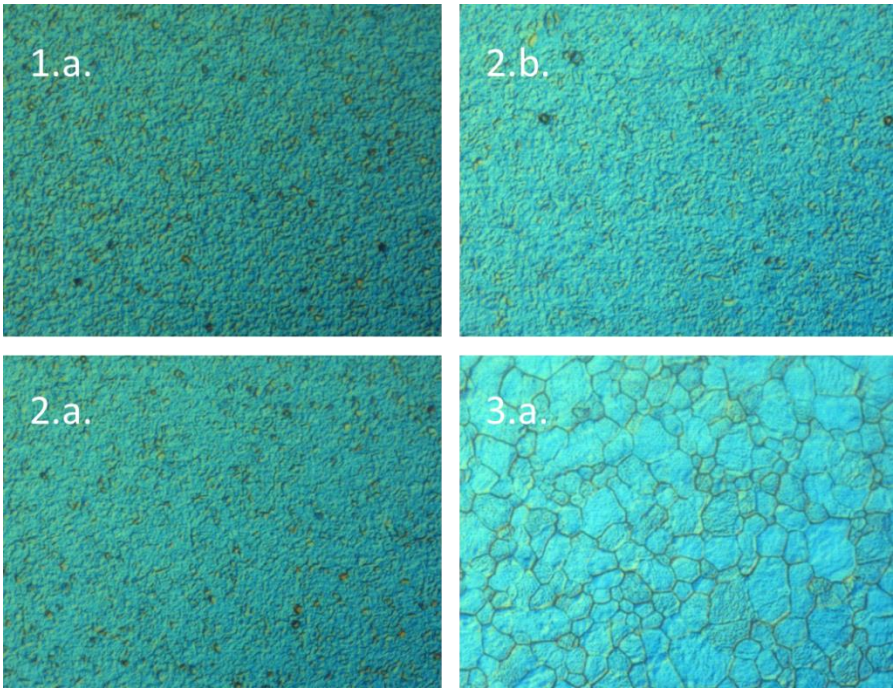


Figure 4. 5. Optical inspection, 100x magnification of Step 2 samples for the evaluation of deposition temperature on AlSi grain size (see Table 4.2.). (1a) Preheat 300°C, deposition at 160°C. (2a) Preheat 350°C, deposition at 160°C. (2b) Preheat 350°C, deposition at 200°C. (3a) Preheat 350°C, deposition at 350°C.

Since AlSi_350_350 morphology is close to step 1 samples, processed at lower temperatures, a further investigation on heat sources has been performed. As already pointed out, Varian tool does not provide an in-situ temperature monitoring, since sensors are located on wafer backside. In step 1 no argon flux mode has been adopted. The absence of a mean for heat exchange could produce an accumulation of thermal energy on the front side, resulting in a microstructure typically observed on high temperature deposited layer. This is confirmed by step 3 experiments.

In the experiment wafers are deposited at the same intermediate temperature of 200°C with and without argon flux. Results in terms of morphology demonstrates that samples processed in absence of Ar, produce visible grains (Figure 4.6.a), while samples under cooling flux do not show plate formations (Figure 4.6.b).

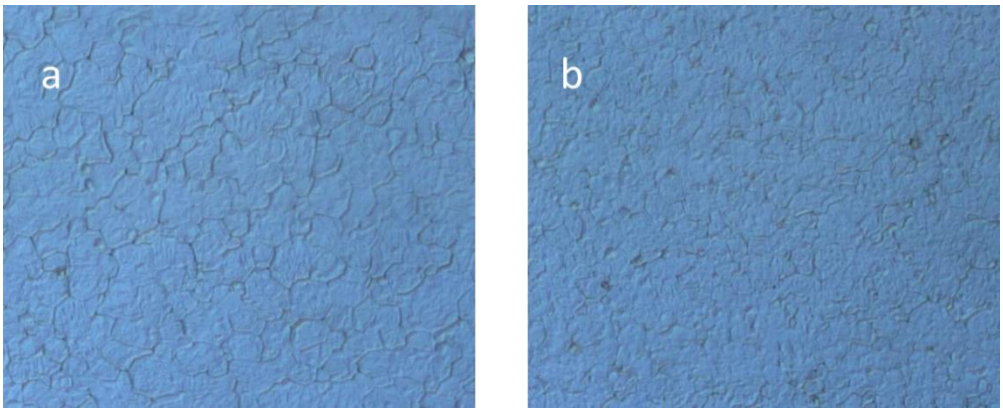


Figure 4. 6. Optical inspection, 100x magnification of Step 3 samples for the evaluation of impact of argon flux on heat accumulation (see Table 4.3.). (a) Deposition at 200°C, no argon flux. (b) Deposition at 200°C, argon flux applied.

In step 2, also changes in reflectivity have been monitored. Values increase steadily from sample AlSi_300_160 to AlSi_350_350, confirming an impact of the deposition temperature on AlSi layer appearance.

Higher reflectivity usually produces more precise mask align processes (Table 4.4.).

Table 4. 4. Reflectivity of Step 2 samples at 480nm.

Sample	*Reflectivity @ 480nm (%) average on wafer*
AlSi_300_160	114%
AlSi_350_160	140%
AlSi_350_200	146%
AlSi_350_350	156%

However, a compromise between grain formation and reflectivity is required to avoid humidity penetration paths. Grain edges represents a fracture where the underlying silicon surface could be exposed. This is visible from electronic microscope investigation (Figure 4.7).

Automotive sector standards require high performance reliability also in harsh working conditions. Moisture absorption is one of the principal causes for degradation. Thus, avoiding cracks and fractures is a priority.

In order to understand stress induced failure modes, aluminum layer has been evaluated on device under specific test. Details are presented in next paragraphs.

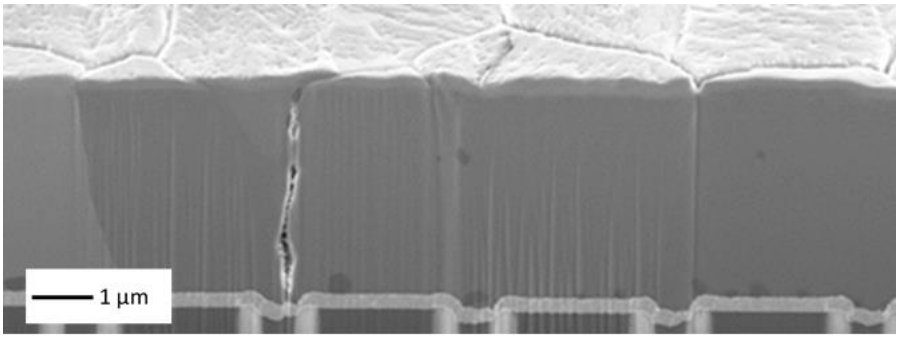


Figure 4. 7. SEM imaging of a cross section of AlSi layer in presence of a grain boundary. Fracture is propagating along all the layer reaching the substrate surface.

4.2.5 Aluminum under stress

The current automotive THB standard test, also known as H3TRB in the AEC-Q101 semiconductor qualification framework, operates under fixed conditions of 85°C, 85% relative humidity (RH), and a maximum reverse bias (Vr) of 100 V, with a target requirement of no failures until 1000 h [3].

For the purpose of this study, a further voltage stress is introduced with respect to the standard: the maximum reverse bias is increased to 80% of the nominal blocking voltage capability of the device, and the 100 V bias limitation is removed. The ability of this test to underline specific failure mode has been proved [4] [5].

4.2.6 Experimental set up

A set of power diodes with a blocking voltage capability of 650 V and an FLR termination structure has been used to test different layers forming the structure. This group of diodes presents a simple passivation structure composed of oxide, a silicon resistive layer as primary passivation, and an additional polyimide (PI) layer as secondary passivation (Figure 4.8). The devices have been assembled in standard TO-247 plastic packages and in MTP power module packages. Both were then subjected to HV-THB tests with 520 V reverse bias.

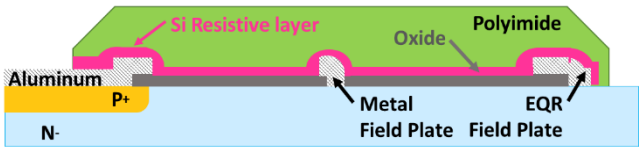


Figure 4. 8. Passivation structure of devices under test (typical HV planar termination). The structure is composed of oxide, silicon resistive layer, and polyimide (PI). Aluminum metal field plate and equipotential ring (EQR) field plate are visible.

It is important to underline that the same configuration of DUTs passed the standard AEC-Q101 H3TRB automotive test procedure.

After the tests, the diodes assembled in the TO-247 package were decapsulated using hot sulfuric acid at 150°C. Due to lack of selectivity the PI layer has been dissolved as well the package. Diodes assembled in the power modules were treated with DOWSIL 3522 at 40°C to remove the protective silicone gel. In this case, the solvent did not affect the PI layer.

4.2.7 Experimental set up

In devices failing the HV-THB test, the first sign of degradation is represented by the presence of bubbles in the polymide layer (Figure 4.9.).

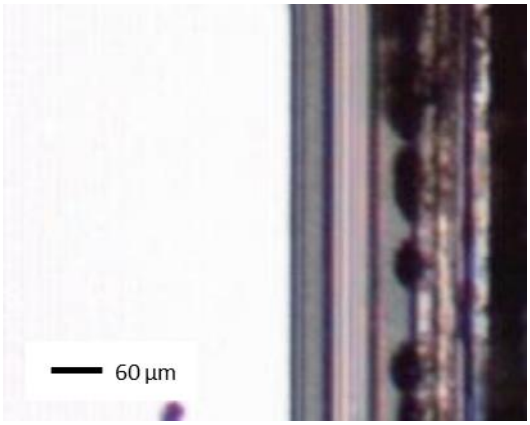


Figure 4. 9. Optical microscope inspection of bubbles in the device termination region after HV-THB test failure.

A SEM image of a FIB cross-section, performed on a bubble in the failed termination area, highlights that the organic materials did not degrade, but lifted, possibly as a result of corrosion of the underlying layer of resistive silicon and of the aluminum field plate. Indeed, the aluminum field plate appears swollen, with a change in conformity near the edge (Figure 4.10).

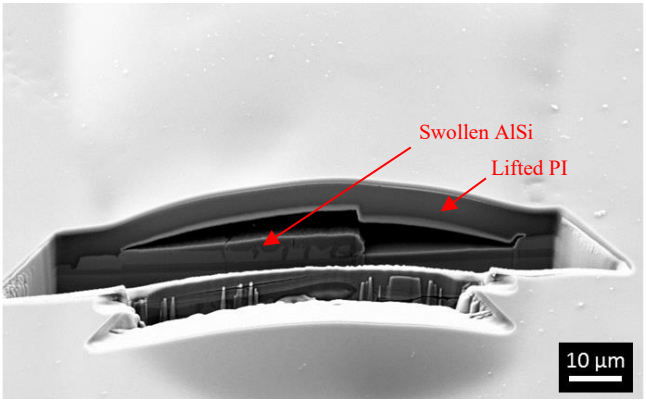


Figure 4. 10. SEM image of an FIB cut of a bubble in the failed termination area. The PI has lifted, and the aluminum has a swollen appearance.

EDX analysis was performed to evaluate the change in composition along the aluminum field plate. Comparing data acquired from untouched aluminum portions and from degraded ones, it was possible to observe different peaks (Figure 4.11). The presence of silicon can be explained by migration from the upper silicon resistive layer with the formation of aluminum silicide [6] [5]. Instead, the oxygen peak could indicate the formation of aluminum oxide species.

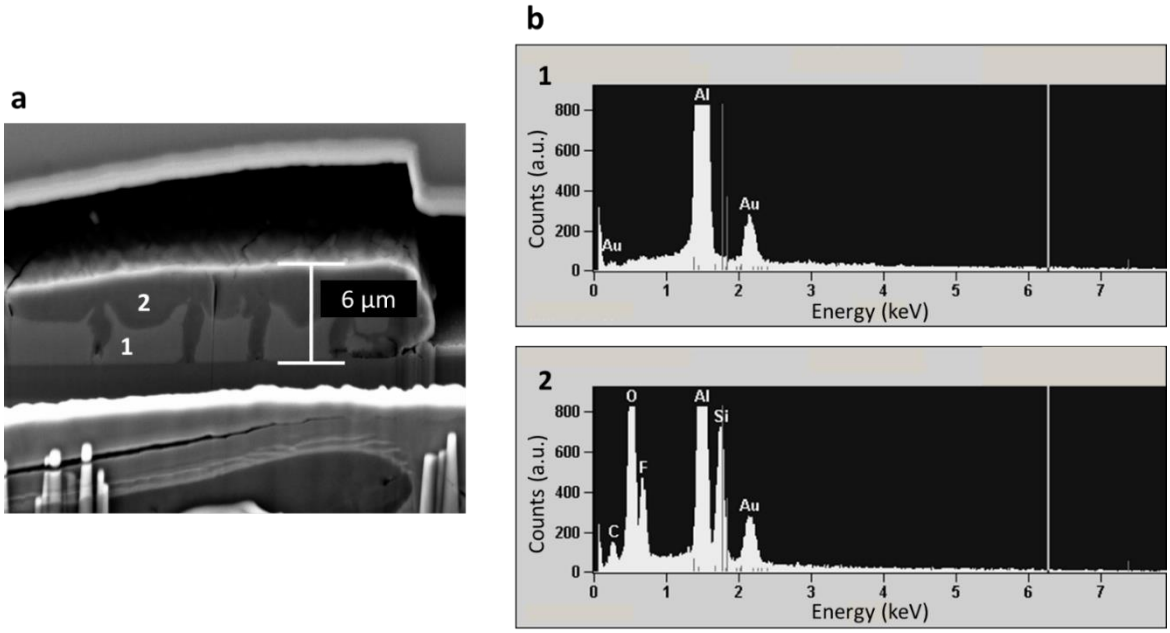


Figure 4. 11. (a) SEM image of an FIB cut across the aluminum field plate, for DUTs having P-doped oxide, after 200 h of testing. (b) EDX analysis on two different points of the aluminum field plate: 1) untouched portion 2) degraded portion. EDX spectra comparison reveals AlO_x and aluminum silicide formation (migration from resistive layer). Peaks of fluorine and carbon can be attributed to previous plasma etching (with SF_6) or cleaning (diluted HF) processes, and to the presence of organic materials such as PI.

These species derive from a combination of humidity penetration, electrochemical phenomena, and the high chemical reactivity of aluminum with water *[7]*. More specifically, when water is adsorbed and an external bias is applied, a pH gradient forms due to the separation of H^+ and OH^- ions. In this environment, different types of reactions can occur. The general behavior for metal atoms in these conditions is as follows:

$$M \rightarrow M^{n+} + ne^-$$

at the anode,

$$M^{n+} + ne^- \rightarrow M$$

at the cathode.

Aluminum, is known to be particularly reactive in the conditions previously explained since easily forms hydroxides when in contact with water [8]. These

compounds are quite stable in neutral solutions, but in the presence of acids or bases, they dissolve rapidly resulting in layer corrosion.
The proposed reactions are as follows:

$$Al + 3H_2O \leftrightarrow Al(OH)_3 + {}^{3}/_{2}\, H_2$$

(overall reaction of aluminum with water).
In neutral environments, $Al(OH)_{3\ amorphous}$ is transformed to the stable hydrated oxide:

$$Al(OH)_3 \rightarrow Al_2O_3 \cdot H_2O$$

which has a free energy of formation of -436.3 kcal, and acts as a passivated barrier.
Alkaline solutions are able to destabilize this protective oxide that forms AlO_2^-, and can therefore cause rapid dissolution of aluminum at room temperature, which continues to react and consume water [9]. In high-humidity conditions, this equilibrium is completely right-shifted, causing H_2 formation, which could explain the spongy appearance of the aluminum layer and polyimide bubble formation [10].

4.2.8 Conclusions

Aluminum deposition process can be strongly influenced by preclean and temperature settings. Once fixed surface treatment, a fine tune of process parameters is essential to obtain high performance in terms of whole device reliability. Aluminum layer microstructure not only influences substrate ohmic contact, affecting electrical parameters, but it also conditions the photo mask alignment process repeatability.

Deposition temperature appeared as one of the most crucial variables. If compared with other heat sources the wafer is subject before, during or after aluminum sputtering, it can produce permanent effects on the layer which can influence next process and test phases.

High deposition temperatures can induce the formation of a grain structure which crosses the whole layer thickness, exposing the underlying substrate surface and resulting in a device failure.

Indirect parameters related to microstructure are reflectivity and permeability. The first one impacts the next photo patterning processes, the second is related to device robustness when working in harsh environments.

Due to the presence of humidity, in the current automotive stress tests, such as HV-H3TRB (HV-THB), aluminum is subjected to a series of chemical reactions shifted by the pH gradient formed during the high voltage application. For this reason, a strong passivation design is required.

However, the influence of process parameters on materials final characteristics and on product performance is evident.

4.3 Nickel

Nickel (Ni) belongs to the transition metals group of the periodic table. It is a hard and ductile material, with a slow oxidation rate under air exposure, at room temperature. However, when threated thermally it produces stable oxides.

In the semiconductor industry it is adopted to improve the adhesion of metal layer used for soldering. In this thesis, nickel layers have been deposited via magnetron sputtering. Due to its ferromagnetism, in this type of processes it is found as vanadium alloy (NiV).

Stress induced by metal film deposition represents an important complication to address when dealing with thin wafers (> 10 mils). Solicitation can be measured both in terms of residual tension and bowing. The first one results in surface cracks and damages during several process steps (such as thinning, cutting and

assembly) [11]. The second causes problems during handling and testing, or in worst cases brings to wafer breakage (e.g. when moving in/out the cassette).
Process set up and alloys concur to provide different options to solve these issues. One of the most suitable solutions when solder metals are involved is the adoption of nitrogen (N_2) during deposition. Even if silicon nitride is well known as a material with low flexibility, this is not always true for metal nitrides such as nickel nitrides [12]. To be more precise, the implementation of a nitrogen flux during sputtering deposition can reduce film tension up to one order of magnitude. Considering a more general approach, there are several methods to reduce wafer bowing. The first one is to produce compensating front and back metal metalization. This solution requires equally stressed layer structure with opposite force type (see Figure 4.12).

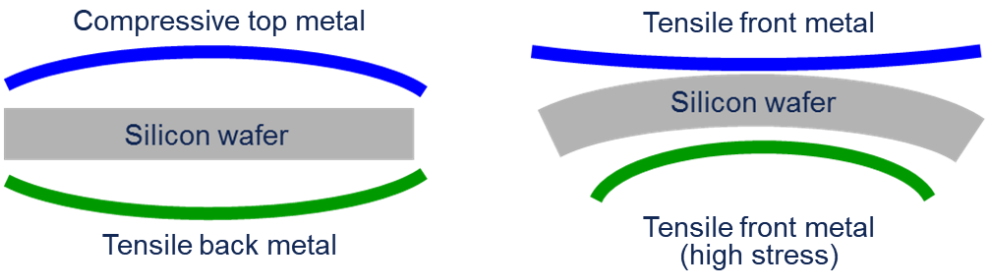


Figure 4. 12. Effects of different types of stress on a silicon wafer. On left side, a compensating metallization with compressive top and tensile back produces a planar structure. On the right a typical wafer with not optimized metal layers.

Usually, each metal layer presents its intrinsic stress type, which can be tensile or compressive. Process set up such as sputtering deposition power, temperature and time are able to reduce or increase this value, but not to modify its type. This variation is caused by a reorganization of the layer without a change in its properties. The addition of elements such as nitrogen apports a modification in the lattice and thus in the material physical characteristics [13] [14]. For this reason, this type of solutions produce more important improvements.

4.3.1 Solder metal layer requirements

Solderable metal stacks require good adhesion, low contact resistance and low intrinsic stress. The typical scheme is composed by an adhesion layer to the substrate, a solder layer, and a protective noble metal layer to avoid oxidation and increase solder wettability.

Adhesion materials are usually deposited as thin films (from 700 to 1500 Å) and present high intrinsic tension. Metals adopted in this context are chromium and titanium.

Solder metalizations are composed by nickel or nickel alloys and require a minimum thickness of 2000 Å for soft solder processes (with low temperature and/or single reflow) up to a maximum of 6000 ÷ 7000 Å for hard solder ones (with multi reflow). In the latters, Ni results consumed, thus an adequate barrier is essential to avoid compromising the underlying adhesion layer.

Protective noble metal layers necessitate a minimum thickness of 3000 Å to avoid oxygen penetration and consequent Ni layer oxidation.

4.3.2 Issues related to residual stress

When thin wafers are produced (≤ 250 μm), residual stress causes several issues that need to be addressed to avoid yield losses. Tension can affect not only processes but also the devices final performances. Some of common problems include:

- wafer breakage during handling due to high bowing (Figure 4.13),
- crack formation before or after wafer thinning,
- crack formation during wafer cutting,
- die breakage in bonding process (Figure 4.14),
- reliability failures.

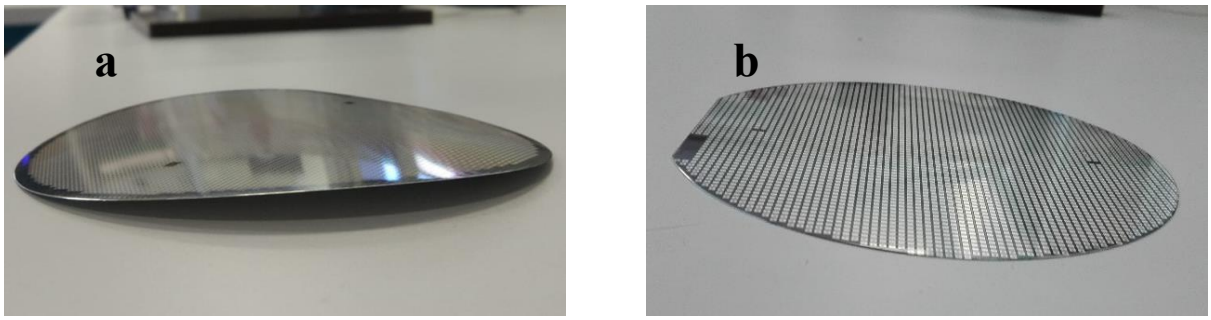


Figure 4. 13. 120 μm thick wafers with 5000 Å NiV (a) and 5000 Å NiVN (b)

Wafer back grinding is surely among the most stressing steps in this type of manufacturing, and a variety of solutions have been introduced, but more general studies attribute the major cause of breakage to a not adequate overall stress reduction.

To act in this direction these are the principal implementations:

- perform a silicon etch on wafer back side to remove microcracks induced by back grinding,
- **adopt compensating metalizations,**
- **choose low stressed metal alloys to be deposited.**

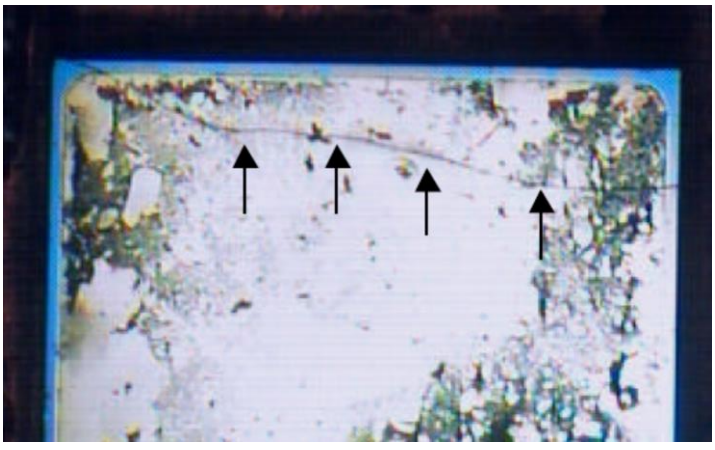


Figure 4. 14. Fracture after die bonding process.

In this Chapter the attention is on the last two options which focus of the metal-based materials optimization.

4.3.3 Experimental set up

In this work a nickel vanadium (7% wt) target has been used to produce uniform solder metalization. Samples have been deposited by magnetron sputtering using Apollo 200 sputter (Nexx ASM) to form 5000 Å thick layers.

The process is performed in a high vacuum chamber and triggered by the injection of argon gas (Ar) under high voltage. A variable percentage of nitrogen (N_2) has been introduced to verify its impact on the film residual stress.

As substrate, CZ silicon wafers with [100] orientation have been used.

Film stress measurements have been obtained with Tencor Flexus FLX-2320 optical laser system.

Investigation of samples was performed by transition scanning microscopy (TEM) using a FEI TECNAI F20ST microscope, equipped with a field emission gun (FEG) operating at 200 kV. TEM samples in cross-section were prepared using in situ focused ion beam (FIB) lift out technique with ZEISS Auriga dual beam system. The protection Pt cap layer was in situ deposited, with the use of both electron and ion beams.

EDX analysis for nitrogen detection was performed at 4keV in top view at FESEM (ZEISS Supra 40), since in cross-section by TEM was not enough sensible.

A further surface analysis with Auger electron spectroscopy (AES) has been performed with PHI 680 Auger Nanoprobe, 30° tilt, electron beam 10kV/10nA, ion beam Ar^+, 3keV. AES depth profiles have been obtained by alternating data acquisition cycles with sputtering cycles, during which material is removed from the sample surface using an ion beam source (sputter rate 88 Å/min SiO_2 equiv.). To eliminate crater edge effects, the data are acquired from a smaller region within the center of a larger sputtered area. The sputter rate is calibrated using

SiO_2, for this reason depth profile data cannot be used to establish absolute film thicknesses, but to provide a description of the nitrogen percentage along the material.

The crystalline structure of materials was examined using a Panalytical X'Pert Pro X-ray diffractometer in Bragg/Brentano configuration with Cu (Kα) as an X-ray source.

X-ray photoelectron spectroscopy (XPS) was carried out using a PHI 5000 Versaprobe scanning X-ray photoelectron spectrometer (monochromatic Al K-α X-ray source with 1486.6 eV energy) to investigate the chemical composition. Survey and high-resolution (HR) spectra were acquired on 500 × 500 μm2 regions. Different pass energy values were employed for survey spectra (187.85 eV) and for high-resolution acquisitions (23.5 eV). All the spectra were acquired with simultaneous charge compensation. CasaXPS software was used for data analysis. All core-level peak energies were referenced to the C 1s peak at 284.8 eV (C−C/C−H bonds).

4.3.4 Results and discussion

Thick NiV layers without stress compensation create high bowing on thin wafers [15]. The incorporation of nitrogen, forming nickel vanadium nitride (NiVN) [13], produces strong improvements in reducing residual stress [16]. A preliminary visual comparison between two wafers with equal solder metal thickness but processed with or without nitrogen, shows a significant difference in terms of wafer warpage (Figure 4.13 above).

Plotting wafer stress data with N_2%, a considerable variation is evident when nitrogen concentration increases. The maximum improvement is obtained with 40% of N_2.

The presence of nitrogen in samples has been confirmed by EDX analysis on 5000 Å thick layers. Spectra for NiV and NiVN are presented in Figure 4.16. This measurement is enough sensitive to detect nitrogen from the as-grown samples applying relatively low voltages. This set up assures the beam is confined within the NiV/NiVN film and not located on the silicon substrate.

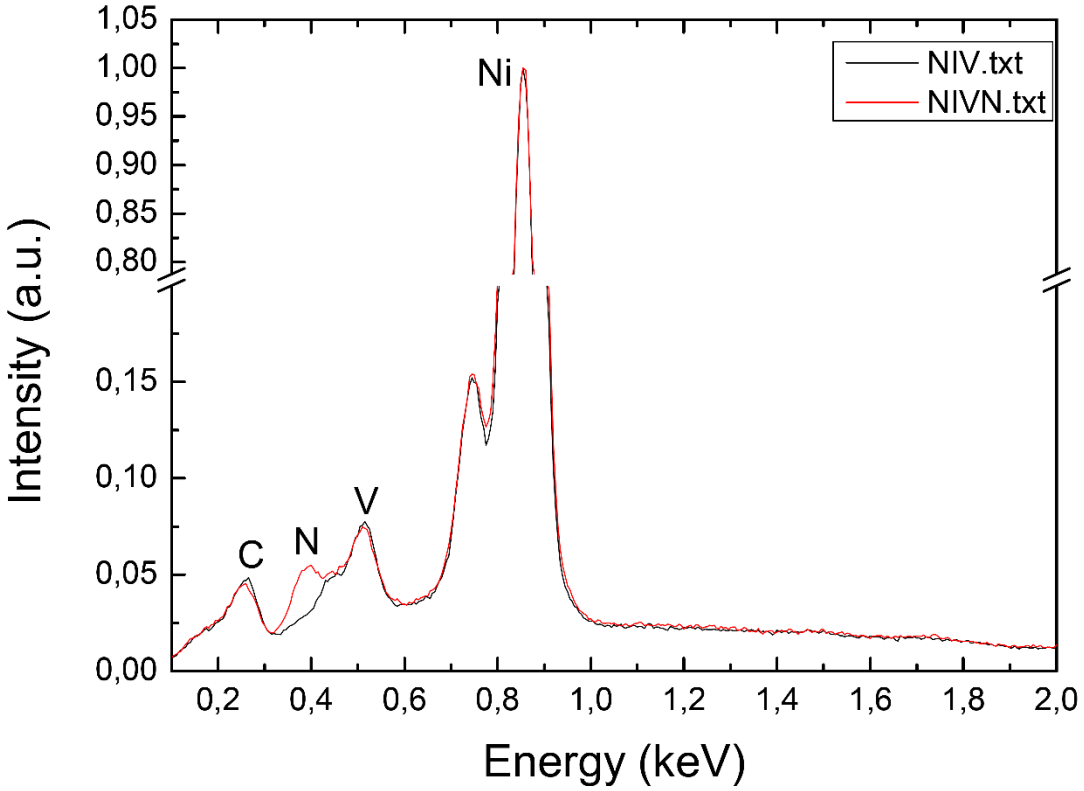


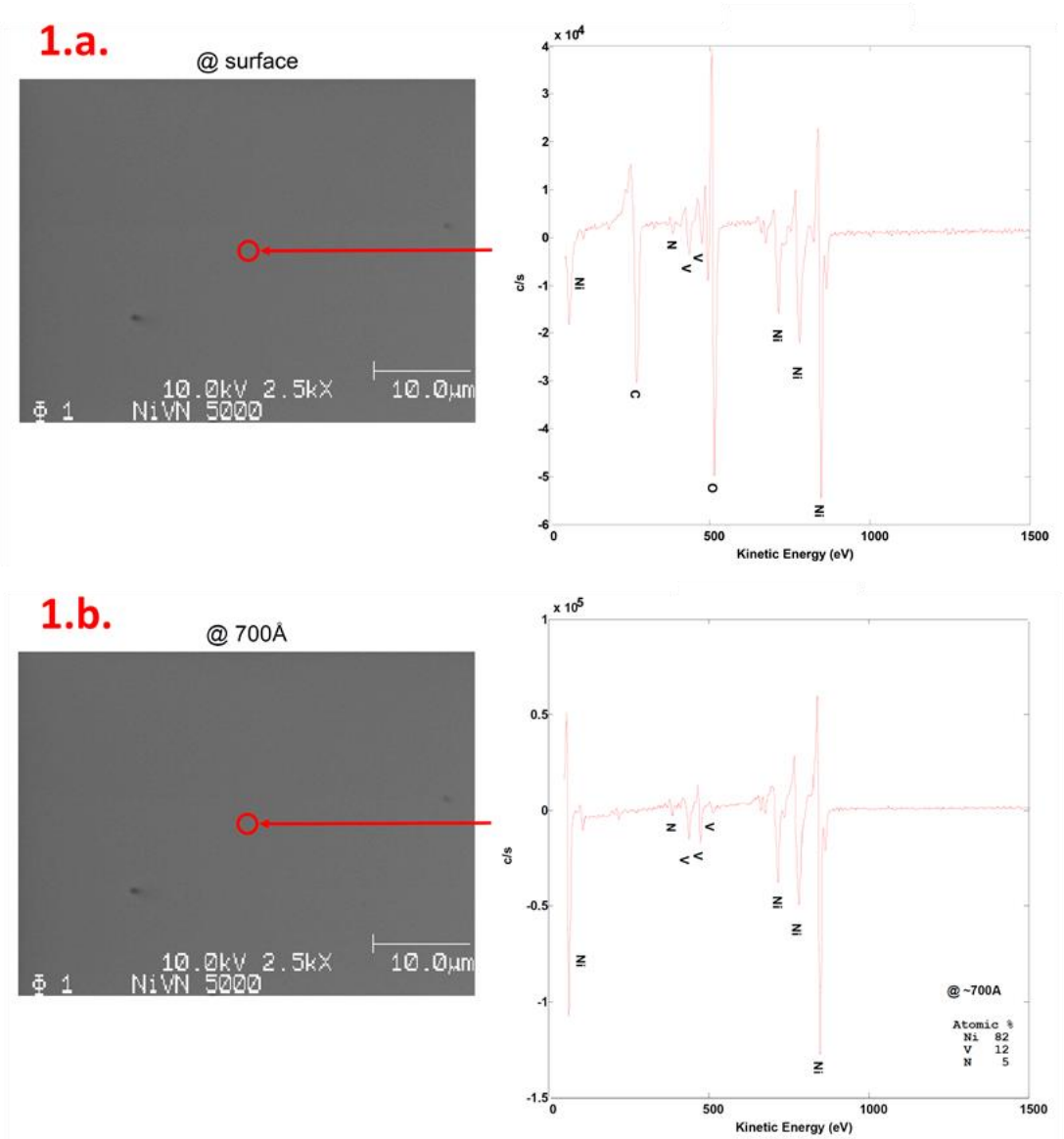
Figure 4. 16. EDX performed in top view by FESEM at 4keV. Spectra for NiV and NiVN are shown. Nitrogen peak is visible only for NiVN sample.

A Further investigation on nitrogen incorporation has been performed with AES, comparing NiVN layers sputtered with different percentage of N_2.

As first step, to establish the effective absence of nitrogen in NiV films, an AES analysis at surface and near surface has been performed on a NiV and a NiVN

(40% N_2) sample. The nitrogen peak has been identified near 400KeV as agreed by literature for nitrogen in metals [17] [18].

Both surfaces present oxygen and carbonium contamination, but only the NiVN shows the characteristic above mentioned N peak (Figure 4.17).



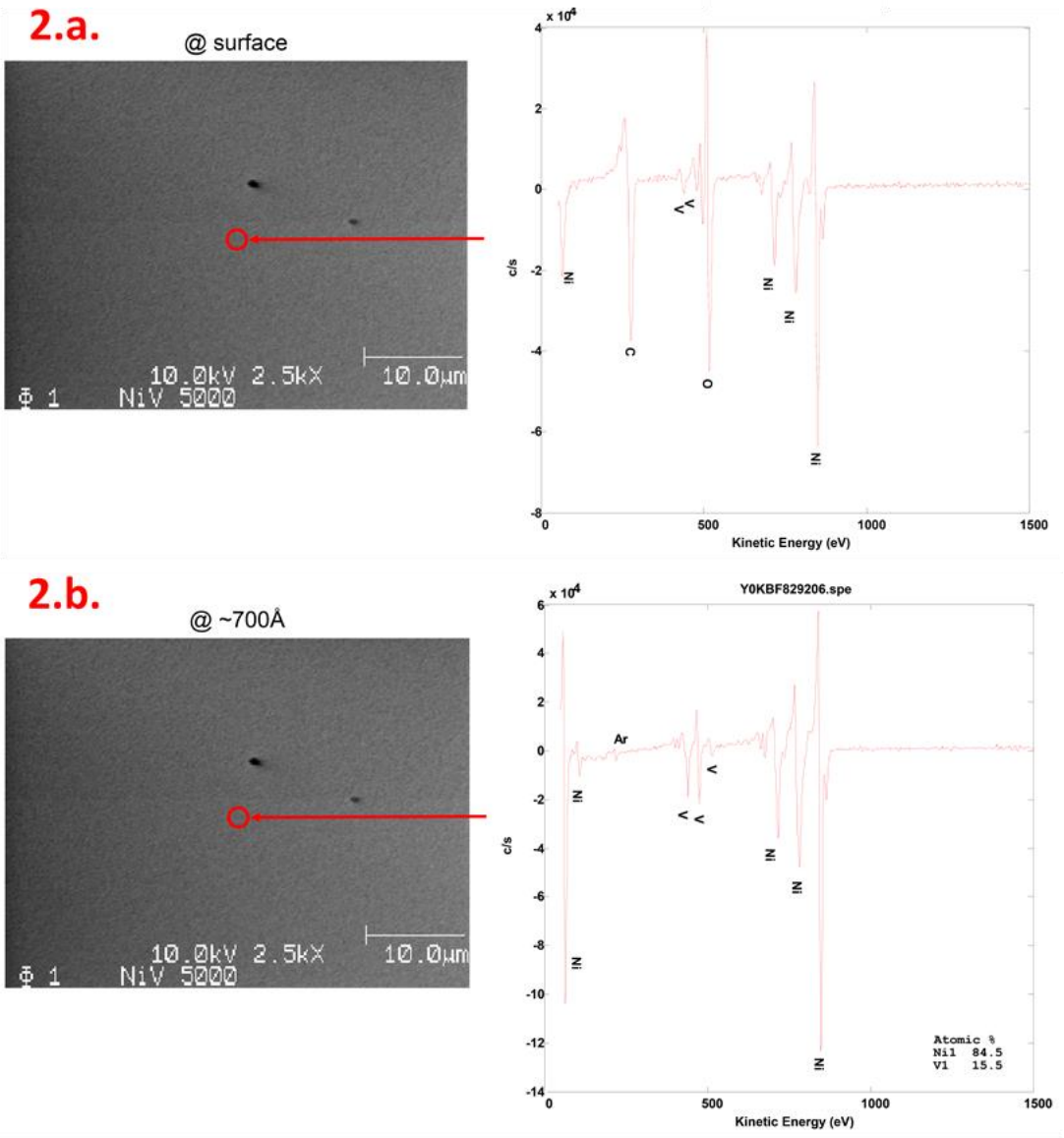


Figure 4. 17. AES spectra at surface and near surface of NiVN (1) and NiV (2) samples. (1.a.) NiVN at surface. Oxygen and carbon contamination is evident as well as nitrogen presence. (1.b.) NiVN AES spectra collected at ~700 Å depth. Cross-contamination absent, nitrogen peak visible. (2.a.) NiV at surface. Oxygen and carbon contamination is evident, nitrogen peak is not present. (2.b.) NiV AES spectra collected at ~700 Å depth. Cross-contamination absent, nitrogen still absent.

AES depth profile has been used to evaluate the uniformity of N incorporation along all the layer thickness.

Table 4.5. illustrates the atomic composition (%) at different depth and Figure 4.18 is a plot of the AES data collected during profile analysis.

Nitrogen appears to be uniform along all the layer thickness suggesting an inglobation during layer-by-layer deposition.

Table 4. 5. NiV and NIVN comparison of atomic composition % at different depth. Data are normalized to 100% of the elements detected. AES does not detect H or He. Dash line "-" indicates the element is not detected. Less than symbol "<" indicates accurate quantification cannot be done due to weak signal intensity.

	Depth	***C***	***N***	***O***	***V***	***Ni***
NiVN 5000 Å	surface	41.7	1.5	29.3	3.9	23.6
	200A	-	5.7	-	12.1	82.2
	700A	-	5.3	-	12.3	82.3
	3100A	-	7.5	-	12.1	80.4
NiV 5000 Å	surface	46.5	-	25.8	2.3	25.5
	200A	-	-	-	14.9	85.1
	700A	-	-	-	15.5	84.5
	3100A	-	-	-	16	84

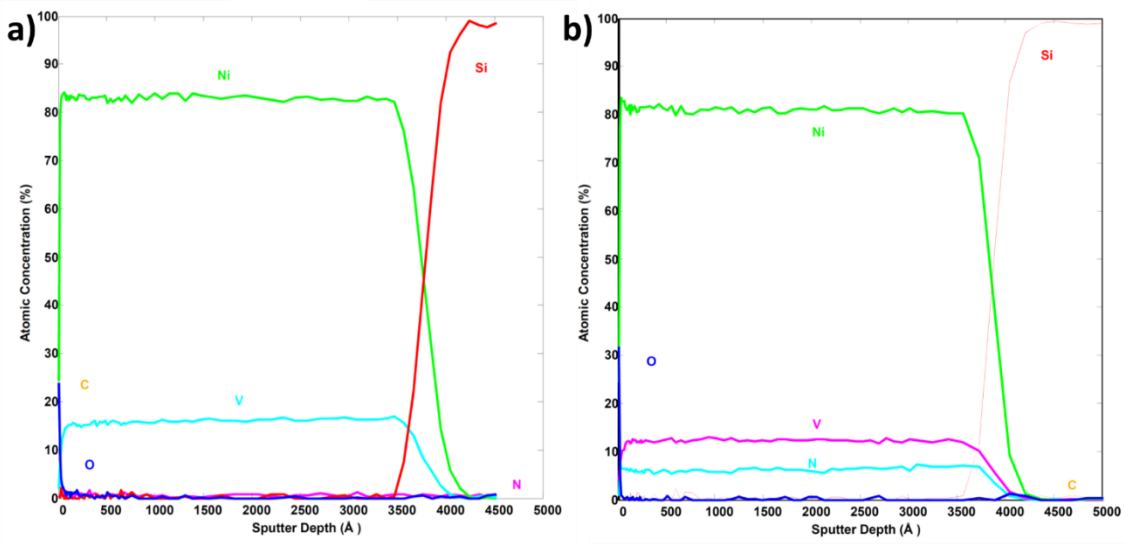


Figure 4. 19. Atomic concentration data plot from AES after normalization to 100%. a) NiV sample. b) NIVN sample.

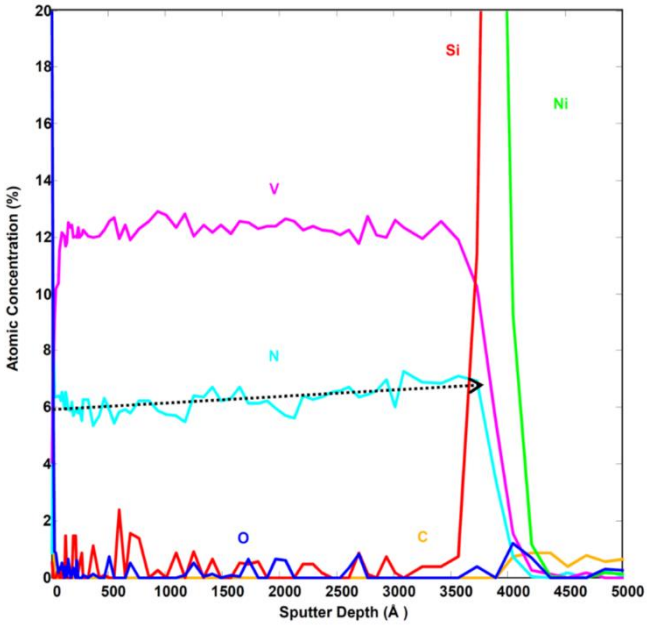


Figure 4. 18. Detail of NiVN sample atomic concentration plot. Focus on nitrogen % variation. A slight increment near Si substrate is visible but to be considered not significant.

From Figure 4.19, it is possible to have a detail of the nitrogen concentration

curve, showing a slight increment near to the substrate. This variation can be considered not significant.

A further investigation has been performed varying gas relative pressures during deposition, in order to understand if the inglobation increases steadily with N_2 flow percentage.

Optimized nitrogen gas concentration during deposition is 40%, with 60% of Ar. AES analysis has been achieved with 30% and 10% concentrations.

Considering quantification data obtained at surface and at 275 Å depth, nitrogen incorporation seems to remain steady near the top and increases with N_2% immediately below (Table 4.6.).

Table 4. 6. Sum up of atomic concentration (%) of different elements at surface and near surface for NiVN samples produced with different N_2/Ar percentage during deposition.

N_2/Ar percentage	***C***	***N***	***O***	***V***	***Ni***
10% N_2, 90% Ar					
@surface	*28.7*	*2.7*	*26.2*	*6.4*	*36*
@275 Å	*-*	*≤1.8*	*-*	*15*	*83.2*
30% N_2, 70% Ar					
@surface	*28.8*	*2.6*	*31.8*	*7.1*	*29.8*
@275 Å	*-*	*4.2*	*-*	*12.8*	*83*

This type of distribution suggests a solubilization of nitrogen in the film structure during deposition and the creation of an equilibrium at the surface, under air exposion. Nitrogen solubility could have been reduced by partial oxidation. This variation was also visible in the 40% sample (Table 4.5.). AES depth profile are presented in Figure 4.20 where it is clear nitrogen total content varies significantly with N_2 gas flow percentage in process.

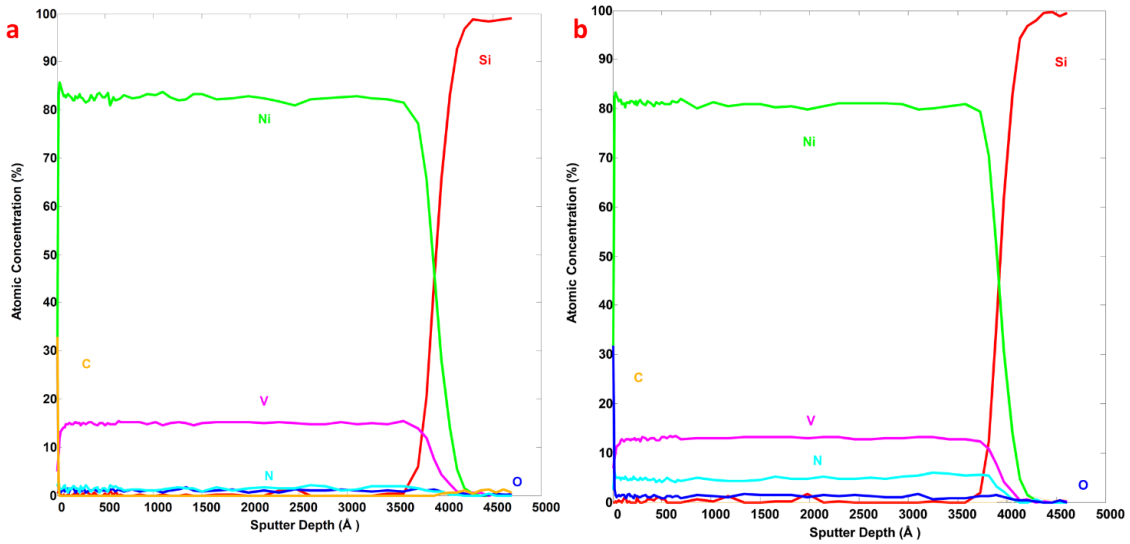


Figure 4. 20. Atomic concentration plot of data from AES after normalization to 100%, with depth variation. (a) NiVN sample produced with N_2/Ar 10%/90% during process. b) NiVN sample produced with N_2/Ar 30%/70% during process.

Once established the successful incorporation of nitrogen in samples and clarified its distribution, an analysis of film morphology has been achieved with TEM. Figure 4.21 highlights the creation of conic columnar structures in the NiV layer, which are absent in the NiVN one. This type of arrangement is usual in metals deposited via PVD techniques [15] and is likely to introduce a tension. This tension can be represented as a stretch due to the conic structures widening at the surface, resulting in a curved wafer.

Since NiVN layer does not present this structure its stress results lower.

To establish the origin of changes in material properties XPS and XRD analysis have been completed.

Samples have been prepared depositing a NiV or NiVN layer on silicon [100] substrate monitors. From XRD analysis a clear shift of peaks is visible. Figure 4.22 presents the XRD spectra compared to the bare silicon one. Silicon peaks are evident from 60°.

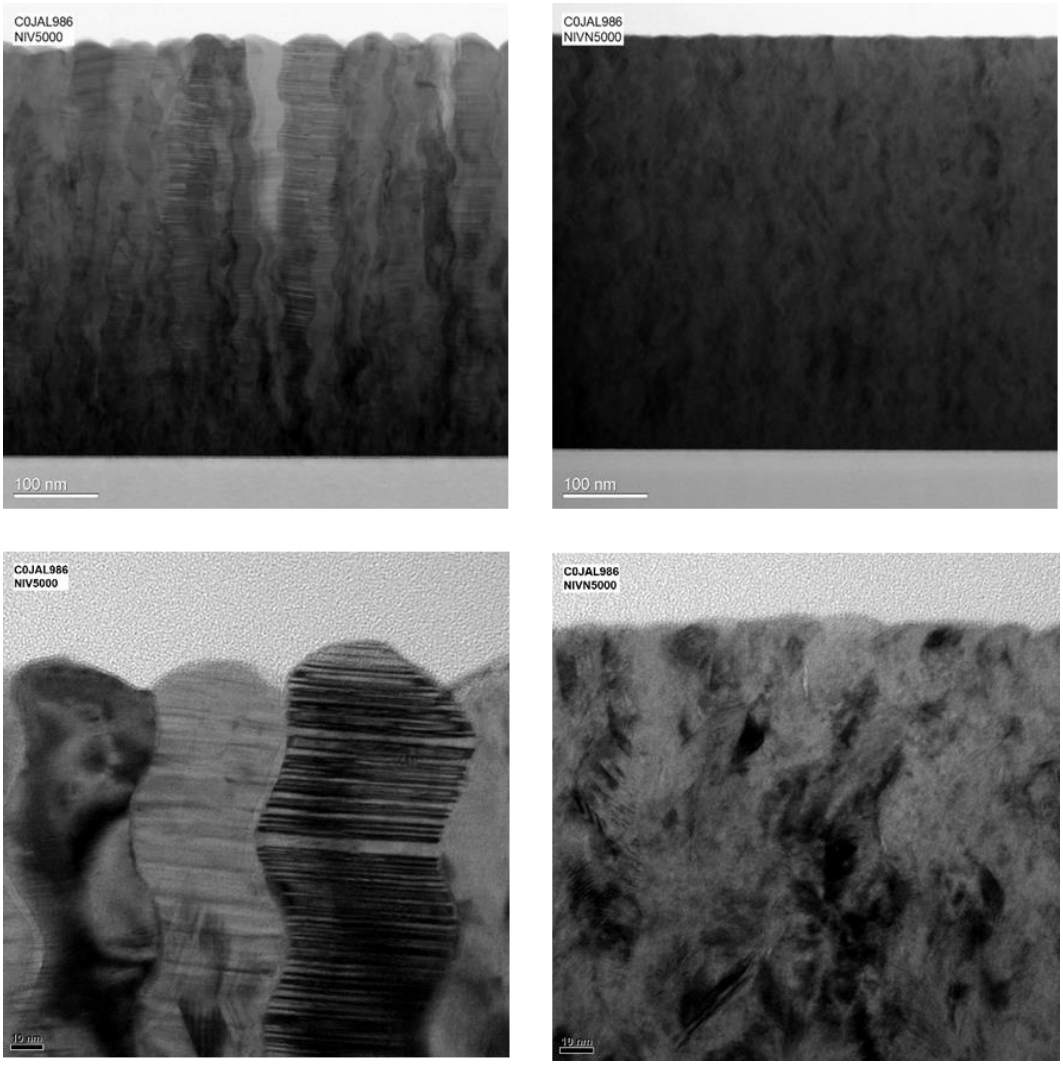


Figure 4. 21. TEM imaging of 5000 Å NiV (on the right) and NiVN (on the left) samples. The formation of conic structures is visible in the NiV layer.

Pure nickel crystal structure is face-centered cubic (fcc). Looking at the NiV sample, nickel characteristic peaks are located around 40° and 50° (▼) [19]. In this pattern, the first one is originated by the [111] plane while the second refers to the [200]. Close to the [111] signal, Chen et al. confirmed the presence of another one attributable to NiO [200] (●) [20].

Considering the NiVN spectra, an important left shift on both characteristic signals is visible. Peak around 45° might be associated with a left shift or with the presence of NiO.

A shift to lower angles can be originated by an increment of the distance between two adjacent planes. The insertion of nitrogen atoms in the fcc structure could have generated this increment.

To understand the nature of the doping and the type of interaction between nickel

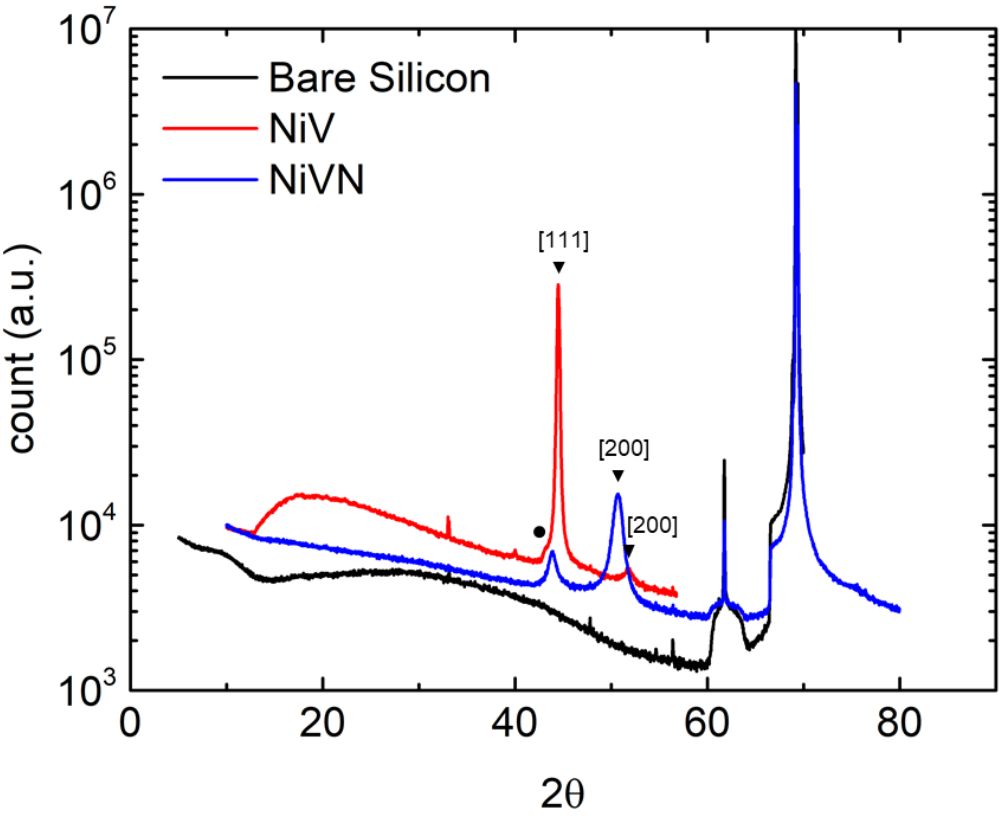


Figure 4. 22. XRD spectra of NiV and NiVN samples compared with bare silicon.

and nitrogen the XPS technique has been adopted. Spectra have been obtained before and after Ar cleaning (2 KeV for 1 minute). Before surface sputtering a C and O contamination is evident for both materials (Figure 4.23).

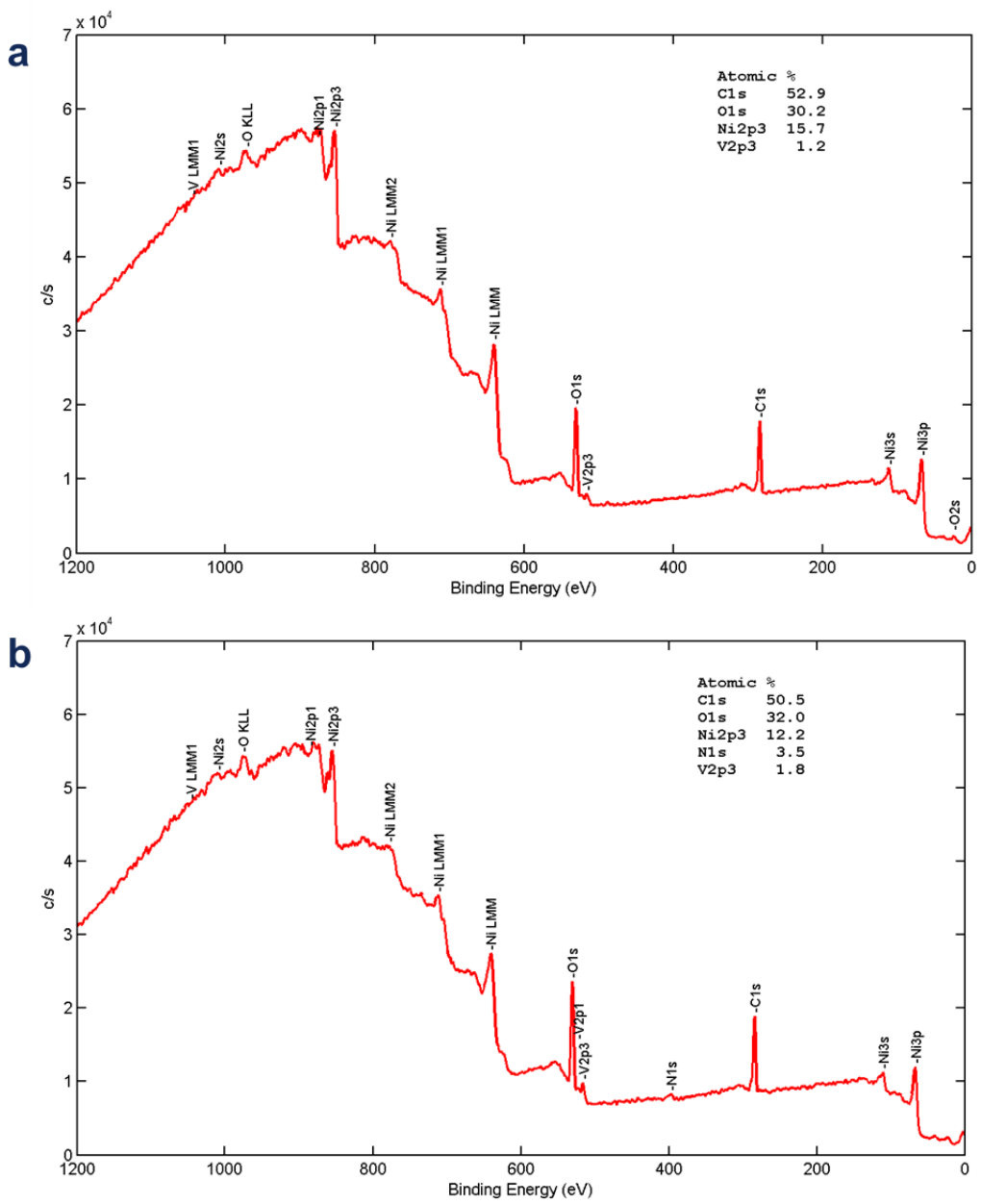


Figure 4. 23. Survey scan before cleaning with Ar. (a) NiV 5000 Å. (b) NiVN 5000 Å. C and O contamination is evident as shown in atomic composition detail box.

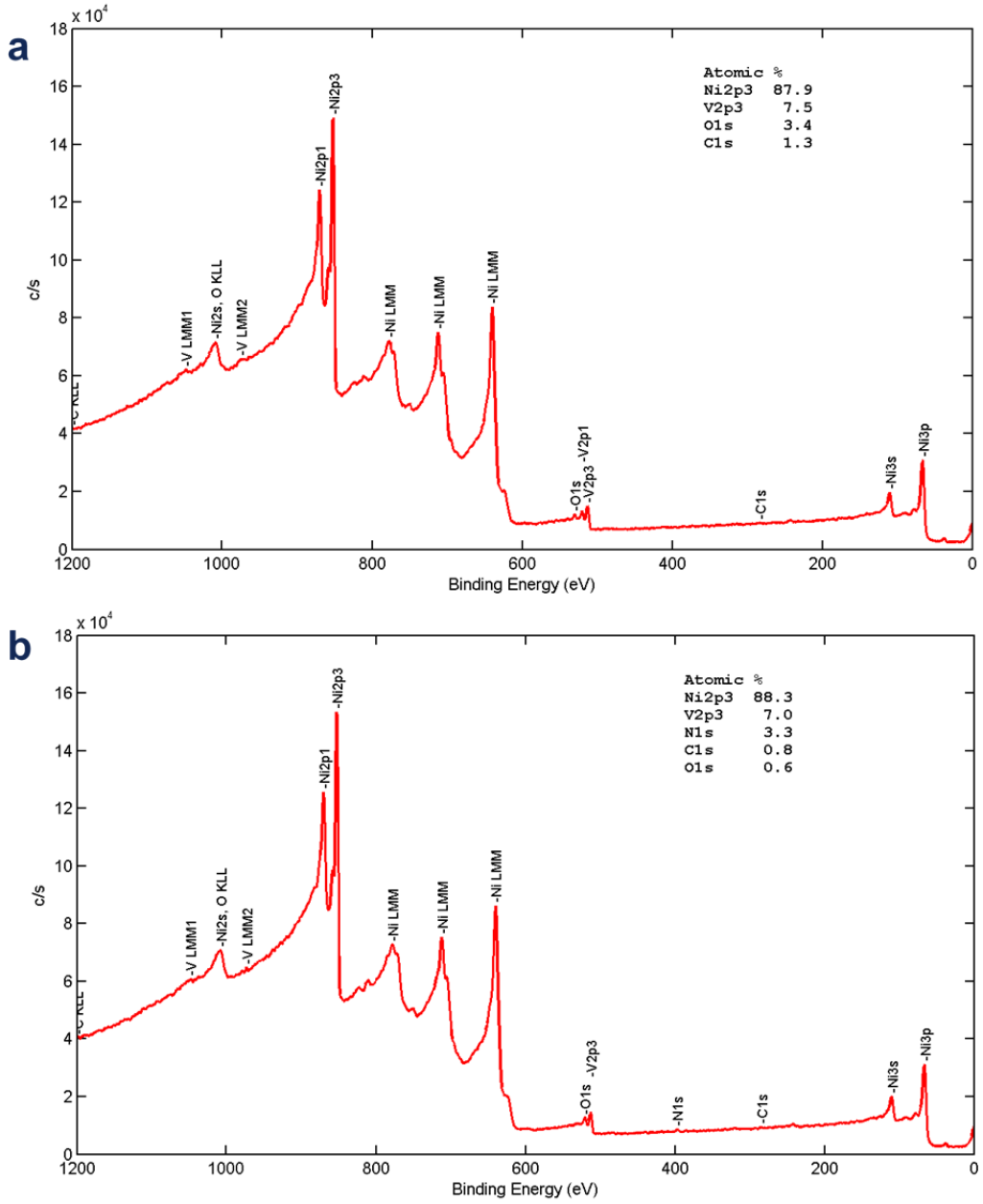


Figure 4. 24. Survey scan after 1 minute cleaning with Ar. (a) NiV 5000 Å. (b) NiVN 5000 Å.

After removing first angstroms, elements appear as nickel and vanadium for NiV

sample and nickel, vanadium and nitrogen for NiVN sample (Figure 4.24). The NiV layer shows an oxidized nickel and a vanadium in different states (0, 2, 4) before cleaning, and this is compatible with a surface oxidation with the formation of NiO_x and V_xO_y species (Figure 4.25 and 4.26).

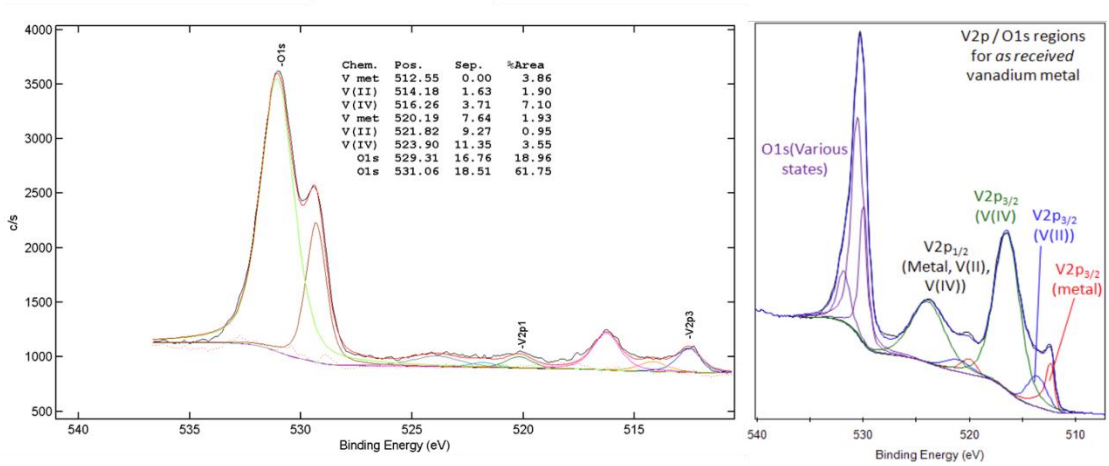


Figure 4. 25. NiV sample, HR scan before cleaning with Ar. Detail of O1s + V2p orbitals, confirming the oxidation of vanadium, which results in various states.

After Ar sputtering Ni and V appear in their metallic state (Figure 4.27 and 4.28). These results are in line with NiV XRD pattern with higher peaks related to pure nickel in its fcc structure and a smaller one attributable to oxygen presence.

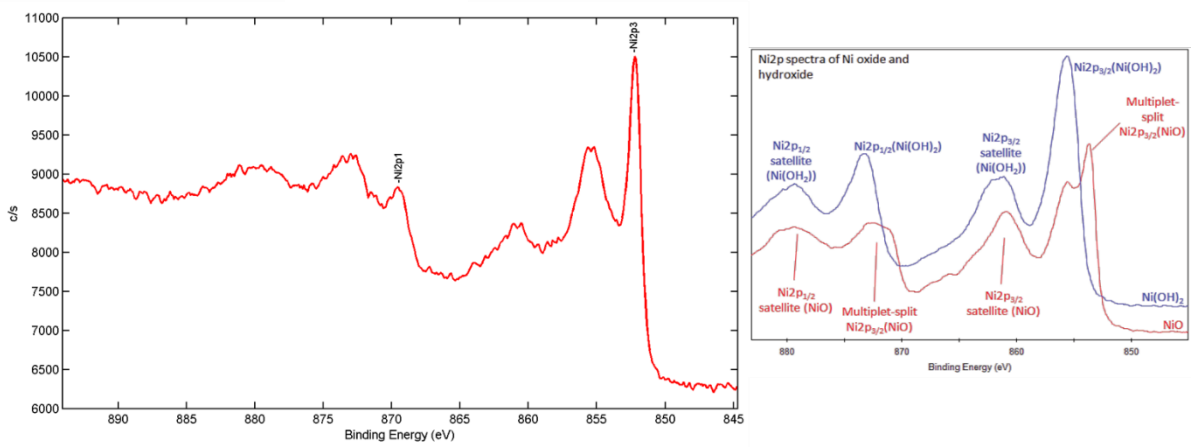


Figure 4. 26. NiV sample, HR scan before cleaning with Ar. Detail of Ni2p orbitals, consistent with the formation of hydroxides and NiOx species.

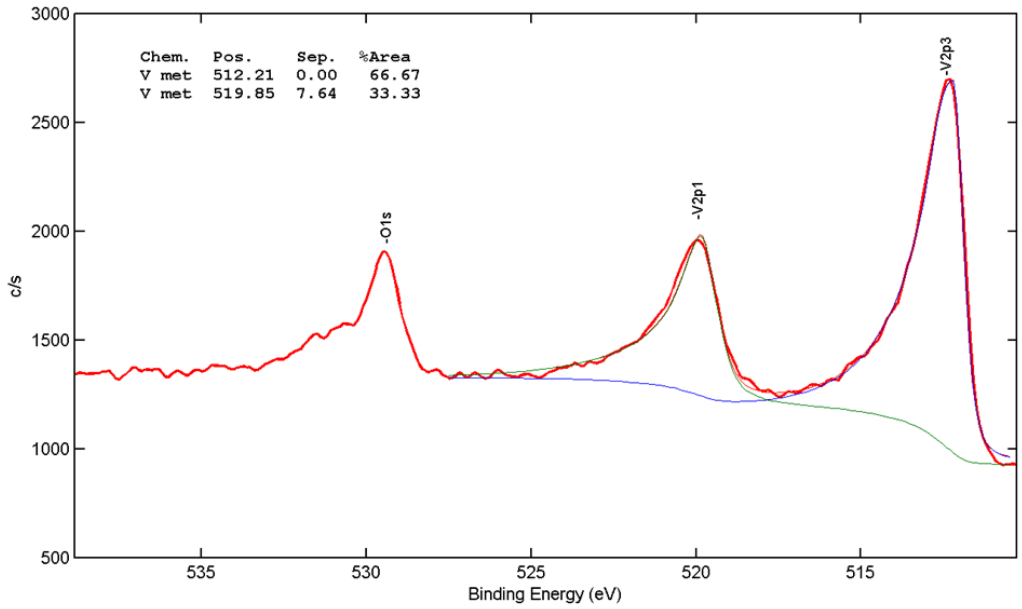


Figure 4. 28. NiV sample, HR scan after 1 minute cleaning with Ar. Vanadium appears in its metallic state.

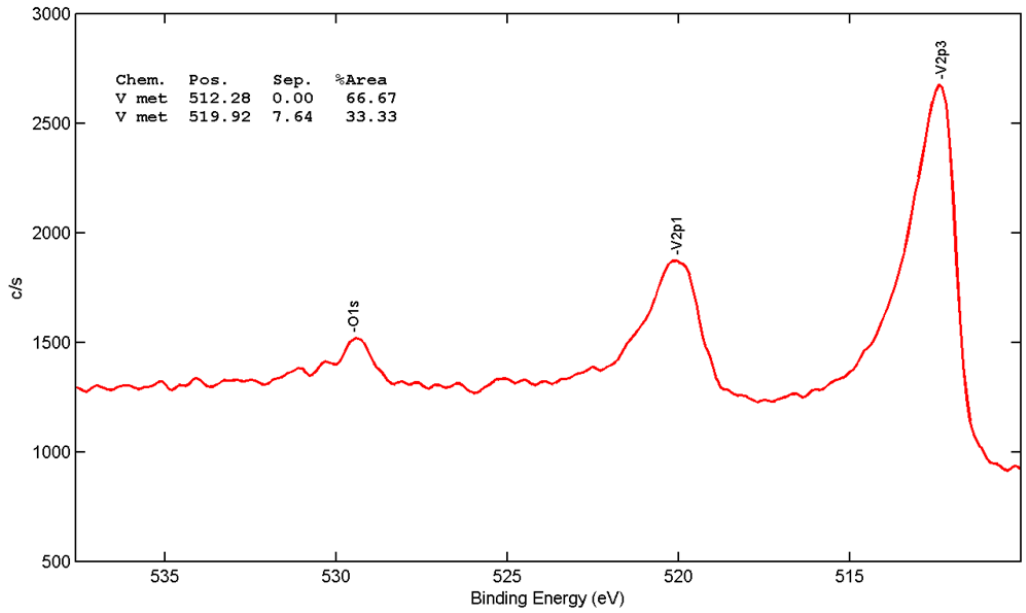


Figure 4. 27. NiVN sample, HR scan after 1 minute cleaning with Ar. Vanadium appears in its metallic state.

The NiVN layer presents a behavior close to the previous except for the nitrogen signal. Its location and its intensity are consistent with metal nitrides (Figure 4.29), which usually forms fcc crystal structures, as well as pure metals. This could suggest a substitutional doping of nitrogen forming nitrides with vanadium and nickel.

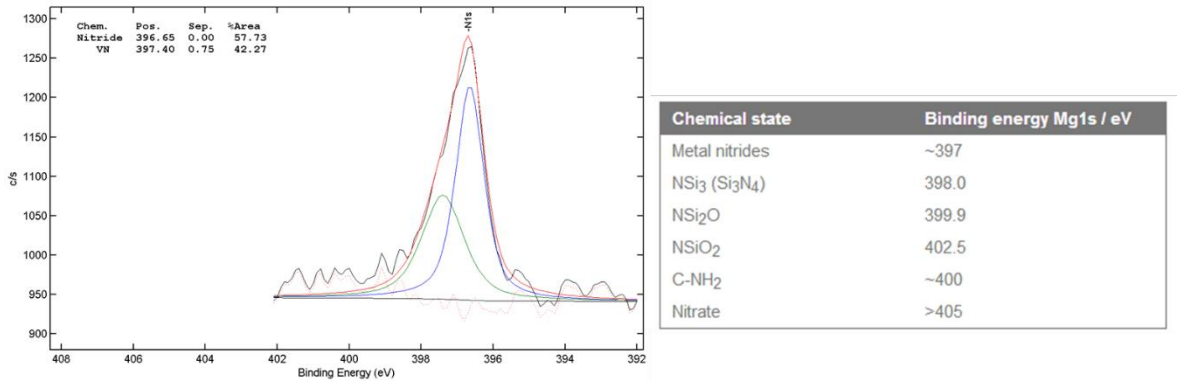


Figure 4. 29. Nitrogen peak in NiVN sample spectra. The signal is consistent with vanadium nitride and metal nitride species.

Comparing principal peak intensity of NiV and NiVN samples, oxygen O1s signal results lower for the nitrogen doped sample. The solubilization of nitrogen could have reduced the oxygen penetration by substituting it in the crystal structure (Figure 4.30).

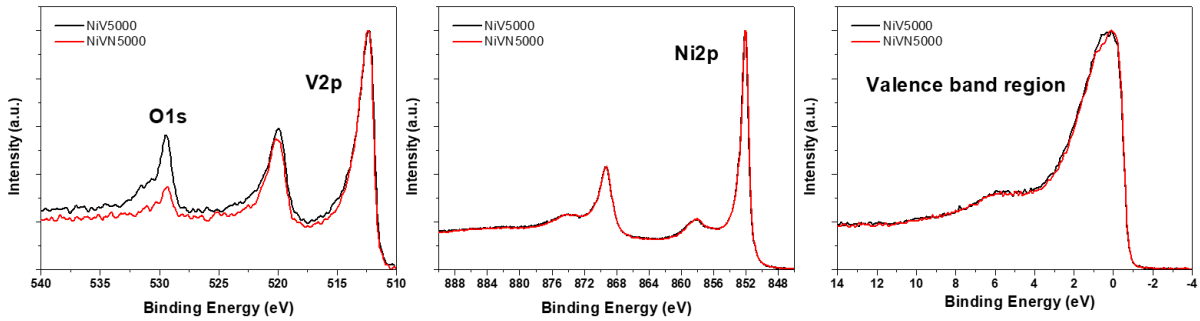


Figure 4. 30. Principal peak comparison of NiV and NiVN samples. Oxygen (O1s), vanadium (V2p), nickel (Ni2p) and valence band region signals are superimposed to highlight differences in terms of intensity.

4.3.5 Conclusions

Stress induced by metal film deposition represents an important complication to address when dealing with thin wafers. In this work, the adoption of nitrogen during deposition of nickel metalizations has been investigated to understand its influence on film residual stress and physical structure.

A considerable variation in terms of wafer bowing is evident when nitrogen concentration increases during deposition. The maximum improvement has been obtained with 40% of N_2 and 60% of Ar. The presence of nitrogen in samples was confirmed by EDX analysis. Moreover, a further investigation on nitrogen incorporation has been performed with AES, comparing NiVN film sputtered with different percentage of N_2. Consequently, nitrogen concentration appeared to be uniform along all the thickness indicating an inglobation during layer-by-layer deposition. The analysis of film morphology has been achieved with TEM and revealed the creation of conic columnar structures in the NiV layer, which were absent in the NiVN one. This type of geometry is usual in metals deposited via PVD techniques and is likely to introduce a tension.

To establish the origin of changes in material properties XPS and XRD analysis have been completed. Considering the NiVN diffraction spectra, an important left shift on both characteristic signals is visible. Above mentioned rearrangements can be originated by an increment of the distance between two adjacent planes, suggesting a possible insertion of nitrogen atoms in the fcc structure.

Furthermore, nitrogen signal in XPS is consistent with metal nitrides, which usually forms fcc crystal structures, as well as pure metals. This evidence supports a substitutional doping of nitrogen forming nitrides with vanadium and nickel.

In conclusion, a detailed description of the effects of nitrogen incorporation in nickel thin films has been outlined and the improvements on wafer residual stress proved. Different techniques have been adopted to investigate the nature of doping and the type of interaction between Ni and N, each supporting the creation of metal nitrides species.

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Chapter 5

Insulators

5.1 Degradation of materials in electronics

Electronic devices corrode in the same ways as automobiles, bridges and pipelines, but due to their small dimensions, failures are more severe. As any other body or material they are subjected to oxidation and deterioration, which are is accelerated by our atmosphere composition and by the presence of light [1] [2] [3].

Even if corrosion is often seen as a threat, these reactions are not always unwanted. In effect, under control, these interactions are categorized with the name of galvanic chemistry and are employed to create functional films, but when they occurs under devices working condition (e.g. in the presence of humidity or ionic contamination) they can cause catastrophic electrolytic dissolutions.

Luckily catastrophic corrosion failures can be minimized by selecting appropriate integrations of corrosion-resistant coatings, which in semiconductor fabrications are usually defined passivations. In this context, recently advances rely on the introduction of new materials with innovative properties or (more often) on new combinations of materials in ad hoc structures [4].

This thesis work adopts the second approach, considering termination design and passivation materials as an ensemble that should be optimized simultaneously to increase device lifetime and robustness.

These effects are a basic requirement nowadays where devices and components *must* perform with a high degree of reliability, especially when intended for the automotive sector [5].

For this research a high-voltage temperature humidity bias (HV-THB) test has been adopted to investigate synergies between the various passivation materials and trigger specific device failures. Details on this test characteristics have been explained in Chapter 3.

5.2 Silicon based thin film to prevent corrosion

The corrosion behavior of any material or structure is determined by the nature of its local environment. Important factors include humidity, temperature and available species. When these ones can not be modified, because represent the specific conditions to which a product is expected to work in, the solution is the creation of ad hoc packaging or coating [6] [7].

For this reason, the utility of thin silicon based films to serve as corrosion barriers has been extensively studied.

These films are usually represented by amorphous silicon, amorphous silicon nitride, amorphous silicon carbide and amorphous silicon oxide [8] [9] [10]. The first two have been used in this work as passivation layer to prevent electrical field surface peaks and protect devices from the outside environment. The last one, obtained by low thermal deposition has been investigated as an alternative to silicon nitride.

5.3 Amorphous silicon

In Chapter 4 the importance of termination region in devices with high blocking voltage capability (≥ 600 V) has been discussed. The introduction of a silicon

resistive layer, contributes to spread the voltage drop across that area, avoiding peaks of electrical field and assuring the required performance.

This type of films is usually formed by amorphous silicon (a-Si) or semi-insulating polycrystalline-silicon (SIPOS). A typical scheme of devices passivated with amorphous silicon is presented in Figure 5.1.

Since their properties varies significantly with process parameters (sintering temperature, oxygen content, hydrogen presence, grain dimension…) a comparison between some of the principal deposition methods has been performed.

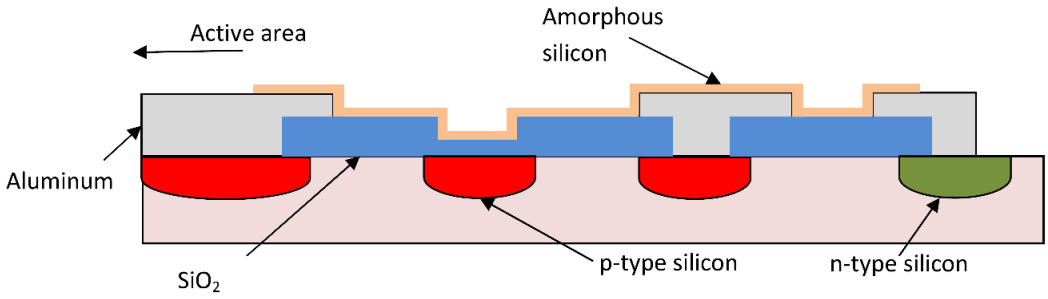


Figure 5. 1. Typical HV termination. Amorphous silicon on top is used as passivation.

Furthermore, even this material represents a minor portion of the device, it introduces appreciable complexity to the system. Thus, its characteristics should be tuned carefully to achieve the correct impact on electrical parameters. In this context, the leakage current represents the principal variable to consider, since any contamination or defect in the film structure has a direct impact on the material conductivity [11] [12].

5.3.1 Physical properties

a-Si differs from monocrystalline or polycrystalline silicon because of its continuous random network (Figure 5.2). Instead of forming a four-bonded tetrahedral structure, in fact, the atoms present numerous unconnected dangling bonds.

These dangling bonds directly impact on a-Si physical properties causing poor conductivity. When a-Si is passivated by hydrogen, these effects vary and, depending on the application, can be modulated.

Chemically, hydrogen atoms interact with the dangling bonds to produce hydrogenated amorphous silicon (a-Si:H), which is often used in electronics. More specifically, these dangling bonds produce a clear electron spin resonance (ESR) signal [13], which has been used to evaluate changes in the chemical-physical behavior of the material under different conditions or treatments.

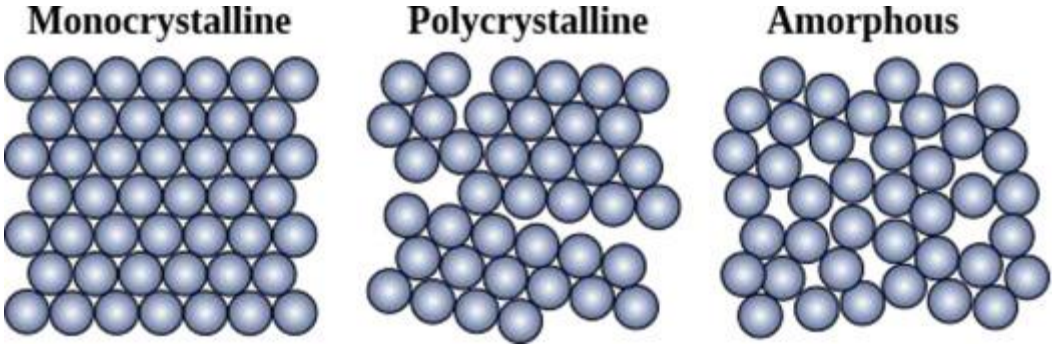


Figure 5. 2. Comparison between a crystalline, polycrystalline and amorphous material.

From these studies appeared that the room temperature electrical conductivity decreases proportionally with annealing at temperatures between 50 and 500°C. However, throughout this temperature scale no significant changes in short-range order have been found by X-ray diffraction analyses [14].

The most promising theory sees variations in the electrical conductivity as related to the restoration of surface, micro-voids responsible for the ESR signal, as a result of the thermal treatment.

In addition, a-Si physical properties depend on different factors including deposition process type and layer thickness. Brodsky et al. reported that some of them are influenced by the optical and thermal history of the layer in a reversible way. In particular, long exposure to light seems to decrease the conductivity far

more significantly than heating, so that an exposure at 150°C returns it to its original value.

Since leakage current characteristic of devices working at high blocking voltage represent a critical parameter and is strictly related to the termination passivation region [4] [15], further investigations on a-Si impact on this characteristic have been performed.

5.3.2 Experimental set up (Part 1)

Amorphous silicon layers have been deposited using a DC magnetron sputter and an e-beam evaporator. These layers have been applied on a set of 600V power diodes, then presenting a simple passivation structure composed of silicon oxide, amorphous silicon and polyimide (Figure 5.1).

An additional silicon nitride (Si_3N_4, from here referred as SiN) layer has been deposited by PECVD.

Wafers subjected to sintering process have been heated in a fast-ramping furnace (ATV PEO-601) for 30 minutes. Thickness of films have been acquired by reflectance measurements using a N&K 1500-D analyzer.

Power diodes under investigation have been tested using Accretech UF190R prober.

Next tables summarize experimental structure then covered in detail in the following paragraph.

Step 1: Evaporator Vs. Sputter process comparison.

A group of identical wafers have been a-Si passivated respectively with sputter and evaporator methods, varying only this step in their manufacturing process. Three different thicknesses have been evaluated and the sintering process has been fixed to 380°C.

Table 5. 1. Step 1 experiment summary.

a-Si deposition	*Thickness (Å)*	*Annealing temperature*	*SiN layer*
Evaporator	1800	380°C	no
	1300		
	800		
Sputter	1800		
	1300		
	800		

Step 2: Investigation of a-Si annealing temperature effect on electrical parameters.

Fixing same thickness for both deposition methods, a sintering temperature screening has been performed in order to understand its impact on the a-Si layer. Sinter process requires a temperature close to 400°C, in order to promote silicon penetration in the AlSi underlying layer. Higher degrees may produce a complete solubilization of Si in Al, for this reason, 380°C and 400°C have been selected for this experiment.

Table 5. 2. Step 2 experiment summary.

a-Si deposition	*Thickness (Å)*	*Annealing temperature*	*SiN layer*
Evaporator	1300	380°C	no
		400°C	
Sputter	1300	380°C	
		400°C	

Step 3: Addition of a silicon nitride layer on top of a-Si.

A further silicon nitride passivation layer is added over the a-Si one to increment devices performance during humidity tests. The sintering process is then

performed before and after SiN deposition. Because of the heating caused by this PECVD process, the same two annealing temperatures of step 2 have been tested.

Table 5. 3. Step 3 experiment summary.

a-Si deposition	*Thickness (Å)*	*Annealing temperature*	*Annealing before/after SiN deposition*	*SiN layer*
Evaporator	1300	380°C	Before	yes
			After	
		400°C	Before	
			After	
Sputter	1300	380°C	Before	
			After	
		400°C	Before	
			After	

5.3.3 Experimental results (Part 1)

As previously explained, when adopted in power diodes application, amorphous silicon layer can directly influence electrical parameters, such as leakage. In order to characterize the a-Si layer behavior when applied as resistive film in passivations, an analysis on the impact of its deposition on product final performance has been performed.

As first step, a comparison between leakage measurements at probe level between a-Si evaporated and sputtered wafers has been performed. Different layer thicknesses have been considered, fixing sintering temperature to 380°C. Film depth was confirmed by reflectance measurements on monitors. Once recipes were optimized, three wafers per thickness have been produced and tested.

From this initial test appeared that diodes with evaporated a-Si were less affectable by film variation. No significant difference in terms of leakage has been

found comparing different thicknesses. On the other hand, diodes produced with sputtered a-Si showed higher variability (Figure 5.3 and Table 5.4).
In all cases, lower thicknesses seem to induce lower leakage values.

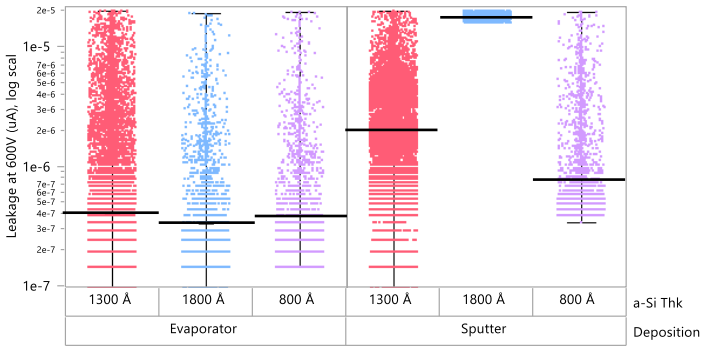


Figure 5. 3. Variability plot of the Logarithmic of the Leakage current at 600 V Vs. different a-Si thickness and deposition methods. Evaporator samples appear as the most stable.

Table 5. 4. Variability summary of data obtained in Step 1. See Figure 6.3.

Variability Summary for Leakage at 600V	**Mean**	**Std Dev**	**Observations**
Deposition[Evaporator] a-Si Thk[1300 Å]	4.17E-07	1.40E-06	68326
Deposition[Evaporator] a-Si Thk[1800 Å]	3.46E-07	1.06E-06	10517
Deposition[Evaporator] a-Si Thk[800 Å]	4.08E-07	1.16E-06	10845
Deposition[Sputter] a-Si Thk[1300 Å]	2.04E-06	1.92E-06	64329
Deposition[Sputter] a-Si Thk[1800 Å]	1.78E-05	9.55E-07	6502
Deposition[Sputter] a-Si Thk[800 Å]	7.62E-07	1.45E-06	10717

Leakage current moves across the termination following the scheme in Figure 5.4. For this reason, a reduction in film thickness is comparable to a reduction in the section of the current flux vector.

The possibility to obtain repeatable and stable processes with sputters instead of evaporators is a key to reduced cycle times, increase capacity and improve automation. In effect, evaporation techniques, are characterized by labor and time which can be up to 10 times higher than sputter-based ones, affecting product final cost.

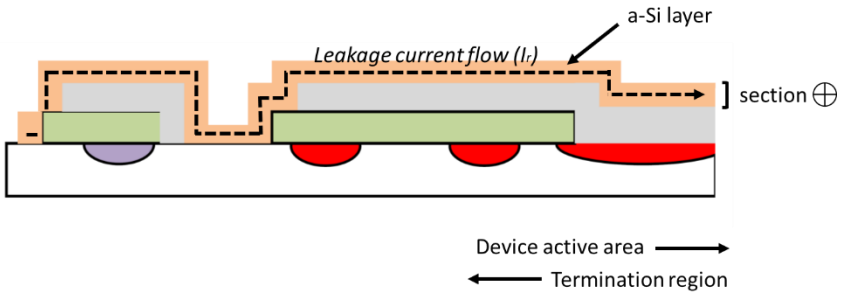


Figure 5. 4. Leakage current flow inside the device in reverse bias using amorphous silicon to conduce current.

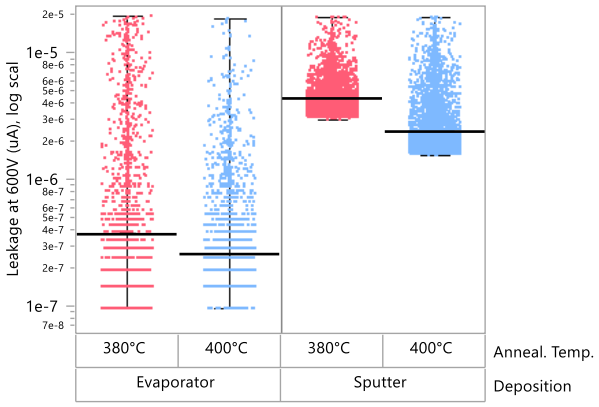


Figure 5. 5. Variability plot of the Logarithmic of the Leakage current at 600 V Vs. different sinter temperatures and deposition methods. Sputter deposited samples present the highest values.

Table 5. 5. Variability summary of data obtained in Step 2. See Figure 6.5.

Variability Summary for Leakage at 600V	**Mean**	**Std Dev**	**Observations**
Deposition[Evaporator] Anneal. Temp.[380°C]	3.88E-07	1.47E-06	10804
Deposition[Evaporator] Anneal. Temp.[400°C]	2.68E-07	7.54E-07	10894
Deposition[Sputter] Anneal. Temp.[380°C]	4.35E-06	1.26E-06	14133
Deposition[Sputter] Anneal. Temp.[400°C]	2.52E-06	1.74E-06	10852

As second step the influence of two different sintering temperatures has been evaluated, and also in this case, evaporated samples resulted less subjected to variations (Figure 5.5 and Table 5.5). Moreover, sputtered ones do not present comparable performance yet.

The sintering process is adopted to improve a-Si adhesion on the underlying layer of AlSi alloy. Increments in temperature usually contributed to leakage reduction allowing microcracks restoration.

As third experiment the addition of a SiN layer has been tested. This layer can be useful to improve device reliability when working in harsh environment. Since its deposition apport another thermic treatment, different sintering temperature have been investigated.

As previously found higher the temperature to which a-Si layer is exposed, higher is the reduction of the leakage current. In particular with the combination of a 400°C annealing, performed after SiN deposition a-Si sputtered samples reached performances close to the evaporator ones (Figure 5.6 and Table 5.6).

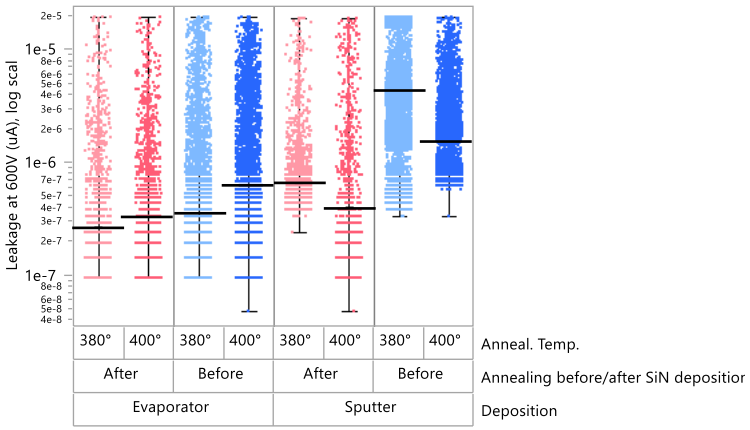


Figure 5. 6. Variability plot of the Logarithmic of the Leakage current at 600 V Vs. different sinter temperatures and deposition methods. Samples have been improved with a SiN layer as further passivation and annealing has being performed before or after its deposition.

Table 5. 6. Variability summary of data obtained in Step 3. See Figure 6.6.

Variability Summary for Leakage at 600V	**Mean**	**Std Dev**	**Observations**
[Evaporator] Annealing before/after SiN [After] Anneal. Temp.[380°C]	2.80E-07	0.000001	10826
[Evaporator] Annealing before/after SiN [After] Anneal. Temp.[400°C]	3.10E-07	1.05E-06	10826
[Evaporator] Annealing before/after SiN [Before] Anneal. Temp.[380°C]	3.46E-07	1.16E-06	46482
[Evaporator] Annealing before/after SiN [Before] Anneal. Temp.[400°C]	6.54E-07	1.84E-06	21554
[Sputter] Annealing before/after SiN [After] Anneal. Temp.[380°C]	6.80E-07	9.90E-07	10834
[Sputter] Annealing before/after SiN [After] Anneal. Temp.[400°C]	4.22E-07	1.55E-06	7089
[Sputter] Annealing before/after SiN [Before] Anneal. Temp.[380°C]	4.90E-06	5.80E-06	42138
[Sputter] Annealing before/after SiN [Before] Anneal. Temp.[400°C]	1.77E-06	1.71E-06	21487

5.3.4 Analysis of amorphous silicon films resistance

In power diodes, leakage current represents one of the principal causes of failure and power loss. Among the materials usually adopted in the termination region, a-Si has an active role in improving efficiency through its resistance.

In their work, Brodsky et al. proposed a relation for the calculation of the electrical conductivity of amorphous layers of IV group elements of the period table (such as silicon and germanium) [13]:

$$\sigma = \sigma_0 \, exp[-(T_0/T)^n]$$

In this equation T is the temperature (at which calculation is performed) and σ_0 and T_0 are model dependent parameters; n can be any number up to unity and is often found in literature as $\frac{1}{4}$.

However, although experimental distributions appeared to fit this equation with a good grade of approximation, there is no consensus in defining a general correlation. Moreover, several issues related to measure effective I-V curves have contributed to the lack of a common resistivity constant definition for this material. Van den Berg et al. affirmed that this problem is principally related to the change of a-Si characteristics with long term light exposure [16], but another reason is the significant variation of properties of these amorphous layers depending on their treatments and local defects [12].

In this thesis a new approach has been ideated and adopted to evaluate the impact of annealing on layer resistance.

5.3.5 Experimental set up (Part 2)

For this purpose 8 wafer monitors (20 Ω cm fixed resistivity) have been patterned with a-Si layers of different thickness producing a series of 0.88 x 0.88 cm pads. These ones are then contacted with aluminum and insulated by a polyimide layer on the edges (Figure 5.7 and Table 5.7).

Figure 5. 7. Cross section scheme of device adopted for a-Si layer resistance evaluation. Measures are performed perpendicular to wafer (red arrow).

Differently from other usual designs adopted in these contexts, this one is thought to work perpendicularly to wafer and not parallelly [17] [18] . The wafer monitors

here prepared, in fact, are characterized by a resistance around six orders of magnitude lower than the a-Si expected one, and do not represent a source of error.

This design presents pros and cons. Among the positives, the possibility to reduce extreme high values of resistance, because film layers can be deposited in very low thicknesses and do not risk electrical discharges. On the other hand, one of the negative aspects is the possible effect of the substrate bulk acting as a spreader. In any case, the objective of this experiment is to evaluate the impact of annealing on film properties from a qualitative point of view. In particular, this test is to understand if high temperature sinter plays a significant role in reducing leakage, as appear from previous experiments, by incrementing amorphous silicon resistance.

a-Si here analyzed has been deposited by sputter and half of the samples have been subjected to a 30 min at 380°C thermal treatment. For the direct resistance measurement Keysight B1505A curvetracer has been used. Higher thicknesses have also been prepared but are not here presented since characterized by a very poor correlation. This is to be attributed by a design which favorites thin film evaluation.

Table 5. 7. Split table of experiment samples.

ID	*Process*	*Tool*	*AmSi thk*	*Sinter*
16	Sputter	534	2500	yes
17	Sputter	534	2500	no
18	Sputter	534	1800	yes
19	Sputter	534	1800	no
12	Sputter	534	1300	yes
13	Sputter	534	1300	no
22	Sputter	534	1000	yes
23	Sputter	534	1000	no

5.3.6 Experimental results (Part 2)

To extract resistance data, I-V curves have been acquired on samples with different a-Si layer thicknesses. Resistance is related to voltage and current by the equation

$$R = \frac{V}{I} = \frac{\rho L}{A}$$

where V and I are respectively the registered tension and current, ρ is the intrinsic resistivity, L the length (in this case the a-Si layer thickness) and A is the section (corresponding to the pads area).

The local resistance R is then calculated as the angular coefficient of the V-I curve. Due to the creation of Schottky barrier, between a-Si an Al pads, instead of a ohmic contact, curves tend to a logarithmic behavior (Figures 5.8, 5.9 and 5.10). For this reason, the angular coefficient has been calculated considering a linear fit not in the origin.

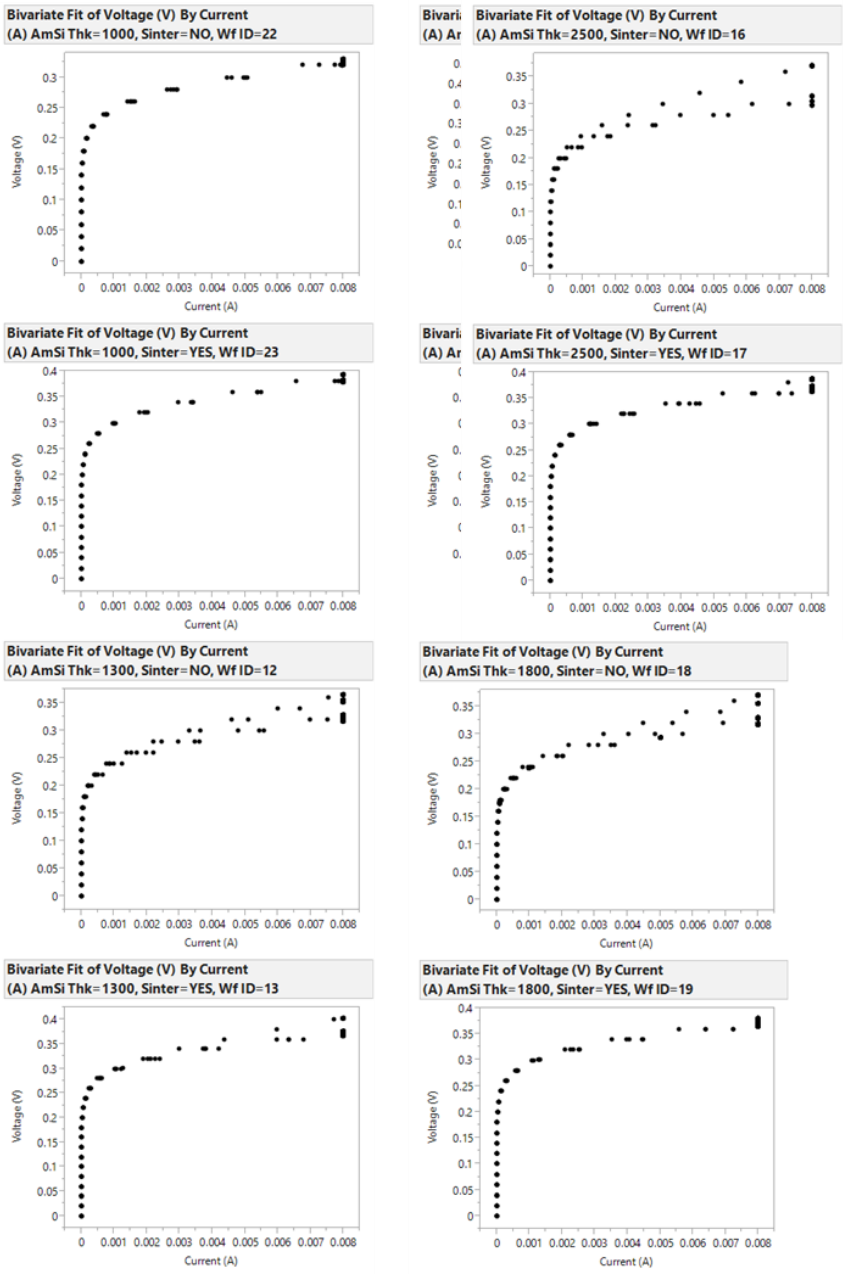
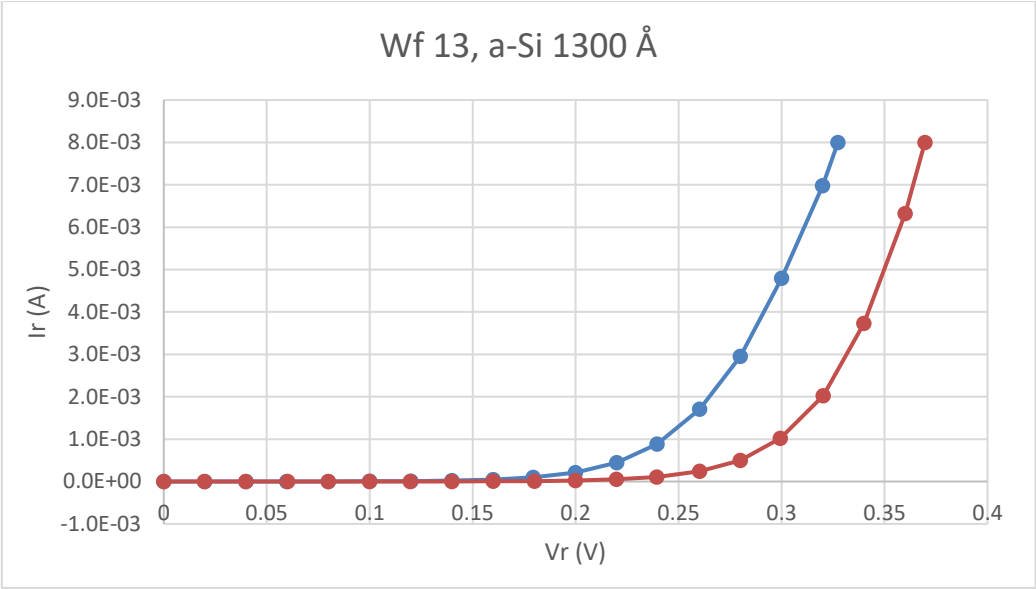


Figure 5. 8. Bivariate plots of Voltage Vs Current. Each one is composed by 5 different measurements on equivalent pads. For the resistance calculation, the second part of the curve (at higher V values), where a linear behavior is present, has been considered.



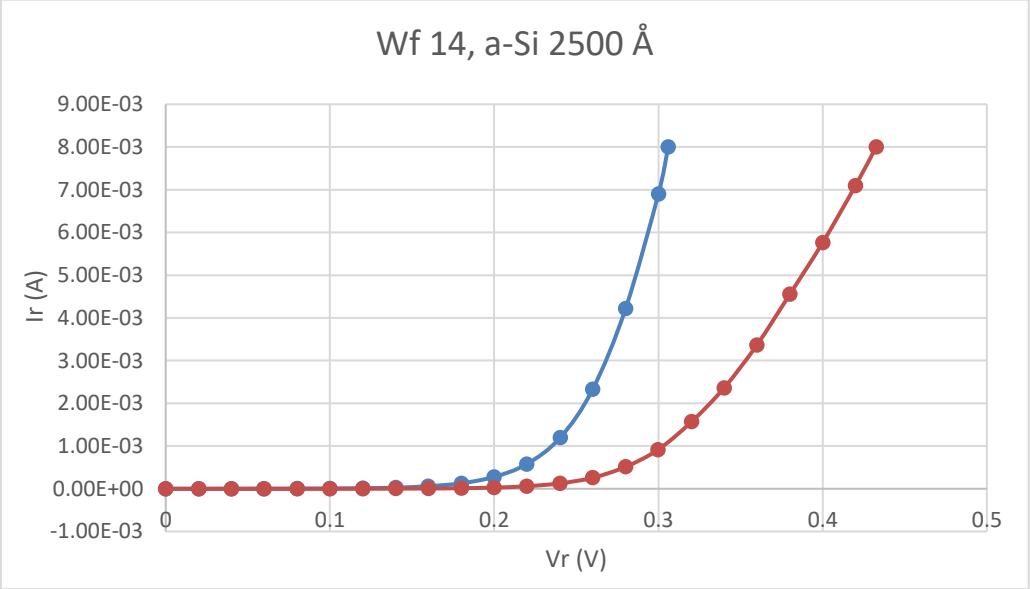
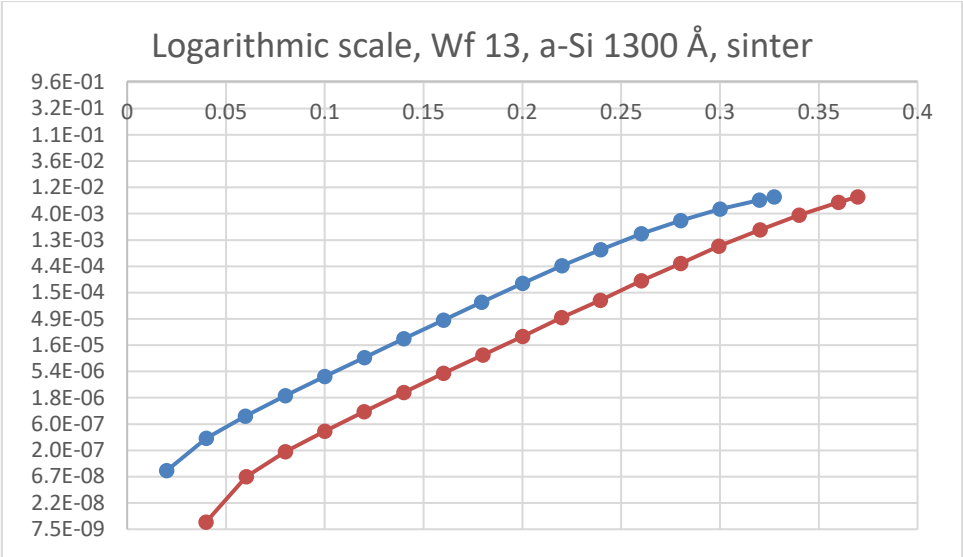


Figure 5. 9. Detail of I-V curves for two of the thicknesses. Single measurement plotted: in blue, no sintered samples; in orange, sintered ones.



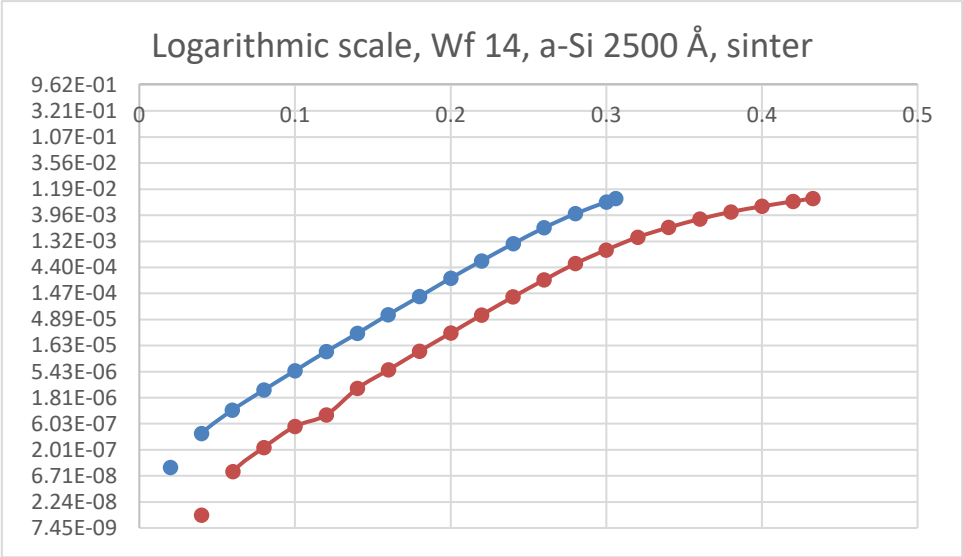


Figure 5. 10. Logarithmic scale of samples 13 and 14: in blue, no sintered samples; in orange, sintered ones.

More in detail, for the purpose of resistance extrapolation, the fit has been performed the linear region of the I-V curves, at higher voltages.

Data and fits are presented in Figure 5.11 and in Table 5.8 and 5.9.

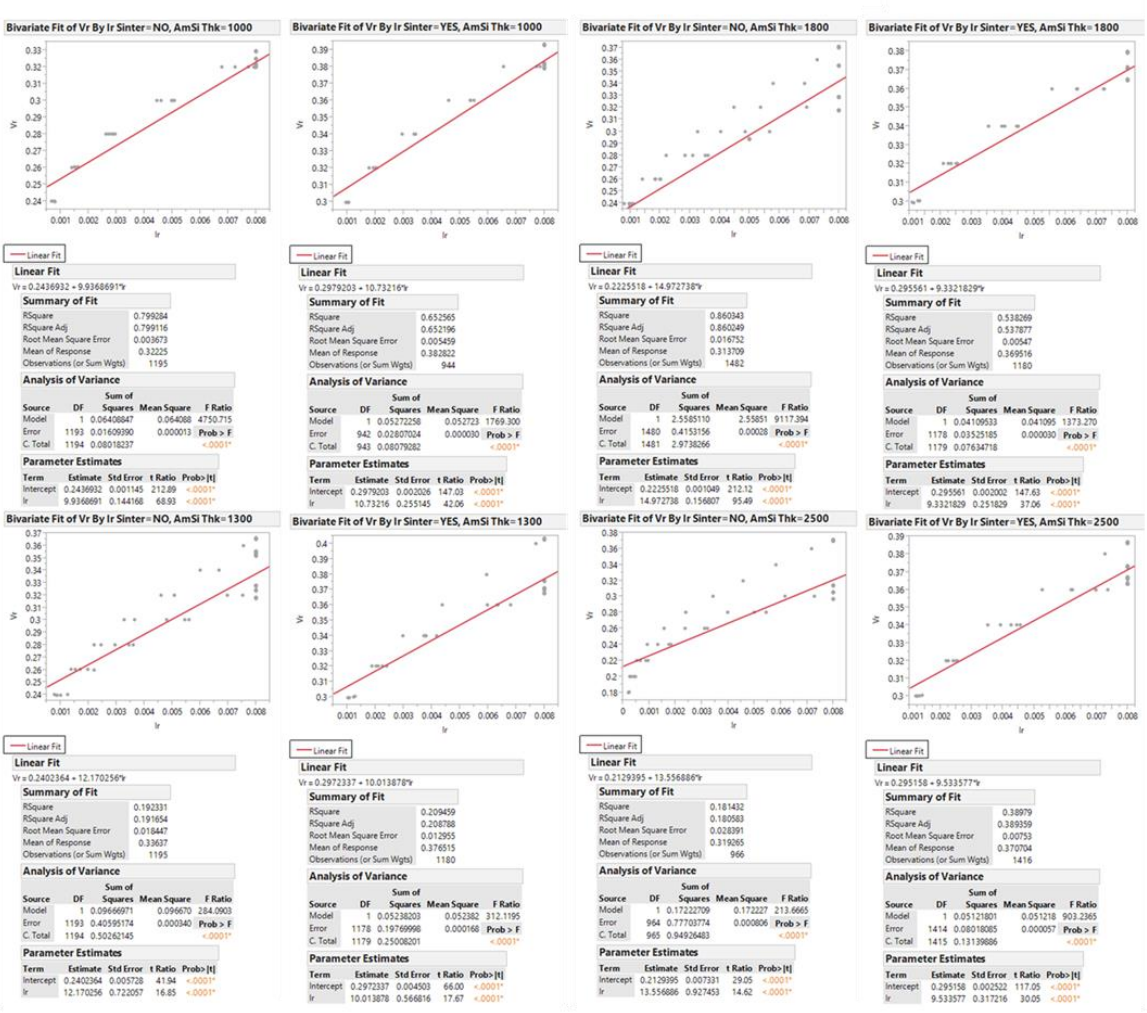


Figure 5.11. Linear fit of data once considering only linear region of the V-I curve. Values of sintered samples are more spreaded and result in poor goodness of fit.

Table 5. 8. and 5.9. Calculated angular coefficients of linear fits of sintered and non sintered samples.

No sinter	
Thk Å	R (linear coefficient) Ω
1000	9.937
1300	12.170
1800	14.973
2500	13.557

Yes sinter	
Thk Å	R (linear coefficient) Ω
1000	10.732
1300	10.014
1800	9.332
2500	9.534

From these results, no clear extrapolation can be made. Values of sintered samples are more spreaded and result in poor goodness of fit. However, sintering seems to apport a general modification of the film resistance. In particular, when low thicknesses are considered a compenetration between aluminum and silicon is likely generated. This effect may result in a general conversion towards a common values of resistance generated by the modification of film structure.

5.4 Amorphous silicon nitride and silicon oxide

To improve device performance under stress test, a further test was performed by adding two capping layers of PECVD silicon nitride and PECVD silicon dioxide to complete the passivation structure [19].

Silicon nitride (SiN_x) is one of the most powerful materials for coating and passivation films used in electronics. Its low-temperature deposition allows applications on completed wafer structures without risk of damages [20]. Moreover, as described previously in this Chapter, the light apport of thermal energy this process con produce, has been demonstrated as a valuable addition to improve contact and sintering between layers reducing leakage current dissipation.

SiN_x films have been extensively studied but their applications have been limited by their fragility. In effect, thick silicon nitride layers suffer from crack formation, which causes premature device failures. Their combination with more flexible materials such as organic polymers resulted the perfect compromise [4].

The advantage of organic films is that polymers have lower internal stress and less mechanical and thermal mismatch with respect to silicon [21]. On the other hand, they usually present higher water uptake when subjected to humid environments [22] [23]. Specifically, for the MTP power module, a weight difference of 1.9 g was measured after 24 h at 85% RH [4].

In this work, deposited silicon oxide integrated with Polyimide (PI) has been tested as a more flexible alternative to SiN.

5.4.1 Experimental set up

Two sets of 650 V power diodes, having the same primary passivation structure of silicon oxide plus a-Si and PI, were produced by adding either a silicon dioxide (sample A) or a silicon nitride (sample B) interlayer with the same thickness. These films have been produced by PECVD (Figure 5.12).

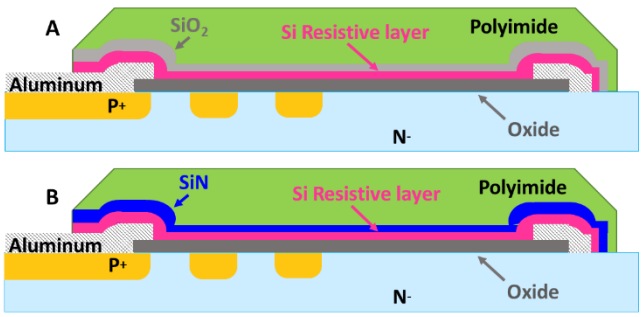


Figure 5.12. Passivation details: SiO_2 capping layer (sample A) and SiN capping layer (sample B) applied to a typical planar HV termination.

Following fabrication and assembly in MTP power modules, the devices were stressed by performing HV-THB tests at 85°C, 85% RH, with 520 V applied bias (V_r at 80% of rated voltage capability).
After test, further investigations on devices have been performed by optical microscopy using a Nikon Eclipse LV150, and by scanning electron microscopy using an AURIGA, ZEISS FIB-SEM system.

5.4.2 Results and discussion

Inorganic dielectric materials such as silicon oxide and silicon nitride, represent a strong barrier against contamination and moisture. However as previously described in Chapter 2 silicon oxides is easily doped by introducing atoms and ions in its loose structure. To evaluate its behavior under humidity, contact angle measurements have been conducted on silicon resistive layers deposited on doped or non-doped oxides. The adoption of amorphous silicon as interlayer helped to better discriminate between the two sample types, amplifying the effects with its predisposition to water absorption.
These investigations showed that resistive layers deposited on P-doped low thermal oxide presented higher surface wettability and sharp angle drop shape. The same measurements performed on the silicon resistive layer deposited on undoped materials instead appeared with a more hydrophobic behavior (Table 5.10 and Figure 5. 13).

Table 5. 10. Contact angle measurements on resistive silicon deposited on doped and undoped oxide.

Calculated angles for water drop on a-Si over:	
a) Doped oxide	32.6°
b) Undoped oxide	46.4°

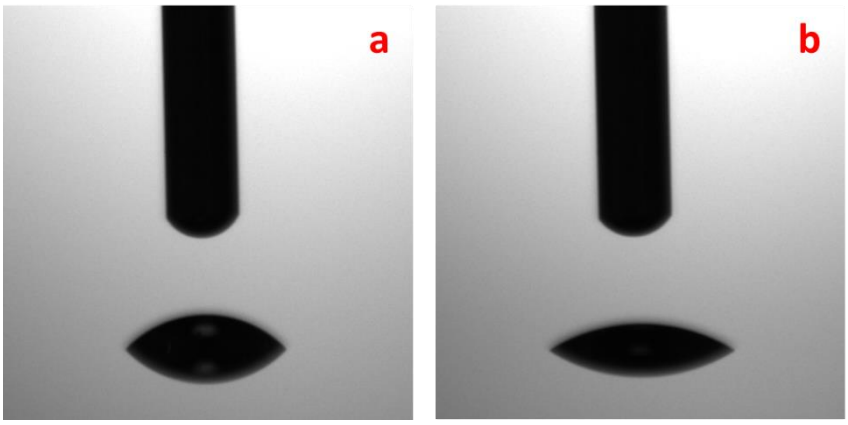


Figure 5.13. Contact angle comparison between amorphous silicon resistive layer deposited on (a) undoped oxide (b) doped oxide

After this first evaluation, HV-THB reliability tests have been focused on evaluating two different complete passivation structures, in which the samples had the same first level passivation, but different secondary passivation: silicon oxide (sample a), silicon nitride (sample b).

Before and after each step of the HV-THB test (Chapter 3), the DUTs were subjected to I-V analysis of the diode reverse characteristics.

As result, devices with a silicon nitride capping layer did not exhibit any shift or significant electrical characteristic variation, presenting a stable leakage current level up to 1500 h. In contrast, the devices with a SiO_2 capping layer displayed a leakage shift above the imposed threshold after 750 h, and so the test was stopped before further deterioration.

After device decapsulation, failure analysis proceeded with an optical inspection of the selected DUTs. Optical microscope evaluation of the SiO_2 samples, which failed after 750 h, seemed to evidence no physical change in the device structure. As expected, the same result was obtained for the silicon nitride samples, which were still presenting good electrical characteristics after 1500 h. However, an in-depth observation performed with SEM on an FIB cut of the DUTs that failed after 750 h highlighted small voids in the Si resistive layer and on the capping oxide. The leakage degradation is then attributable to the morphological variation

of the interface between the oxide capping layer and the silicon resistive layer (Figure 5.14.a).

Figure 5.14.b shows the SEM image of a silicon nitride sample that still showed good electrical characteristics after 1500 h of the HV-THB test, with no sign of physical degradation.

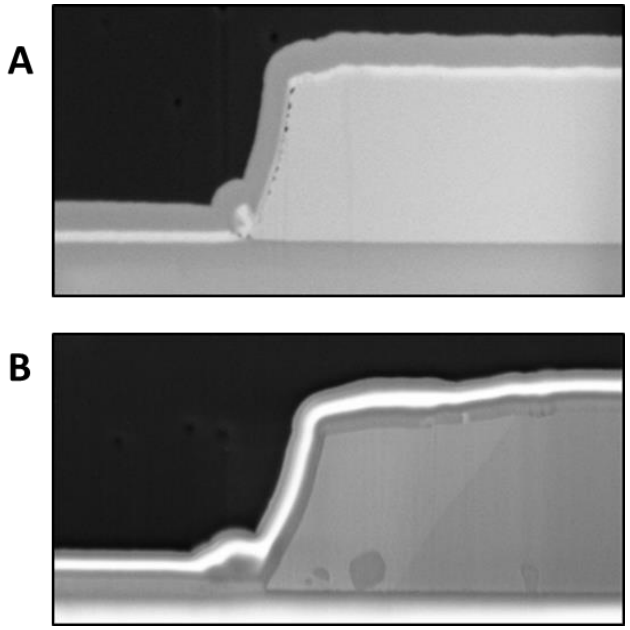


Figure 5.14. (a) SEM image of an FIB cut of SiO2 DUT that failed after 750 h. Small voids on the Si resistive layer and on the oxide capping interface are evident. (b) SEM image of an FIB cut of silicon nitride DUT that showed good electrical characteristics after 1500 h of HV-THB testing. No signs of variation are present between the passivation layers.

5.5 Conclusions

In this Chapter the importance of corrosion in electronics has been discussed with a focus on its effects on amorphous materials composing a typical passivation structure for HV planar devices.

In fact, corrosion failures can be minimized through selection of appropriate coatings for the termination region, and by combining improved designs and passivation structures this work aims to increase device lifetime and robustness.

In this context, amorphous silicon films play a role in reducing leakage current through their resistance, but this activity might be compromised by external contaminations or humidity penetration. Furthermore, even this material represents a minor portion of the device, it introduces appreciable complexity to the system since any defect has a direct impact on the material conductivity. From here the importance of investigating not only its physical and chemical characteristics, but to study its resistance as well.

Thus, a-Si deposition process, thickness and annealing temperature have been examined in order to understand their influence on the device electrical performance. Comparing devices with same design but different a-Si layer types, a correlation between amorphous silicon layers deposited with sputter technique and higher leakage currents has been found. More specifically, these devices appeared far more sensitive to any change in the a-Si layer (such as thickness, or heat treatment), with significant variations in leakage registered at probe level.

In addition, in situ resistance analyses on a dedicated design highlighted that annealing is likely to modifie the structure of these films, producing a change in resistance. In this aspect further investigation are needed but, since devices produced with sintered a-Si have shown an evident improvement on leakage parameter, this process step appeared as necessary to our scopes.

Afterwards, amorphous silicon nitride and oxide layers have been introduced as further protection beside organic passivation upon the amorphous silicon one, and the HV-THB test has been adopted to trigger specific failures and investigate materials reliability. In these evaluations, silicon nitride appeared as the best candidate for this role since it successfully passed the 1000h threshold imposed by the automotive specifications.

In conclusion, the primary and secondary level of passivation of a class of HV planar devices have been improved by selecting specific parameters for the amorphous silicon deposition in order to tune its resistance and thus the device leakage current. This development has been further enhanced by a silicon nitride capping layer to increment device robustness and avoid humidity penetration.

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Chapter 6

Conclusions

In this work, the primary and secondary passivation level of a class of HV planar devices have been improved by selecting specific process parameters and modifying its design through the implementation of a capping layer.

This achievement was essential to meet the latest automotive sector requirements in terms of efficiency and reliability, and in this context the high-voltage temperature humidity bias (HV-THB) test represents a valid assessment to determine device robustness up to 1000 hours (Chapter 3). Furthermore, this test has been adopted to investigate interactions and synergies between the various layers because able to trigger specific device failures, which successively examined have brought to the explanation of degradation mechanisms involved (Chapters 4 and 5).

At the same time, considering termination design and passivation structure as an integrated ensemble to be optimized simultaneously, this study focused on material analysis and process optimization by adopting a layer by layer approach which is reflected on the chapter subdivision.

In effect, materials properties can be strongly affected by processes in which they are involved. These influences may vary from microstructure (for aluminum) to

atomic disposition (for nickel) and from layer resistance (for amorphous silicon) to moisture absorption (for dielectrics) .

Metal deposition processes have been evaluated to understand their impact on device electrical performance and wafer residual tension. Temperature appeared as one of the most crucial variables in aluminum deposition, because able to increment grain size and producing microcracks which reduce ohmic contact and device resistance to humidity.

Besides, nitrogen presence in the sputtering chamber resulted as a key factor in producing low stress nickel metalizations, which are known to be the most impacting on wafer. The nature of this type of doping has been analyzed with different techniques and descripted in detail in Chapter 4, as well as the aluminum above mentioned features. Both have been fine tuned to produce the most suitable solution for this class of HV planar devices.

Afterwards these devices degradation has been discussed in Chapter 5, with a focus on its effects on amorphous materials composing their passivation structure.

Moreover, through a monitoring of the leakage parameter and resistance measurements, the a-Si layer has been optimized and enhanced by the introduction of a silicon nitride capping layer. This combination has been adopted to increment device robustness and avoid humidity penetration.

In conclusion, a systematic approach has been used to study and validate the complex termination–passivation plurality. The interactions between different materials constituting the structure of a class of power diodes devices have been investigated, while a process optimization and layout improvement have been accomplished.

The combination of high voltage, temperature and relative humidity has appeared to be the most stressful one for the devices, and HV-THB’s capability to trigger failure modes has been employed to analyze the principal degradation phenomena. Furthermore, a full description of the involved chemical physical mechanisms has been proposed.

Eventually, this research contributed to validate new device designs with optimized passivation structure and superior reliability performances.