Grid Fault Current Injection using Virtual Synchronous Machines featuring Active Junction Temperature Limitation of Power Devices

# Grid Fault Current Injection using Virtual Synchronous Machines featuring Active Junction Temperature Limitation of Power Devices

Fabio Mandrile, *Member, IEEE,* Fausto Stella, *Member, IEEE,* Enrico Carpaneto, *Member, IEEE* and Radu Bojoi, *Fellow, IEEE*

***Abstract*—The recent years have seen an exponential growth in the electric generation from renewable energy sources, such as wind and sun. This scenario represents an opportunity to decarbonize part of the energy sector and phase out fossil fuels. However, particular care must be taken to ensure the correct operation of the electric grid. With a large penetration of power electronics based generation, special care must be taken in case of grid faults, due to limited short circuit current capabilities of static converters, supporting the grid in case of faults. For this reason, static converters have to be transiently overloaded to inject fault currents larger than their nominal limit, mimicking the behavior of synchronous generators. Therefore, this paper proposes the combined solution of a transiently overloadable virtual synchronous machine (VSM) converter equipped with real-time semiconductor junction temperature limitation. The VSM provides the necessary short circuit current references and the inverter can be overloaded with an active thermal control strategy, avoiding the oversizing of the power semiconductors, by properly exploiting their thermal limits. This represents a possible path for further power electronics integration into the grid.**

***Index Terms*—Virtual Synchronous Machines, VSM, Virtual Inertia, Grid-connected Converters, Junction Temperature Estimation, Short Circuit Current, Silicon Carbide, SiC, Thermal Sensitive Electrical Parameter, TSEP**

## I. Introduction

THE recent energy policies have encouraged a radical shift towards more sustainable electricity sources. The strict limitations on greenhouse gas emissions are encouraging renewable energy sources (RESs), such as wind and sun. This transition presents, however, several challenges. The electric power system stability relies in fact on the so called ancillary services (i.e., active and reactive support) provided by the synchronous generators (SGs) connected to it. Therefore, a too large penetration of non-synchronous generation, such as from wind and sun, would reduce the power system strength [1], [2] due to the limited overload capabilities of the converters. In fact, the power system requires each generating unit connected to the grid to instantaneously inject fault current during voltage dips. This has two purposes:

1) Trigger the overcurrent and impedance protection relays, which depend upon the detected instantaneous fault currents. A too small fault current would not trigger the protection devices;
2) Increase the retained voltage at the healthy nodes during the fault.

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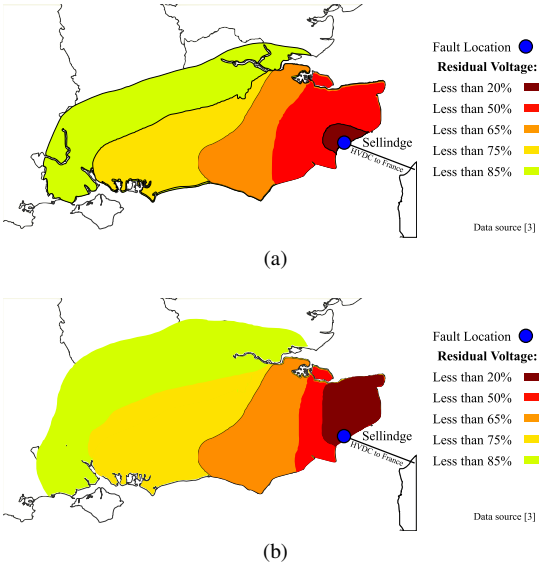


Fig. 1. Simulation comparison of a three-phase fault on the 400 kV network in the UK power system. Data from [3]. From top to bottom:
a) Current network effect of a three-phase earth fault at Sellindge;
b) 2025 network effect of a three-phase earth fault at Sellindge with a large penetration of renewable sources ("Gone Green" Scenario).

In the current scenario, traditional SGs automatically provide such fault current and can even be transiently overloaded without incurring into thermal issues, given the long thermal time constants of the machines. However, the future perspective of a larger energy production from converter-based renewable sources raises the issue of how to provide such fault current. In fact, electronic power converters do not automatically inject fault currents, as they require proper control strategies during faults and cannot be overloaded as the SGs, due to the very short thermal time constants of the power devices. Several studies have been carried out to foresee the impact of such limitations on the voltage profile of power systems, as the one reported in Fig. 1 [3]. This simulation compares the impact of a three-phase to earth fault in the UK grid in the present scenario (see Fig. 1a) and in a hypothetical future scenario with a large penetration of renewable energy sources (see Fig. 1b). The outcome of this study shows that with a large penetration of RESs, the fault would affect the

electric grid in a larger area, reducing the residual voltage at the healthy grid nodes. Therefore, more advanced control strategies and more stringent technical requirements [4] in terms of fault current injection will be compulsory for static converters connected to the grid.

To this purpose, a viable control strategy is the virtual synchronous machine (VSM). This concept emulates the grid side behavior of SGs through static converters [5]–[8]. Despite their effectiveness in generating the necessary current references during voltage dips [9], VSM converters still have some hardware limitations compared to SGs, such as the limited overloadability of static power converters and the long term reliability of power semiconductors.

As said, real SGs (made of steel and copper), can cope with transient overloads thanks to their large thermal capacity. Typical thermal constants for synchronous generators are in the orders of minutes, therefore they can be easily overloaded (up to 5–7 pu) to inject fault currents. Electronic power converters, on the other hand, are far from being overloadable. Generally, the thermal capacity of the semiconductor die and its enclosing package is considered as negligible. Therefore, the rated and overload current of the converters are generally identical, independently from the duration of the overload. Only the heatsink thermal capacitance can be exploited. However, this enables a very limited overload of the converter. Moreover, in recent years, the introduction of new packaging solutions combined with innovative semiconductors technologies such as Silicon Carbide (SiC) has made it possible to increase the power densities of the semiconductor dies, further stressing their thermal capabilities. Besides, they are much more expensive compared to classic Silicon based devices. Therefore it is even more critical to fully exploit the safe operating area (SOA) of such devices, with no unnecessary oversizing of the semiconductor part of the converters.

According to the grid operators [10], static power converters should be transiently overloadable of a factor 1.5–2 in the time range of 80–500 ms (typical duration of dips [11]) to effectively support the grid. Although this degree of overload capability seems negligible compared to classical SGs, it is important from the grid operator perspective [12]. With classical designs, the power semiconductors would be sized for the maximum overload current that the converter has to provide. This would however lead to a costly oversizing of the power semiconductors, which would be underexploited most of the time. Therefore, **the main contribution of this paper is a semiconductor-based VSM with fault-current overload capability**. A VSM strategy is integrated for the first time with a real-time junction temperature control to provide fault currents larger than 1 pu for short transients. This solution is appealing for next-generation grid converters based on innovative semiconductor materials, such as SiC, as it avoids expensive oversizing of the semiconductor part. Moreover, such converter is virtually failure free from the thermal point of view during both normal and grid fault operation thanks to the estimation of power semiconductors' junction temperature. Finally, the large short-circuit current references of the VSM control can contribute to the correct operation of modern grids in case of faults.

This paper is organized as follows. Section II presents the overall structure of the proposed converter structure. Then, the VSM model is described in Section III. The junction temperature estimation technique is detailed in Section IV and its control in Section V. Finally, Section VI contains the experimental validation of the proposed solution with symmetrical voltage dips. The conclusions are provided in Section VII.

## II. Block Diagram of the Converter

The proposed control strategy is implemented on a two-level, three-phase inverter interfaced to the grid through an LCL filter, as shown in Fig. 2. The dc side is an ideal voltage source.

### A. Control Strategy

The proposed controller consists of two major blocks:

- **S-VSC**: the adopted VSM solution is the Simplified Virtual Synchronous Compensator (S-VSC) [9]. The S-VSC generates compensating power references $P_v$, $Q_v$ in case of abnormal grid conditions (e.g. voltage dips).
- **Junction temperature estimation and control**: this block estimates the junction temperature $T_j$ of the power switches and generates the maximum allowable output current signal $I_{max}$. The thermal management part of the semiconductor junction temperature is divided into two stages. First, the semiconductor junction temperature $T_j$ is estimated from its on-state resistance. This requires the measurement of the on-state voltage drop $V_{SWx}$ and current $i_{SWx}$ across each switch. Then, this temperature $T_j$ is limited to its reference value $T_j^*$ reducing the maximum inverter current output.

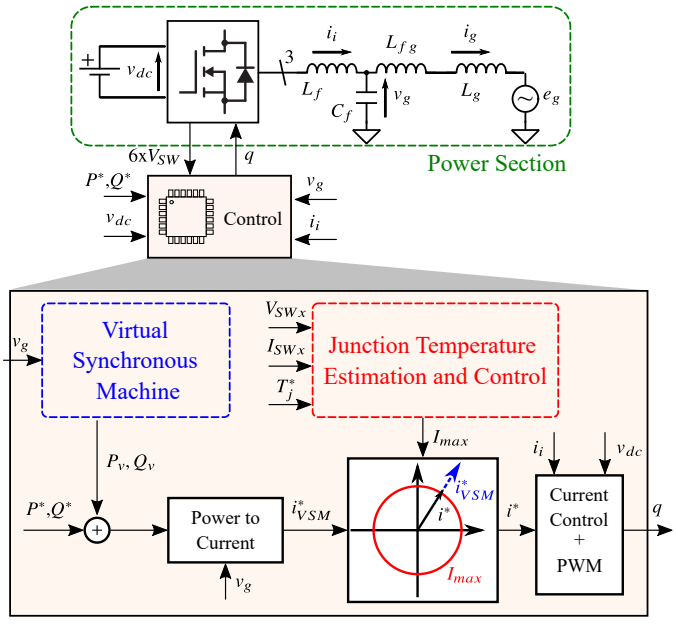


Fig. 2. Block diagram of the proposed VSM converter with active semiconductor junction temperature limitation.

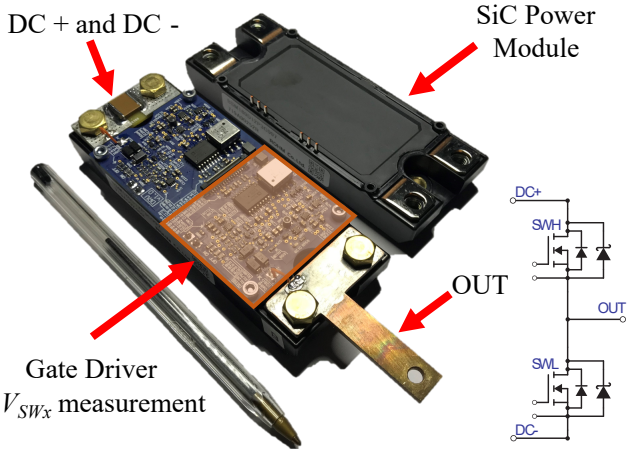


Fig. 3. Picture of the employed BSM180D12P3C007 SiC power modules and of the designed gate driver with on-state voltage $V_{SWx}$ measurement.

TABLE I
BSM180D12P3C007 POWER MODULE RATINGS.

| | | | |
|---|---|---|---|
| Rated Current ($T_c = 60°C$) | 180 A | $R_{ON}$ @ 50°C | 11 mΩ |
| Breakdown Voltage | 1200 V | $T_j^{max}$ | 175 °C |

### B. Hardware Setup

The proposed solution is implemented on a three-phase inverter, which uses three ROHM SiC power modules BSM180D12P3C007 in half bridge configuration, as shown in Fig. 3. The ratings of the adopted power modules are listed in Table I. Each power module embeds two SiC MOSFETs with two SiC antiparallel diodes for better commutation and conduction performance of the device. The schematic of the power section of the proposed test rig is reported in Fig. 4, where the sampled quantities are marked in red. Compared to classical three phase inverters for grid applications, there are the additional measurements of the six MOSFETs conduction voltages ($V_{SWx}$) detailed in [13]. The other measurements, such as the dc link voltage, the phase currents, the line voltages and the heatsink temperature are already part of a standard three-phase grid converter. The red quantities are sampled at each control period (50 µs in this setup) and are known to the control.

## III. Virtual Synchronous Machine Control

The S-VSC operates in parallel with the main power channels of the inverter [9]. This means that the S-VSC only generates the compensation power references $P_v$ and $Q_v$, enabling the converter to provide ancillary services to the grid (i.e., inertial power, reactive support). The S-VSC is implemented in per unit values (base voltage $V_b$, base power $S_b$ and base angular speed $\omega_b$). This VSM consists of 4 key blocks, as shown in Fig. 5.

First, the model of the virtual rotor of a SG (mechanical emulation block), which implements the following simplified swing equation [9]:

$$\omega_r = \frac{P_{set} - P_v}{2Hs}; \quad \theta_r = \frac{\omega_b}{s}\omega_r \tag{1}$$

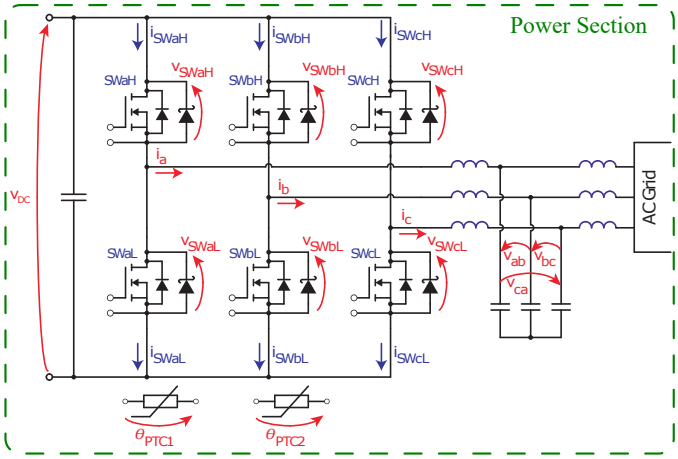


Fig. 4. Schematic of the power section of the adopted test rig.

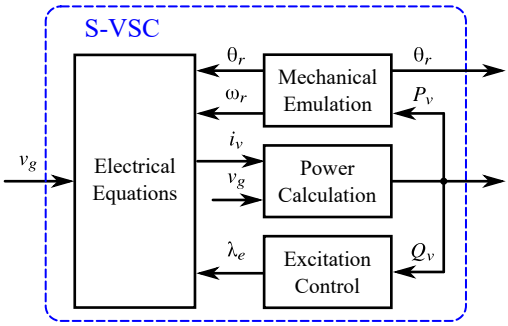


Fig. 5. Diagram of the employed VSM control: the simplified virtual synchronous compensator (S-VSC).

where $\omega_r$ and $\theta_r$ are the virtual rotor speed and position; $P_{set} = 0$ is the reference active power of the S-VSC, which is always set to 0, as per S-VSC parallel operating concept [9] and $H$ is the virtual inertia constant of the S-VSC. This block is in charge of the power synchronization to the grid and provides the reference angle for the inner current controller. It also provides inertial active power references in case of grid frequency variations. However, the inertial action is outside the scope of this paper, requiring usually current levels well below the maximum admissible value of the converter.

The second block implements the virtual stator and damper equation (electromagnetic equations of the machine). The virtual stator is implemented in the virtual rotor frame ($d$,$q$) and models a virtual resistance $R_s$ and inductance $L_s$. This block also provides damping to the S-VSC using a simplified $q$-axis damper winding [9]. The working principle and the tuning of this damper winding are not further described as not part of the scope of this paper, being already available in the literature.

The third block is the excitation control. This block is crucial in the scope of fault current injection and reactive support, as it regulates the reactive power exchange with the grid and the fault current dynamic during dips. The adopted excitation control structure is of integral type [14], as depicted in Fig. 6. This excitation control guarantees transient reactive support in case of voltage dips, by regulating the virtual

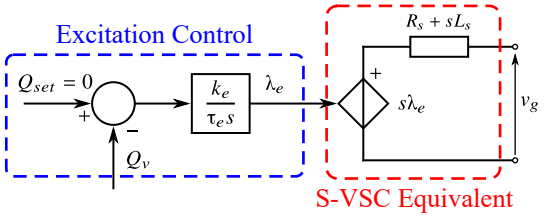


Fig. 6. Diagram of the excitation control of the S-VSC. The S-VSC can be modeled as a Thèvenin equivalent connected to the grid when analyzing the fault transients.

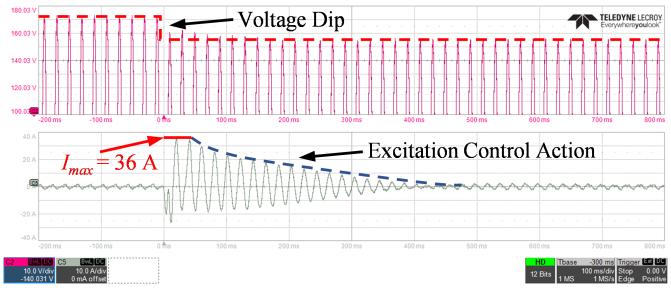


Fig. 7. Example of transient reactive support provided by the S-VSC. From top to bottom: Grid voltage positive envelope (10 V/div); Grid current (10 A/div).

excitation flux $\lambda_e$ of the machine with the desired time constant $\tau_e$. In case of grid faults (i.e., voltage reduction at the converter terminals), the S-VSC will behave as the Thèvenin equivalent circuit of Fig. 6 and will inject reactive current to support the grid and to trigger the protection relays of the power system. An example of this action is available in Fig. 7, where the S-VSC injects current to counteract a voltage dip of −10 % with a phase jump of −5°. The converter injects a fault current up to its set limit (in this example 36 A) with an amplitude profile depending on the time constant $\tau_e$ (100 ms in this example).

Finally, the power calculation block computes (in per unit) the feedback virtual active and reactive power of the S-VSC $P_v$ and $Q_v$ from its virtual stator current $i_v$ and the measured grid voltage $v_g$ as follows:

$$P_v + j \cdot Q_v = \left(v_{gd} + j \cdot v_{gq}\right)\left(i_{vd} - j \cdot i_{vq}\right) \qquad (2)$$

This virtual power is added to the external references $P^*$,$Q^*$, thus emulating an SG.

The current controller tracks the current references $i^*$, receiving the measured current $i_i$ as feedback. In the block diagram of Fig. 2, the controller is paired with the pulse width modulator (PWM) which generates the switching signals $q$ of the transistors using the duty cycles computed from the reference voltage and the measured dc-link voltage $v_{dc}$. In this paper, a space vector modulation is considered, but any other technique can be employed (e.g., discontinuous modulation). Moreover, any current control strategy is valid (linear controller, predictive...). In this paper a simple proportional-integral (PI) regulator was implemented in the S-VSC ($d$,$q$) rotor frame.

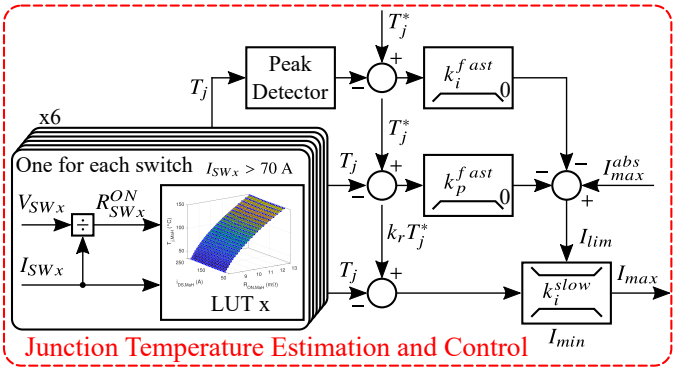


Fig. 8. Diagram of the adopted active junction temperature controller.

## IV. Junction Temperature Estimation

During the years, multiple methodologies have been developed to measure or estimate the junction temperature of the power semiconductors. State-of-the-art power converters use model based techniques to estimate the junction temperature of the power devices [15], [16]. Starting from the direct measurement of the heatsink or direct bonded copper (DBC) temperatures obtained by a thermistor, the junction temperature is calculated with the use of a thermo-electrical model of the system. However, the thermal and the losses model of the system are usually known very roughly. This allows to obtain only an approximate estimate of the junction temperature, thus forcing to maintain large safety margins.

Therefore, in the last years, the Thermo Sensitive Electrical Parameters (TSEPs) techniques have gained the interest of the scientific community [17], [18]. This family of techniques make use of indirect indicators such as currents and voltages to estimate the junction temperature of the devices. Multiple TSEPs can be used depending on the target semiconductor. For the MOSFET commonly used TSEPs are: the gate threshold voltage [17], [19]–[21], the saturation current [22]–[24], the di/dt during commutation [24]–[26], the body diode threshold voltage [18], [24], [27] and the conduction resistance [25], [28], [29]. These techniques are usually compared in terms of linearity, sensitivity and easiness of calibration.

It is well known from the literature that thermal cycling strongly affects the lifetime of power electronic components [27], [30]. TSEP techniques easily allow monitoring the thermal stress on the power semiconductors during the converter operation. Therefore, enabling predicting aging-related failures and scheduling preventive maintenance. This allows lowering maintenance costs, particularly in applications where unscheduled repairs can be costly, such as offshore wind farms [31]–[33]. The adopted solution belongs to the TSEPs families, in particular it is based on the well-known correlation between the conduction resistance of MOSFETs and their junction temperature.

### A. $R_{ON}$-based Junction Temperature Estimation

The main focus of this paper is not to investigate the technology used to estimate the junction temperature of the power switches, therefore only a summary explanation will

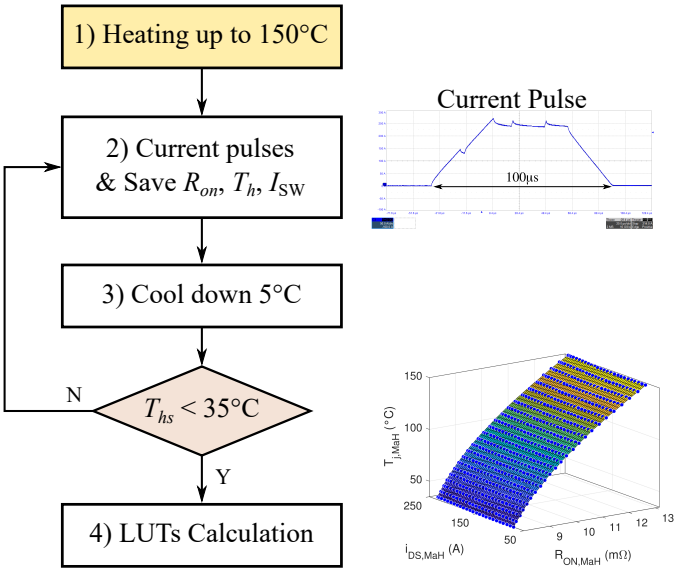


Fig. 9. Calibration test flowchart. The iterative calibration process returns a look up table relating the current $i_{SWx}$ and on-state resistance $R^{ON}_{SWx}$ to the junction temperature $T_{jx}$ for each switch.

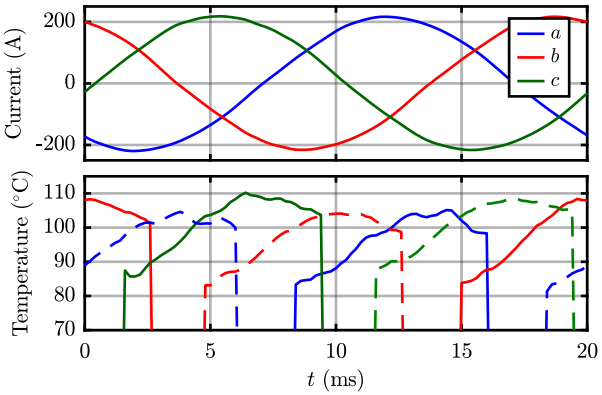


Fig. 10. Estimated junction temperature $T_{jx}$ of each inverter switch. Top: sampled phase currents of the converter. Bottom: estimated junction temperature. Dashed line: low-side switches. Solid line: high-side switches.

be provided here. As mentioned, the adopted technique is based on the well-known correlation between the junction temperature of a MOSFET and its conduction resistance. The functional block of the proposed temperature estimator is shown in Fig. 8. At each PWM period, the currents $i_{SWx}$ (reconstructed from the inverter output currents and the duty cycles) and the conduction voltages $V_{SWx}$ of the six switches are measured. These quantities are the inputs of six look up tables (LUT) (one for each MOSFET) to estimate the junction temperature of each device.

These LUTs are in the form $T_{jx}(R^{ON}_{SWx}, I_{SWx})$ and are calibrated in the commissioning phase of the target inverter. The calibration process, detailed in [34], follows the iterative diagram of Fig. 9 and is summarized as follows:

1) The aluminum plate is preliminary heated to 150°C, according to the two PTC thermistors on the aluminum plate. The hotplate is turned OFF and the aluminum plate starts cooling naturally;
2) At this temperature, short current pulses (less than 100 µs) from 10 A to 240 A with steps of 10 A are commanded in open loop fashion for each of the six inverter axes [13]. For each temperature, the currents pulses of growing amplitude are repeated along the six inverter axes. Between each current pulse there is a waiting time of 200 ms to avoid heating of the devices. This enables to map all the six switches within 240 A, for both positive and negative currents;
3) Every time the temperature drops by 5°C (variable waiting time) a new set of current pulses is commanded along the six inverter axes;
4) The test stops when the heatsink reaches the room temperature. In this case the test was stopped at 35°C.

After the calibration test, the junction temperature of the six MOSFETs can be estimated in real-time during the normal operation of the converter using the junction temperature estimation and control block shown in Fig. 2. According to this functional block, the junction temperature of the six MOSFETs is estimated only for $i_{SWx} > 70$ A, due to the difficulty of correctly estimating the conduction resistance at low currents. However, at low current the junction temperature of the device is not thermally critical. Moreover, for negative currents it is not possible to compute the current sharing between the MOSFET and the antiparallel diode. However, also this case is not thermally critical for two reasons:

1) Part of the current of the MOSFETs is conducted by the antiparallel diode;
2) For $i_{SWx} < 0$ the switching losses on the MOSFET are negligible (zero voltage commutation).

The junction temperature estimation technique has been validated previously with a high speed thermal camera in [35]. An example of the real-time junction temperature estimation is shown in Fig. 10. The positive envelope of these temperatures represents the warmest switch and it is fed to the subsequent temperature controller. When the current in the switch is lower than 70 A, the estimated junction temperature is set to 0 and discarded. The choice of 0 is arbitrary and it is useful to visualize when the estimation is not active.

## V. Junction Temperature Control

Thanks to the real time estimation of the junction temperature of all the six MOSFETs, the control can automatically reduce the maximum allowable output current of the converter when the junction temperature tends to exceed a certain safety level set by the user. Various control algorithms can be implemented to limit the maximum allowable current in the converter when overcoming the maximum allowable junction temperature. The functional block of the control algorithm used to limit the maximum junction temperature of the power semiconductors is shown in Fig. 8.

The proposed junction thermal control strategy must keep the maximum junction temperature $T_j$ of all six MOSFETs below a preset threshold $T^*_j$, at the same time avoiding low frequency distortion of the converter output currents. This

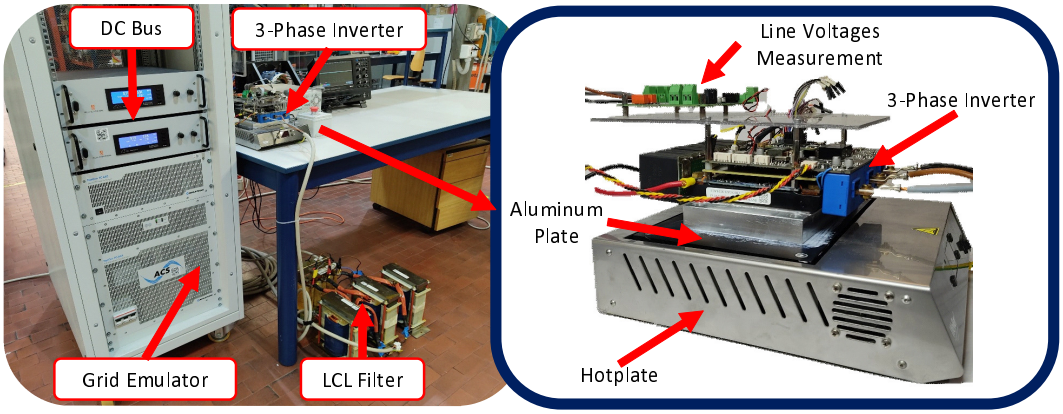


Fig. 11. Overview of the experimental setup.

action is performed by adjusting the converter maximum output current $I_{max}$ between two limits, while keeping its switching frequency constant. The lower limit $I_{min}$ represents a thermally safe condition for the converter and it coincides to the minimum calibrated current for the junction estimation (in this case 70 A). The upper limit is the absolute maximum current limit of the converter $I_{max}^{abs}$ and it is related to e.g., protection devices (fuses), current sensing limitations or saturation of the LCL filter inductors. In this paper it was set to 240 A to comply with the limitations of the available grid emulator.

This thermal control strategy is based on the following two controllers:

1) A fast proportional-integral (PI) controller quickly reduces the maximum allowable current in the converter, to limit the temperature of the warmest MOSFET within the reference temperature limit (parameters $k_p^{fast}$ and $k_i^{fast}$);
2) A slow integral (I) controller, used to increase back the maximum allowable current in the converter when the thermal stress decreases (parameter $k_i^{slow}$).

The fast PI action consists of a proportional part, directly acting on the maximum junction temperature error, and of an integral part. Using an integrator might lead to tracking problems, as the junction temperature varies at six times the grid frequency (temperature of the warmest switch, as shown in Fig. 10). Therefore, it is suggested to insert a peak calculator block, which returns the largest junction temperature value over a grid period (obtained from the S-VSC angle $\theta_r$). This block does not alter significantly the regulation dynamic, but avoids oscillating behavior around the temperature setpoint.

The tuning of this fast PI regulator is based on the thermal impedance and the loss model of the MOSFET. This results in a non-linear system, as the device losses are not linear with the device current and temperature as shown in (3) [36], where $R_{ON}$ is the ON-state MOSFET resistance, $k$ is a constant for the switching losses given a fixed dc-link voltage and switching frequency. The factor $K_i$ is the exponent of the current dependency [36].

$$P_j = R_{ON}(T_j)I^2 + k(v_{dc}, f_{sw}, T_j)I^{K_i} \tag{3}$$

It is therefore recommended to perform a preliminary tuning targeting a specific operating point (current and temperature), and then refining it on the final experimental bench.

The slow integral controller must restore the current limit when the junction cools down. Moreover, two countermeasures are taken to avoid oscillating interactions with the fast PI regulator. First, the gain $k_i^{slow}$ can be tuned to a much smaller value than $k_i^{fast}$ (in this paper $k_i^{slow} = 0.15 \cdot k_i^{fast}$). Moreover, it is advisable to scale down the reference temperature of the slow integrator of a reducing factor $k_r$ (in the range 0.95–0.97). As a result, the poorly damped oscillatory behavior of the slow integrator does not interact with the faster dynamic of the fast PI, thus not leading to current amplitude oscillations. These amplitude oscillations may cause phase current distortion, thus resulting in additional low frequency harmonics (i.e., degradation of the power quality of the system).

## VI. Experimental Validation

The proposed control of Fig. 2 has been experimentally validated. The adopted test bench is displayed in Fig. 11, showing the inverter augmented with the online junction temperature estimation connected to a grid emulator (220 Vrms line-line at 50 Hz). The switching frequency $f_{sw}$ of the converter is 20 kHz and so is executed the control task, which includes all the functional blocks depicted in Fig. 2: S-VSC, junction temperature estimation and control and current control (a PI current regulator in the rotating S-VSC rotor ($d$,$q$) frame). The parameters of the experimental setup are summarized in Table II.

To validate the proposed strategy, a realistic voltage dip was emulated. The profile of the voltage dip was taken from statistical data [11] (i.e., −16% for 500 ms). The reference junction temperature was chosen $T_j^* = 110°C$, to prove the proposed concept while complying with the current limit of the grid emulator.

Fig. 12 shows the current and junction temperature profiles during the emulated voltage dip. The response can be divided into 3 sequential phases, marked as ①, ② and ③.

During phase ① (first instants of the fault) the converter injects the maximum absolute allowed current (240 A, due to the grid emulator current limitations) and the MOSFETs

TABLE II
INVERTER AND S-VSC PARAMETERS FOR THE EXPERIMENTAL TESTS.

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $V_b$(Phase) | $120\sqrt{2}$ V | $S_b$ | 50 kVA |
| $f_{sw}$ | 20 kHz | $V_{dc}$ | 470 V |
| $L_f$ | 300 µH | $C_f$ | 40 µF |
| $L_{fg}$ | 270 µH | $L_g$ | 300 µH |
| $L_s$ | 0.1 pu | $R_s$ | 0.02 pu |
| $H$ | 4 s | $\tau_e$ | 1 s |
| $k_r$ | 0.95 | $k_p^{fast}$ | 4.5 A/°C |
| $k_i^{fast}$ | 160 A/(°C·s) | $k_i^{slow}$ | 25 A/(°C·s) |

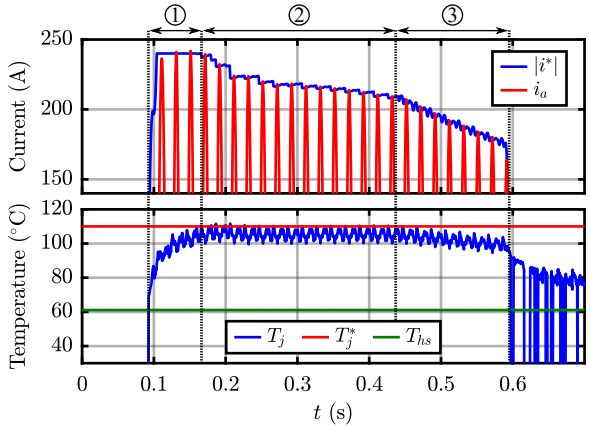


Fig. 12. S-VSC fault current injection during a 500 ms voltage dip. Top: phase $a$ current $i_a$ of the converter (red) and peak value of the reference current $|i^*|$ (blue). Bottom: maximum estimated junction temperature $T_j$, maximum set temperature $T_j^*$ (red) and heatsink temperature $T_{hs}$ (green).

heat up, as shown by the estimated temperature trend shown in the bottom part of Fig. 12. Then, in phase ②, as soon as the limit temperature is reached, the active temperature limitation strategy quickly reduces the maximum allowable output current $I_{max}$, maintaining the junction temperature below its setpoint. This limiting action is performed until the reference current generated by the S-VSC control falls below the thermal limit (phase ③). Here, the junction temperature is lower than its setpoint. Therefore, the current $i^* = i^*_{VSM}$ required by the S-VSC can be delivered without incurring into thermal limitations.

The contribution of the S-VSC is clearly observable in Fig. 13, showing the comparison between the reference current $i^*_{VSM}$ before saturation and the actual converter current reference $i^*$. As the S-VSC generates current references as a real SG, the reference current magnitude depends on the dip depth and the virtual stator inductance of the VSM. These references present an immediate peak (phase ①) and then decrease with an exponential trend during the rest of the dip, as the excitation control regulates the excitation flux linkage $\lambda_e$ of the S-VSC. If these reference are larger than the maximum allowed current $I_{max}$, they are limited (phases ① and ②). Otherwise, they are directly fed to the current regulator (phase ③).

At all times the thermal limitation is effective, as shown in Fig. 14. The temperature regulator is able to both limit the junction temperature, which does not overstep the given limit of 110°C, whilst guaranteeing the current sinusoidal shape of

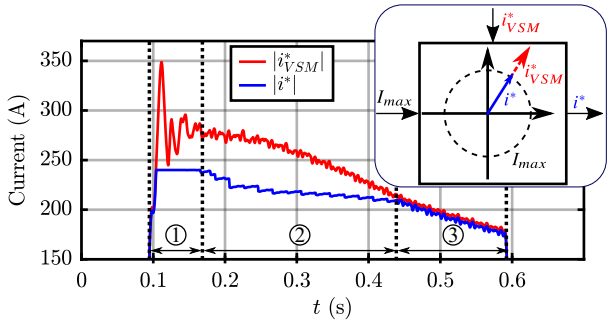


Fig. 13. S-VSC reference current $|i^*_{VSM}|$ (red) and saturated current reference $|i^*|$ (blue) after the limitation $I_{max}$ imposed by the temperature controller during a 500 ms voltage dip.

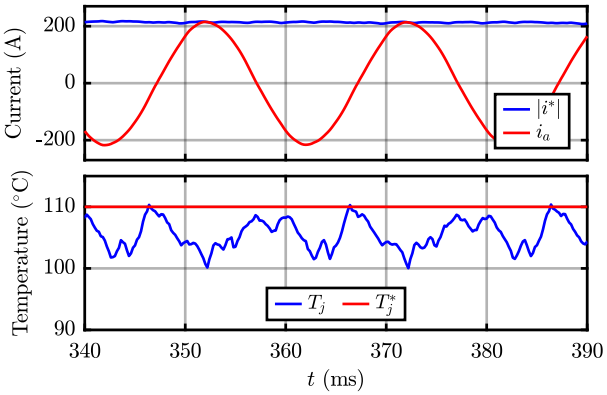


Fig. 14. Detail of the S-VSC fault current injection during a 500 ms voltage dip. Top: phase $a$ current $i_a$ of the converter (red) and peak value of the reference current $|i^*|$ (blue). Bottom: maximum estimated junction temperature $T_j$, maximum set temperature $T_j^*$ (red).

the current.

The importance of a proper tuning of the junction temperature controller is demonstrated experimentally in Fig. 15. In this test, two sets of tuning parameters for the junction temperature controller have been compared. Set 1 (blue) is a well tuned regulator, while set 2 features much larger gains than set 1. For both sets the temperature controller is still able to correctly limit the junction temperature below the setpoint. However, the effect of the improper tuning is evident on the grid currents shape, which is strongly deteriorated and features a larger harmonic content.

Finally, the benefits of the proposed control strategy can be noted by comparing it to a more standard converter able to operate up to its rated power without transient overload capabilities. The same voltage dip as the first test was applied and two conditions were compared:

- Standard converter with no overload capabilities: maximum inverter current 180 A = 1 pu (continuous inverter current capability) and no junction temperature control;
- Proposed converter with overload capabilities: maximum inverter current 240 A = 1.33 pu (grid emulator current limit) with junction temperature control active and setpoint 110°C.

The results are shown in Fig. 16 and it can be observed that the larger current capability of 240 A has two effects:

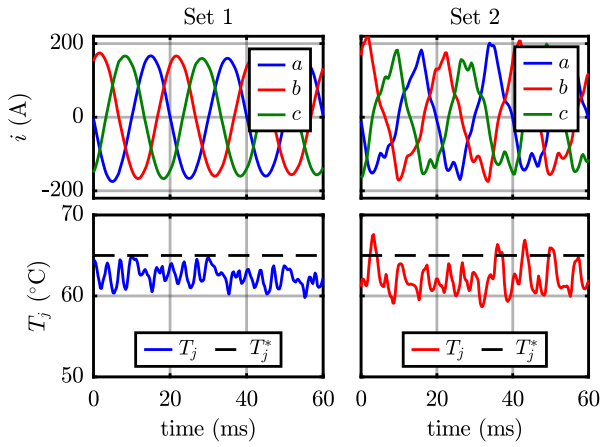


Fig. 15. Comparison of junction temperature controller tuning. Set 1, correct tuning and 2, non correct tuning, are compared. Top: converter phase currents. Bottom: maximum estimated junction temperature $T_j$ and maximum set temperature $T_j^*$.

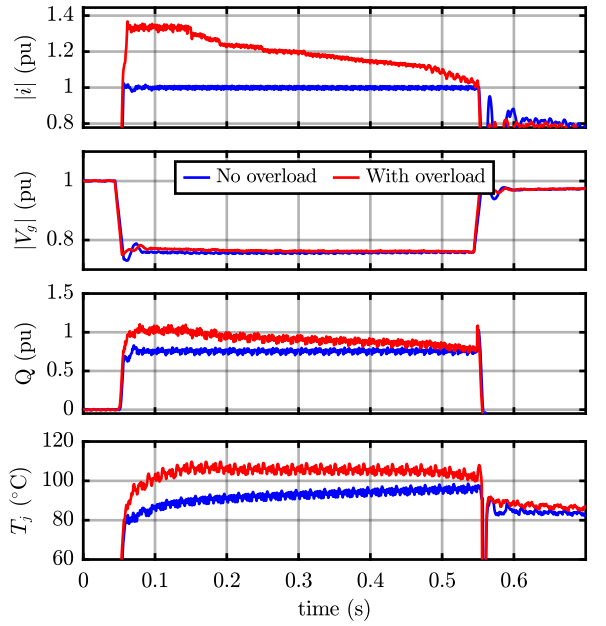


Fig. 16. Fault behavior with two different current limits (180 A and 240 A). First: peak current injected by the inverter. Second: Grid voltage peak. Third: reactive power injection. Fourth: junction temperature.

first, it contributes more to the short circuit current, therefore helping triggering the protection devices. Second, it provides more reactive power support to the grid, as it shown in Fig. 16. Moreover, the proposed temperature limitation can achieve a current overload of several tens of percent, while ensuring the reliability and safety of the converter, as the junction temperature of each device is monitored and limited in real-time. Therefore, the proposed solution is able to exploit the device thermal capacitances to enable the converter overload without overcoming the junction temperature setpoint.

## VII. Conclusion

Future power systems, featuring a large penetration of renewable energy sources, must be supported from the point of view of short circuit current provision by static converters. Therefore, this paper proposed for the first time a transiently overloadable VSM converter. The transient overloads required by the VSM strategy are achieved through better exploitation of the SOA of the semiconductors, so as to eliminate or reduce the need for oversizing of the power electronics.

In particular, the proposed junction temperature estimator, combined with the VSM concept enables to:

- Fully exploit the the thermal capacitance of the semiconductor die and package, to increase the short circuit capability of the VSM;
- Reduce the temperature safety margins commonly adopted in converter design based on thermo-electrical models, thanks to the accurate junction temperature estimation.

The proposed solution is even more advantageous when implemented on new generation power converters based on costly semiconductor technologies like SiC. Moreover, once the junction temperature is known to the control, advanced thermal management techniques can be implemented, thus increasing the lifetime of the converter and ensuring a virtually zero-failure operation.

The proposed solution has been validated experimentally by emulating a realistic symmetrical voltage dip. The tests show that the converter can inject a current larger than its rated value for a few hundred ms, therefore transiently supporting the grid. Thanks to the monitoring and limitation of the junction temperature, the converter is safely overloaded without any risk of failure. Moreover, the large thermal swings during the voltage dips do not impact significantly on the aging of the components, due the sporadic nature of the faults.

Future work will deal with asymmetrical voltages dips.

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