New Reliable Operation Infrastructure for Dynamic, High-dependability Applications

Thomas Lange

Due to the technology scaling, lower supply voltages and higher operating frequencies, modern electronic devices become more and more vulnerable to transient faults. At the same time the number of transistors in a single chip and the complexity of modern systems is increasing. This creates a challenge for performing a reliability assessment on today's circuits and requires many resources in terms of human efforts, processing power and cost. The thesis addresses some of these issues by advancing current analysis techniques on higher abstraction levels, especially focusing on a functional analysis.

In the first part, two new machine learning based approaches are presented to assist the functional failure analysis of complex circuits. The methodologies aim to reduce the efforts needed to determine the functional failure rate of the circuit's sequential logic. The machine learning models use a feature set which was developed to characterizes each sequential element in the circuit. The features combine attributes from static elements and dynamic elements.

The objective of the first approach is to accelerate a fine grained functional failure analysis. It reduces computational cost to determine the Functional De-Rating (FDR) factors of the circuit's sequential logic. The aim is to predict factors per individual instances, which is particularly difficult to obtain using classical approaches such as clustering, selective fault simulation or fault universe compaction techniques. The methodology was applied in a practical example where several machine learning models were evaluated, predicting different failure classes. It was shown that the cost of a fault injection campaign can be reduced by a factor of 2 up to 5 in comparison to a classical statistical fault injection campaign. Further, the ability of the method to be used in early design phases has been assessed. Therefore, a feature subset was identified which can be extracted from an elaborated Register-Transfer Level description of the design. The results have shown that the impact on the prediction performance was marginal.

The second machine learning based methodology uses clustering techniques to group flip-flops together which are expected to have a similar contribution to the overall functional failure rate. In this way the fault space is reduced which allows a more efficient fault injection strategy. The advantage in comparison to already other already existing clustering approaches is that this approach is more flexible and no assumption of the circuit or its representation is made. The effectiveness of the grouping by different machine learning clustering algorithms was evaluated on a practical example and compared to a random and ideal solution. With the approach it was possible to reduce fault injection efforts by a factor of 5× to 20×.

Typical design flows are hierarchical and rely on assembling many individual technology elements from standard cells to complete boards. Providers use compact models to provide simplified views of their products to their users. De-

signers group simpler elements in more complex structures and have to manage the corresponding propagation of reliability and functional safety information through the hierarchy of the system, accompanied by the obvious problems of IP confidentiality, the possibility of reverse engineering, etc. Therefore, in the second part of the thesis, a methodology is proposed which aims to help experts to deal with the complexity of hierarchical modelling of reliability and functional safety metrics. The presented approach allows the use, elaboration and distribution of compact machine learning models in a uniform and systematic manner, minimizing both human and CPU efforts while maintaining high accuracy and fidelity. The trained machine learning models will be able to quickly evaluate a large variety of effects, encapsulating very useful reliability and functional safety data in a compact and efficient solution that can be used and reused further down the design and manufacturing flow.

In the third part of the thesis, the focus is shifted to Single-Event Transients (SETs) in Clock Distribution Networks (CDNs). A methodology is proposed to analyse how SETs in the clock distribution network are impacting the functional behaviour of a circuit. A methodology and a fault model are presented which implement the main radiation-induced effects in clock networks. The method enables the computation of the functional failure rate in a logic-level simulation based on the RTL description of the design. Thus, a faster evaluation can be performed than by simulating on the electrical level or gate-level. The analysis is extended by introducing a Temporal Masking effect for SETs in clock distribution networks. The Temporal Masking is based on the shortest input path delay of the flip-flops and the shortest output path delay, which are defining an SET Timing Window within the clock cycle. SETs occurring outside of this window are masked. The fault model was extended considering this Temporal Masking effect which allows to compute the functional failure rate weighted with Timing De-Rating (TDR) of a circuit. The approach was applied in a practical example where SET were injected into the clock network of the circuit under test in a fault injection campaign. It was shown that the proposed Temporal Masking implementation is able to compute a pessimistic worst case.