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From 0.18µm to 28nm CMOS Down-scaling for Data Links in Body Dust Applications

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***Abstract*—In this work, we study the effect of transistor downscaling in a wireless communication circuit for Body Dust application. The system requires a chip lateral size smaller than 10 µm miming the typical size of a red blood cell and so, supporting free circulation in human tissues. Moreover, an ultra-low-power architecture is needed since the system is battery-less and wirelessly powered via acoustic power transfer. The aim of this paper is to present a data communication system for Body Dust systems, which works from the multiplexed sensor read-out front-end to the transmitter back-end taking account diagnostic information on different metabolite concentrations in human body. This work shows that scaling the architecture from a 0.18-µm to 28-nm CMOS processes, it is possible to improve both size and power consumption. The improvement is about 40 times in size (2000 µm^2 down to 50 µm^2) and two order of magnitude in average power consumption (10 µW to cents of nW).**

***Index Terms*—Body Dust; ULP CMOS design; Transistor downscaling; Active Biosensors; sub-10 µm CMOS Architectures; OOK modulation.**

I. Introduction

"Body Dust" research is a huge worldwide effort [1], [2] with the goal of developing new highly innovative solutions for precision medicine applications, obtaining a more efficient monitoring, for example in oncology. Among the wireless power transfer methods toward miniaturised implants [3], Body Dust system is ideated to be powered via UltraSounds (US). An external array of US transmitters are used to wirelessly supply drinkable and ingestible micro-active sensing-chip, which are able to communicate through backscattering [4]. The CMOS Body Dust cube is ideated to include: (i) a bio-sensing front-end with five nano-biosensors mounted on the top metal layer; (ii) a potentiostat; (iii) a current-to-frequency (I-to-f) converter to convert the sensed current from the front-end to a frequency-modulated signal; (iv) a multiplexed layer with sub-Hz oscillation to read in series the five nano-biosensors' outputs [5]; (v) a power management unit; and (vi) a communication circuit to modulate and transmit the diagnostic information to the external base station, as validated in [6], [7]. The challenging in the Body Dust system is the miniaturisation toward a sub-10- µm-size, being area consumption the first critical point of the system. The second big challenge remains the power consumption since rectifying the US incoming signal, only few µW are exploitable for the functioning of the entire system [8]. In this paper, we present a sub-10-µm-size CMOS transmitter able to communicate with the external environment exploiting the On-Off Keying (OOK) modulation through backscattering. This transmission approach has been used for Neural Dust sensing system [9]. In that case, the architecture was composed by three different nodes (an external and a sub-dural transmitter and the proper neural dusts) while in our system the external base station and the body dust tags are only expected. Moreover, in that architecture any communication circuit was implemented (the impedance modulation was made through a switching MOSFET only). To this end, we based our design following the event-driven digital architecture implemented in UMC 0.18 µm CMOS technology [10], that has shown very promising results [11]. In this regard, the study of transistor downscaling is an interesting aspect that has been largely investigated in the recent years [12]. Moreover, planar technologies, such as Fully Depleted Silicon On Insulator (FDSOI), provides improved speed, simplified manufacturing and reduced power compared to bulk silicon technologies. Therefore, in this paper we investigated the possibility to scale the nodes from the UMC 0.18 µm to the FD-SOI 28 nm CMOS technologies for data links in sub-10-µm-size Body Dust systems.

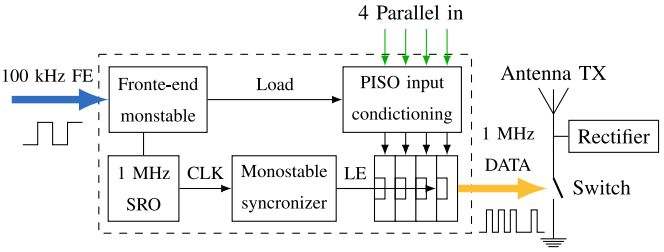


Fig. 1: System block diagram.

II. Proposed Architecture

The proposed communication circuit is constituted by: a 1 MHz Starved Ring Oscillator (SRO), a Front-End (FE) monostable, a monostable synchronizer, a four-inputs Parallel-Input Serial-Output (PISO) register and a modulator switch (Fig. 1).

The FE input signal comes from the sensor front-end layer, as in [2]. In particular, the biological signal is extracted by a potentiostat, followed by a I-to-f converter with a sensitivity of 7 kHz/nA [2]. For currents in the range of 1-5 nA and a sensor sensitivity of almost $1.8 \cdot 10^{-7} A/(mmol \cdot mm)$), the maximum frequency of the FE input pulse is almost 100 kHz. This quasi-digital signal will be used to trigger an event-driven wireless transmitter, as the impulse radio proposed in [13]. However, a unique 3-bit address is taken from the multiplexer of the Body Dust chip, used to distinguish among five different quasi-digital signals extracted by different sensor front-end. All the blocks will be now discussed as regard its implementation in UMC 0.18 µm CMOS technology.

A. The Starved Ring Oscillator

The function of the ring oscillator is to synchronize the shifting register in order to create a serial 1 MHz data. The oscillation frequency is approximated by (1):

$$f = \frac{I}{N \cdot C_{tot} \cdot V_{dd}} \tag{1}$$

in which I is the current flowing through the ring, N is the number of stages, C_{tot} is the total capacitance and V_{dd} is the supply voltage (e.g. 1.8 V). We designed a three-stages-starved-ring oscillator (Fig. 2). Capacitances and MOSFETs' size have been designed following the trade-off between the desired oscillation frequency of 1 MHz with the overall size of the component (in particular C=200 fF). As a matter of fact, the total capacitance can be decreased operating on the length of the transistors. As a result, the total area improvement is less than 10% at the cost of a reduced SRO performance reliability and an highly dependence on parasitics. Post-layout simulations also show a 1 % frequency variation among a temperature sweep from 27°C to 47°C (reasonable ranges for biomedical application). Table I compares the SRO performance with two frequency to voltage converters [14], [15].

B. The PISO register

We designed a 4-inputs PISO register through four D-latches, which are triggered by a Latch Enable (LE) signal driven by the monostable synchronizer (Fig. 3). With respect to a PISO made by Positive Edge Triggered (PET)-D Flip Flop, this configuration improves synchronization and area consumption. The parallel address is driven by a combinational circuit in which the LOAD signal, triggered by the front-end monostable, specify the writing or the shifting times. More in detail, when LOAD is "H", or "L", the word is respectively written, or shifted, in the latches. As a result, after four clock hits the serial address will be used to modulate the final switch. Minimum size transistors are used to save area, so that technology node downscaling is promising toward miniaturisation. As in [16], the transmitted packet is constituted by an header (bit 1 always) and three bits A_2, A_1, A_0 for the signal address.

TABLE I: SRO features comparison.

	[14]	[15]	This work
CMOS nodes	130nm	130nm	180nm
Voltage supply (V)	3.3	3.3	1.8
External component	Yes	No	No
Frequency (MHz)	22.5-360	1	1
Power (µW)	5000*	287.1	9.5
Area (mm^2)	0.05	0.054	0.00116

*At 200 MHz

C. The Front-end Monostable

The FE monostable is the only block that receives the FE signal. It works as a rising edge detector (using a D-latch as delay element) and its output is the LOAD signal which operates on the PISO register. LOAD signal needs to be large enough (almost 1 µs) in order to detect the possible variations of the parallel word coming from the multiplexer and to be sure that the clock can be seen into this interval. As a result, a LOAD pulse is triggered at each FE rising edge.

D. The Monostable Synchronizer

The Monostable Synchronizer is an inverter-based delay block sized accordingly to the number of components receiving the trigger (i.e. four latches for the PISO and one for the FE block). The output is almost a 1 ns pulse that needs to be over the transistors' activation threshold. The layout connection is made in order to be symmetrically centered with respect to all the triggered latches, so improving the synchronization [17].

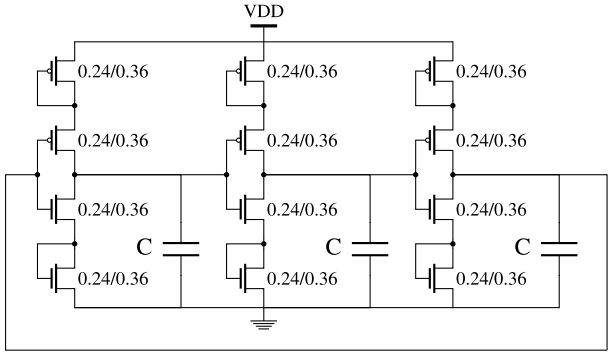


Fig. 2: Three stages Starved Ring Oscillator (SRO).

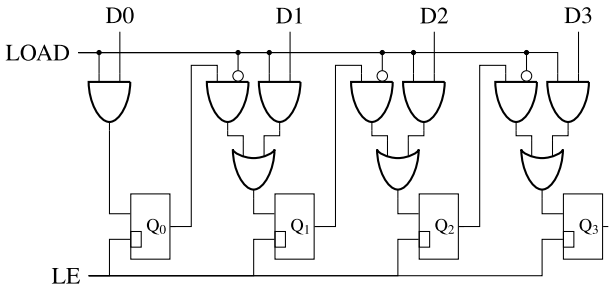


Fig. 3: Four inputs PISO register.

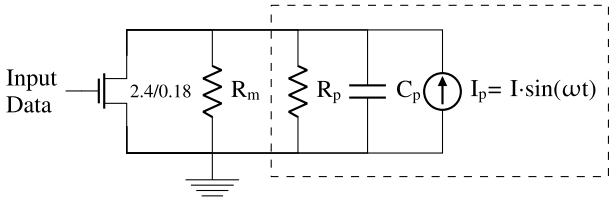
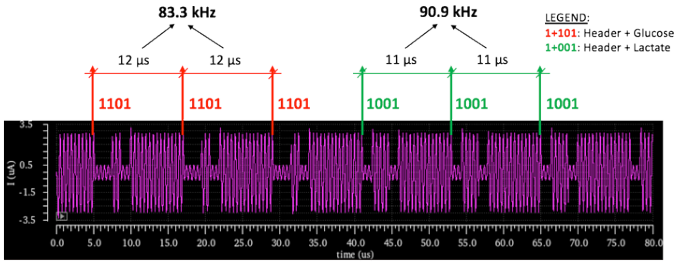


Fig. 4: Electrical model of the PZT receiver (dotted box), modulator R_m and NMOS-based switch.



Address	Signal	Measured Freq.	Current	Concentration
1+101	GLUCOSE	83.3 kHz	11.90 nA	0.066 mmol ∗ mm
1+001	LACTATE	90.9 kHz	12.99 nA	0.072 mmol ∗ mm

Fig. 5: Transient analysis to reconstruct different molecules concentration (i.e. glucose and lactate) using two different addresses (i.e. 1101 and 1001).

III. OOK Modulator

The final OOK modulation is made using an NMOS-based switch. Impedance modulation is performed controlling the drain current. Therefore, the transistor is sized accordingly to the transducer electrical equivalent impedance. The circuit is shown in Fig. 4, in which the resistance R_m of the modulator is exactly equal to the lumped resistance of the PZT receiver in order to implement the correct OOK modulation. Fully matched condition is achieved once the switch is open (R_m = R_p). On the other hand, when the switch is closed, the modulator is in parallel with a short circuit (R_m = 0), and the mismatched condition is achieved. In particular, $R_m = 3552\ \Omega$, $C_p = 62.75\ pF$ and $I = 10\ \mu A$ [6], [10].

IV. Results and Down-scaling

A full-circuit simulation is presented in Fig. 5. Two different addresses (i.e. 1101 and 1001) permit the reconstruction of two different molecules concentrations (i.e. glucose and lactate). In particular, the pink wave of Fig. 5 represents the received signal at the control station (losses due to tissue absorption and reflection are neglected). Therefore, the information could be reconstructed by measuring the frequency across the same signal-type.

A. UMC 0.18 µm CMOS Technology

The above described circuit has been implemented in UMC 0.18 µm CMOS technology. The total chip area is about 43x44 µm^2, exceeding the restrictive constrain of the Body Dust research. The majority of the area and more than 95% of the averaged power is consumed by the SRO. Post-layout simulations shows a total power consumption of 9.7 µW. The instantaneous power needed for the oscillation is 630 µW/pulse, while 810 µW/pulse are needed for the total transmission.

B. FD-SOI 28 nm CMOS Technology

Critical limitation of the cheaper UMC 0.18 µm CMOS technology are solved using a more expensive and relatively new CMOS technology like the FD-SOI 28 nm. Together with the transistor down-scaling, some circuital adjustments have been applied. In particular, high resistive pass transistor, exploited using the smallest transistor channels provided by 28 nm process, combined with the effect of the parasitic capacitances finally result in the SRO miniaturisation. More in detail, the dominant effect of the parasitic is located between the output of the i-stage of the SRO and the input of the (i+1)-stage. As a result, three parasitic capacitor replaces the ones of Fig. 2 needed in 0.18 µm process. Accordingly to (1), the transistors have been sized limiting the current flowing across the ring. The SRO finally consumes an averaged power of about 100 nW while the instantaneous power needed for the oscillation is less than 250 nW/pulse, almost three order of magnitude less than the same circuit implemented in UMC 0.18 µm [10]. Then, using Transmission Gates (TG) the number of transistors of the D-latch is further reduced (i.e. 22 down to 8 [18]). This configuration also improves noise performances of the circuit, in particular during post-layout simulations. Finally, the total size of the full circuit implemented in FD-SOI 28 nm is smaller than 50 µm^2, while the majority of the area, almost 65%, is still occupied by the SRO. The implemented architecture also answers to ULP constrain, being the average power consumption smaller than 200 nW and the instantaneous power consumption during the transmission smaller than 500 nW/pulse.

V. Conclusion

A novel sub-10-µm-size CMOS architecture for data transmission in Body Dust diagnostics has been presented. This study demonstrated the feasibility to design an UltraSound-based architecture for data transmission by using a 0.18-µm CMOS process. As a result, the average power consumption is less than 10 µW with a total chip area of 43x44 µm^2. Transistor downscaling have shown a final improvement of about 40 times in size (2000 µm^2 down to 50 µm^2) and almost two orders of magnitude in average power consumption: from 10 µW down to 200 nW. Future work will include corner analysis, fabrication and testing of the proposed system. At the very end, we have demonstrated that, opportunely scaling the nodes of the CMOS technology, it is truly feasible to design an ultra low power OOK modulation circuit for drinkable and sub-10 µm-size Body Dust systems.

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