Doctoral Dissertation
Doctoral Program in Computer and Control Engineering (33th cycle)

New Design Techniques for Dynamic Reconfigurable Architectures

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Summary

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Over the past decades, reconfigurable computing had increasingly gained attention for the high integration, performances, and in-field upgradability it can provide to a computing system. In fact, its main novelty consists of offering on a single platform the benefits of hardware customization coupled with the flexibility typical of software programming.

This has driven the effort in proposing and developing several reconfigurable architectures to efficiently tailor various and increasingly complex applications. Such trend led to the state-of-the-art architecture, consisting of a heterogeneous processing system including on-chip processors coupled with dynamically reconfigurable fabric to implement custom and run-time upgradable cores.

Today, the commercial technology to implement the reconfigurable fabric is represented by the SRAM-based Field Programmable Gate Array (FPGA) and consists of one layer of programmable resources and one layer of configuration, an SRAM memory holding the configuration data defining the behavior of the resource layer. These devices enable to access and modify specific portions of the memory content from the resource layer without stopping the application execution to adapt its functionality to requirements varying over time, to maximize its performance, and to increase its dependability.

This feature, called Dynamic Partial Reconfiguration, has been one of the leading characteristics that drove the rapid growth of this computational paradigm and increasingly widened the deployment of SRAM-based FPGAs in many computational-intensive and high-reliability applications, such as networking, High-Performance Computing, and satellite or high energy physics experiments fault-tolerant electronics.

However, the current SRAM-based FPGA architecture embeds some functionalities that demand to be addressed to fully express the promises of the reconfigurable computing paradigm and that provide opportunities for enhancing reconfigurable systems performance and dependability.
The performance optimizations are related to the relatively long time required to perform run-time reconfiguration in commercial devices that, if not properly managed, can jeopardize gain achieved through to the in-field upgradability.
SRAM-based FPGAs' dependability instead becomes crucial when they operate in presence of radiation, as in aerospace and high energy physics experiments, due to their configuration memory sensitivity to radiation-induced errors that must be considered and characterized according to the mission environment before deployment to avoid failures.
In this view, the doctoral research presented in this dissertation addresses dynamically and partially reconfigurable architectures' performance through novel techniques for the enhancement of the reconfiguration procedure, and self-reconfigurable systems dependability through the analysis of their radiation sensitivity to radiation-induced effects.
Therefore, the main opportunities and challenges embedded in reconfigurable architectures are firstly introduced and followed by an overview of the state-of-the-art architectural solutions and applications for high-performance and high-reliability reconfigurable platforms.
The main contributions to the optimization of the reconfiguration procedure performances are provided in the ***Part 1*** of the dissertation.
In detail, the Frame-driven Routing Algorithm (FeDRA) is presented as a novel and generalized approach to optimize within the development process the amount of configuration memory data involved in the reconfiguration of circuits deployed on commercial SRAM-based FPGAs. The proposed approach enables to achieve a consistent reduction of the reconfiguration overhead when compared to solutions obtained with the standard process.
Subsequently, the Reconfigurable Multipotent (ReM) cell, developed as the basic reconfigurable unit for novel architectural solutions oriented to the fast and detailed in-field reconfiguration, is presented. In detail, the proposed reconfigurable cell enables bit-level reconfiguration within a single clock cycle while minimizing the amount of data involved in the procedure thanks to the key feature of reconfiguring itself and the contiguous units.
The ***Part 2*** of the dissertation instead presents the main contributions to reconfigurable FPGAs dependability that consist of radiation sensitivity analyses centered on the self-reconfiguration controller, which represent the key component enabling in-field reconfiguration.
In detail, a soft-error analysis on different implementations of the self-reconfiguration controller managing the configuration memory access in dynamically and partially reconfigurable applications is presented. This analysis, which has been performed by miming different radiation profiles through detailed fault-injections, allowed to obtain indications about the controllers' dependability and applicability in different radiation environments according to their operational goals.
Accordingly, a self-monitoring setup based on the most suitable self-reconfiguration controller and instrumented for the online and automated radiation analysis of SRAM configuration memory sensitivity is presented. The proposed setup enabled the usage of a Neutron Generator as a radiation source and strongly reduces the time and the cost required by typical radiation testing facilities and approaches.