Ultra-Low Power Discrete-Time Readout for CMOS Radiation Sensors

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S. Durando
Politecnico di Torino and INFN, on behalf of the ARCADIA collaboration

***Abstract*—This paper presents the design of a discrete time front-end electronics for CMOS radiation sensors with a power consumption of 11 nW/pixel. The architecture is inspired by the DRAM sensing techniques and it is suitable for small pixel readout. The design is implemented in a 110 nm CMOS technology and consists of a discrete time binary front-end composed by a source follower input stage, an inverting discriminator with offset compensation and a digital buffer.**
The work is carried out in the framework of the ARCADIA collaboration, which aims to develop fully-depleted monolithic CMOS sensor with low noise, fast charge collection and low power readout, compatible with standard fabrication processes.
The first prototype of the discrete-time front-end is implemented in a 2x2 mm^2 matrix composed by 4 sectors of 6 columns of 24 50 μm pitch pixels.
Simulations show a power density below 1 mW/cm^2 for a frame rate of 10 KHz. The circuit performance have been simulated with systematic and random process variation Monte Carlo simulations.

***Index Terms*—CMOS radiation sensors, Low power electronics, CMOS technology, Space experiments, Silicon trackers, DRAMs.**

I. Introduction

MONOLITHIC CMOS pixels integrate in the same substrate both the sensor and the electronic readout.
Since the prototypes, huge steps forward in High Energy physics applications have been made. Developments in the last decades have increased their radiation tolerance and have made it possible to meet most of the requirements in the fields.
The ARCADIA collaboration is developing a new CMOS sensor, with full depletion, high signal to-noise-ratio, fast charge collection by drift, high radiation tolerance and ultra-low power capability [1]–[3]. Fig.1 shows the sensor concept [4].

Hybrid silicon sensors are the most widespread solution in silicon trackers. Concerning space satellites experiments, silicon microstrip detectors have been the preferred choice so far. The main advantage is the low power density, which is due to the low number of channels and to the small contribution of the sensor. Strip detectors have also reached high spatial resolution when combining two layers, varying from 3 μm [5] to 10s of μm [6].
However, silicon microstrips detectors show some disadvantages. Sensor production requires dedicated fabrication processes. This increases the costs and restricts the number of foundries. In addition, microstrip sensors require ASICs coupled to the sensors, increasing the costs, the material budget, and decreasing the signal to noise ratio. Moreover, two dimensional position reconstruction is affected by ghost hits ad fake hits, which has an impact on the reconstruction and data analyses.

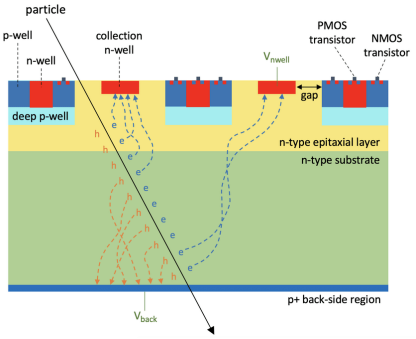

Fig. 1. ARCADIA sensor concept, [4]. The full depletion allows for collecting the charge mainly by drift instead of diffusion. Deep p-well inplants shield the electronics from the sensor.

Monolithic pixel sensors solve most of these problems. They use standard fabrication processes, and have the front-end electronics directly integrated on pixel. Therefore, they decrease the production costs and the material budget, and also simplify the assembly. Furthermore, pixellated systems avoid the ambiguities generated by the strips geometry.
ALPIDE [9] is the state of the art for advanced MAPS. Its last design will be installed in the ALICE ITS2, at CERN, and it is implementing in the silicon tracker of the new HEPD-02, a payload of the second China Seismo-Electromagnetic Satellite CSES-02 [10], becoming the first MAPS to be used in space experiments. Still, it is far from having the power consumption density achieved by microstrips detectors in space silicon trackers, which is below 1 $\frac{mW}{cm^2}$ [7]. A CMOS sensor with power consumption competitive to microstrips detectors has never been designed before.
Power consumption density has two major contributors. One is the digital circuitry, which can be made rate dependent. The other is the analog power consumption. It plays a crucial role, and it depends on the specific front-end architecture, it is a function of the charge collected and the sensor capacitance: P = (C/Q)^m, (m = 2÷4) [8], [11].
In this work, an ultra low-power discrete-time in-pixel analog front-end designed for fully depleted CMOS sensors is proposed. The goal is to reach the same power density offered by systems based on microstrip detectors.

II. The Front-End Circuit

In the past few years, continuous time systems have been the preferred choice in HEP front-end electronics. Deep-submicron technology nodes reduce however the charge injection which affects switched capacitor techniques, and lead to consider again discrete-time analog front-ends.
The design is inspired by the DRAM readout methods, which show some analogies to the front-end specifications in tracking applications. Indeed, these multi-cells systems have to fit small area in order to have high memory density. Each memory cell is made of a capacitor of tens of fF which is comparable to CMOS sensor capacitance, and a transistor that works as a switch. Signals of tens of mV are discriminated when the cell is read. The readout occurs with compact discriminators composed of CMOS inverters which are used as positive feedback amplifiers [13]. These stages use switched capacitor techniques to auto compensate the offset induced by the mismatch variations at the input node, and can be interesting in multichannels systems such as high density matrix with the front-end electronics implemented on pixel.

The present architecture (fig.2) has been implemented in a 110 nm technology with a 1.2 V power supply.
The first stage of the proposed front-end is a dynamic source follower that works as an analog buffer when it is enabled. A coupling capacitor connects the first stage to the discriminator, which is a positive feedback amplifier. The latter is composed by a CMOS inverter with a second CMOS inverter in a feedback loop. The coupling capacitor has a capacitance of 10 fF and it is used to compensate the offset of the discriminator.
The circuit is shown in figure 2. The principle of operation is as follows:

- The input node is charged to V_{ref2}. Then, the offset compensation sets in_disc to V_{thr_inv}.
- The switches are opened. If a particle hits the sensor, the collected charge can be stored on the input node capacitor.
- After a time T, which is defined by the readout frequency, the input node is set to V_{ref1} in order to introduce a threshold Δv_{thr}.
- The first stage is switched on, then the first inverter, and finally the feedback loop is closed and the out node voltage reaches the supply.

The offset compensation is carried out by shorting the output and the input of the first inverter. Therefore, the offset dc voltage is stored on capacitor C_{oc} and the input of the inverter is set to Vdd/2. As a consequence, both transistors in the inverter work in saturation, and the stage is set to its maximum gain. The drawback to this is the introduction of a static power consumption. Therefore, switching off the inverter is necessary to reduce the power consumption and to store the inverter node voltage at the trip point for the next discrimination.
The main feature of this design is the use of the switched technique to store the signal charge on the pixel capacitor and to turn on the front-end just to readout the pixel. Thence, the power consumption is defined mainly by the time required by the pixel to be read and set for the new acquisition, and secondly by the leakages and the off-currents while it is turned off. In silicon trackers for space applications, the event rate is low, then, the ratio between the on and off time can be set very small, reducing the power consumption.

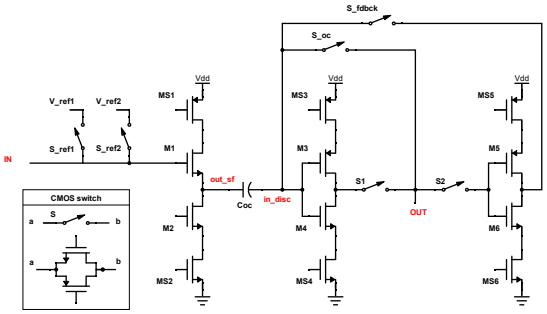

Fig. 2. Front-end circuit scheme.

III. Simulation Results

To simulate the circuit behavior, a sensor model composed by an ideal current generator in parallel with a detector capacitance has been used. The capacitance has been estimated to be 5 fF for the 50x50 μm^2 pixels of the test prototype.
Transient analyses have been carried out to verify the readout procedure of the front-end. The circuit performance have been evaluated at several readout frequencies. A minimum readout frequency of 1 KHz should be applied in order to prevent a significant leakage of the charge stored in the high impedance nodes
Different Monte Carlo simulations have been carried out to evaluate the behavior of the circuit with random and systematic process variations.
The yield of the circuit for minimum charge discrimination (0.4 fC) is greater than 99.9 $\%$ in both random and systematic Monte Carlo simulations.
Noise analyses together with Monte Carlo simulations have been used to define the minimum threshold to avoid fake hits rate which has been estimated to be lower than 0.01 $\%$.
The average power consumption of the circuit depends on the readout frequency and it has been computed in transient analysis. At 10 kHz the single channel average power consumption is 11.2 nW, and it decreases to 7 nW at 5 kHz. In table I is reported the power consumption estimated in simulations as a function of the readout frequency. The power density is estimated in the case of the prototype pixel size (50 μm).

TABLE I
Power consumption depends on the readout frequency.

f [kHz]	5	7.5	10
P [$\frac{mW}{cm^2}$]	0.28	0.39	0.47
P [$\frac{nW}{Pixel}$]	7.0	9.69	11.2

IV. Layout and Test Prototype Architecture

The layout of the analog front-end fits a small area ($\simeq$ 10x10μm^2) which is mainly occupied by the metal-insulator-metal capacitor used for the offset compensation. The circuit is compact, and allows for small pixel size.
A first test prototype has been produced, it is a 2 x 2 mm^2 matrix of 4 sectors of 6 columns with 24 pixels each. The padframe consists of 60 pads to control the digital readout and the front-end's analog signals and for different testing purposes (fig. 3). The pixel size is 50 x 50 μm^2.
The matrix implements a rolling shutter readout. Each pixel of the same sector is eventually read, column by column, through a shift register, and the outputs are sequentially fed to the same output line.
The matrix has been manufactured and delivered by the foundry and test results are expected within the next year.

The present architecture can be useful when the requirements are a high spatial resolution and very low power consumption. The former can be reached by using a small pixel size allowed by the compactness of the front-end. The latter depends on the event rate requirement. In order to avoid pile up, it is possible to define the maximum event rate by considering the Poisson distribution of the probability of having *n* events in a process that has a certain mean number of events. Fixing the probability to have *n* equal to zero to 99.9 %, considering a readout frequency of 10 kHz the resulting maximum rate is 10 Hz per pixel. With a pixel pitch of 50 μm, the rate is 400 kHz/cm^2.

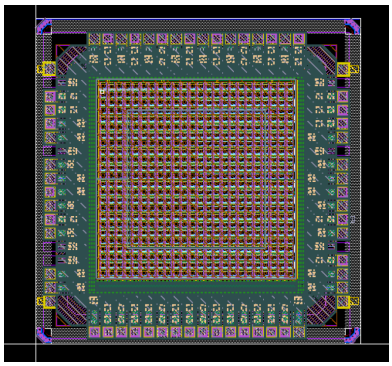

Fig. 3. First prototype, full matrix layout.

V. Conclusions

A binary front-end CMOS sensor has been designed in 1.2 V, 110 nm technology . The circuit will be tested within the next year with a first prototype of 2x2 mm^2 matrix.
The circuit is inspired by DRAM sensing techniques and it works in discrete time. Its power consumption decreases with the readout frequency, which makes the front-end optimized for low event rate requirement, $\leq$ 1 MHz/cm^2 with the prototype pixel size.
The simulations show a power consumption of 11.2 nW/pixel at a readout frequency of 10 kHz. A pixel pitch of 50 μm lead to a power density of 0.47 mW/cm^2 which is comparable to the ones offered by microstrip detectors.
Adopting CMOS pixel sensors reduces the material budget, suppresses fake hits rate and reduces the system integration complexity. Future prototypes with smaller pixel size allowed by the compact design will lead to better spatial resolution ($\simeq \mu$m) with a low power density ($\leq$1 mW/cm^2), and could be a promising alternative to silicon microstrip detectors in several applications.

References

[1] P. Pancheri et al, "Fully Depleted MAPS in 110-nm CMOS Process With 100–300-m Active Substrate" in IEEE Transactions on Electron Devices, vol. 67, 2020.
[2] C. Neubüser et al, "Sensor Design Optimization of Innovative Low-Power, Large Area FD-MAPS for HEP and Applied Science" in Frontiers in Physics, vol. 9, 2021.
[3] M.Rolo,"ARCADIA, project proposal" Italia, Torino, INFN, 2018.
[4] L. De Cilladi et al, "Fully Depleted Monolithic Active Microstrip Sensors: TCAD Simulation Study of an Innovative Design Concept" in Sensors, vol. 21, 2021.
[5] M. Pearce "The status of the PAMELA experiment" in Nuclear Physics. B, Proceedings Supplements, Netherlands, vol. 113, 2002.
[6] A. Tykhonov et al, "Internal alignment and position resolution of the silicon tracker of DAMPE determined with orbit data" in Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, vol. 113, 2018.
[7] W.B Atwood "Gamma Large Area Silicon Telescope (GLAST) applying silicon strip detector technology to the detection of gamma rays in space" in Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, vol. 342, 1994.
[8] N. Wermes "Depleted CMOS pixels for LHC proton–proton experiments" in Nucl. Instrum. Meth., vol. A824, 2016.
[9] M. Mager, "ALPIDE, the Monolithic Active Pixel Sensor for the ALICE ITS upgrade" in Nucl. Instrum. Meth., vol. 824, 2016.
[10] C. De Santis, S. Ricciardini, "The High Energy Particle Detector (HEPD-02) for the second China Seismo-Electromagnetic Satellite (CSES-02)" in PoS, vol. ICRC2021, 2021.
[11] W. Snoeys "CMOS monolithic active pixel sensors for high energy physics" in Nucl. Instrum. Meth., vol. 765, 2014.
[12] W. B. Atwood et al, "The Large Area Telescope on The Fermi Gamma-Ray Space Telescope Mission" in *The Astrophysical Journal*.
[13] C.Villa, "Semiconductor memories: circuitry design management of challenges" in *Presentation, Micron technology*, Milan, May, 2019.