A 12-bit 100 MHz SAR ADC in 110-nm CMOS for MAPSs

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***Abstract*—This paper presents a fully differential 12-bit SAR ADC developed for high-voltage CMOS sensors. The converter has been designed in compliance with low power consumption, high resolution and low material budget requirements.**

A merged capacitor switching method is employed to decrease power consumption and the capacitor array has been split up into two sub-DACs in order to reduce the area. The prototype has been implemented in a 110-nm CMOS technology. With a power supply of 1.2 V and a 100 MHz clock, simulations show an ENOB 9.87 of and a SFDR of 73.42 dB. The power consumption of the ADC is 513 μW while the Figure of Merit (FOM) results 54.8 fJ/conv-step. The final chip includes also a calibration engine to minimize the capacitor mismatch effect thus further improving the resolution.

***Index Terms*—SAR ADC, split capacitor, low power**

I. Introduction

Monolithic active pixel sensors (MAPSs) are becoming more and more popular in High Energy Physics (HEP) experiments due to their higher performance compared to hybrid pixels. This technology provides reduced pixel pitch, low power consumption and smaller area. Therefore, MAPSs can be of interest also in other fields such as X-ray imaging, medical physics and space instrumentation. The use of high voltage bias allows to deplete the substrate and collect the charge by drift, improving device speed and radiation tolerance. In the technology adopted for this work, a back-bias voltage of about 200 V allows to obtain an active substrate up to 300 μm [1].

In some applications, it can be of interest to measure the collected charge with high resolution. In this case, the analog information is stored in a capacitor in the pixel and then transferred to the periphery, where it is digitized by column-parallel ADCs. A SAR ADC can provide in this case an optimal compromise between conversion speed, power consumption and area.

In this paper, a power efficient, high radiation tolerant and high resolution converter with a target resolution of 12 bit is presented. This makes the ADC also suitable as a monitoring ADC to measure the on-chip parameters that need to be tracked, such as bias voltages or temperature.

One of the most important source of power consumption in a SAR ADC is the switching operation in the capacitor array. Considering that the single-ended architecture based on the charge redistribution technique has not a power efficient switching algorithm, a fully differential topology with merged capacitor switching method has been selected.

A first prototype has been developed in a 110 nm CMOS technology. The final layout of the ADC has a size of $(371.7 \times 229.3)\mu m^2$. In simulations, the converter shows a 8.3 MS/s operation speed with 12-bit resolution. However, it can achieve up to 40 MS/s with a resolution of 10 bits, which is an adequate value for most applications. Simulations with 1.2 V supply and 100 MHz clock frequency show an Effective Number Of Bits (ENOB) of 9.87 and a Spurious Free Dynamic Range (SFDR) of 73.42 dB before calibration. Moreover, the power consumption of the ADC results equal to 513 μW which corresponds to a 54.8 fJ/conv-step FoM. A calibration engine has been embedded on chip. Thanks to its features, this device can be suitable to be embedded in readout circuits. Furthermore, if a higher sampling rate is needed, these converters can be organized into a time interleaved configuration thus increasing the operational speed.

The paper is organized as follows. Section II describes the architecture of the ADC. Section III shows the guidelines for the physical implementation. The simulation results are shown in Section IV while first experimental results are depicted in Section V. Finally, Section VI draws the conclusions.

II. ADC Architecture

The classical topology adopted for SAR ADC is the charge redistribution technique [2]- [3]. However, the performance of the converter can be affected by external noise due to the single ended architecture. Moreover, the switching algorithm is not power efficient. Therefore, a fully differential architecture has been chosen. In this case, the difference between the two inputs is digitized making the circuit robust to noise. As a matter of fact, common disturbances on both lines are rejected.

The merged capacitor switching method has been selected [4]. During the sampling phase, the input signal is sent to the top plates of the DAC while the bottom plates are connected to the common mode voltage, V_{cm}. For the evaluation of the Most Significant Bit (MSB), the difference between the two inputs is checked without switching any capacitor. If the result is positive, the bit is set to 1 by switching the bottom plate of the largest capacitor in the top array from V_{cm} to the reference voltage, V_{ref}. At the same time, the largest capacitor in the

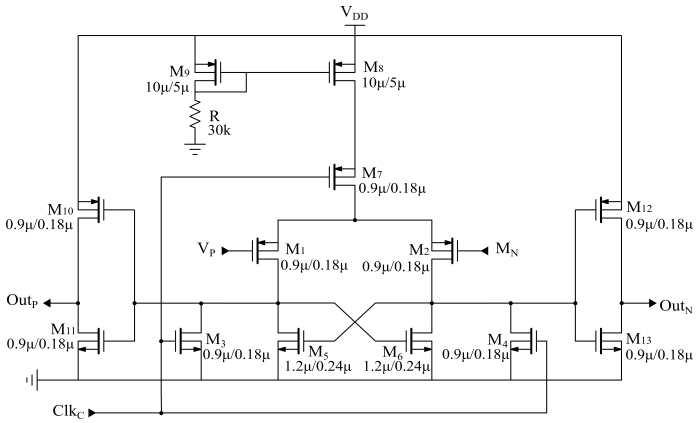

Fig. 1. Dynamic latched comparator schematic.

bottom array is switched to GND. In this way, a voltage equal to $V_{ref}/4$ is subtracted to V_+ and added to V_-. On the other hand, if the difference between the two inputs is negative, the MSB is set to 0 and the opposite operation is performed. The same procedure is carried out to determine the other bits.

A further advantage of this architecture is that the common mode voltage at the input of the comparator is constant in contrast to the step-down switching method presented in [5]. This allows to not affect the behaviour of the comparator.

The main building blocks of the converter are a dynamic latched comparator, a binary weighted Digital-to-Analog Converter (DAC) and a control logic. Moreover, an offset injection circuit, which is useful for the calibration engine, has been embedded. These blocks will be described in the next sections.

A. Comparator architecture

Fig. 1 shows the schematic of the dynamic latched comparator which employs a positive feedback to generate two digital levels [5]. The load consists into a latched stage composed by transistors M5 and M6 in the figure. Moreover, two inverters are embedded in the output stage in order to further speed up the regeneration of the amplifier output into a full swing digital CMOS signal.

Two NMOS switches (M3 and M4 in the figure) are connected in parallel with the load to disable the positive feedback. Furthermore, a PMOS switch (called M7) is connected in series to the output branch of the current mirror in order to avoid static power consumption when the comparator is in the reset phase. For this reason, power is consumed only in the transition between the two logic levels thus making the design suitable for low-power applications.

During the reset phase, the path between the two power rails is disconnected and both the inputs are held to V_{DD}. On the other hand, by enabling the differential pair, the input transistors start working. If V_p is greater than V_n, V_{outp} is driven to 0 faster than V_{outn}, so the positive feedback pulls V_{outp} up and V_{outn} down.

B. DAC architecture

The schematic of the proposed ADC is shown in Fig. 2.

In the SAR ADC, a binary weighted DAC is employed both as a sample and hold block and to provide fraction of the reference voltage. In the layout, most of the area is taken by the DAC. As a matter of fact, every bit of resolution added doubles the DAC occupied area. Moreover, this causes the increase of the load at the input of the comparator. For these reasons, the capacitor array has been split up into two sub-DACs connected by using a coupling capacitor [6]- [7].

The value of the coupling capacitor is such that the capacitance which is seen by the main-DAC is equal to the unit capacitance C_{min}.

In the converter, the bits have been split up into a main-DAC of 9 bits and a sub-DAC of 3 bits. Since $C_{min} = 2fF$, the total capacitance C_{TOT} for the segmented DAC is equal to 1040 fF. On the other hand, for a classical DAC having the same minimum capacitance, C_{TOT} results equal to 8192 fF.

In order to reduce the mismatch, in the sub-DAC the value of the minimum capacitance has been doubled (4 fF). Therefore, the total capacitance has a slight increase going from 1040 fF to 1056 fF. Nevertheless, the segmentation offers the best choice.

C. SAR control logic

The SAR ADC needs a control logic for storing the value of the bits after the conversion result. This circuit is composed of a shift register and D-type flip-flops in which the bits are memorized [5].

Two control signals called *sample* and *convert* are used to manage the SAR logic operation. When both of them are high, the sampling phase is enabled, so the shift register and the flip-flops are in the reset state. When the conversion phase starts ($sample = 0$ and $convert = 1$), a logic "1" is shifted through the register at every clock cycle. The outputs of the shift register are used to sequentially pick out the flip-flops in which the comparison results would be stored. Hence, the value of the bit is stored in the selected flip-flop. The last output of the shift register is the *End of Conversion* (EoC) signal which is used to points out the end of the conversion.

D. Offset injection circuit

Due to the high resolution required, a perturbation-based digital calibration algorithm is embedded to correct non-linearities of the converter. The Offset Double Conversion (ODC) technique has been chosen [8].

In the ODC technique, each analog sample which has been digitized has to be converted also injecting two analog offsets ($+\Delta_a$ and $-\Delta_a$). These offsets have the same absolute value but opposite sign. Hence, two raw codes, D_+ and D_-, are provided to the digital calibration. The offsets can be removed from the output codes and, in case of an ideal converter, the results should be equal to the digitization of the analog sample to which no offset has been added. In case of mismatches, the calibration engine evaluates the error and corrects the bit weights.

Therefore, an offset injection circuit has been embedded. It is composed of the capacitance C_{cal} which can be connected

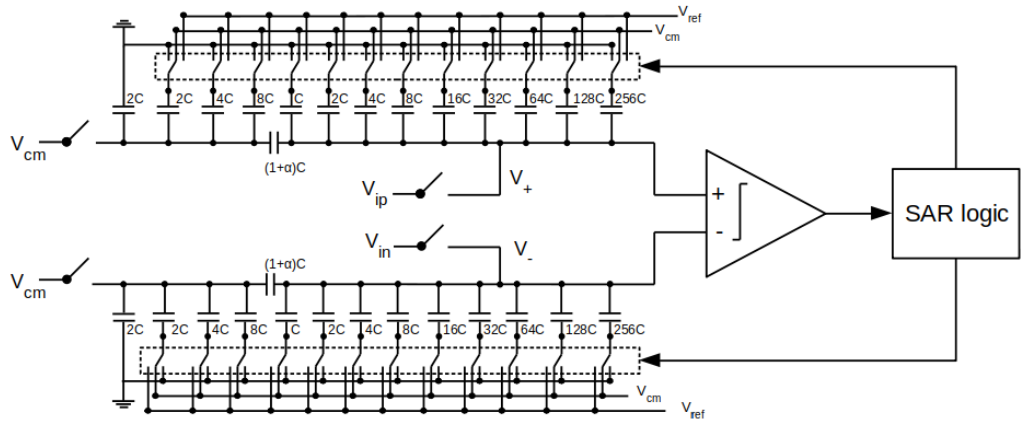

Fig. 2. Proposed SAR ADC with segmented capacitor array.

to the top plate of the main-DAC through a switch . The other plate of the capacitor can be connected to V_{cm}, V_{ref} or ground. The same circuit is embedded both in the top and in the bottom array.

During the sampling phase, no offset is injected, so the calibration capacitance is connected between V_{cm} and the input voltage. Hence, the input signal is sampled and converted without any added offset.

Then, without carrying out a new sampling, a positive offset is injected by connecting the calibration capacitance of the top array to V_{ref} while the one in the bottom array to GND. Thus, the new value equal to $V_{in} + \Delta_a$ is digitized.

Eventually, the opposite operation is performed for injecting a negative offset. As a result, $V_{in} - \Delta_a$ is converted.

The value of the calibration capacitance has been chosen equal to 10 fF in order to inject a voltage corresponding to 40 LSB. Since $V_{ref} = 1\,V$ and $V_{cm} = 0.5\,mV$, the injection is $\sim 9.6\,mV$ on each array that corresponds to $\sim 19.2\,mV$ peak-to-peak.

III. Physical implementation

Since crossing particles can degrade the circuit operations, the layout design had to be carried out considering the radiation tolerance of the device. As a matter of fact, transients in the substrate can lead to latch-up. In order to prevent latch-up, a high number of substrate contacts has been added thus reducing its resistance. Moreover, guardrings have been placed around the blocks.

The supplies for the analog blocks and for the digital ones are kept separated in order to protect the analog circuits from digital noise. Furthermore, a dedicated power supply bus has been embedded for the comparator which is both sensitive and noisy. Hence, a total of three power supply busses are present.

In the DAC, a proper number of unit capacitors connected in parallel are used instead of employing a single capacitor for every bit in order to obtain different capacitance values.

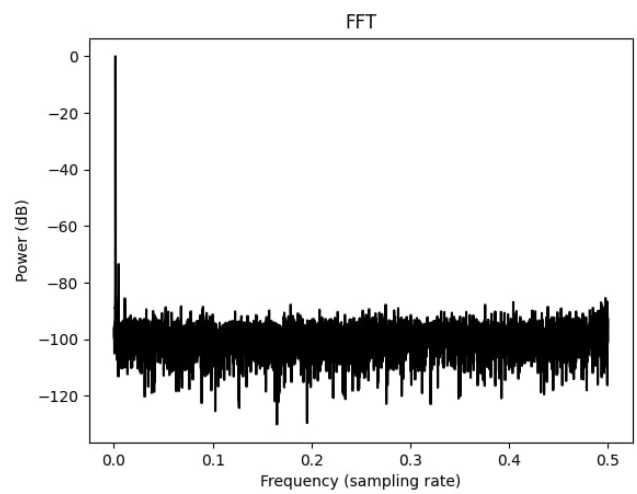

Fig. 3. FFT at 100 MHz clock with input sinusoid of 15.6 kHz.

This allows to improve the capacitor matching and reduce the non-linearities.

The total area occupied by the ADC is $(371.7 \times 229.3)\mu m^2$. The final chip has a size of $(3 \times 1.5)mm^2$ with a core of $(2.4 \times 0.9)mm^2$ and includes both the converter and the calibration engine.

IV. Simulation results

For the simulations, a 1.2V power supply has been used. The converter has been simulated without including the digital calibration circuit. The input sinusoid had a frequency of 15.9 kHz and an amplitude equal to the reference voltage (1V). The clock frequency was equal to 100 MHz and the sampling was 8.3 MS/s. A number of 8192 samples has been taken and the Fast Fourier Transform (FFT) is reported in Fig. 3.

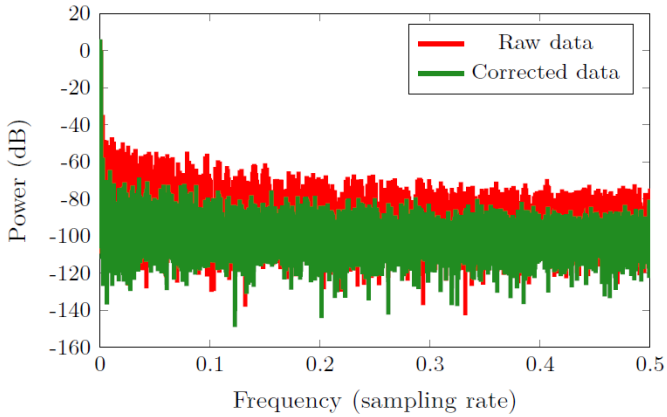

Fig. 4. FFT of a 3.015 kHz sinusoid before (red) and after the calibration (green).

From the FFT, the main parameters to evaluate the dynamic performance of the ADC can be calculated. The Signal to Noise and Distortion (SINAD) is evaluated as follows:

$$SINAD = 20\log\sqrt{\frac{A_f^2}{\sum_{k=0}^{f-1} A_k^2 + \sum_{k=f+1}^{N/2} A_k^2}} \quad (1)$$

From the SINAD, the ENOB can be calculated:

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (2)$$

For the presented ADC, the SINAD results equal to 61.16 dB and the ENOB is 9.87. The SFDR is calculated as:

$$SFDR = 20\log\sqrt{\frac{A_f^2}{A_{spurious}^2}} \quad (3)$$

From the simulation results that SFDR = 73.42 dB. The power consumption of the converter is 513 μW. Hence, the FOM of the ADC can be evaluate as:

$$FOM = \frac{P}{f_s \times 2^{ENOB}} \quad (4)$$

where P is the power consumption and f_s the sampling frequency. The FOM of this converter corresponds to 54.8 fJ/conv-step.

V. First experimental results

The ADC has been tested by using a 3.015 kHz sinusoidal waveform as input signal and a 100 MHz clock frequency corresponding to a 8.3 MS/s. The FFT has been evaluated by collecting 2^{15} samples. The plot is shown in Fig. 4.

The raw data coming from the ADC shows a high amount of missing codes. These errors can be well reproduced by assuming a significant mismatch among the unit capacitors. For the chosen capacitors, Monte-Carlo models were not available at the time of the design and the statistical mismatch could not be properly accounted for. However, a mean of 3 bits can be retrieved thanks to the calibration engine. Hence, a ENOB of 8.5 bits, which is equivalent to a 9 bit ADC, is achieved.

VI. Conclusion

In this paper, a 12-bit fully differential SAR ADC was presented. The prototype has been implemented by using 110 nm CMOS technology. The design has been optimized by employing the merged capacitor switching method, which is a power efficient switching procedure in order to reduce power consumption. Moreover, the total area has been decreased by using a segmented capacitor DAC. Another key feature of this converter is the high radiation tolerance.

The simulations show a ENOB of 9.87 and a SFDR of 73.42 dB. This resolution is suitable for most applications. However, it can be improved by using a digital calibration circuit that has been integrated in the final chip. The power consumption is equal to 513 μW which is appropriate for low power MAPS sensors.

First experimental results shows that some codes are missing due to the mismatch between the capacitors of the DAC. An ENOB of 8.5 bits has been achieved after digital correction.

References

[1] Pancheri, Lucio, et al. "Fully Depleted MAPS in 110-nm CMOS Process With 100–300-um Active Substrate." IEEE Transactions on Electron Devices 67.6 (2020): 2393-2399.

[2] James L. McCreary and Paul R. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques - Part I", IEEE J. Solid-State Circuits, vol. SC-10, pp. 371-379, Dec. 1975.

[3] Angelo Rivetti, Giovanni Anelli, Francis Aghinolfi, Giovanni Mazza, Francesco Rotondo, "A low-power 10 bit ADC in a 0.25-μ m CMOS: design considerations and test results". In: *2000 IEEE Nuclear Science Symposium. Conference Record (Cat. No. 00CH37149)*. IEEE 2000, pp 9-15.

[4] V. Hariprasath, J. Guerber, S.-H. Lee, and U.-K. Moon. "Merged capacitor switching based SAR ADC with highest switching energy-efficiency". Electronics Letters, 46, 2010.

[5] Chun-Cheng Liu et al., "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure". In: *IEEE Journal of Solid-State Circuits* 45.4 (2010), pp. 731–740.

[6] Y. S. Yee, L. M. Terman, and L. G. Heller, "Two-Stage Weighted Capacitor Network for D/A-A/D Conversio", IEEE J. Solid-State Circuits, vol. SC-14, no.4, pp. 778-781, Aug. 1979.

[7] Wei Tung and Shu-Chuan Huang, *An Energy-Efficient 11-bit 10-MS/s SAR ADC with Monotonic Switching Split Capacitor Array*. In: *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE. 2018, pp 1-5.

[8] Wenbo Liu, Pingli Huang, and Yun Chiu. "A 12-bit, 45-MS/s, 3-mW redundant successive-approximation-register analog-to- digital converter with digital calibration". In: IEEE Journal of Solid-State Circuits 46.11 (2011), pp. 2661–2672.