Three-Level Unidirectional Rectifiers under Non-Unity Power Factor Operation and Unbalanced Split DC-Link Loading: Analytical and Experimental Assessment

to as zero mid-point current modulation (ZMPCPWM) and ensures the converter operation with ideally zero low-frequency charge ripple [8,15,19].

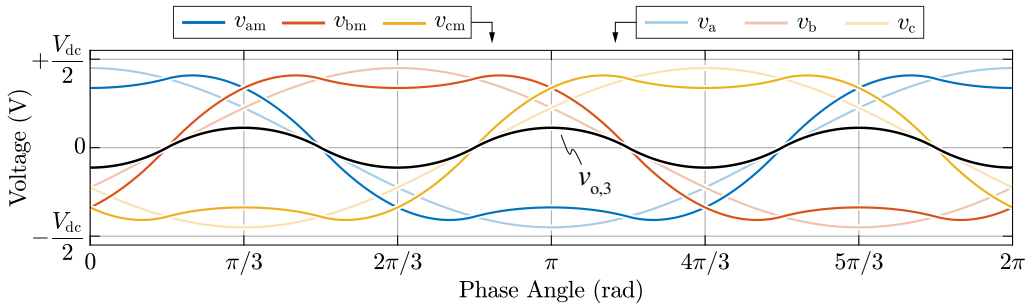

Figure 9. Zero-sequence voltage injection $v_{o,3}$ according to the zero mid-point current modulation (ZMPCPWM) with $M = 0.9$ and $\varphi = 0$. The reference phase voltages v_a, v_b, v_c and the resulting bridge-leg voltages v_{am}, v_{bm}, v_{cm} are shown for completeness.

Unfortunately, the adoption of ZMPCPWM cannot ensure $i_m = 0$ over the complete period when $\varphi \neq 0$, as pointed out in Section 2.5, since $i_{m,max}$ and $i_{m,min}$ cross the line defined by $i_m = 0$ (see Figure 7). In fact, $v_{o,3}$ encounters the zero-sequence voltage limits $v_{o,max}$, $v_{o,min}$ as soon as $\varphi \neq 0$ (see Figure A4 in Appendix B). Nevertheless, the injection of (26) ensures the minimum possible value of $\Delta Q_{m,pp} = \Delta Q_{m,pp,min}$ for a given power factor angle φ, since the saturated v_o is as near as possible to the desired $v_{o,3}$ value. Therefore, the adoption of ZMPCPWM allows the minimization of the size of the split DC-link capacitors for a given mid-point voltage ripple requirement and is therefore particularly beneficial in three-level rectifiers.

Figure 7 shows the mid-point current local average obtained with ZMPCPWM (i.e., $i_{m,ZMPC}$) for different values of φ. It is directly observed that higher absolute values of φ increase the minimum mid-point charge ripple.

The exact analytical expression of $\Delta Q_{m,pp,min}(M, \varphi)$ is derived in Appendix B for the complete operating region of the converter (i.e., $0 \leq M \leq 2/\sqrt{3}$ and $-\pi/6 \leq \varphi \leq \pi/6$). These results are illustrated in normalized form in Figure 10, where the analytical expression (A13) is compared to experimental measurements (see Section 3.2.4), showing excellent agreement.

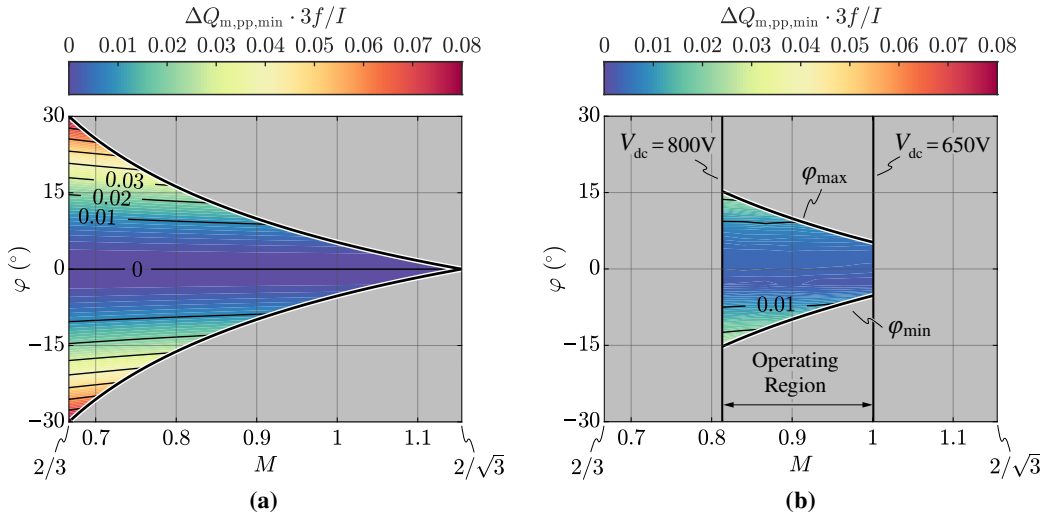

Figure 10. Minimum DC-link mid-point charge ripple $\Delta Q_{m,pp,min}$ (i.e., normalized with respect to the peak phase current I and three-times the grid frequency $3f$) for $2/3 \leq M \leq 2/\sqrt{3}$. (**a**) Analytical results and (**b**) experimental results, limited to the operating region of the rectifier prototype (see Section 3).

It is worth noting that (A13) provides a straightforward approach to size the three-level rectifier DC-link capacitors according to a maximum mid-point voltage ripple $\Delta V_{\mathrm{m,pp,max}}$ criterion, as

$$C_{\mathrm{dc}} \geq \frac{\Delta Q_{\mathrm{m,pp,min}}(M, \varphi)}{2\,\Delta V_{\mathrm{m,pp,max}}}, \tag{27}$$

where M and φ must be selected as the worst-case values within the operating range of the considered application. However, since (27) tends to 0 for $\varphi = 0$ (i.e., the analytical approach neglects the switching-frequency charge ripple), if the rectifier is exclusively operated under unity power factor, C_{dc} can be sized with conventional approaches derived for two-level inverters [38].

3. Experimental Results

In this section, the rectifier limits and performance in terms of displacement power factor (DPF), current total harmonic distortion (THD), maximum mid-point current capability and minimum mid-point charge ripple are experimentally assessed on a digitally controlled T-type converter prototype, supporting the theoretical analysis provided in Section 2, Appendices A and B. For reasons of conciseness, the converter performances are here evaluated only in steady-state conditions, nevertheless a complete assessment of the dynamical behavior of the considered rectifier prototype is provided in [16].

The specifications and the nominal operating conditions of the three-level T-type unidirectional rectifier exploited for the experimental validation are reported in Table 1. It is worth noting that this converter has been designed as the active front-end stage of an electric vehicle ultra-fast battery charger [16,39]. The rectifier prototype is illustrated in Figure 11 and consists of two paralleled three-phase 30 kW units, realized for modularity reasons. Nevertheless, only one converter unit is used in the experimental tests, due to the maximum power limitation of the available equipment.

Table 1. Three-level unidirectional T-type rectifier specifications and nominal operating conditions.

Parameter	Description	Value
f	grid frequency	50 Hz
P	nominal active power	30 kW
S	nominal apparent power	30 kVA
V	peak phase voltage	325 V
I	peak phase current	61.5 A
V_{dc}	DC-link voltage	650–800 V
L	boost inductance	150–190 µH
C_{dc}	DC-link capacitance	4080 µF
$f_{\mathrm{sw}}, f_{\mathrm{s}}$	switching, control frequency	20 kHz

Each converter bridge-leg employs two 650 V Si MOSFETs connected in anti-series (i.e., as 4Q switch) operating at 20 kHz and two 1200 V Si fast-recovery diodes. Furthermore, the converter boost inductors employ XFlux 60µ powder cores from Magnetics [40], which are characterized by a soft-saturating B–H characteristic. This feature leads to a current-dependent variable inductance value (see Table 1), which must be taken into account in the control tuning [16]. The detailed characteristics of the inductor design are reported in [39], obtained as a result of the optimization procedure described in [41].

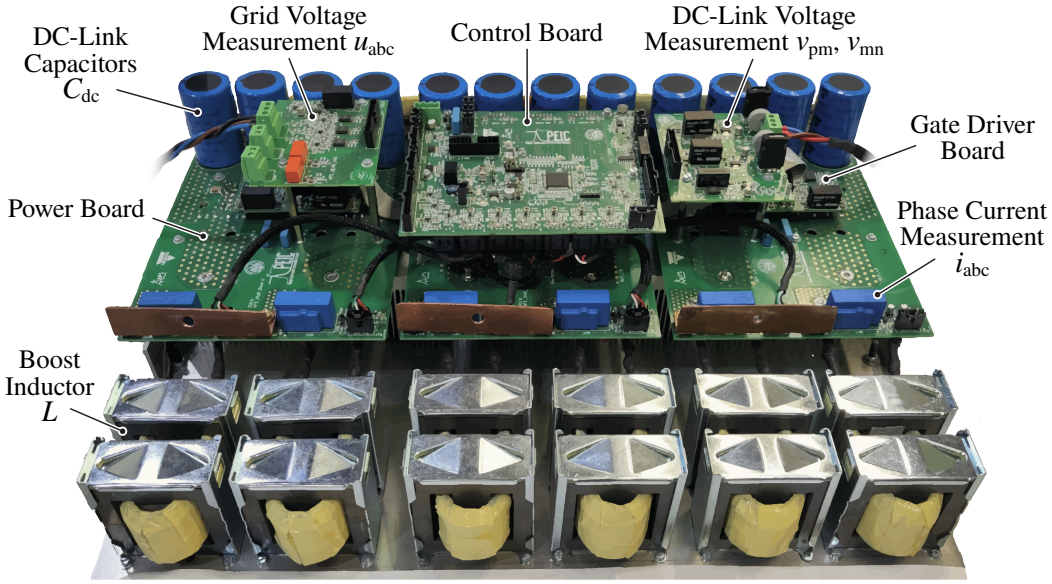

Figure 11. Overview of the three-level unidirectional T-type rectifier prototype used for the experimental tests. The converter consists of two paralleled 30 kW units: only one unit is exploited for the experimental verification, due to the maximum power limitation of the available equipment.

Figure 12 shows a schematic diagram of the adopted experimental setup. The T-type rectifier is connected to a grid emulator (i.e., emulating the 50 Hz, 400 V European low-voltage grid) by means of an *LCL* filter, consisting of the converter boost inductors (L), filter capacitors ($C_f = 15\,\mu F$) equipped with series damping resistors ($R_f = 0.8\,\Omega$), and grid-side inductors ($L_g = 100\,\mu H$). The main scope of the *LCL* filter is to eliminate the switching-frequency harmonic content from the grid currents $i_{g,abc}$ [17,42], so that a lower current total harmonic distortion (THD) is achieved and the converter may comply with grid-code standards [43,44]. Furthermore, the presence of the *LCL* filter allows isolation of the low-frequency component of the distortion, which depends on the control strategy, from the switching-frequency one, which only depends on the selected modulation scheme, allowing for a proper assessment of the converter closed-loop control performance. In the present case, the values of C_f and R_f are selected according to [39], and the value of L_g is representative of an equivalent inner grid impedance of ≈0.02 pu. On the DC-side, the converter is connected to two independent electronic loads, which emulate the rectifier split DC-link loads. The measurements are performed both with a Teledyne LeCroy 500 MHz, 12-bit, 10 GS/s, 8-channel oscilloscope (i.e., employing isolated high-voltage differential probes for voltage measurements and standard current probes for current measurements), and with an HBM GEN4tB 2 MS/s data acquisition system, leveraging current and voltage sensors with high rated accuracy (i.e., <0.1 %). In particular, the latter approach has been exploited to automatically map the rectifier performance over its complete operating region.

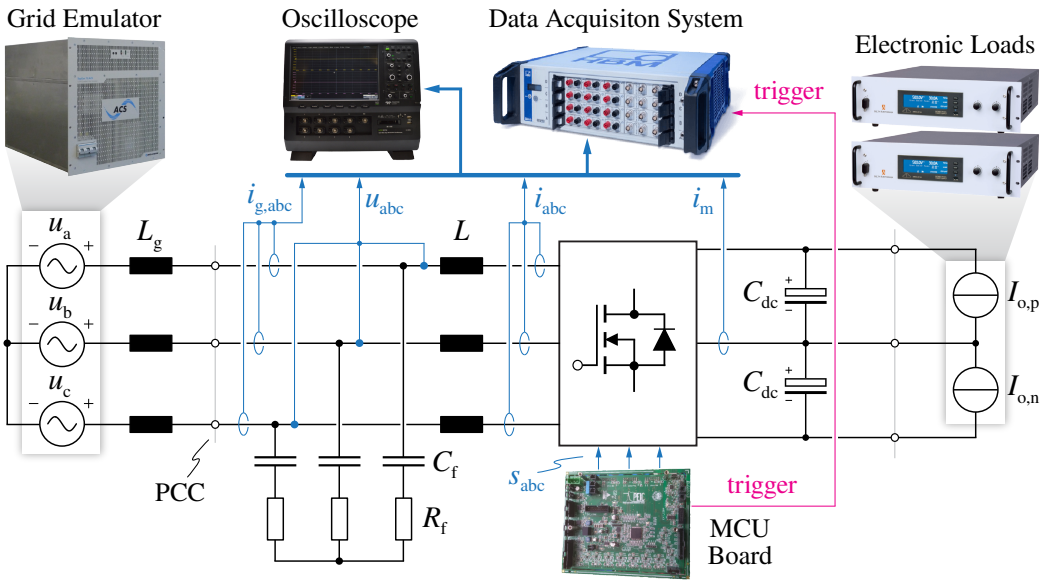

Figure 12. Simplified schematic diagram of the experimental setup.

3.1. Multi-Loop Control Scheme

The rectifier is controlled with the full-digital multi-loop control strategy reported in [16], where the detailed description and tuning of all loops is provided. A conventional voltage-oriented dq current control scheme is adopted [17,45–47], complemented by a DC-link voltage loop, tracking the desired DC-link voltage value V_{dc}, and a DC-link mid-point voltage balancing loop, ensuring limited steady-state and dynamical V_m voltage deviation. A simplified block diagram of the complete system and the adopted control strategy is provided in Figure 13.

The voltages at the point of common coupling (PCC) are measured to achieve the reference frame synchronization with the grid by means of a phase locked loop (PLL) [48,49]. The measured grid voltages are then fed forward in the current control loop, to unburden the integral part of the PI regulator. Even though the digital sampling and update process is performed once per switching/control period, the i_{abc} current feedback values are obtained by means of oversampling (32 samples per control period) and averaging, to enhance the measurement quality around the current zero-crossings. In fact, traditional synchronous/asynchronous sampling approaches do not provide the correct average current value when discontinuous conduction mode (DCM) takes place [21,50], thus affecting the current control accuracy and leading to increased low-frequency distortion. The DC-link voltage loop controls the active power transfer of the rectifier and therefore provides the reference to the d-axis current control loop. The q-axis current i_q, instead, is typically controlled to compensate the reactive power injected by the filter capacitors C_f (i.e., to ensure unity power factor operation at the PCC), nevertheless it can be set to any value that complies with the converter-side power factor angle limitations of the rectifier (see Section 2.4), being $\varphi = \tan^{-1}(i_q/i_d)$. Finally, the DC-link mid-point voltage balancing loop ensures $V_{pm} \approx V_{mn}$ at all times, acting on the zero-sequence voltage v_o injection [9,14–16,51]. In particular, this control loop theoretically does not interfere with the others, as v_o affects neither the active power transfer nor the phase current formation process (see Section 2.1.1). Furthermore, the measured V_m is passed through a moving average filter operated at $3f$, so that the control loop does not react to the possibly occurring low-frequency mid-point voltage oscillation.

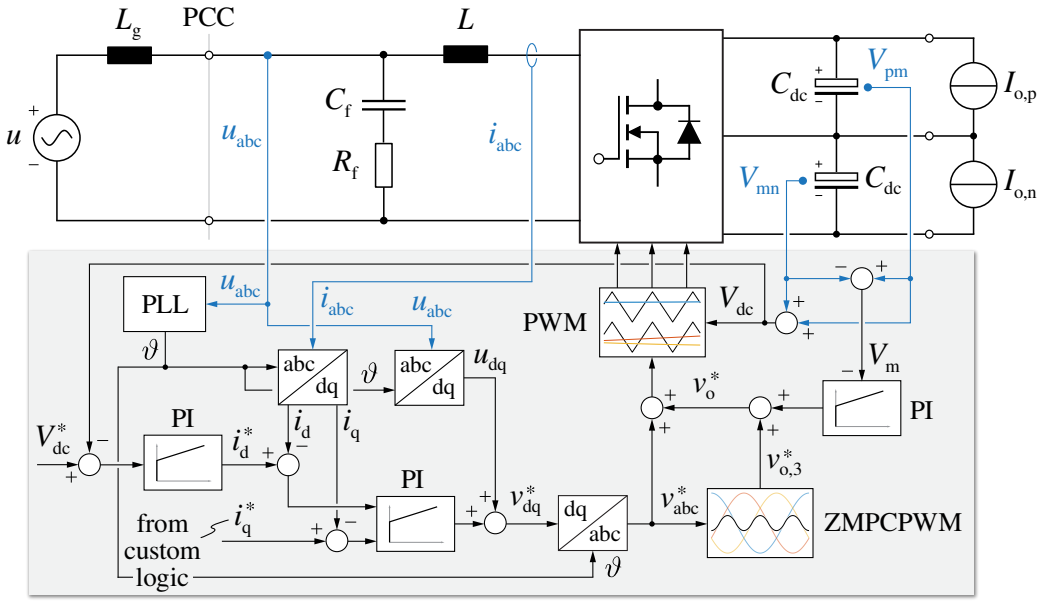

Figure 13. Simplified single-phase equivalent circuit of the considered system and overview of the adopted digital multi-loop control strategy [16].

In practice, the complete converter multi-loop control strategy is implemented on a STM32G474VE MCU from ST Microelectronics [52] with an interrupt service routine running at $f_s = 20\,\text{kHz}$.

3.2. Steady-State Performance Evaluation

The most significant rectifier waveforms in steady-state operation are illustrated in Figure 14, where the grid voltages u_{abc}, the converter-side currents i_{abc} and the grid-side (i.e., filtered) currents $i_{g,abc}$ are shown for $V_{dc} = 800\,\text{V}$, $\varphi = 0$ and different values of transferred power. It is observed that the grid-side current quality improves with the rectifier loading. For instance, at 10% of the rated power (see Figure 14b) the converter-side current ripple amplitude becomes comparable to the current peak value, therefore leading to marked low-frequency zero-crossing distortion that bypasses the filter capacitor and appears in the grid-side currents. Even though the distortion at light load may seem large, the pronounced DCM operation of unidirectional rectifiers typically leads to much higher distortion levels [21]. In the present case, the pseudo-sinusoidal shape of the currents is maintained thanks to the adopted current oversampling and averaging strategy, the high current control loop bandwidth and the feed-forward contributions reported in Figure 13 [16]. At 50% and 100% of the rated power (see Figure 14c,d the quality of both converter-side and grid-side currents improves substantially, as the relative amplitude of the current ripple decreases and the zero-crossing distortion related to DCM operation is mostly eliminated by the current control loop [16].

Both instantaneous and local average values of the DC-link mid-point current i_m for $V_{dc} = 800\,\text{V}$ ($M \approx 0.81$), $\varphi = 0$ and $P = 30\,\text{kW}$ are illustrated in Figure 15, where a focus is also provided in (b). Although the instantaneous value of i_m jumps between the converter-side phase current values $\pm i_a$, $\pm i_b$, $\pm i_c$ and 0 (i.e., visible from the current envelopes), the local average value of i_m remains approximately 0 along the complete grid period, due to the adopted zero-mid-point current modulation (ZMPCPWM) strategy. A focus of the instantaneous values of i_a, i_b, i_c and i_m towards the end of current sector ① is provided in Figure 15b, where the mid-point current is shown to jump between $+i_a$ (state 100), $-i_a$ (state 011), $+i_b$ (state 010) and $-i_c$ (state 110), as expected from space vector theory (see Figure 3b).

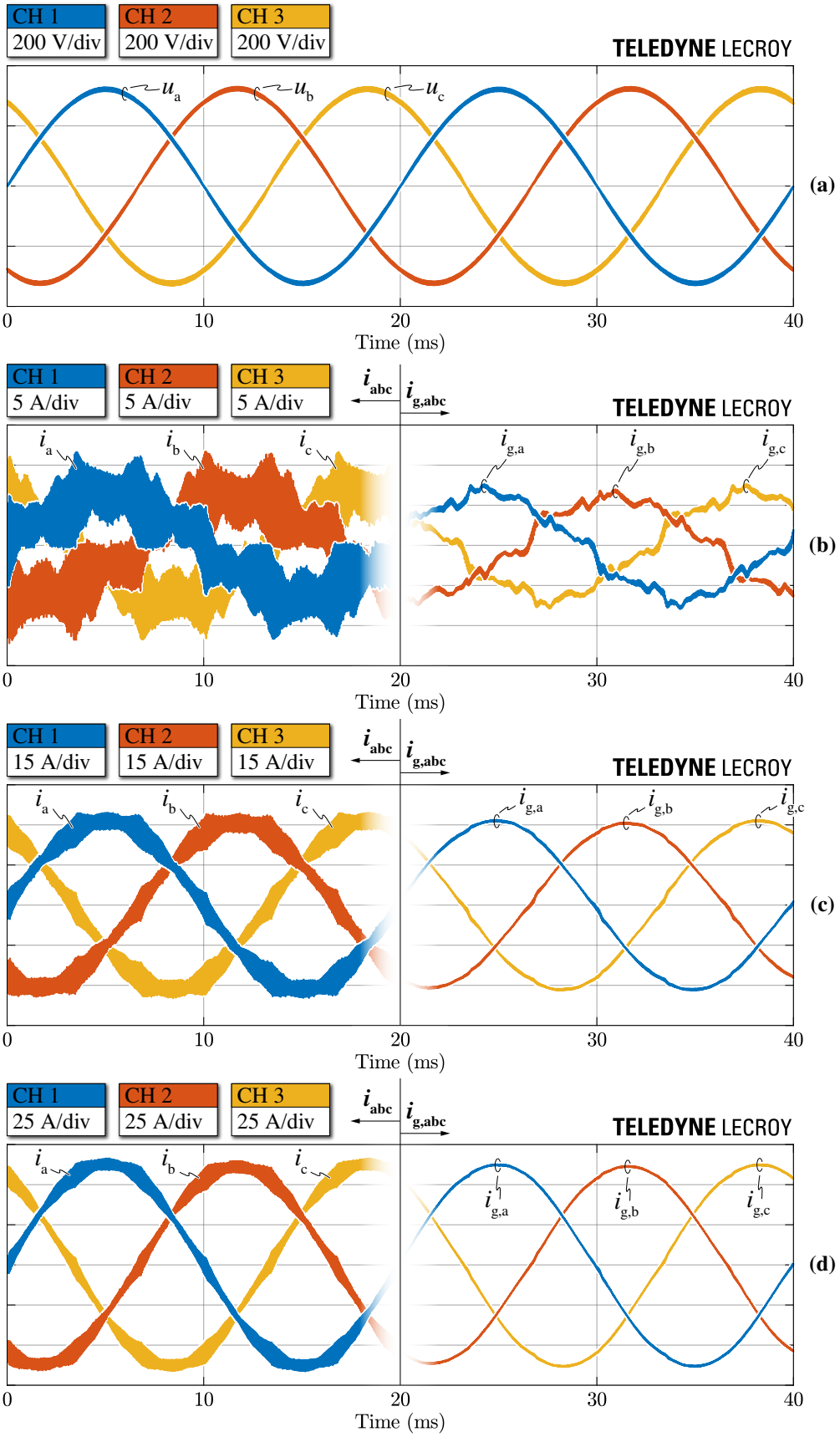

Figure 14. Experimental waveforms in steady-state conditions with $V_{dc} = 800\,\text{V}$ and $\varphi = 0$. Measured grid voltages u_{abc} (**a**) and both converter-side currents i_{abc} and grid-side currents $i_{g,abc}$ at (**b**) 10%, (**c**) 50%, and (**d**) 100% of the nominal power (i.e., $P = 30\,\text{kW}$).

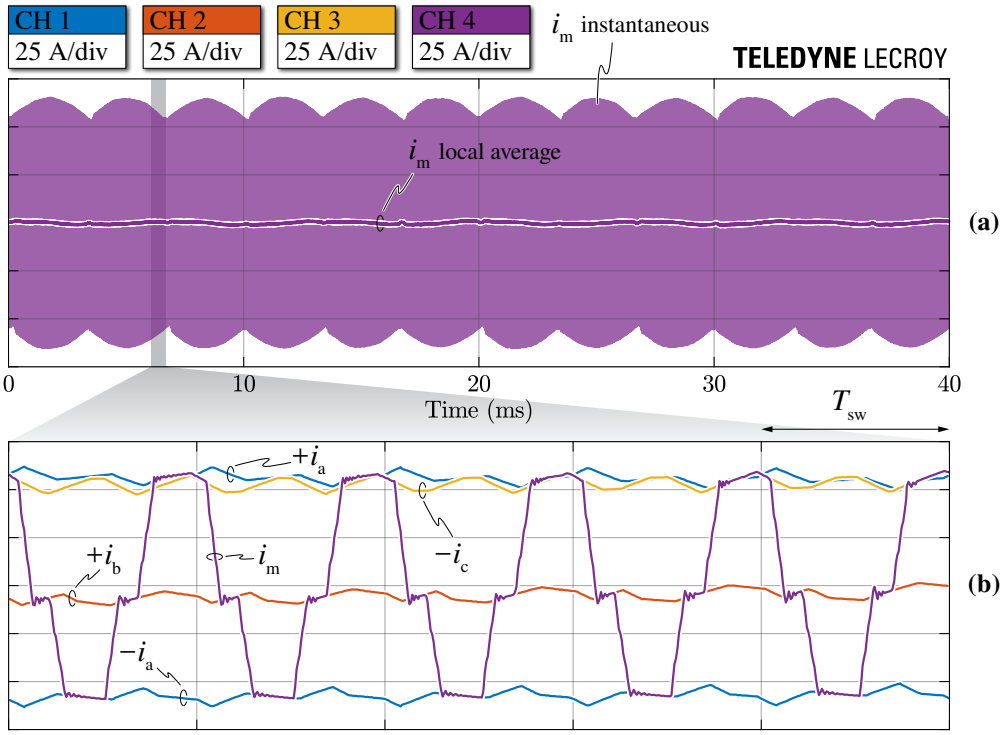

Figure 15. Experimental waveforms of the mid-point current i_m instantaneous and local average values in steady-state conditions with $V_{dc} = 800\,V$, $\varphi = 0$ and $P = 30\,kW$ (**a**). Focus of the instantaneous mid-point current towards the end of current sector Ⓘ (see Figure 3) and converter-side phase current values $\pm i_a$, $+i_b$, $-i_c$ (**b**).

It is worth noting that the measurement of the instantaneous mid-point current value is not common in the literature (i.e., the only case known to the authors is [53]), as it represents a challenging task to achieve. In practice, the current measurement must be placed within the commutation loop of all bridge-legs, thus negatively affecting the switching performance of the rectifier. In the present case, the measurement of i_m has been achieved by placing the current probe between the bridge-leg decoupling capacitors (i.e., 220 nF ceramic capacitors) and the DC-link capacitors (i.e., 4080 µF electrolytic capacitors), as schematically illustrated in Figure 16. Even though the decoupling capacitors are placed in parallel to the DC-link capacitors, their small capacitance value does not substantially affect the mid-point current, especially considering the relatively low switching frequency of the rectifier.

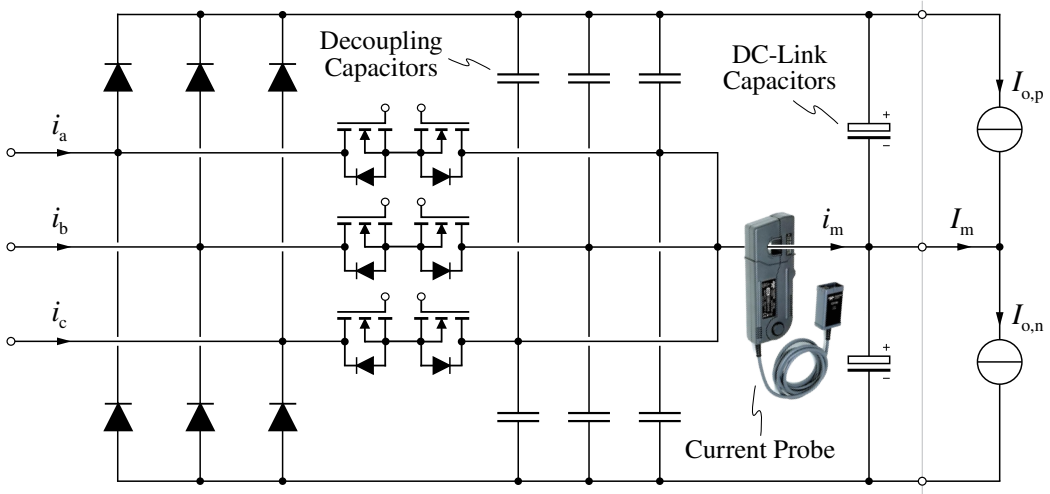

Figure 16. Schematic overview of the DC-link mid-point current i_m measurement setup. The current probe is placed between the bridge-leg decoupling capacitors and the DC-link capacitors.

Figures 17 and 18 show the most relevant rectifier waveforms under non-unity power factor operation and constant zero-sequence voltage injection, respectively. In particular, the reference bridge-leg voltages v_{am}, v_{bm}, v_{cm}, the reference zero-sequence voltage v_o, the converter-side currents i_{abc}, the grid-side currents $i_{g,abc}$ and the DC-link mid-point current i_m are shown for $V_{dc} = 800\,V$ and $S = 15\,kVA$. Furthermore, the effect of the zero-sequence voltage saturation $v_{o,max/min}$ on all measured quantities is highlighted by comparing the results with a conventional control implementation (i.e., with no saturation acting on v_o). It is worth noting that v_{am}, v_{bm}, v_{cm} and v_o are obtained from separate digital-to-analog converters (DACs) of the MCU (i.e., with a 0–3.3 V scale) and are thus rescaled in Figures 17a and 18a.

Figure 17 shows the operation of the rectifier with $\varphi = 15°$. In particular, Figure 17c highlights that non-unity power factor operation generates a large zero-crossing distortion if no zero-sequence voltage saturation is implemented. The enforcement of $v_{o,max/min}$, in fact, allows the rectifier to correctly apply the desired bridge-leg voltage values even when the phase currents are phase-shifted with respect to the reference voltages, as described in Section 2. Consequently, undistorted operation under non-unity power factor is achieved. Furthermore, Figure 17d shows that by saturating the zero-sequence voltage, a larger mid-point current local average i_m and thus a higher DC-link mid-point peak-to-peak charge ripple $\Delta Q_{m,pp}$ are obtained. This is because, to ensure the undistorted operation of the rectifier, the applied zero-sequence voltage v_o departs from the ideal $v_{o,3}$ value introduced by the ZMPCPWM (see Figure 17a). It is also worth observing that the local average of i_m obtained experimentally is in good agreement with the simulated waveforms reported in Figures 7 and A4b.

The rectifier waveforms with a constant zero-sequence voltage $v_o = 0.15\,V_{dc}/2$ added to $v_{o,3}$ (i.e., ZMPCPWM injection) are shown in Figure 18. This injection emulates the converter performance under unbalanced split DC-link loading, i.e., when a constant mid-point current periodical average $I_m = I_{o,n} - I_{o,p}$ is required. This is highlighted in Figure 18d, where the injection of a positive zero-sequence voltage is shown to generate a negative value of mid-point periodical average I_m, as expected from theoretical considerations. Additionally in this case larger i_m and $\Delta Q_{m,pp}$ ripple values are obtained when the $v_{o,max/min}$ saturation is enabled. Figure 18c shows that the zero-sequence voltage saturation $v_{o,max/min}$ allows substantial improvement of the phase current waveforms. Nevertheless, in this case the zero-crossing distortion cannot be completely avoided, since the injection of the constant zero-sequence voltage contribution increases the amplitude of the converter-side current ripple (see Figure 14c for comparison), which widens the DCM window around the current zero-crossings and leads to higher distortion. It is worth noting that this issue can be greatly reduced in practice by independently controlling the two anti-series mid-point switches, such that the free-wheeling of the current through the mid-point is always possible [26]. In fact, even though in the present case the two anti-series switches are supplied by independent gate drivers, they receive equal PWM signals, greatly simplifying the modulation and the control of the rectifier. It should be pointed out that the low-frequency distortion would mostly disappear at full load (i.e., $P = 30\,kW$), due to the lower ratio between the current ripple and the current peak. However, this condition could not be tested, due to the power limitations of the adopted electronic loads.