Doctoral Dissertation
Doctoral Program in Electrical, Electronics and Communications Engineering (32nd Cycle)

Multi-objective optimization of power electronic converters

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Context of the Research

Electronic Power Conversion is a key element for the development of sustainable modern lifestyle, and represents both an interesting field of research and a challenging market. The optimization of the power conversion application is a process running since several years, and the efforts required to achieve significant benefits are constantly growing, while gradually evolving toward complete redesign of the systems. This means that for small system performance variations, very different requirements for the single components may be necessary, involving completely different technologies and manufacturing capabilities. Different technologies require time and investments for the industry to be implemented efficiently on a large production scale required by electronics, so understanding the various possibilities for the market and being able to predict the next steps of evaluation of the applications is key to have the right technology ready to kick in when the marker requires it.

Hence the present thesis in collaboration with **Vishay Semiconductor Italiana** is a contribution to the improvement of an existing Multi-Objective Optimization framework for power electronics converters.

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1 Introduction

The electrification of transportation and the data center revolution is driving the development of power electronics.

Given the scarce power density of Li Ion Batteries (200-300 kWh/kg) compare to gasoline (12000 kWh/kg) [1] and their charge limitations, there is a need to optimized power electronics in the vehicles in order to reach the autonomy and performance of Combustion Vehicles (CVs).

In the last decade significant advances were made, enabling Electric Vehicles (EVs) transition from unpractical, luxury vehicles to affordable, everyday vehicles. EVs Battery Charger power capacity, power density and efficiency increased. Li Ion prices went down, thanks to scale economy. Improving autonomy, charging times and efficiency.

Meanwhile the growth of services provided by internet has increase the demand for Data centers. Currently, Amazon produce more of the 50 % of its revenue from its data center business.

In general, in both sectors there is a constant need to increase the efficiency, power density, power capacity, reliability and robustness of power converters. Moreover, with the introduction of new services new requirements are needed. For example, Vehicle to Grid (V2G) power transfer for EV Chargers require bidirectional converters.

Given that designing a power converter is not a straightforward task, one of the hot topics of power electronics is the development of a framework for the converter design and Multi-Objective Optimization of its figures of merit.

Up to now the Center for Power Electronics Systems (CPES) at Virginia Tech University and the Power Electronic Systems Laboratory (PES) at ETH Zürich have led the development of a framework for the Multi-Objective of power electronic converter. The framework consists of 4 levels/steps (Figure 1):

Materials Selection: The raw materials and the process used to transform that materials in a component have a direct impact in the performance of the devices. For examples for semiconductors the raw materials can be either Silicon (Si), Silicon Carbide (SiC) or Gallium Nitride (GaN), and the process could refer to the doping profile or the structure (e.g. trench). The material and process choice has a direct impact in the die area, power losses and the thermal properties of the device.

Components Selection: Each one of the fundamentals building blocks of the power converters. They could be either active or passive:

- Active Components: Semiconductors.
- Passive Components: Inductors, Transformers, Capacitors and Resistances.

System Selection: Is the combination of the Topology and the Control Strategy. The Topology dictates the part count of both active and passive components, the current and voltage rate of semiconductors devices while the Control Strategy determines the inductor and transformers requirements and the required capacitors characteristics for the power converter DC-Link.

Performance Space: Could be either a 2D, 3D space or a radar diagram in which each axis represents a figure of merits of the power converters (e.g. power density ρ, efficiency η , cost ($\$, £, €$) , part number, robustness, weight or weight density (α), etc.

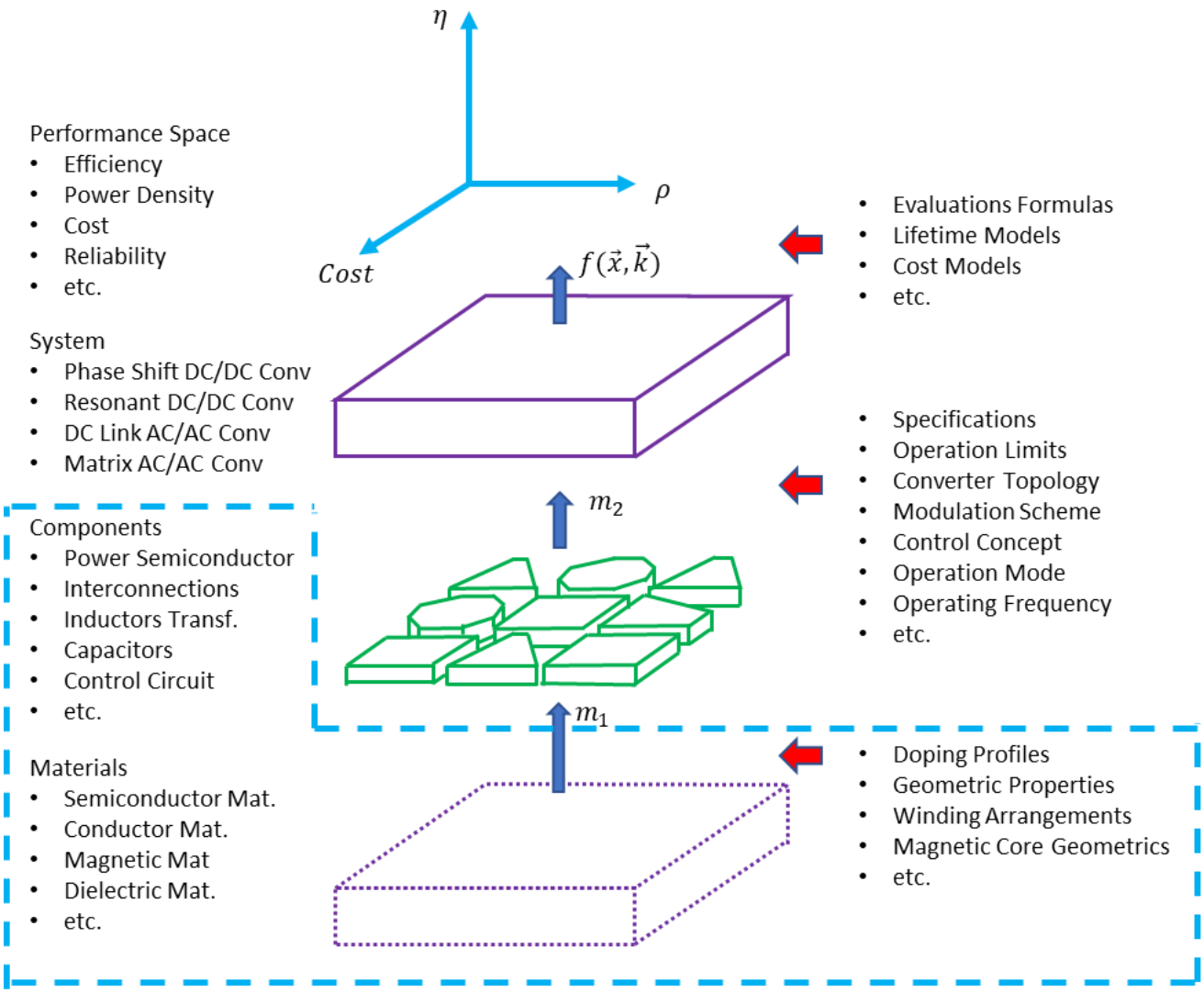


Figure 1: Multi-Objective Optimization Framework Levels [2]

Figure 2 illustrates how the performance space of different converters topologies (represented with a prefix letter) and different control strategies (represented by a suffix number) are evaluated using the characteristics of a single type of semiconductor devices.

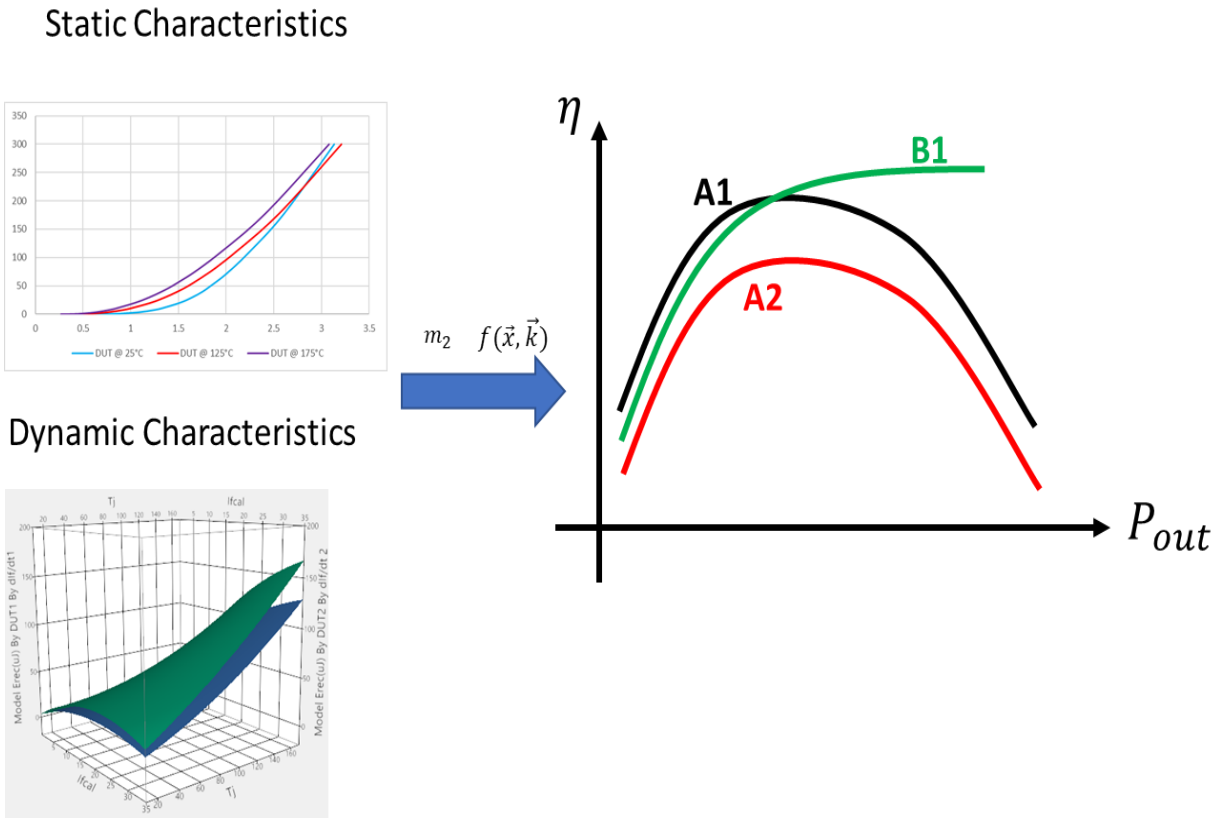


Figure 2: Multi-objective Optimization (Simplify example) where Pout:output power

Even though as shown in Figure 1 the choice made in the lower level have a direct impact in the upper level, for designers is more natural to follow a top-down approach. Starting from the Topology and the Control strategy selection, follow by the component's selection, which is equivalent to making a component and material selection at the same time. Finally, the performance space of the converters is calculated based either on analytical or computational model

Usually, attention is focused in the system and performance space level, undermining the impact of the choice made in the first two levels of the framework on the overall figures of merits of the converter. The latter due to two reason:

1. From a power converted designer point of view it is not possible to make slight variation in the first level of the of the Multi-Objective Optimization framework.

Hence power converters designers tend to expend more time in the upper levels of the framework.

2. Up till this year, with the introduction of 600 V SiC devices to the market, there were a limited choice of semiconductor devices technologies and as a consequence limited component that could be used for a given design solution. Moreover, the performance-cost tradeoff of the available devices was very obvious so in most cases common sense was enough to make a correct component choice. For example, SiC Carbide MOSFETs were first introduce as 1200 V devices in order to cope high frequency application where the Si devices existing at the time (2012) where not able to cope with the efficiency and thermal requirements of the application. There was a performance gap between SiC MOSFETs and Si IGBTs, and as a consequence there was also a cost gap.

In order to cope with today's converters requirements, it's compulsory to optimize the converter at the material and component level. Moreover, figure of merits like cost and reliability could be optimize only by acting in the material and component level. For a semiconductor device manufacturer like Vishay understanding the impact of design choices in the lower level of the framework will:

- Enables to make more competitive devices focus in mainstream applications
- Enable to understand the boundary condition between semiconductors technology in terms of desire performance and cost of a given application.
- Find new market niche where it is possible to sell derivative products of the existing Vishay catalog.

Similarly, for magnetic components (i.e., inductors and transformers), there is a correlation between design choices like winding arrangement, core material selection on the overall performance of the converter and the overall performance of the converter that are not straightforward.

Therefore, this thesis enlightens the material and component selection process by explaining in depth the correlation between the latter and the overall figures of merits of the power converter for both active and passive components. Moreover, algorithms and strategies for components selection are given which can be integrated to the work done by CPES and PES in order to improve the accuracy of the Multi-Objective Optimization framework and be able to consider variables like cost and reliability.

The current chapter (Chapter 1) describe the motivation and the scope of the following thesis.

In Chapter 2 the different materials and structures used for semiconductors devices are introduced. Then, an in-depth explanation of the performance tradeoff of the

different semiconductor technologies is given. Finally, an algorithm for semiconductor and heatsink selection is given.

Chapter 3, focus on passive components. It starts by discussing the accuracy and complexity of magnetic components reluctance and power loss model available in literature. Then, in proposing an algorithm for inductor/transformer design. Finally, capacitors technology and application are discussed.

In Chapter 4, a case study of a Multi-Objective Optimization of an LLC converter for an EV Charger is presented. In this case it is shown how using the techniques learned in Chapter 2 and 3 is feasible to extend the operation region of the LLC converter to the buck region.

Finally, conclusions are presented in Chapter 5.

2 Semiconductors Components and Driver

Wide Bandgap (WBG) devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are key enablers of the next generation of power converters. They enable to reduce both conduction and switching losses, increasing the efficiency, power density and operation temperature limit of power converters. Moreover, they enable to extend power converter applications (e.g. electric aircrafts, ships).

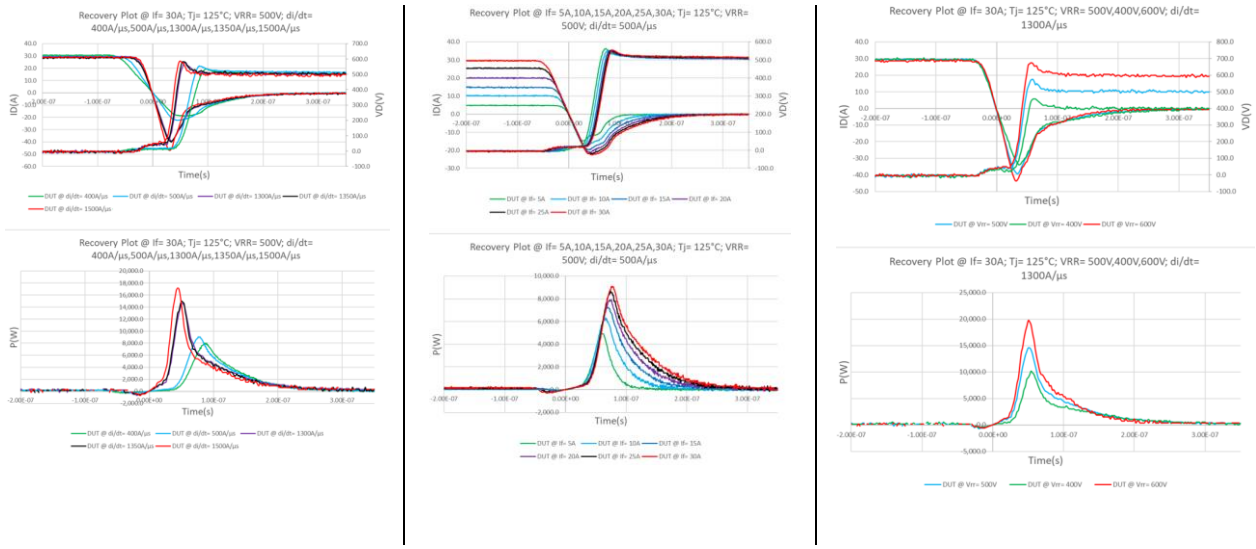
WBG superior characteristics give the illusion of a direct replacement of Silicon (Si) devices by WBG devices, enable to exploit all their benefits. Designers should be aware of the technical challenges of implementing each semiconductor technology. These challenges could be either related to the desired operation condition (e.g. crosstalk and voltage overshoot in half bridge switching at high frequency) or to the semiconductor technology itself (e.g. E-mode GaN devices are susceptible to noise due to the narrow-allowed gate voltage). Moreover, the performance of semiconductor devices during switching depends on: the characteristics of the device, the gate driver, switching conditions, the switching cell, the layout and switching type (Table 1).

Characteristics of the devices	MOSFETs: – Input Capacitance $C_{iss} = C_{GD} + C_{DS}$ – Reverse transfer capacitante $C_{rrs} = C_{GD}$ – Output Capacitance $C_{oss} = C_{DS} + C_{GD}$ – $g_m = \partial I_{DS}/\partial Vgs$ @ T_j Where T_j: Junction temperature g_m: Transconductance – I_D vs V_{DS}, V_{GS} @ Tj – Thermal coefficient	DIODES: – $C_{j,D}$: Diode Junction Capacitance – I_D vs V_{DS}, V_{GS} @ Tj – Thermal coefficient
Gate driver	– Voltage source gate drive (VSG) – Current source gate drive (CSG) – Active gate drive	
Switching Conditions:	– If: Forward Current flowing through the devices prior to the commutation – Vrr: Is the value of the reverse bias voltage that the devices should have after commutation – Di/dt: Descending slope of current during the turn-off of a Si diodes – T_j: Junction temperature of the DUT	
Layout	– Refers to the stray inductance and parasitic capacitance due to the layout.	

Switching Type:	– Hard Switching (HS) – Zero Voltage Switching (ZVS) – Zero Current Switching (ZCS)
Switching Cell	– Half Bridge – MOSFET in tandem with a Diode – Vienna Switching Cell – Neutral Point Clamped – …

Table 1: Factors that impact switchign performance

For example, Figure 3 show a parametric study of the change of the dissipated energy during switching in function of dI/dt, I_f, V_{rr} for Silicon diode.



(a) *(b)* *(c)*

Figure 3: Si diode parametric analysis of $\mathrm{E_{rec}}$ (a) with respect to $\mathrm{dI/dt}$ (b) with respect to $\mathrm{I_f}$ (c) with respect to $\mathrm{V_{rr}}$

Hence when performing a multi-objective optimization of a power converter the semiconductors devices cannot be consider individually, instead as a combination of the factors stated in Table 1.

The first 3 parameters in Table 1 are selected at semiconductor level while the last 3 parameters are fixed at system level. The latter, are a consequence of the selected topology and the control strategy of the converter.

Finding the combination with the optimum performance-cost tradeoff is not straightforward. The dynamics between the factor in Table 1 change depending on the semiconductor technology (i.e. Si, SiC and GaN). In this chapter the aforementioned dynamics will be clarified, enabling to make a proper semiconductor selection and minimize switching losses.

This chapter starts by giving a snapshot of the current status of Si, SiC and GaN technologies and commercial discrete devices with a breakdown voltage between 600V and 1200V. Then, the relation between the active area of the device and the conduction and switching losses will be explain in order to understand how to select the component current rate required by the application. Next the dynamic between the parameters stated in Table 1 in the case of Hard-Switching commutation and a voltage gate driver for Si, SiC and GaN devices will be clarify using the power loss model presented in [*3*]. Next, the tradeoffs between the driver circuit and the overall converter switching losses, cost and robustness will be explained. After that, the procedures used to measure the switching losses of WBG devices will be presented. Finally, the electrothermal model of semiconductor devices used for multi-objective optimization of a power converter will be presented.

2.1 Semiconductors technology current status

Devices characteristics depends in both the physical properties of semiconductors materials (Figure 4) and the structure of the devices. The latter are select by semiconductors manufacturers based on device time to market, the fabrication process knowledge, feasibility, cost, stability and reliability.

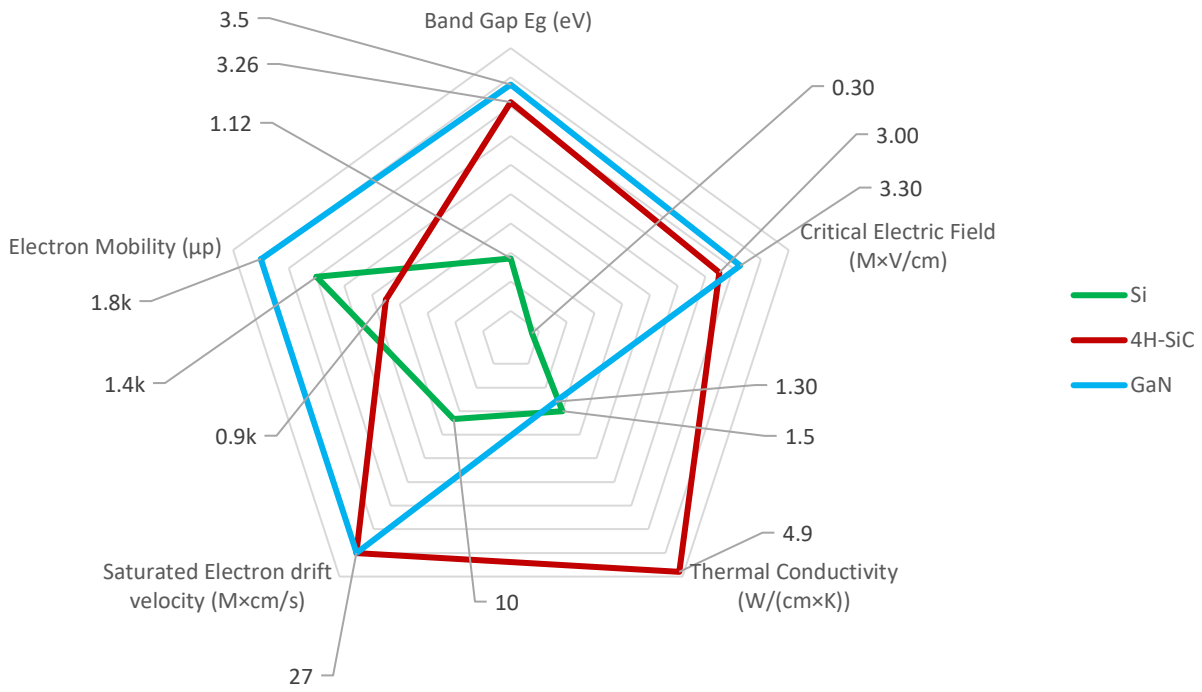


Figure 4: Si and Wide Band Gap materials properties [4]

SiC, like Si, enable n- and p-type control across wide doping range and thermally grown SiO_2 on the surface. Hence, both Si and SiC devices using vertical structures for efficient current distribution and implanted source/drain regions on MOSFET and anode regions on Diodes are possible.

On the other hand, GaN power devices have their roots in RF amplifying devices. Therefore, the process technology and the structure of commercial GaAs RF High Electron Mobility Transistors (HEMTs) are the basis for GaN power devices. Owing the low cost, large diameter and process maturity of Si Wafers, commercially GaN power devices have been grown on 6- and 8-in (111) Si Substrates.

In order to understand the state of the art of semiconductors technologies it's necessary to understand the current state in the life cycle of each technology and how the intrinsic properties of the devices (Figure 4) and there structures are related to the components characteristics (Figure 5).

Figure 5 Relation between material properties and the characteristic of the components for vertical devices.

Currently there are three commercially available semiconductors technology, Silicon (Si), Silicon Carbide (SiC) and Gallium Nitride (GaN) devices.

Silicon Devices:

Si devices have been available in the market for more than 50 years. During this time, the scientific community was able to fully understand the physics behind the technology. Semiconductors designer mature experience that enables to improve the performance, reduce fabrication cost and correct flaws identified both in the design stage and in applications. Therefore, Si is the most mature and reliable technology.

Currently Si devices performance is near Si material theorical limit [*5*], there has not been a significant progress since the introduction of Super Junction (SJ) MOSFETs by Siemens, now Infineon, in 1998 [*6*]. SJ technology enables to reduce the $R_{DS,on}$ and the input and output parasitic capacitance (C_{iss} and C_{oss}) of the MOSFET by introducing n/p stripes in the depletion region (Figure 6). However, it introduces a nonlinearity in the C_{oss} that can cause turn on and turn off delays. They are available with voltage-rate between 600V and 900V

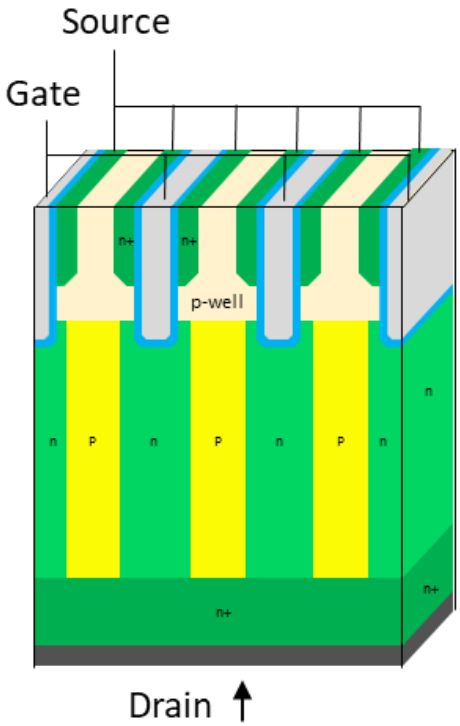


Figure 6: 3-D structure of a Si Super Junction MOSFET

Si device manufactures offer different families of product; with different tradeoff between conduction and switching losses. Given that the dynamic recovery characteristics of the devices in datasheets are reported in different switching conditions it's not possible to make a one-to-one comparison between different components. A graph of the forward voltage at nominal current versus the energy dissipated during one commutation (E_{rec}) (Figure 7) in a representative switching condition of the target application is proposed as a graphical method to understand the tradeoff between conduction and switching losses of each device in Hard Switching applications. For the switching conditions, the forward voltage I_f and the reverse voltage V_{rr} can be derived from the power converter simulation, T_j can be estimated as well as the dI/dt. The former by setting up a safe margin from $T_{j,max}$, the second one based on the switching cell (i.e. Half-Bridge, Diode in tandem with MOSFET, NPC switching cell, etc.) , the potential switching devices (i.e. SJ MOSFET, Si IGBTS) and the best experience of designers with Si semiconductors (ex. Si IGBTs 200A/us-300A/us and Si SJ MOSFET 400A/us-1400A/us) .

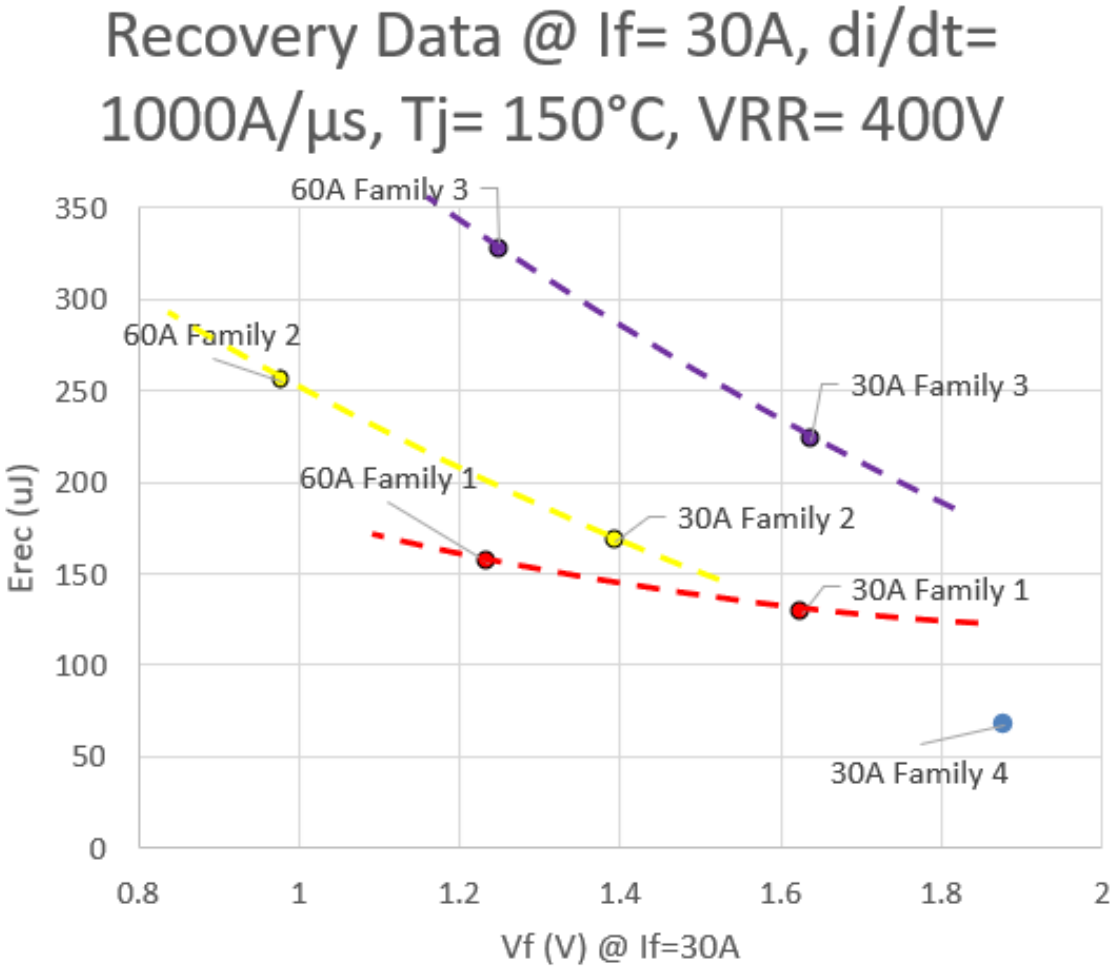


Figure 7: Trade-off between conduction and switching losses at $\mathrm{I_f} = 30\mathrm{A}$, $\mathrm{dI/dt} = 1000\mathrm{A/us}$, $\mathrm{T_j} = 150\mathrm{°C}$ and $\mathrm{V_{rr}} = 400\mathrm{V}$

In Figure 7 each diode is represented by a point in the graph. Diodes belonging to the same family with different current rate will be in a curve that represent the trade-off between switching and conduction losses of that family of devices. Even though Figure 7 represent a single operation conditions, it is enough to make a preliminary screening of the devices that could be mounted in the converter and understand the difference between different families of products.

A similar graph could be draw to make a fine tuning of the current and voltage skews (if possible) during commutation. Typically, the worst-case condition of operation is used as the reference conditions. In this case special attention should be paid when fine tuning the current skew, there is a tradeoff between E_{rec} and EMI. The optimum current skew will minimize losses without creating EMI problems

Despite Si MOSFETs and Rectifiers lack of performance with respect to WBG devices, the bast catalogue of available devices in the market, the low cost of Si technology and an accurate selection of the devices enable to exploit each cent of the cost. Making Si devices the first choice in power electronics. Moreover, resonant power converters topologies like LLC and CLLC enables to extends the switching frequency capabilities of Si rectifiers. LLC rectifier at the secondary side, experience either zero current switching or hard switching with a dI/dt value between 3 $A/\mu s$ and 50 $A/\mu s$. Hence, switching losses are either zero (in the case of ZCS) or one order of magnitude smaller with respect to conventional hard switching applications (ex. In a PFC application).

Silicon Carbide Devices:

Similar to Si devices, the fabrication process has been tweaked in time to optimized their designs in terms of performance, cost and reliability. SiC has a critical electrical field an order of magnitude larger than Si (Figure 4) enabling the fabrication of devices with higher break down voltage. Their bandgap and thermal conductivity is 3 times bigger than Si (Figure 4) which translate in a better stability at higher temperatures and better heat dissipation capability respectively. Hence, SiC devices maximum temperatures are between 175°C and 200°C. Moreover, SiC critical electrical field (10 times of Si) allows thinner and highly doped drift layer, that translate in smaller forward voltage for SiC diodes and smaller on-resistance $R_{DS,on}$ for SiC MOSFETS with respect to their Si counterpart.

SiC Diodes

SiC diodes were a disruptive technology introduced to the market as Schottky diodes by Infineon in 2001 and as JBS diode a year later by Cree. Prior to SiC diodes, hard switching applications like Power Factor Correctors (PFCs), were limited by Si diodes excessive switching losses due to their recovery. Designers had to limit the maximum power ($P_{o,Max} < 2kW$) and switching frequency ($F_{sw} < 50kHz$) to prevent diodes junction temperature $T_{j,Diode}$ from exceeding their maximum junction temperature ($T_{jMax,Diode}$). Moreover, the on-switching losses of MOSFET where limited by diodes since their recovery is strongly related to diodes $\left.\frac{dI}{dt}\right|_{I_D=0}$ when switching. A direct drop-in replacement of Si diode with their SiC counterpart constitutes a dramatically

reduction of the overall losses of the diode due to their negligible recovery, improving power converter efficiency η , $P_{o,Max}$ and thermals. SiC diodes enable designers to work at higher frequency in order to reduce the size of magnetic components and improve the power density. Moreover, their recovery is not sensible to $\left.\frac{dI}{dt}\right|_{I_D=0}$ when switching, allowing to increase the on switching speed of MOSFET and reduce their on-switching losses.

There are four types of SiC diodes (*Figure 8*):Schottky Barrier Diode (SBD), PIN Diode, Junction Barrier Schottky diodes (JBS) and Merged PIN Schottky (MPS)

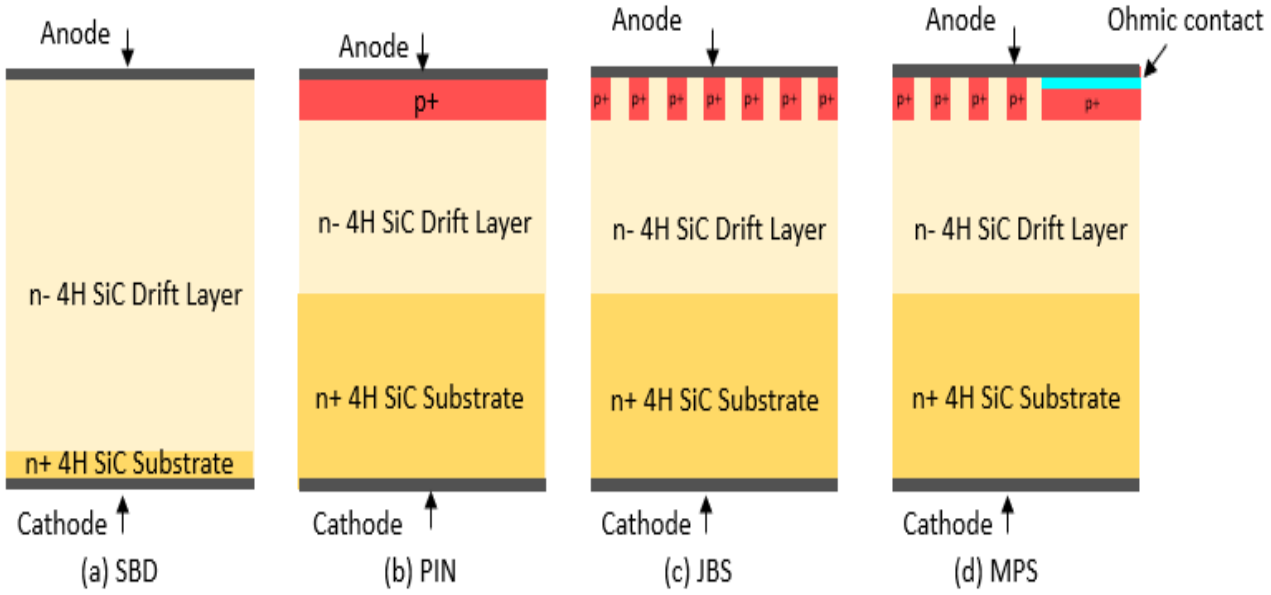


Figure 8: SiC diodes Structures (a) Schottky Barrier Diode (SBD) (b) PIN Diode (c) Junction Barrier Schottky (JBS) (d) Merged PIN Schottky (MPS).

Schottky Barrier Diode (SBD): They are unipolar devices that features low forward voltage and virtually zero reverse recovery, making it the first choice for power converters designers. However their voltage rate is limited to 600V, given that their leakage current increase rapidly with temperature; potentially creating a thermal run away problem. Moreover, SBD does not possess surge capability.

PIN Diode: They are bipolar device with a highly doped and narrow p+ region for the anode, a lightly doped drift region and wide N- region at the cathode. They are usually used in high voltage application; above 3.3kV; where their conduction losses are superior to SiC SBD,JBS and MPS diodes thanks to conductivity modulation that

reduce the drift region resistance at high currents. Contrary to SiC SBD, PIN Diodes have low leakage currents and reverse recovery.

JBS Diode: This device is a hybrid diode with interdigitated Schottky contact and p+ implanted regions for the anode, and a highly doped N+ region for the cathode [*7*]. In reverse conduction the pin depletion regions shield the metal contact, pushing away the maximum electrical field away from the ohmic contact to the bottom of the P+ region. Hence, it has low leakage currents even at high temperatures. For small V_f, MPS diodes work as a Schottky diode; majority carriers are injected to the drift region only through the Ohmic contact. When voltage increases, the p+ implanted regions inject minority carriers (holes) in the drift region reducing the resistance of the drift region as a PIN diode would do. The aforementioned minority carrier system gives JBS diodes surge capabilities and immunity to high di/dt and dv/dt ratings

MPS Diode: They have a very similar behavior and structure to the JBS Diodes, therefore in literature the term MPS is consider a synonym for JBS diodes. They differ in that MPS diodes have p+ implanted regions with ohmic contact, given an additional degree of freedom to control both diodes V_f, surge [*8*] and avalanche capabilities [*9*].

SiC MOSFETs

SiC MOSFETs were released to the market in 2011 by Cree outperforming 1200V Si IGBTs. At the time, the small wafer sized (4-inch) compromised SiC MOSFET cost, limiting their used to high-end applications. However, in the last decade SiC device manufacturers have managed to expand wafers size up to 6-in , improving devices characteristics and widen the available voltage rate overlapping with Si SJ MOSFETs in the 650V-900V range.

Currently, there are to two types of SiC MOSFET available in market: SiC MOSFETs with a planar gate structure call DMOS and with a Trench structure.

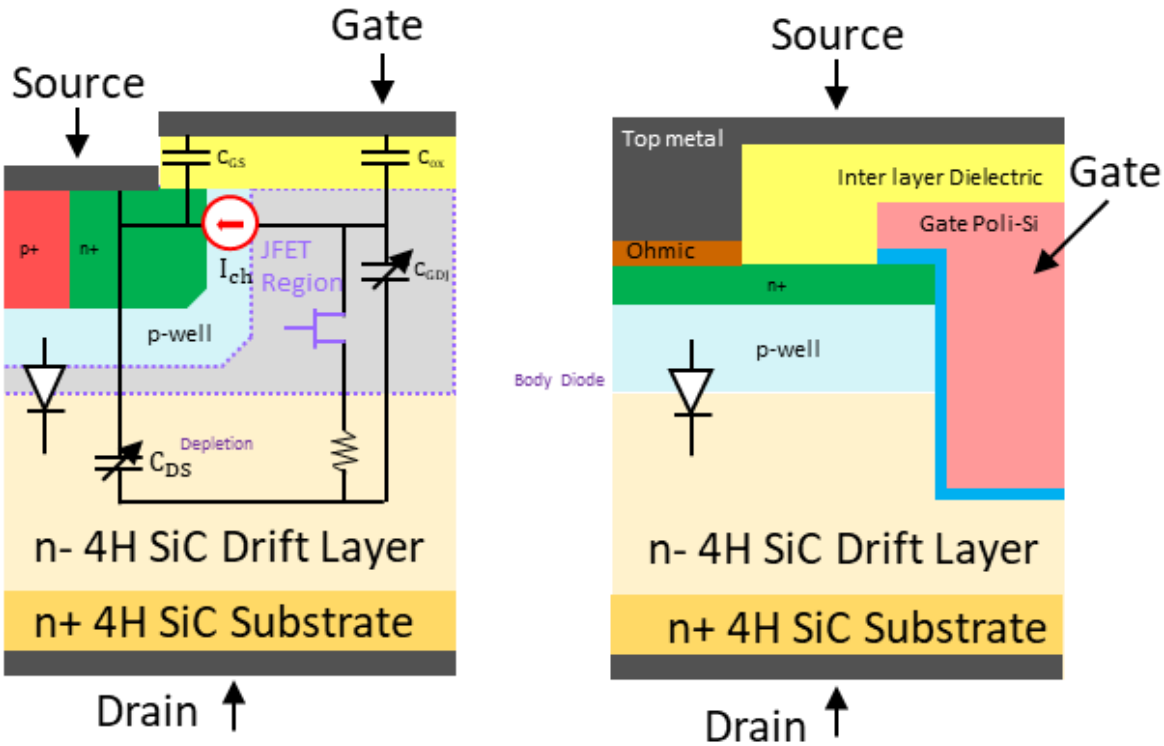


Figure 9: Types of SiC MOSFETs (a) SiC DMOS (b) SiC Trench

SiC Trench MOSFET have a lower Rdson than DMOS, given the absence of JFET region and improved channel density. However, the electric field stress at the corners of the trench structure could cause gate oxide reliability problems that could be avoided with the DMOS structure. Therefore, the first generation of commercial 1200V SiC MOSFET presented by Cree in 2011 had a DMOS structure. Nevertheless, SiC devices manufacturers like Rohm, Infineon and Mitsubishi are using trench structure in their last generations devices.

A review of the static and dynamic characteristics of 1200V commercial SiC MOSFETs can be found in [*10*].

Gallium Nitride Devices:

GaN-based power devices is an emerging technology. The absences of low-cost low defect GaN bulk substrate, the material and process technologies similarities between GaAs and GaN, and the possibility to epitaxially grow GaN over a high

diameter low-cost Si substrate focus the attention of scientific community on the development of GaN-on-Si HEMTs.

Contrary to Si and SiC power devices, they are based on a lateral structure (High Electron Mobility Transistor) that suffer from several shortcomings that have hindered their widespread in power electronics applications.

GaN HEMT consist of an AlGaN/GaN heterojunction in which the polarization charges induce a high-density high-mobility two-dimensional electron gas (2DEG) reducing considerably the $R_{DS,on}$ with respect to Si and SiC-based devices.

The epitaxial growth of the aforementioned structure in a Si substrate is not straightforward. There is a lattice and thermal expansion coefficient mismatches between Si and GaN. Hence, the GaN buffer layer adopts a stack structure (*Figure 10*):

- AlN Nucleation Layer: prevent Si from diffusing in the GaN epilayer.
- Strain Relief Layer: Cope lattice and thermal mismatch
- Carbon-Doped Layer: Suppress vertical leakage currents, enhancing the breakdown characteristics of the device.
- Undoped-GaN Layer: In order to minimize trapping effect, the Carbon-doped Layer must be distanced from the 2-DEG.

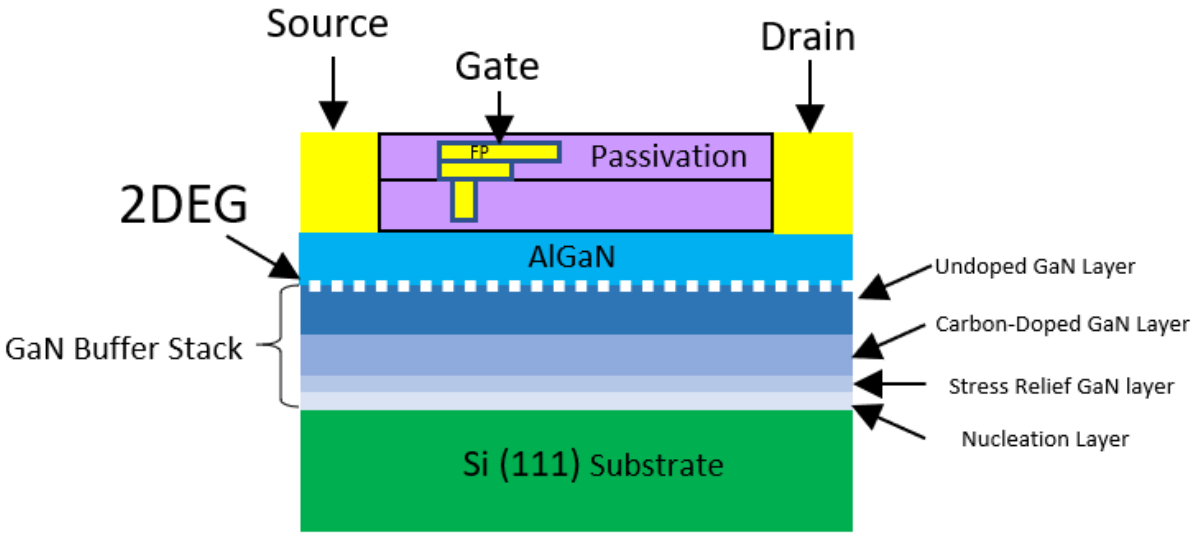


Figure 10: GaN Device Cross Section

The 2DEG is inherently a normally-on channel (D-mode), in order to turn it off a negative voltage should be applied. In power electronics switches must be normally-off devices for fail-safe and efficiency reason. Two strategies are used to realize normally off GaN HEMT (Figure 11):

1. A cascode configuration with a 30V Si MOSFET and a high-voltage D-mode GaN HEMT inside a single package.

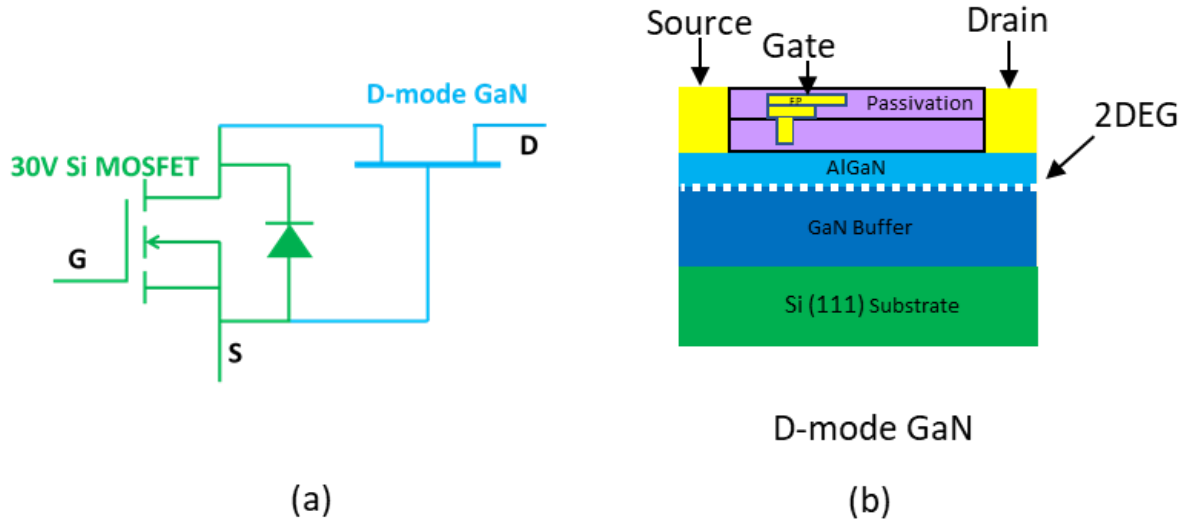


Figure 11: Cascode GaN-on-Si HEMT (a) Cascode GaN on Si Circuital Representation (b) D-mode HEMT Cross Section

2. Adding an additional gate structure able to deplete the 2DEG channel with zero gate bias. Today, there are two structure to realize normally-off GaN HEMT: MIS-Gan HEMT and p-GaN HEMT (Figure 12).

   - **MIS-GaN HEMT:** The AlGaN barrier layer under the gate is etched away and an isolating dielectric layer is added in order to remove positive polarization charger and suppress the leakage current respectively.

     These devices are not yet available in commerce given the fabrication process difficulty to stabilize the threshold voltage and the reliability concerns of the gate dielectric.

   - **p-GaN HEMT:** A p-n junction is created between drain and source by inserting a p-type GaN layer between the gate and the AlGaN layer.

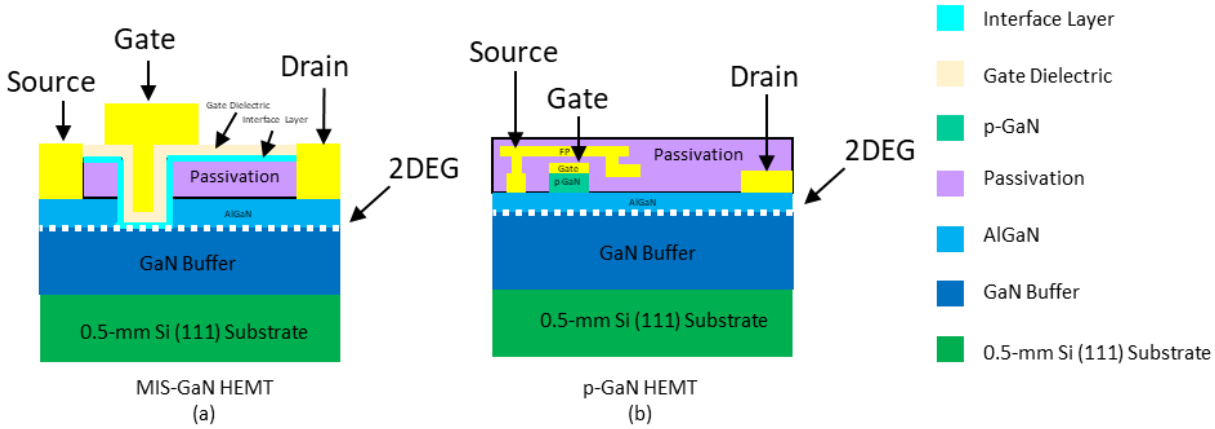


Figure 12: Cross section of E-Mode Devices (a) MIS-GaN (b) p-GaN

GaN devices are a promising technology in terms of cost and performance. In a decade it could have a similar price as Si devices thanks to scale economy and fine tuning of the production process. Currently GaN devices are in the early stages of its life cycle. The first generations were launched by Transphorm and GaN System in 2013 and 2014 respectively. Transphorm presented a D-mode GaN with a 30V Si JFET in a cascode structure while GaN System presented an E-mode GaN device. Since then, several studies have revealed a series of problems and challenges that must be solved in order to profit from the superior characteristic of GaN technology.

GaN HEMT Problems:

Dynamic on resistance $R_{DS,on}$:

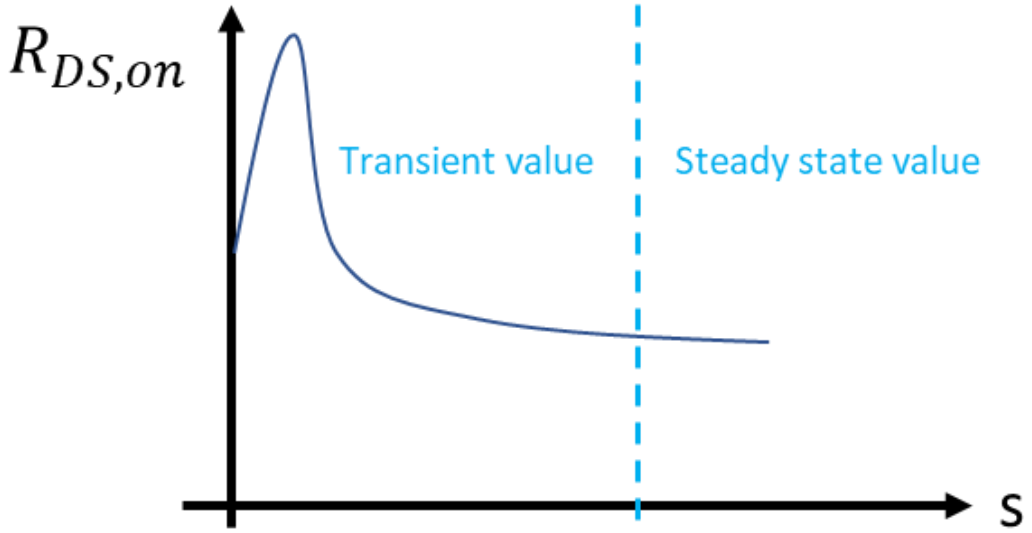


Figure 13: Dynamic $R_{DS,on}$

When the devices switch from the off-state to the on state the initial value of the $R_{DS,on}$ is considerably greater than its steady state value (Figure 13) generating transient losses that can be greater or equal to the steady state losses in conduction mode and as a consequence increasing conduction losses, junction temperature and bringing out reliability concerns.

Dynamic $R_{DS,on}$ in GaN HEMT is a hot topic in power electronics. Despite, the effort of several groups to characterize the phenomenon using a Double Pulse Test circuit with a clamping circuit to measure voltage during turn-on, to best of the author knowledge, there is not a consensus in the scientific community of the best practice to measure this phenomenon. Moreover, the dynamic $R_{DS,on}$ dependency on the time the device remain in off-state (t_b), make the characterization of the phenomenon, time consuming as the measurement should be done in steady state. Hence, Semiconductor manufacture should tackle this problem since is the main inhibitor of the widespread of GaN HEMT in commercial power applications. Undermining transient switching losses due to dynamic $R_{DS,on}$ can lead to a junction temperature higher than the one the devices is able to stand. On the other hand, overestimating transient loses due to dynamic $R_{DS,on}$ could lead to an oversized die area device and as a consequence higher cost.

In literature this phenomenon is also known as current collapse and is due to different trapping mechanism that are activated under different bias condition:

1. **Off-State Trapping**: when the device is reverse bias with a large drain to source voltage (VDS) a large electric field is generated between the drain and the gate causing electron injection from the gate and trapping at the passivation/AlGaN-barrier interface [*11*] of p-GaN- and MIS-HEMTs, and additional trapping in the gate-dielectric/AlGaN interface in MIS-HEMTs. In the meantime a large electric field is generated between the drain and the substrate inducing electrons injection from the Si substrate and trapping in both the carbon doping layer and the transition layer of the GaN buffer. In the carbon layers because impurities induce traps and in the transition layer because of the crystalline defects.

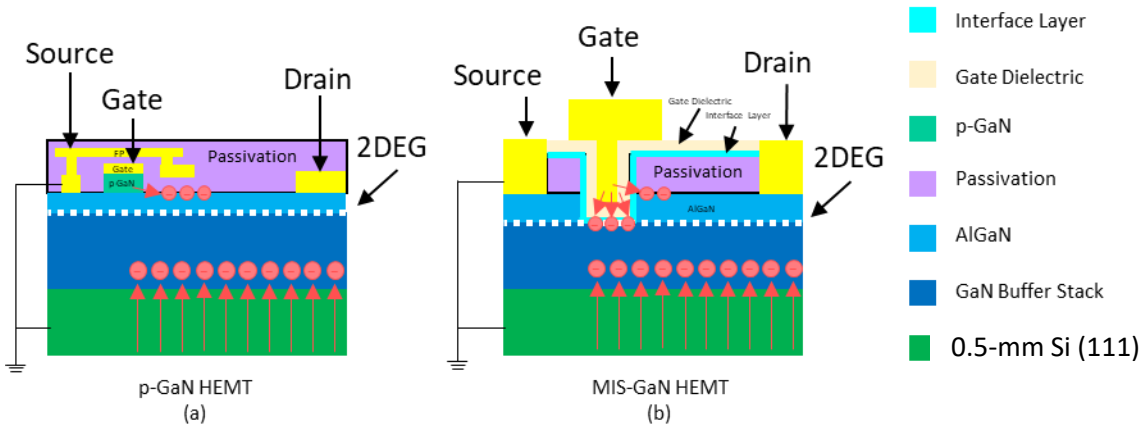


Figure 14: Off-State Trapping in E-Mode GaN

The trapped electrons depend on the blocking voltage and the time the device remains in off-state (t_b). Blocking voltage increases the number of acceptors that could be ionized and t_b increases the quantity of filled traps.

2. **Hot-Electron Trapping:** During hard switching hot electrons can be generated in the 2DEG. These electrons can be trapped in the C-doped layer, the conduction channel and the gate drain region.

Moreover, the electron trapping near the Gate region causes a positive shift of the gate voltage. Hence, there is an increased of $R_{DS,on}$, due to a reduction of the gate overdrive (Vgs-Vth).

Recently Panasonic, proposed a hybrid-drain embedded GIT structure that minimizes current collapse. This structure is a p-GaN HEMT with and additional p-GaN layer near the drain electrode, that its electrically connected to the drain. During turn-off under a high V_{DS}, p-GaN HEMT injects holes to the buffer, counteracting the electron trapping in the GaN Buffer and as consequence dynamic $R_{DS,on}$ suppressing current collapse. However, Panasonic devices are not available in commerce.

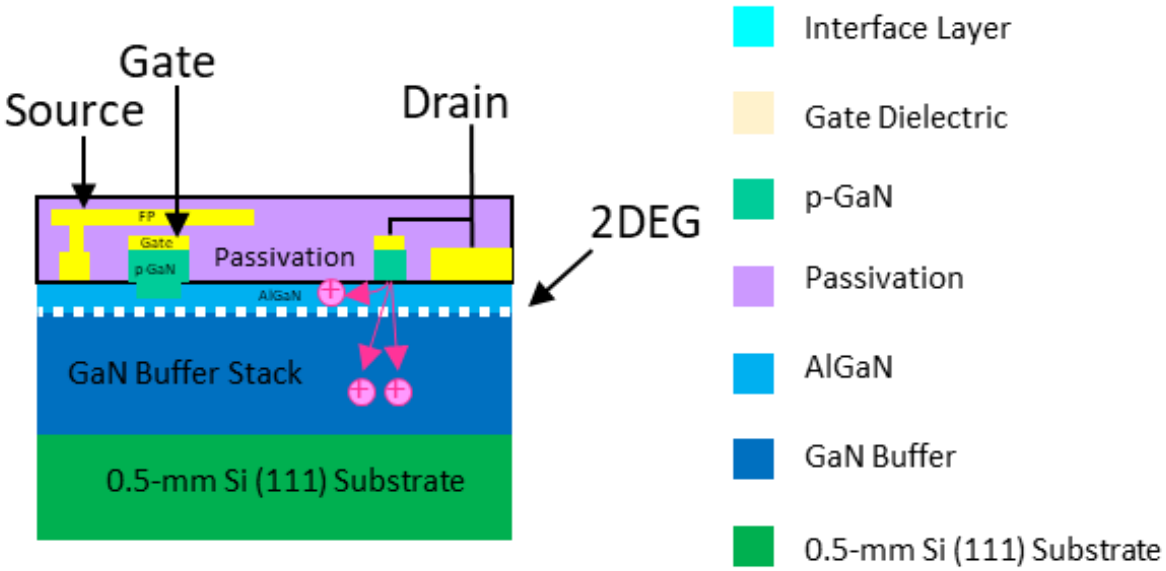


Figure 15: Panasonic E-Mode GaN HEMT Structure

Packaging:

GaN Cascode were the forerunners in the 650V range. In an attempt to provide a straightforward replacement for Si devices, they were offered in traditional packages (i.e. TO220 and T0247). These packages are easier to assemble and there are a wide variety of heat dissipation techniques inherited from Si power semiconductors. However, long lead through hole packages adds source lead parasitic inductances hindering the switching speed and creating unwanted ringing effect during commutation [*12*].

To cope with the aforementioned problems in May 2020, Transphorm introduce a QFN package, similar to the proprietary package DFN8x8 and GaNPX®-T used for E-mode device. This package has low parasitic inductance, kelvin connection and low thermal resistance. However, given the reduce footprint and scarce thermal conductivity of GaN with respect to Si and SiC devices, special attention should be paid to the thermal management.

GaN HEMT Challenge (Gate Driving):

The cascode structure has the gate threshold voltage of the silicon MOSFET and the breakdown voltage of the GaN-HEMT. Hence, commercial gate drivers for Si MOSFET are compatible.

For a cascode devices during the turn-off switching transient the gate source capacitance of the D-mode HEMT $C_{GS,HEMT}$ and the output capacitance of the Si MOS $C_{oss,Si}$ is charged in parallel with the D-MODE channel current I_{ch} until the gate source voltage of the D-MODE HEMT reaches the threshold voltage $V_{th,HEMT}$. At this point, the D-MODE HEMT is turn off and the $C_{DS,HEMT}$ is charged in series with the output capacitance of the Si MOSFET ($C_{oss,Si}$). In this last stage, the current charging the $C_{DG,HEMT}$ flows out of the devices so there is no Miller effect and it is possible to turn-off the devices as fast as possible. For the turn-on instead, since there is not a direct control of the D-Mode HEMT gate source voltage $V_{GS,HEMT}$, the slew rates of the drain current ($I_{D,HEMT}$) and drain source voltage ($V_{DS,HEMT}$) of the D-Mode HEMT are less sensible to the value of the external gate resistance. Hence, it is not possible to make an accurate nor a wide range control of the aforementioned slopes. Given that the turn-on switching losses are higher than the turn-off losses, cascode devices are suitable for Zero Voltage Switching applications (ZVS) where it is possible to exploit both the characteristics of the device and the simplicity of the gate driver.

On the other hand, the gate drive design in E-mode GaN is a daunting task, since the gate voltage Safe Operation Area (SOA) is limited. The driving voltage level are very close to the gate breakdown voltage, so a voltage overshoot or parasitic ringing may easily cause device failure. Moreover, as already discussed, the threshold instability can reduce the gate overdrive.

Nowadays gate drivers for 650V E-mode HEMT are limited in commerce (Table 2).

Manufacturer	MODEL	Datasheet	Comment
Infineon	1EDF5673F	[*13*]	Devices oriented for Infineon CoolGaN devices
Silicon Labs	Si8271	[*14*]	
Analog Devices	ADuM4120	[*15*]	

Table 2: 650 E-mode GaN Commercial Drivers

Hence, Si and SiC gate drivers are usually adapted to respect the gate voltage SOA [*16*], increasing the gate driver complexity, cost and gate loop inductance. Additionally, the performance of the semiconductors is hindered by the Si/SiC driver characteristics and the auxiliary components needed by the driver (e.g. Bootstrap- and Dsaturate-diode).

Moreover, there are some driving challenges for both cascode and E-Mode GaN devices:

- GaN devices lateral structure symmetry enables reverse conduction. A voltage applied between gate and drain higher that the threshold voltage (V_{th}) can turn on the device. That is, if $V_{GS} + V_{SD} = V_{GD} > V_{th}$ the device starts to conduct in the third quadrant. Voltage drop in reverse conduction is considerably higher than Si and SiC MOSFET. Hence, especial attention should be paid to gate drive dead times.

- Delay matching of the gate signals in a Half-Bridge configuration

- The low parasitic capacitance (C_G and C_{GD}) increments the sensitivity to dV/dt . An accurate control of dV/dt is a must to avoid failures and minimize switching losses.

There is a need for integrated gate driver to reduce the gate driver inductance loop, maximize power density, increase noise immunity and be able to switch at higher frequency.

Vertical GaN devices are essential to cope the lack of avalanche capability, voltage-rate and current-rate limitation of lateral GaN-on-Si power devices. Moreover, a vertical GaN structure does not have trapping problems that can induce dynamic $R_{DS,on}$ and have a better thermal conductivity

Today GaN bulk substrate cost is the main obstacle for the development of this technology. The wafer cost of GaN-on-GaN is $\$60 - \$100/cm^2$ while the cost for a 4-inche SiC wafer is (~\$8/cm^2) and 8-inche GaN-on-Si is (~\$1/ cm^2) [*17*].

The scientific community together with GaN manufacturers should resolve the aforementioned problems to prove the reliability of GaN devices. Though there are already automotive graded devices in market, the reliability risk continues to be superior to its performance benefits. Hence, currently GaN devices are not used in the mass market. Given the inherent non-avalanche rated of GaN HEMT research should focus in the process and development of vertical devices.

2.2 Active Area vs Switching and Conductions Losses

For power semiconductors there is a trade-off between switching and conduction losses that is regulated by the active area of the device. For a given switching frequency there is an optimum die size that minimizes the overall losses of the device. Given that the active are is an unknow variable for designers, the forward voltage of Diodes V_f and the $R_{DS_{on}}$ of MOSFET (which are proportional to the device active area) ; are used instead as the reference variables for device selection.

In the past equation (1) was used as a first order approximation of this trade-off between conduction and switching losses for Si MOSFETs in hard switching application.

$$P_T = I_{DS}^2 R_{DS,on} + \frac{1}{2} C_{E,eq}(V_{rr}) V_{rr}^2 F_{sw} \quad (1)$$

Where:

P_T: Total power losses

I_{DS} : Drain to source Current

$R_{DS,on}$: On Resistance

$C_{E,eq}$: Energy equivalent capacitance

V_{rr}: Reverse bias voltage

F_{sw}: Switching Frequency

The optimum area A_{opt} of the device is located in the point where the overall losses P_T are minimum $P_{T,min}$ (Figure 16)

1.

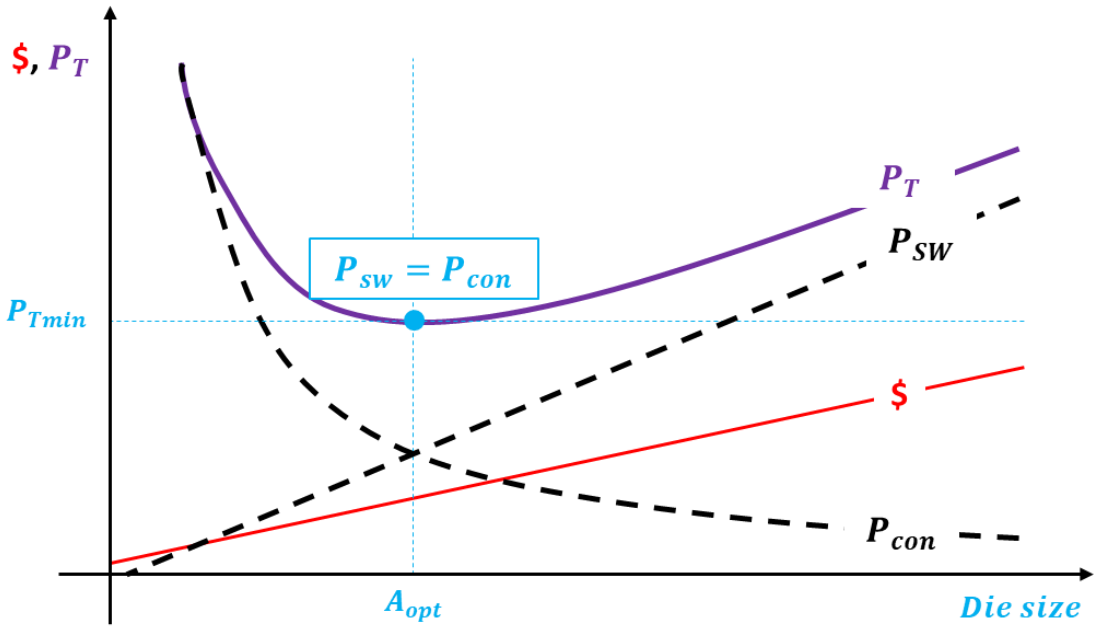


Figure 16: Trade-off between conduction losses (Pcon) and switching losses (Psw) in hard switching at a given F_{sw}

Equation (1) is dated, it neglects switching losses during commutation, it does not account for the thermal capabilities of the semiconductor, it is not applicable for rectifiers and is not able to account for the different switching speeds Si devices can have. Today event driven circuit simulation software like PLECS and PSIM are used to make a more accurate assessment of losses under different operation conditions using look-up tables of the power loss of the devices. Given that simulations can be time consuming, it is important to limit the potential candidates by a correct screening.

The first step of screening consists in using first order approximation (an analytical formula to derive the current rate/nominal current $I_{D,nominal}$ the device should have. Historically devices $I_{D,nominal}$ in datasheets have been determine by equations (2) and (3).

$$I_{D,nominal}^2 V_F \mathrm{R_{TH,jc}} = \mathrm{T}_{j,max} - \mathrm{T_{j,case}} \quad (2)$$

$$I_{D,nominal}^2 \mathrm{R_{DS,on}} \mathrm{R_{TH,jc}} = \mathrm{T}_{j,max} - \mathrm{T_{j,case}} \quad (3)$$

Where:

$\mathrm{R_{TH,jc}}$: is the junction to case thermal resistance of the device.
V_F: Forward voltage at nominal current $I_{D,nominal}$ and $T_j = 25°C$
$\mathrm{R_{DS,on}}$: On resistance at $T_j = 25°C$

In this case $I_{D,nominal}$ is an indicative number, since equation (2),(3) neglects switching losses. However, for WBG devices equations (2),(3) become more accurate as recovery losses are one order of magnitude smaller for SiC devices or zero for GaN devices. Thought the standard convention is to find $I_{D,nominal}$ with a $\mathrm{T_{j,case}}$ of 25°C, sometimes $I_{D,nominal}$ is reported with respect to a different $\mathrm{T_{j,case}}$ value, that at first sight could be misleading. Therefore, it is important to check if $I_{D,nominal}$ is reported with respect to $\mathrm{T_{j,case}} = 25°C$, otherwise use equation (2) and (3) to find it for the potential candidates.

2.3 Hard Switching Semiconductor Losses

In the 1200V range it is clear that SiC devices outperform Si components. The only reason to choose Si over SiC in this range is in cost sensitive application where either there is a switching frequency constraint or it is not possible to significantly increase the switching frequency to reduce the volume and cost of the passive components.

In this case Si technology have several advantages:

- Minimize semiconductor cost
- Minimize gate driver cost and complexity: Given that there are more gate drivers variety for Si MOSFETs, it is possible to choose a driver that matches exactly the needs of the applications without having to expend more money in additional features that are not require by the application and usually require additional auxiliary components.

On the other hand, in the 600V-900V range SiC and GaN devices should compete with Si SJ MOSFET technology. In order to make a one-to-one comparison between Si, SiC and GaN technologies, devices with similar $R_{DS,on}$ and similar package should be used; to guarantee similar power rating, thermal resistance $R_{TH,jc}$ and switching cell layout. Given that today SiC and GaN devices catalog is limited, comparing commercial devices with different semiconductor technologies becomes a blurred task

In any case, in order to make a proper selection of semiconductors it's compulsory to use a semiconductor loss model able to account for all the parameters in Table 1.

In literature several loss models have been proposed to assess power semiconductors losses.

There are three types of loss models for power semiconductors:

Physical Models: They are accurate but they are time consuming and require the device geometry, doping profile, etc. Therefore, they are not used for power converter design

Behavioral Models: They are SPICE models provided by the device manufacture. They are useful for the gate driver design, since designers can explore the effects of changing the gate resistance or gate drive voltage value. However, they are not practical for simulating an entire converter since the small step simulation time. Moreover, the model is valid under certain commutation condition. Since, the device vendors don't specify the aforementioned conditions, power loss studies of semiconductors devices cannot be done with this model.

Analytical model: Based on physical equation. They have an excellent trade-off between accuracy and complexity.

Up to 2010 the analytical piecewise linear loss models [18], [19] were the most popular model to estimate semiconductor power losses because they were simple and able to satisfy the accuracy requirements of the time. With the introduction of WBG semiconductors it's necessary to have a more accurate model able to account for the non-linearities of the junction capacitance, the stray inductances, the gate driver, etc. Given that for WBG, VSG are used, in this section the analytical loss model presented in [3] will be used to enlighten how each factor in Table 1 contributes to the switching performance of Si, SiC and GaN devices, highlighting the benefits and falls of each technology.

In this section components reported in Table 3 will be used to explore the hard-switching characteristics of semiconductor devices.

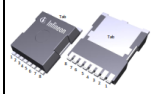
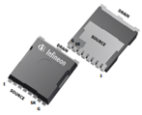
	Infineon IPW65R065C7	Infineon IPT65R075CFD7	ROHM SCT3080ALHR	Cree C3M0060065J	Infineon IGT60R070D1	Gan Systems GS66508B
Package	TO247 	HSOF-8 	TO247 	D2PACK 	GaNPX® 	HSOF-8-3 
V_{DS}	700V	650V	650V	650V	600V	650V
ID Continuous Tcase=25°C	33A	33A	30A	31A	31A	30A
R_{DSon} (Tj=25°C)	65mΩ	61mΩ	80mΩ	60mΩ	70mΩ	50mΩ
R_{DSon}	138mΩ @ VGS=10V,ID=17.1 A,Tj=150°C	138mΩ @ VGS=10V,ID=11.4A, Tj=150°C	115mΩ @ 150°C	80mΩ @ V_{GS} =15V , I_D = 13.2 A, T_J=175°C	100mΩ @ I_D=8A I_G = 26.1 mA T_J=150°C	129mΩ @ I_{DS}=9A T_J=125°C
Input Capacitance C_{iss}	3020pf @ V_{GS}=0V,V_{DS}=400V,f =250kHz	2103pF @ V_{GS}=0V,V_{DS}=400V,f= 250kHz	571pF @ V_{GS}=0V,V_{DS}=500V,f= 1MHz	1020pF @ V_{GS}=0V,V_{DS}=600V,f =1MHz Vac=25mV	380pf @ VGS = 0 V; VDS = 400 V; f = 1 MHz	242pf @ Vds=400V Vgs=0 f=100kHz
Output Capacitance C_{oss}	48pf @ V_{GS}=0V,V_{DS}=400V, f=250kHz	40pF @ V_{GS}=0V,V_{DS}=400V ,f=250kHz	39pF @ V_{GS}=0V,V_{DS}=500V ,f=1MHz	80pF @ V_{GS}=0V,V_{DS}=600V ,f=1MHz Vac=25mV	72pf @ VGS = 0 V; VDS = 400 V; f = 1 MHz	65pF @ VDS=400V VGS=0 F=100kHz
Reverse Revoery Charge Qrr	64nC	0.51µC @ Vr=400V If=11.0A dIf/dt=100A/us	53nC @ If=10A Vr=300V didt=1100A/us	62nC @ V_{GS} = -4 V, I_D = 13.2 A, VR=400V, dI_F/dt = 2300 A/µs, TJ = 175 °C	0nC	0nC
Total Gate Charge QgTot	64nC	51nC	48nC	46nC @ V_{DS}=400V, V_{GS}=-4 V/15 V I_D = 13.2 A	5.8nC @ I_{GS}=0 to 10mA; V_{DS}= 400 V; I_D= 8 A	6.1nC V_{DS}=400V V_{GS}=0 to 6V
Thermal Resitance (Junction-to-Case) R_{THJC}	0.73°C/W	0.67°C/W	0.86°C/W	1.1°C/W	1°C/W	0.5°C/W
Gate to source voltage	-20V to 20V	-20V to 20V	0V to 18V	-4V/15V recommended turn on/turn off	not specify	-10 to +7V
Gate-to Souce Threshold	3.5V	1.2V	2.7V to 5.6V	2.3V	1.2V @ 25°C and 1V @ 125°C	1.7V
Gate Plateau Voltage	5.4V	5.5V	7V to 11V (not flat miller plateau)	from 7V to 8V (not flat miller plateau)	1.7V	3V
Internal Gate Resistance Rg	0.85Ω	8Ω	13Ω	3Ω @ f = 1 MHz, VAC = 25 mV	0.78Ω	1.1Ω
Transient tolerant gate drive	-30V to 30V	-30V to 30V	-4V to +26V	-8V/+19V	not specify	-20V/+10V
Operating Junction Temperature	0.85°C	-55°C to 150°C	-55°C to 175°C	-40°C to 175°C	-55°C to +150°C	-55°C to +150°C
	Max Diode didt 60A/us	Max Diode Didt 1300A/us				

Table 3: 700V-600V 30A-33A MOSFETs

Figure 17 shows a half bridge switching cell, with the stray inductance and parasitic capacitance of the semiconductors, the stray inductance of the circuit layout and a voltage gate driver, that will be used to explain semiconductor commutation.

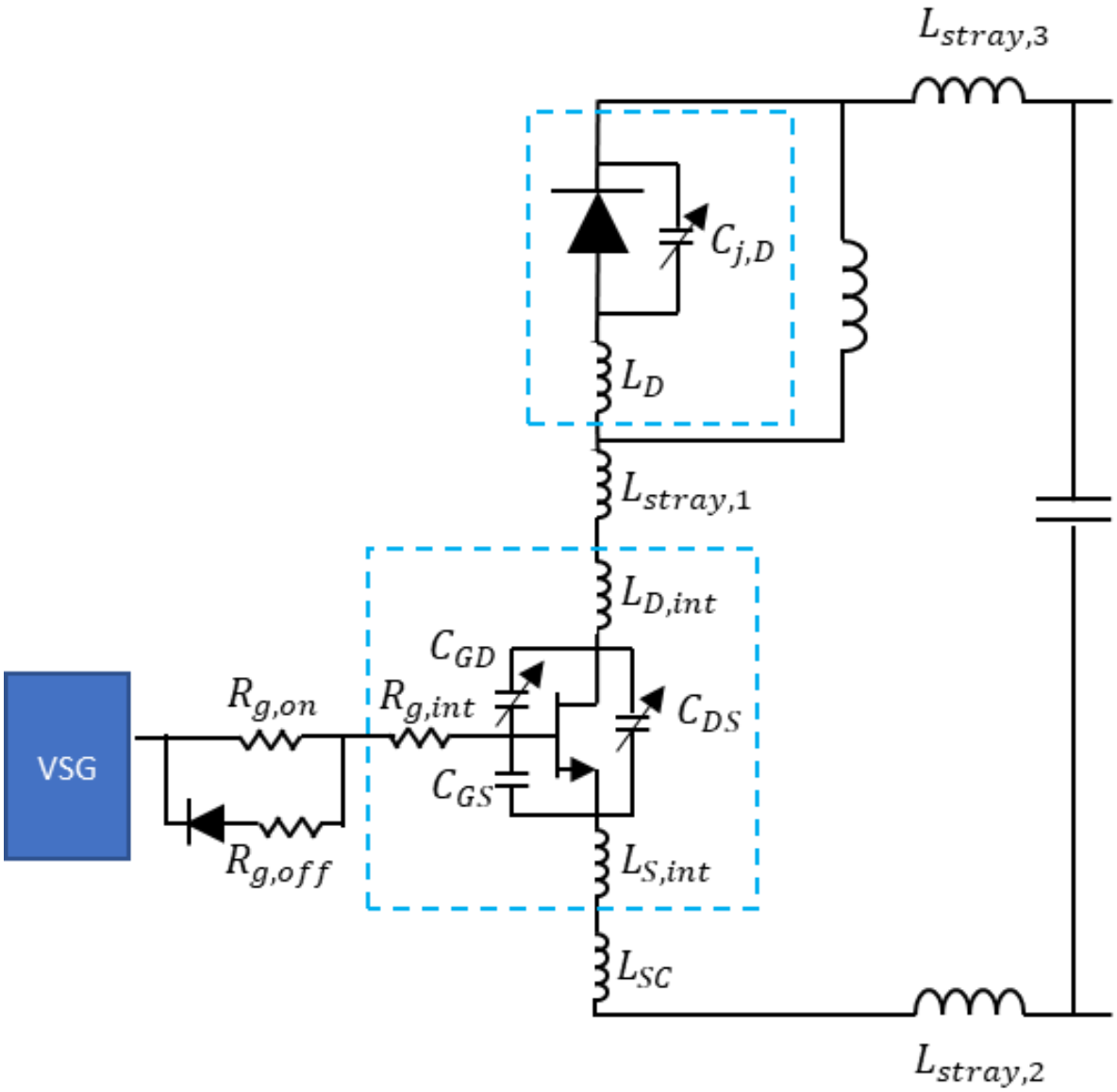


Figure 17: Half-Bridge Switching Cell made of diode and a switch

Turn-On Losses

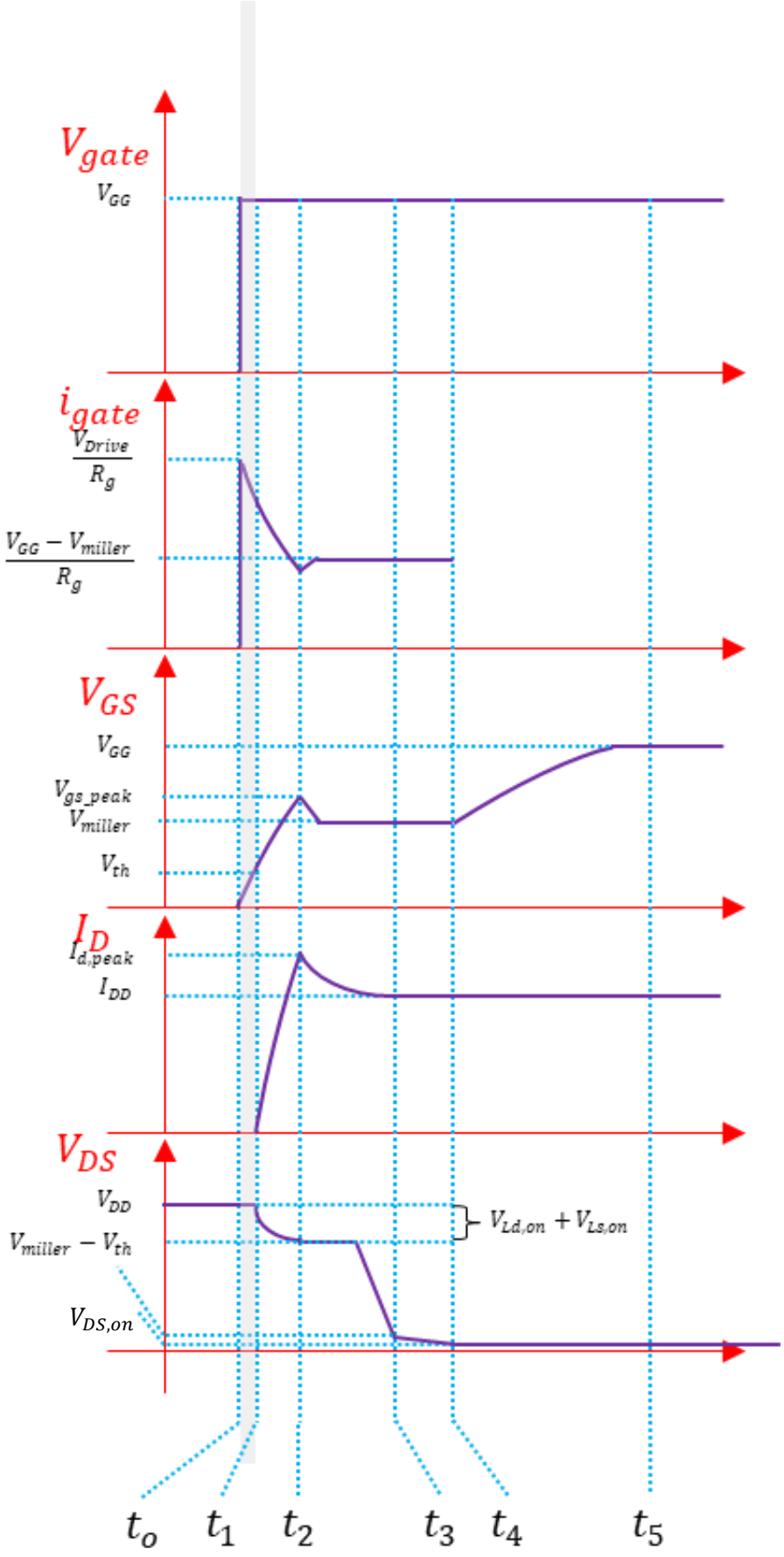


Figure 18: Low Side Switch Turn-On in a Half-Bridge

The turn-on switching interval of the low side components in a half bridge switching cell can be divided in 5 intervals.

t_0 to t_1 interval: “turn-on delay interval”

Switch is in cut-off region. At t=0 The driver voltage rises from 0 to V_{GG} and the gate source voltage V_{GS} rises following equation (4) until it reaches V_{th}

$$V_{GS}(t) = V_{GG}[1 - e^{-\frac{t-t_0}{\tau_{iss}}}] \quad (4)$$

Where $T_{iss} = [R_{gate} + R_{g,int}][C_{GS} + C_{GD}] = [R_{gate} + R_{g,int}] * C_{iss}$.

Despite the potential positive V_{th} shift of GaN HEMT, dead time is very small compare to Si and SiC MOSFET, given that both C_{iss} and Rgate are very small. For SiC MOSFETs, special attention should be paid to the $R_{g,int}$,given that some devices like Rohm SCT3080ALHR reported in table 2 have a high value, that could limit the amount of current injected to Ciss and as a consequence increment significantly the dead time with respect to Si and GaN components. Finally, Si SJ MOSFET have the longest dead time due to the high C_{iss} (Figure 19).

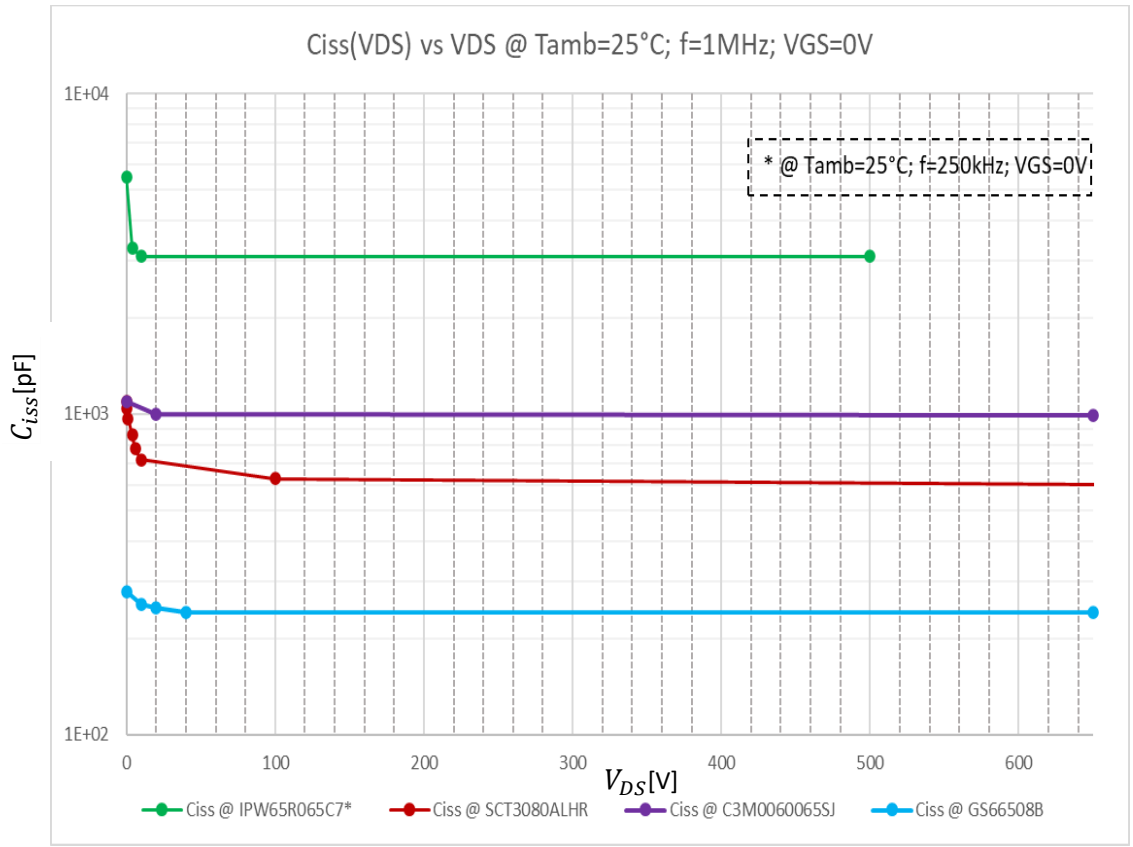


Figure 19: Input Capacitance of the devices reported in Table 3

At t_0 the gate driver should be able to source a peak current equal to $V_{gg}/(R_{gate} + R_{g,int})$.

t_1 to t_2 interval:

At t_1 diode enters saturation region, V_{GS} follows equation (6) until V_{GS} reaches $V_{plateau}$

$$V_{gs}(t) = V_{GG} - \frac{V_{GG} - V_{th}}{\tau_a - \tau_b}\left[\tau_a e^{-\frac{t-t1}{\tau_a}} - \tau_b e^{-\frac{t-t1}{\tau_b}}\right] \quad (5)$$

Where

	$\tau_n = [R_{gate} + R_{g,int}][C_{GD} + C_{GS}] + g_f[L_{s,int} + L_{SC}]$ $= [R_{gate} + R_{g,int}]C_{iss} + g_f[L_{s,int} + L_{SC}]$		(6)
	$\tau_m^2 = [R_{gate} + R_{g,int}]C_{GD}(V_{DS}) * g_f[L_D + L_{stray} + L_{Dint} + L_{Sint} + L_{SC}]$		
	$\tau_a = (\tau_n + \sqrt{\tau_n^2 - 4\tau_m^2}/2$	$\tau_b = (\tau_n - \sqrt{\tau_n^2 - 4\tau_m^2}/2$	

Meanwhile MOSFET drain current I_D start to increase following equation (7)

$$I_D(t) = g_f[v_{GS}(t) - V_{th}] \quad (7)$$

Where g_f is the transconductance of the MOSFET defined as

$$g_f(V_{GS}, V_{DS}, Tj) = \left.\frac{dI_D}{dV_{GS}}\right|_{V_{DS}} \quad (8)$$

Transconductance is a function of V_{GS}, V_{DS} and Tj. As V_{DS} increases g_f increases due to drain-induced barrier lowering (DIBL). Traditionally g_f is derived from the $I_D - V_{DS}$ characteristics of the devices measured with a curve tracer where the maximum V_{DS} is limited to 20V to avoid DUT self-heating during measurement. In [*20*] a double pulsed circuit is proposed to derive the $g_f|_{V_{DS}}$ characteristic for SiC MOSFETs at

high-voltage and high-current . However [*20*] is limited for devices with flat plateau regions hence it cannot be used with most of SiC MOSFET which have a non-flat plateau. Despite everything, $g_f|_{V_{DS=20V}}$ measured with a curve tracer and reported in device datasheet is a good starting point to consider switching losses and screen Si, SiC and GaN components even though there will be difference between the analytical and real switching waveforms.

In datasheets the $g_f(V_{GS}, V_{DS} = 20V, Tj)$ can be derived as the slope of the $I_D - V_{GS}$ characteristics (Figure 20) of the devices at a given VGS and T_j.

From the following figure (Figure 20), it can be seen that all the devices except GaN-HEMT GS66508B g_f have a positive thermal coefficient. Moreover, it can be seen that SJ MOSFET have a higher transconductance with respect to SiC devices.

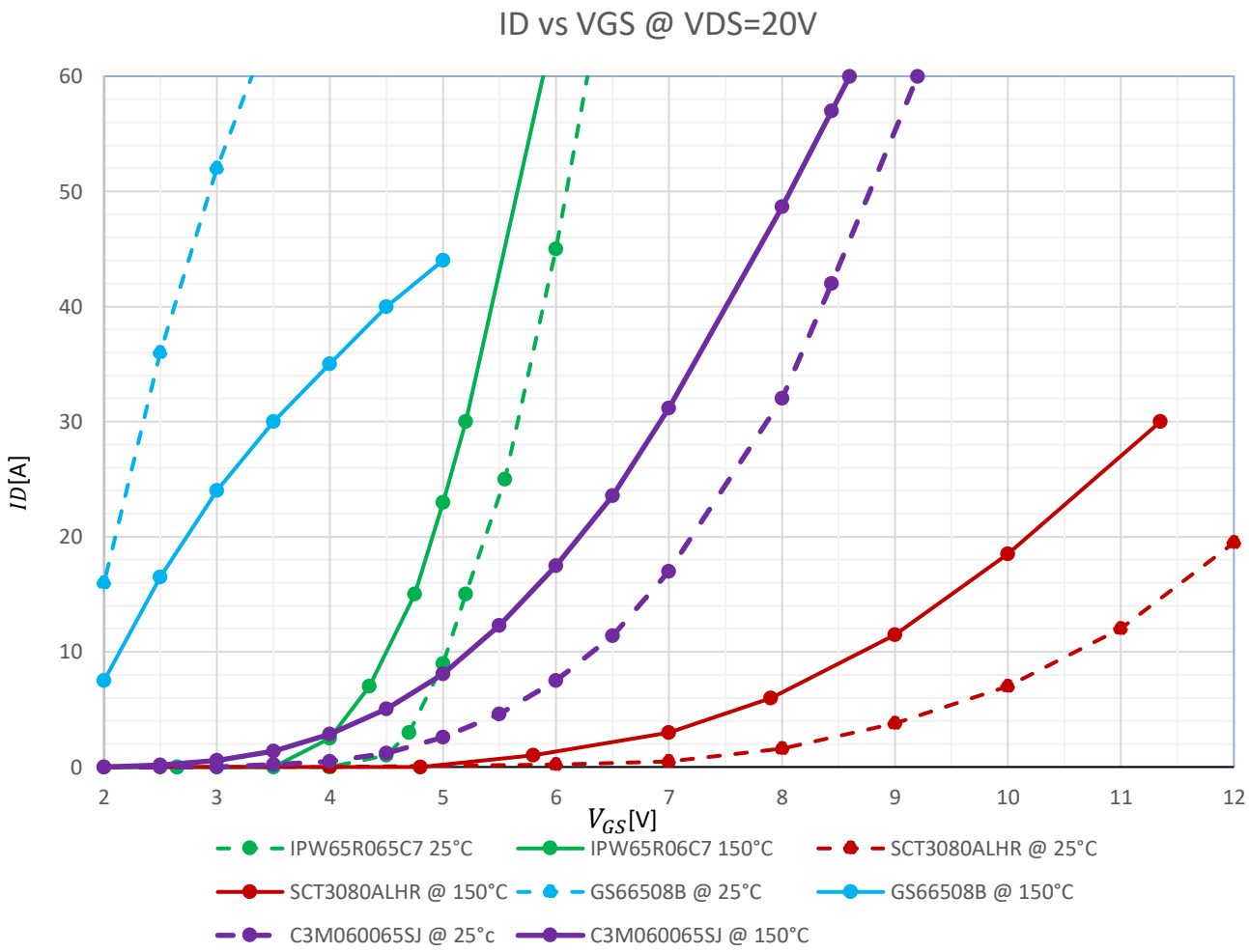


Figure 20: ID-VGS characteristics of devices reported in Table 3

After V_{GS} reached $V_{plateau}$, if the complementary component in the Half-Bridge is made of Si or SiC, its reverse recovery will make V_{GS} rise till a peak value $\widehat{V_{GS}}$ at t2 where the low side switch experiences its maximum current $\widehat{I_D}$ due to the maximum reverse current of the high side device I_{RM} (9).

$$\widehat{V_{GS}} = \frac{\widehat{I_D}}{gf} + V_{th} \tag{9}$$

In the meantime, at t_1 as the current start to rise, there is a voltage drop $\Delta V(t) = [L_D + L_{stray} + L_{Dint} + L_{Sint} + L_{SC}]dI(t)/dt$. Hence during t_1 to t_2 period $V_{DS} = V_{GG} - \Delta V$. This point in time, is helpful when performing electrical measures of the switching power losses as a reference point to correct potential skew problems between current and voltage waveforms.

t_2 to t_3 interval: Voltage Falling Interval

If the complementary component is a Si or SiC device at t_2 both I_D and V_{GS} fall until they reach I_{DD} and $V_{plateau}$ respectively. For SiC MOSFETs with non-flat plateau region V_{GS} will fall from $\widehat{V_{GS}}$ at t_2 till it reaches its maximum value in the plateau region. In both case V_{GS} follows equation (10).

$$V_{GS}(t) = \frac{i_{ch}}{g_f} + Vth = \widehat{V_{GS}} + \frac{1}{gf}\left[\frac{d\mathrm{I_D}(t)}{dt}[t - t_2] - \left[C_{OSS} + C_f\right]\frac{dV_{DS}(t)}{dt}\right] \tag{10}$$

Given that in this case the half-bridge is made of a switch and a diode in (10) C_f is the junction capacitance of the diode. In case the half-bridge was made by two switches C_f will be replaced with the C_{oss} of the complementary device.

During this time interval V_{DS} falls from V_{DD} at t_2 to $V_{plateau}$ at t_3 following equation (11)

$$\frac{dV_{DS}}{dt} = -\frac{V_{GG} - V_{plateau}}{[R_{gate} + Rg, int]C_{rss}} \quad (11)$$

Given that C_{rss} depends on V_{DS} (Figure 21) , in order to make a more accurate prediction of the voltage waveform the techniques presented in [*21*] [*22*] will be used for devices with flat and not-flat plateau regions respectively.

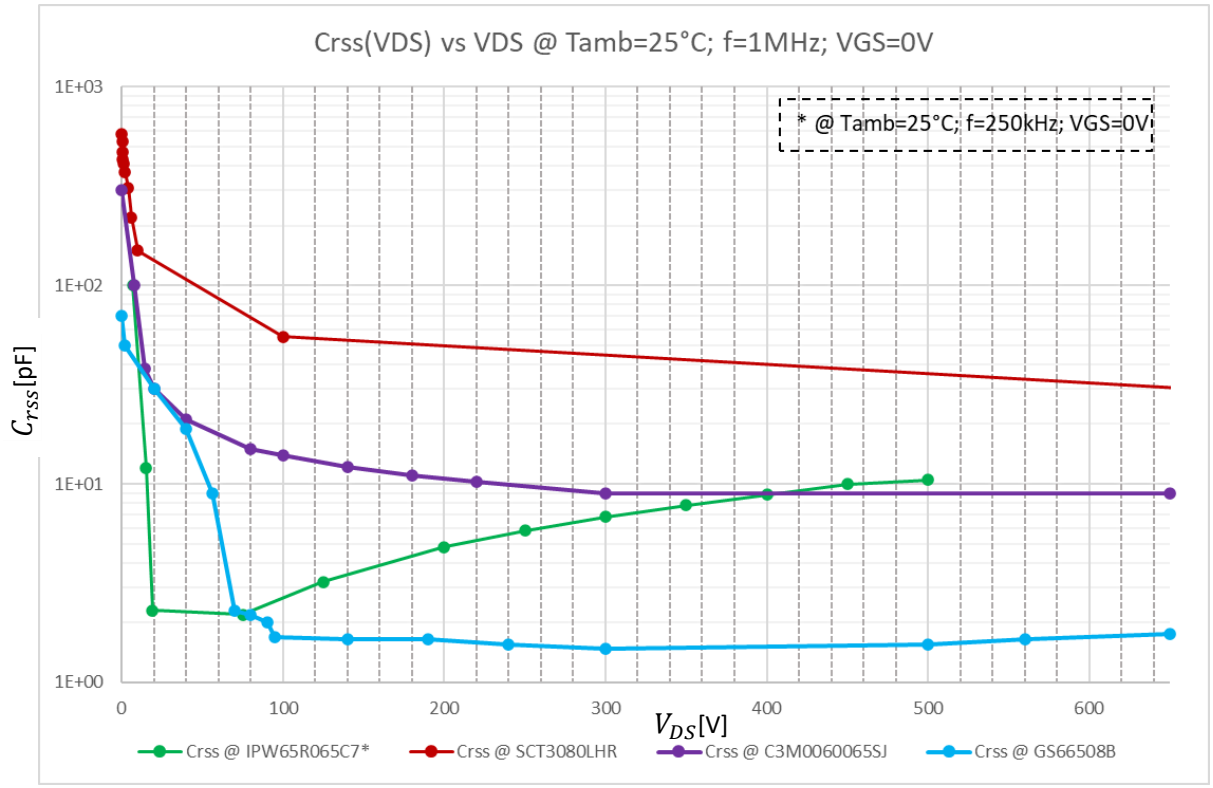


Figure 21: C_{rss} characteristics of devices reported in Table 3

t_3 to t_4 interval:

At t_3 the device enters the ohmic region given that $V_{DS} = V_{GS} - Vth$. From t_3 to t_4 V_{DS} decreases following equation (11) and the techniques in [*21*] [*22*] until it reaches V_{DS} at t_4.

Turn-Off Losses

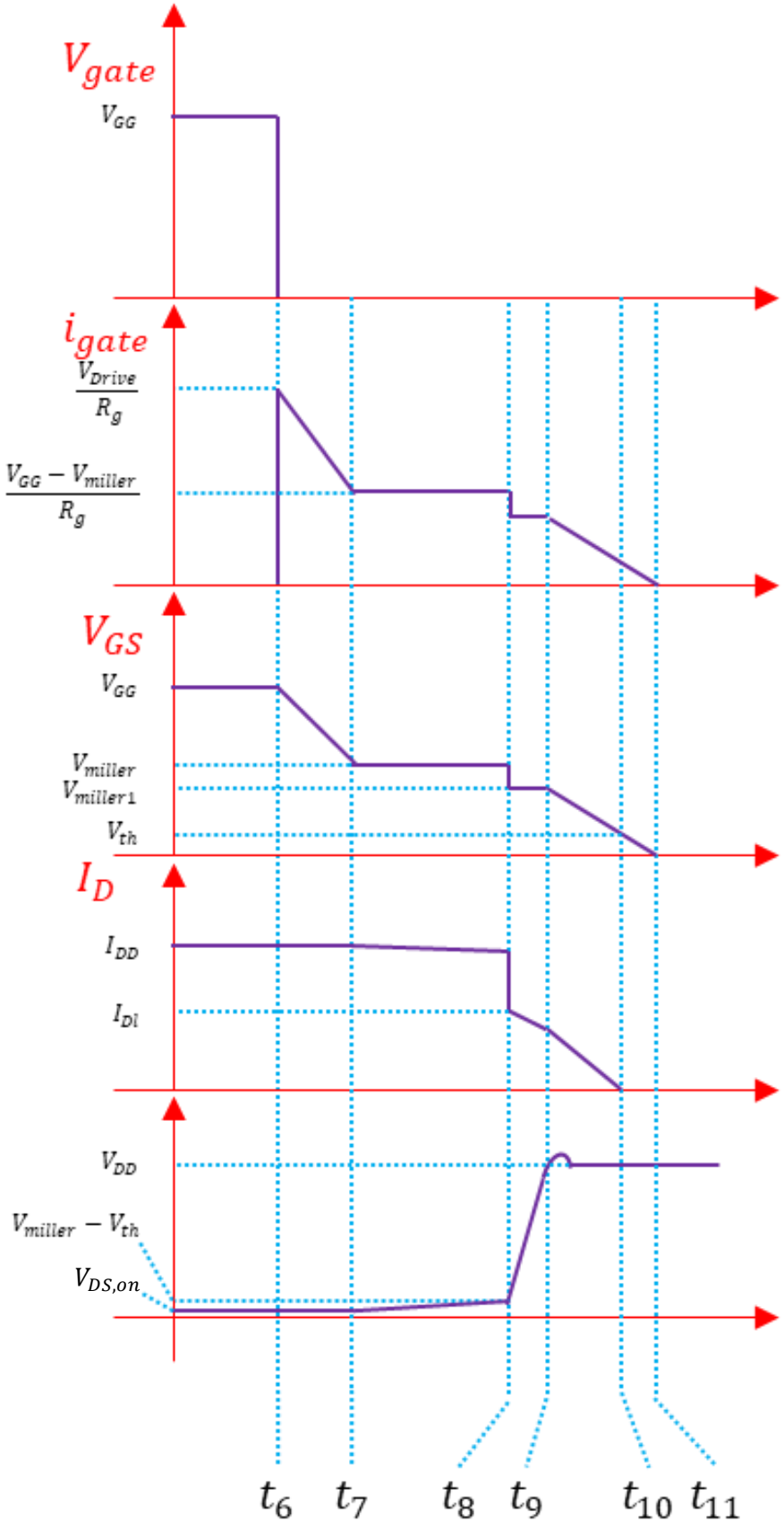


Figure 22: Low Side Switch Turn-Off in a Half-Bridge

2.5 Device Characterization

Currently, power converter efficiency standard is over 94% in 85% of the working conditions. Though the power loss model presented in the last section can be useful to screen components, it is not accurate enough to appreciate small difference in the overall efficiency of a power converter due to small changes in the parameters in Table 1. Hence, it is compulsory to use a test bench that replicated the switching cell present in the converter to assess losses and make a fine tuning of the first 3 parameters in Table 1 that enable to find the optimum tradeoff between minimum losses and contain electromagnetic emissions.

The Test bench can used either an electrical method like Double Pulse Test (DPT) or Calorimetric methods [*23*] to assess losses. Table 4 report the advantages and drawbacks of each methodology.

Switching Losses Methods:	
Electric Method: DPT	**Calorimetric Method:**
Using the circuit presented in Figure 17, two pulses are generated at the gate driver. The first pulse is used to measure the switching turn-off losses in the falling edge of the pulse setting the desire current through the devices under test by changing the width of this pulse. The second pulse instead, is used to measure the turn-on losses on the low-side device in the rising edge, therefor is very short compare to the first pulse.	Calorimetric losses enable to measure the device under test total losses by measuring the dissipated heat by the component. Then by making and assessment of the junction temperature and the conduction losses it is possible to extract the total switching losses.
Advantages: -It is possible to study the transient voltage and current waveform in order to detect faulty conditions like current/voltage ripple and voltage overshoot. -Enables to optimize the gate driver circuit in order two have an optimum $\partial I_{DS}/\partial t$ and $\partial V_{DS}/\partial t$ that enables to	Advantages: -Accuracy -It does not have a bandwidth limitation

reduce switching losses without creating excessive EMI interference.	
Disadvantages: -It cannot be used for wide bandgap devices because of the bandwidth limitation of current probes, oscilloscope and current sensors.	Disadvantages: -Not possible two study the transient voltage and current. -It is time consuming, since it requires to arrive to thermal stationary state in order to make the switching loss measurement. -Its more complex, since it requires an accurate thermal model in order two estimate the junction temperature of the device.

Table 4: Double Pulse Test vs Calorimetric Methods

In the case of electrical methods Table 1 resume the publications that state the best practice and the theorical background necessary to build the most common switching cells for device characterization.

Reference	Topic	Comment
[*24*]	Current shunts	Characterization and limitations
[*25*]	Fixing T_j case for the power loss measurement	
[*26*]	Difference between Half Bridge, T-type and NPC switching cell	Theorical explanation of the difference between switching cells
[*27*]	(Half Bridge) Double Pulse Test Best Practice	
[*28*][*29*]	T-type test bench	
[*30*]	NPC test bench	

Table 5: Publications related to power loss measurements with an electric method

Moreover, from the V_f and $R_{DS,on}$ measured data at different temperatures, it is possible to estimate the temperature coefficient from V_f or $R_{DS,on}$ (12).

$$\frac{\partial V_f(i_D, T_j)}{\partial T_j} \qquad \frac{\partial R_{DS,on}(i_{DS}, T_j, V_{gate})}{\partial T_j} \tag{12}$$

This number quantified the sensibility of the V_f or $R_{DS,on}$ to temperature.

2.6 Thermal Model and Heat Sinks

The junction temperature T_j of semiconductor devices is an important parameter. The reliability and the lifetime of the component depend on T_j. Moreover both P_{cond} and P_{sw} depend on Tj.

In order to accurately assess the thermal resistance of the heatsink computational fluid dynamics (CFD) simulation should be run in conjunction with a thermal model or a thermal study of the converter in the worst-case condition should be perform. Since CFD simulation are time consuming, the thermal study is usually preferred.

A simplified RC lumped element thermal model is usually used to evaluate the T_j of components (Figure 23).

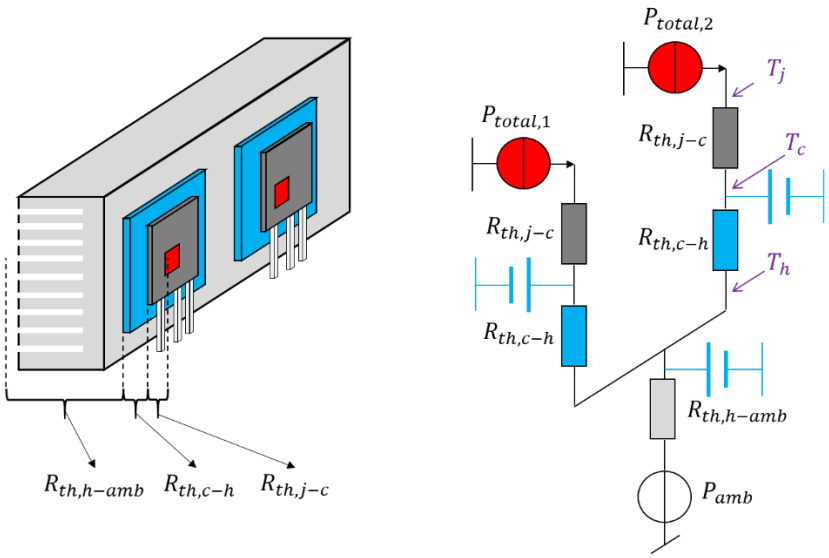


Figure 23: Thermal Circuit

In the equivalent thermal circuits current sources represent the overall power dissipated by each component (e.g. Ptotal,1 and Ptotal,2) while the voltage source the ambient temperature (P_{amb}). The thermal resistance is the ration between the temperature difference between two nodes and the power flowing through the interface between the two nodes. The thermal capacitors in conjunctions with the thermal resistance form the thermal impedance, that describes the transient behavior of the temperature of each node of the thermal circuit.

Semiconductor Thermal Impedance:

The semiconductors thermal impedance is reported in the datasheets either as a RC lumped model or in a graphical way [31]. In the second case the RC model should be found by curve fitting.

Insulation material thermal resistance:

The thermal interface resistance between the components case and the heatsink is:

$$R_{th,c-hs} = \frac{\sigma_{th,c-hs}}{A_{th,c-hs}} \tag{13}$$

Where $\sigma_{th,c-hs}$ is the thermal impedance of the isolation material and $A_{th,c-hs}$ is the area of the thermal interface.

Heat Sink thermal impedance:

The thermal impedance of the heat sink depends on several factors mainly the geometry of the circuit, if there is natural or forced convection and the air flow dynamics inside the converter enclosure.

In steady state the junction temperature of a component x is defined as:

$$T_{j,x} = R_{th,j-c,x} * P_{tot,x} + R_{th,c-hs,x} * \sum_{t=1}^{N} P_{tot,t} + R_{th,hs-amb} * \sum_{l=1}^{M} P_{tot,l} + Tamb \tag{14}$$

Where N are the number of components sharing the same case and M is the number of components placed in the same heatsink. $R_{th,j-c,x}$, $R_{th,c-hs,x}$, $R_{th,hs-amb}$ are the junction to case, case to heatsink and heatsink to ambient thermal resistance.

2.7 Optimization algorithm for Semiconductors and Heatsink

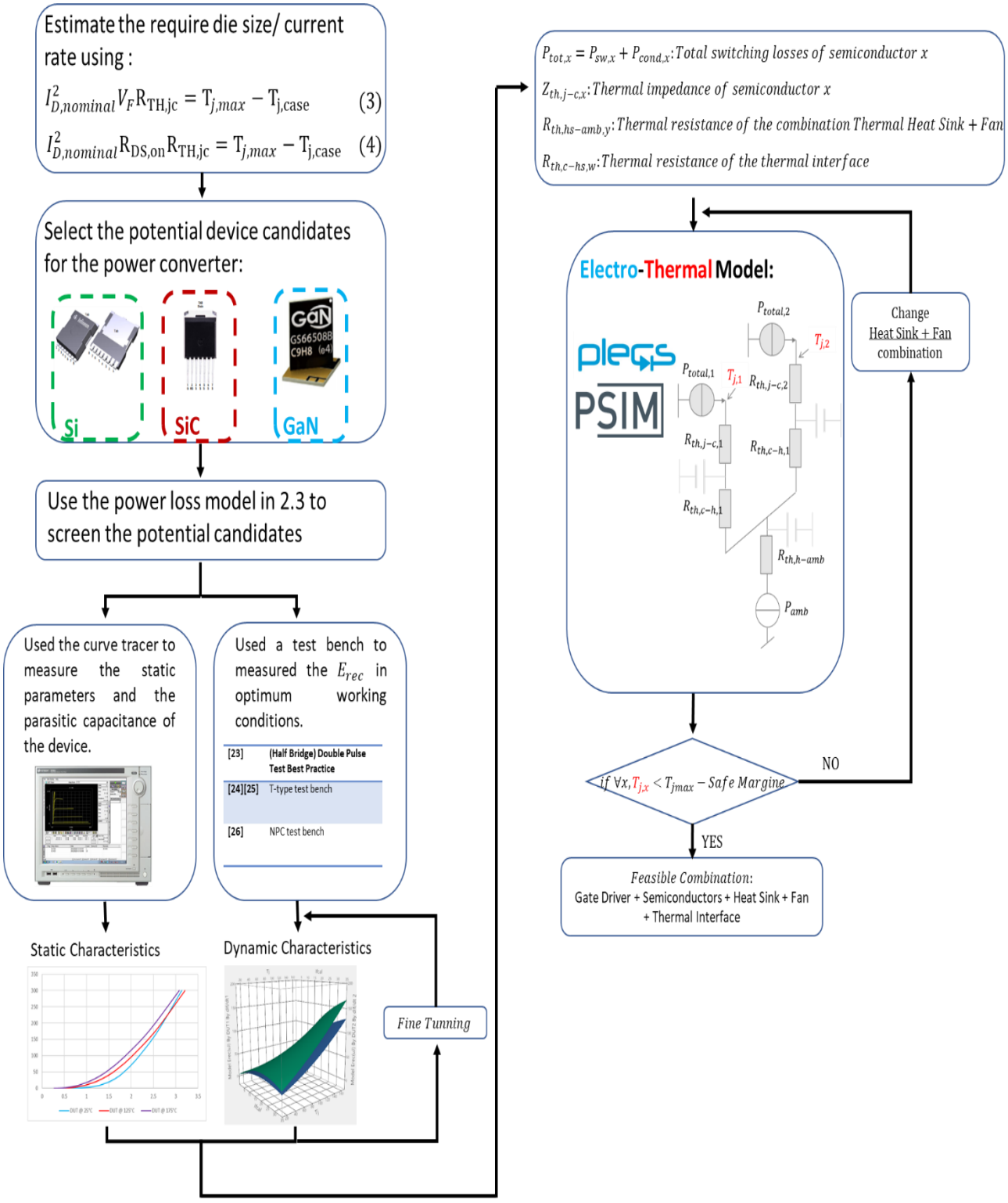


Figure 24: Semiconductor and Heatsink Optimization

For the electro-thermal model, conduction and switching losses can be estimated using PLECS or PSIM. In these programs conduction and switching losses are calculated as follow.

Conduction Losses

- Diodes conduction losses can be calculated with

$$P_{cond}\left(i_D(t), T_j\right) = \frac{1}{T}\int_0^T V_f\left(i_D(t), T_j\right) * i_f(t)dt \qquad (15)$$

  Where I_f is the forward current and V_f is the forward voltage which depends on both I_f and the junction temperature T_j.

- For MOSFETs, conduction losses can be calculated with

$$P_{cond}\left(i_D(t), T_j, V_{gate}\right) = \frac{1}{T}\int_0^T R_{DS,on}\left(i_{DS}(t), T_j, V_{gate}\right) * i_{DS}^2(t)dt \qquad (16)$$

  where I_{DS} is the drain source voltage and the on resistance $R_{DS,on}$ is defined as:

$$R_{DS,on}\left(i_{DS}, T_j, V_{gate}\right) = \frac{\partial V_{DS}(i_{DS}, T_j, V_{gate})}{\partial i_{DS}} \qquad (17)$$

  Where V_{gate} is the gate voltage.

Switching Losses:

$$P_{sw}\left(I_{on}, I_{off}, V_{on}, V_{off}, T_j, V_{Gate,on}, V_{Gate,off}, R_{Gate,on}, R_{Gate,off}\right) = \frac{1}{T} * [\sum_{1}^{N_{sw,on}} E_{on}(I_{on,i}, V_{on,i}, T_j, V_{Gate,on}, R_{Gate,on}) + \sum_{1}^{N_{sw,off}} E_{off}(I_{off,i}, V_{off,i}, T_j, V_{Gate,off}, R_{Gate,off})] \qquad (18)$$

Where $N_{sw,on}$ and $N_{sw,off}$ stands for the total turn-on and turn-off switching transition in a period T respectively. E_{on} and E_{off} are look up tables of the turn-on and turn-off dissipated power where:

I_{on} and I_{off} are the currents prior to the turn-on and turn-off commutation respectively. V_{on} and V_{off} are the on and off voltage of the devices respectively. Finally, $V_{Gate,i}$ and $R_{Gate,i}$ are the gate voltage and the gate resistance for either the on or off commutation. The latter two variables control the gate current I_{gate} but most importantly the $\partial I_{DS}/\partial t$ and $\partial V_{DS}/\partial t$ during commutation.

Final Remark:

Given that processing the static and dynamic characteristics measurements of the device is time consuming and could easily induced errors if its not done in a standard way. An Excel Add-In was developed in order to process measurements, construct a semiconductor database and generate automatic graphs as the ones presented in *Figure 3* and *Figure 7* that enable to speed up the semiconductor selection process and components benchmarking campaigns. However, due to confidentiality agreements with Vishay Italiana Spa, I did not attach this software as a complementary file to this thesis.

3 Passive Components

3.1 Inductors and Transformers

Inductors and transformers provide two main features for power converters:

- the possibility to shape either the input or output current
- isolation between the input and output side of the converter

Their design presents several challenges:

- Microscopic phenomenon's inside magnetic materials are not fully understood by the scientific community
- The geometry of the core introduces several non-linearities.
  - Gaps cause fringing effects that modify the external magnetic field inside the windings.
  - The magnetic flux inside the core is non-homogeneous and changes with the geometry of the core and the winding arrangement.
- As the frequency of power converters tends to increase in order to reduce the weight and volume of magnetic components, different phenomenon's inside the magnetic cores and the winding arrangements exasperate, increasing losses. For example, eddy current in the winding cause skin and proximity effects that cause a non-uniform distribution of the current inside the windings.
- Desktop computers are not able to run 3D simulations of transformers and inductors due to their complexity and the amount of memory required. Typically, when used, 2D simplified FEM models are implemented. However, this simulation cannot be applied to transformers with litz wire windings

In order to deal with these problems several analytical models and empirical models have been formulated to describe the behavior of magnetic component. These models can be classified in reluctance models, power loss models and thermal models. In this chapter the most relevant analytical and empirical models for reluctance and power loss models will be presented. The thermal model will not be

consider in this chapter as the McLyman empirical equation [*32*] for the temperature rise (19) have an optimum tradeoff between simplicity and accuracy.

$$\Delta T = 450 \left(\frac{P_{core} + P_{wires}}{A_t} \right)^{0.826} \tag{19}$$

Where A_t is the outer inductor surface in square centimeters.

Finally, a design algorithm for inductor and transformer design will be presented.

3.1.1 Reluctance Models

The reluctance models are a magnetic circuit that represents either an Inductor or Transformer. A reluctance model describes the behavior of the magnetic flux inside the winding based on the core material properties, the core geometry, the winding arrangement and the current waveform that travels through the windings of the magnetic component. Its main function are stated in Table 6

Inductor	Transformer
Inductance Calculation	Magnetization Inductance L_m
Flux Density control $B_{max} < B_{sat}$	Leakage Inductance L_{lk}
	Flux Density control $B_{max} < B_{sat}$

Table 6: Goals of reluctance models for inductors and transformers

The core and air gap are represented by a reluctance R defined as $R = \frac{MMF}{\phi}$ where ϕ is the magnetic flux through the reluctance R and MMF is the Magneto Motive Force across the reluctance R. Moreover windings are represent by a MMF equal to the current flowing around the core.

Analogous to Kirchhoff's law for voltage and current in electrical circuits, in magnetic circuits Ampere's law for MMF and Gauss Law for the Magnetic flux can be applied to simplify the circuit.

Figure 25 shows a reluctance model of two EE cores Inductor with the winding in the center leg

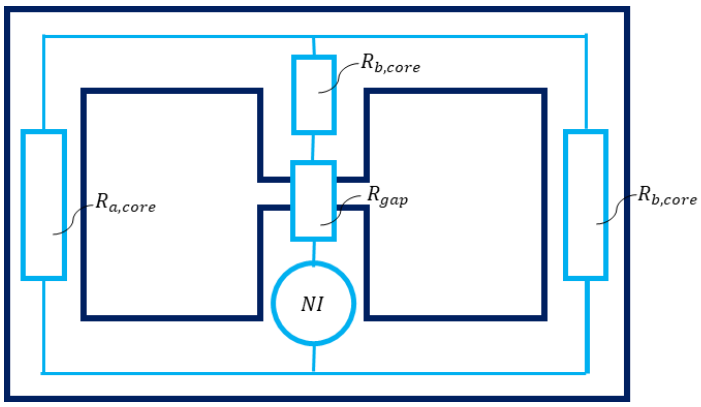


Figure 25: Magnetic circuit of an EE core transformer with the winding in the central leg

The Magnetomotive Force NI represent the winding, where N is the number of turns and I the current flowing through the winding.

The reluctance for each section of the core can be evaluated as

$$R_{i,core} = \frac{l_i}{\mu_r \mu_0 A_c} \tag{20}$$

Where

l_i : length of the segment I of the core

μ_0 : permeability of air

μ_r : relative permeability of the core

A_c : cross sectional area of the segment i of the core

Due to fringing fields, equation (20) cannot be applied to evaluate the reluctance of airgaps. In the following section the two most popular methods in literature two evaluate the air gap of reluctance are introduced.

3.1.2 Air Gap Reluctance Evaluation

Conventional Method:

To account the fringing field in air gaps the first method [*33*] increases the cross sectional area of the core in the x and y direction by the length of the magnetic gap lg. If a core has a width a and depth b equation (20) becomes

$$R_{gap} = \frac{l_g}{\mu_o (a + l_g)(b + l_g)} \tag{21}$$

Method based on Schwarz-Christoffel Transformation:

In [*34*] Muhlethaler based on Schwarz-Christoffel Transformation [*35*] proposed the following method for the evaluation of the air gap reluctance.

1st Divide the air gap in two orthogonal planes (ie. xz plane and yz plane)

2nd For each plane evaluate the reluctance using the criteria illustrated in Figure 26

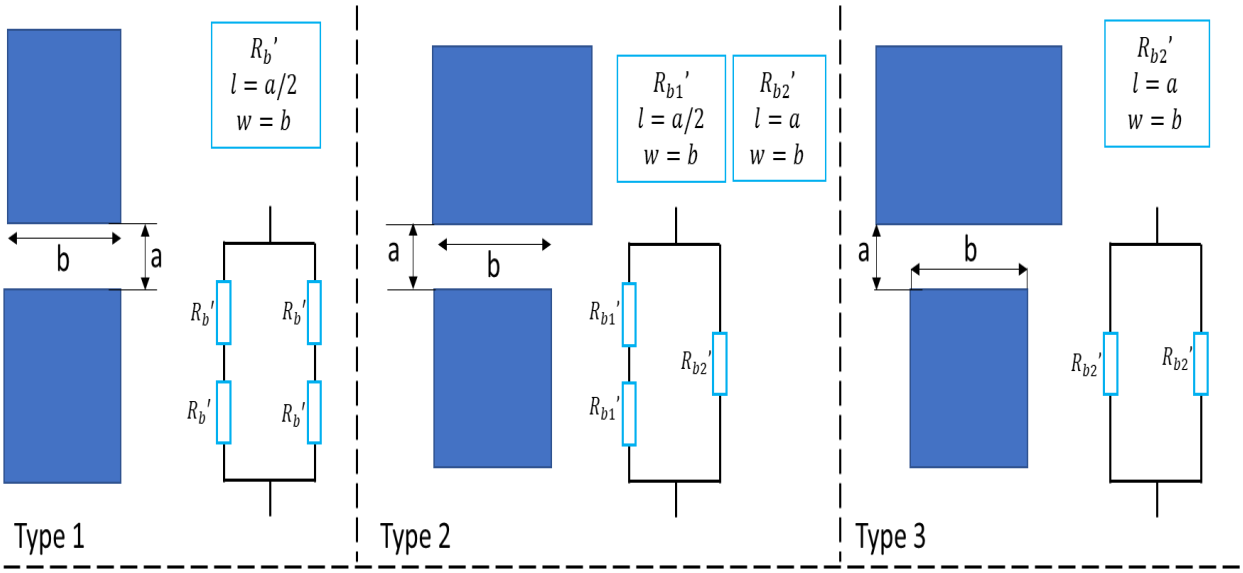


Figure 26 Air Gap classification and their corresponding reluctance models. Figure taken from [34].

Where

$$R'_{bi} = \frac{l_{gap}}{\mu_o[\frac{w}{2l} + \frac{2}{\pi}(1 + \ln\left(\frac{\pi h}{4}\right)]} \quad (22)$$

With h equal to the distance from the air gap to next core corner

3rd Calculate the fringing coefficients σ_x and σ_y

$$\sigma_x = \frac{R'_{xz}}{\frac{a}{\mu_o t}} \qquad \sigma_y = \frac{R'_{yz}}{\frac{a}{\mu_o t}} \quad (23)$$

Where R'_{xz} and R'_{yz} are the equivalent reluctance of the air gap in xz plane and yz plane respectively calculated in the previous step.

4th the 3D reluctance of the fringing factor equals

$$R_{m,airgap} = \sigma_x \sigma_y \frac{l_{gap}}{\mu A_c} \tag{24}$$

3.1.3 Power Loss Models

Power Losses in magnetic components are due to losses in the core and the windings.

There are 3 types of core losses

- Hysteresis Losses
- Eddy-Current Losses: they depend on the conductivity and the geometry of the core.
- Residual losses: Losses related to relaxation effect (i.e. when $\frac{dB(t)}{dt} = 0$)

On the other hand, winding losses are due to

- conduction losses
- eddy currents
  - skin effect
  - proximity effect.

3.1.3.1 Core Losses

In order to cope with the lack of understanding of microscopic phenomenon's in magnetic material, several empirical methods have been proposed to evaluate core losses.

The first empirical model for core losses was proposed by Charles Proteus Steinmetz in 1892 [*36*]. He proposed the following formula for the power loss per volume P_v due to hysteresis losses

$$P_v = \eta \hat{B}^b \tag{25}$$

Where η and b are empirical parameters determined by measurements and $\hat{B}_m$ is the peak magnetic flux density.

Later, a similar formula that take into account the frequency dependency of P_v was introduced and named after Steinmetz.

$$P_v = k f^{\alpha} \hat{B}^{\beta} \tag{26}$$

Where k, α and β are known as Steinmetz parameters. These coefficients are extrapolated from a parametric study of the power density of a toroidal inductor excited by a sinusoidal waveform with different values of $\hat{B}$ and f. Even though cores have different shape, a toroidal inductor is always used for characterization, given that is the only shape in which magnetic flux is approximately homogenous. In the other inductor geometries, magnetic flux tends to concentrate in the inner corners.

Based on (26) publications [*37*] [*38*] leads to the formulation of the improved Generalized Steinmetz Equation (iGSE) [*39*], that enables the calculation of core losses excited by non-sinusoidal waveforms.
In [*39*], Sullivan et al. propose and algorithm to divide the waveform in minor and mayor hysteresis loop where the losses of each loop are equal to

$$P_i = \frac{1}{T} \int_0^{Ti} k_i \left| \frac{dB(t)}{dt} \right|^{\alpha} |\Delta B|^{\beta-\alpha} dt \tag{27}$$

Where, ΔB is the peak-to-peak flux density of the minor or mayor loop, α and B are the Steinmetz Parameters and k_i is defined as:

$$k_i = \frac{K}{2\pi^{\alpha-2} \int_0^{2\pi} |cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{28}$$

Hence the total losses are a weighted sum of the losses of each loop that compose the waveform.

$$P_v = \sum_i Pi \frac{Ti}{T} \tag{29}$$

Figure 27 illustrate the processes of separation of minor and mayor loops for a boost inductor PFC.

1st the waveform must be divided in a rising and in a falling portion

2nd Following an iterative program the mayor loop and minor loop are identified.

3rd Once the major and minor loops are identified equation (27) to (29) can be applied to evaluate the overall power density losses of the core.

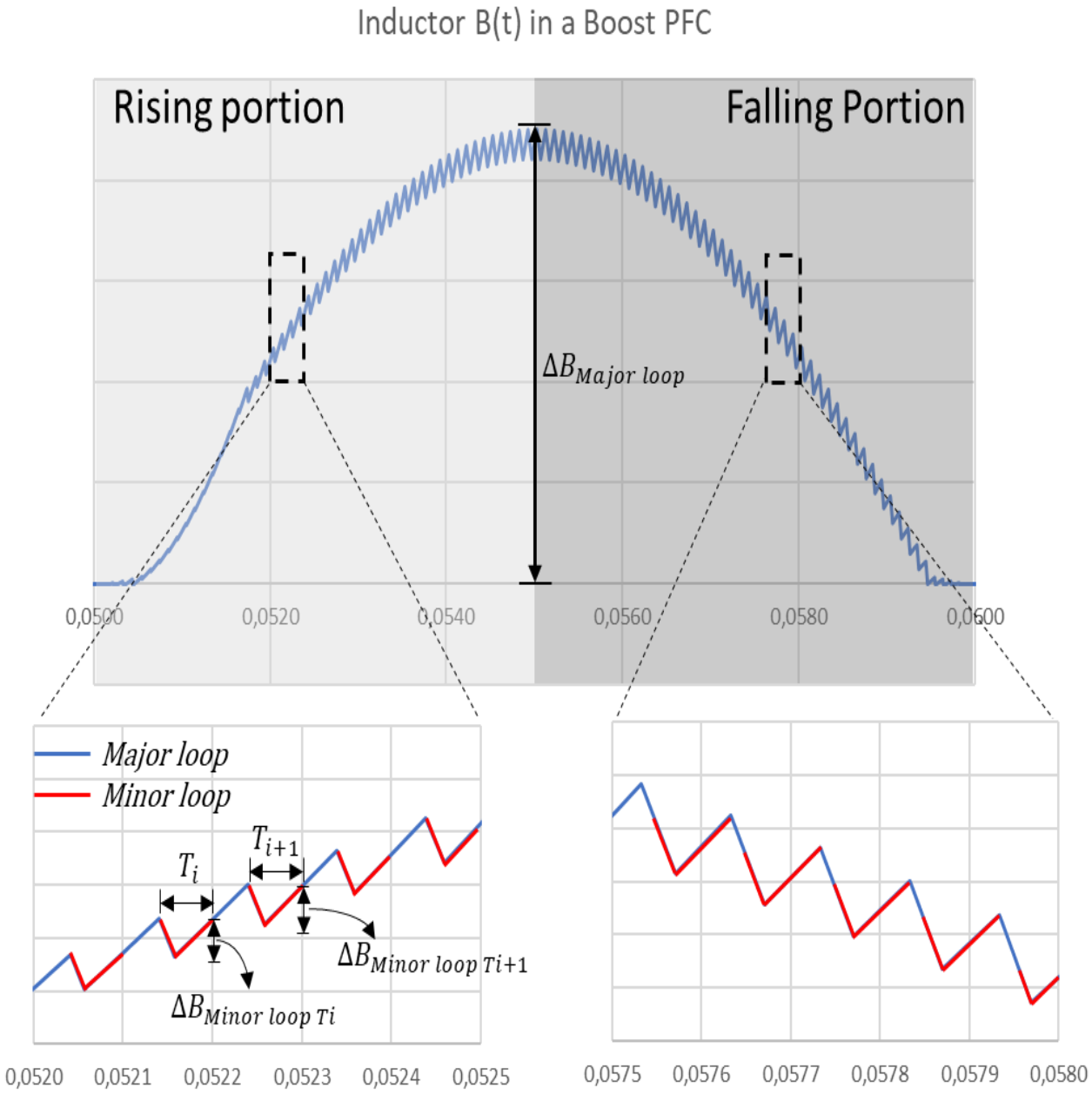


Figure 27: Major and minor loops separation for the magnetization excitation of a Boost PFC inductor

There are some cases where there is not a major loop, for example a PFC inductor working on Discontinuous conduction mode where there are only minor loops. Moreover, there are cases where there is only a major loop like in DAB, Phase Shift and LLC transformers.

Even though iGSE method does not account for pre-magnetization, DC Bias and relaxation effect, is the most popular method due to its optimum tradeoff between accuracy and simplicity.

3.1.3.2 Winding Losses

Conduction losses at low frequency can be calculated with the following equation.

$$Rdc = \frac{lMLTm}{\sigma h_w d_w} \quad \text{Square Conductor} \quad (30)$$

$$Rdc = \frac{4lMLTm}{\sigma \pi d_c^2} \quad \text{Round Conductor} \quad (31)$$

Where:

$m = Number\ of\ layers\ of\ the\ winding$

$MLT = \ Mean\ Length\ per\ Turn$

$l = Number\ of\ turns$

$h_w = Square\ Conductor\ Height)$

$d_w = \ Square\ Conductor\ thickness$

$d_c = \ Round\ Conductor\ Diameter$

$\sigma = Conductivity$

At high frequency, the winding resistance is increased due to skin and proximity effects. Skin effect cause current density to concentrate in the surface of the conductor and reduce it at the center. The distance from the surface of the conductor at which the current density decay by 1/e≈36% is the skin depth.

$$\delta = \frac{1}{\sqrt{\pi \mu \sigma f}} \tag{32}$$

Where μ and σ are the magnetic permeability and the electrical conductivity of the conductor material.

On the other hand, the proximity effect induces eddy current in the winding due to an external field that is caused by the current flowing through the near windings. The analytical formulas used to evaluate these losses are expressed in terms of

$$F_r = \frac{Rac}{Rdc} \tag{33}$$

Winding loss Calculation Methods:

Finite Element Analysis (FEA) is the most accurate method to assess winding losses due to eddy currents. It enables to consider fringing effect in gapped inductors, different core geometry and winding arrangement. However, FEA is limited by the current available computational capabilities. In order to have a good accuracy the FEA mesh size in the winding section should be smaller than the skin depth of the wire or strand diameter. Hence, FEA require a lot of time and memory. To put things in two perspective, Recently realistic simulation of a single wire where run in [*40*,*41*] showing the effect of twisting imperfections and the shielding effects inside the litz wire that have not been studied before.

Modern power converters based on SiC and GaN work at frequencies from 110kHz to the MHz. In this frequency range, is compulsory to use litz wire. Given the aforementioned limitation, litz wires are sometimes simplified by a region with uniform current density like in [*42*]. Even in this case simulation continuous to be heavy.

Therefore, several analytical methods have been formulated. They are not as accurate as FEM simulation, but enable a first order approximation of the losses in a winding arrangement in no time.

Given that analytical methods together with a fine tuning of the converter in laboratory could be more fruitful that launching time consuming FEA simulation, FEA was not pursued in this work.

Prior to explore the methods it is important to define some concepts.

Penetration factor:

$$\Delta = d_w/\delta \tag{34}$$

Where d_w is the conductor thickness; in the case of litz wire it will be the strand diameter.

This method could be applied to non-sinusoidal current waveforms, for each number of harmonics n the skin depth and the penetration ration δ change to

	$\delta' = \frac{\delta}{\sqrt{n}}$	$\Delta' = \sqrt{n}\Delta$	(35)

Dowell's Method:

Bennet and Larson [*43*] were the first to solve 1D Maxwell equation for a winding arrangement, deriving a closed form expression. However, it was Dowell [*44*] who adapted them for a foil winding in a transformer. Dowell derived an expression for the normalized resistance of the m layer of foil winding of the transformer excited by a sinusoid current waveform.

$$Fr, n = \Delta' \left[\varphi_1' + \frac{2}{3}(m^2 - 1)\varphi_2'\right] \tag{36}$$

Where ψ_1 and ψ_2 are the skin and proximity effect factor respectively

$$\varphi_1' = \frac{\sinh(2\Delta') \pm \sin(2\Delta')}{\cosh(2\Delta') - \cos(2\Delta')} \qquad \varphi_2' = \frac{\sinh(2\Delta') - \sin(\Delta')}{\cos(\Delta') \pm \cos(\Delta')} \tag{37}$$

Moreover, Dowell adapted (36) for round conductor, replacing round conductors by square-shaped conductor with equal cross-sectional area (*Figure 28*).

$$d_w = \sqrt{\frac{\pi}{4}} d_r \tag{38}$$

And introducing a porosity factor that takes account of the gaps between adjacent square-shaped conductor representation.

$$\eta = \frac{h_w}{h_c} = \frac{d_w}{p} \tag{39}$$

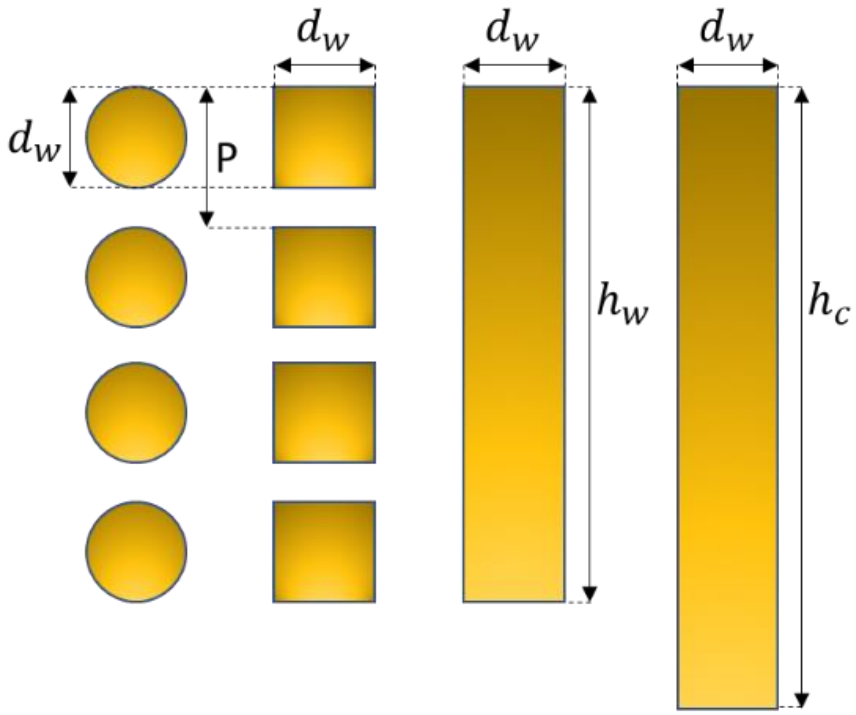


Figure 28:Dowell's conversion from round to rectangular conductors

Modifying the skin depth, the conductivity and the penetration ration

$$\delta'' = \frac{\delta'}{\sqrt{n}} \qquad \sigma' = \eta\sigma \qquad \Delta'' = \sqrt{\eta}\Delta' = \sqrt{\eta n}\Delta \tag{40}$$

The Dowell equation for round conductor is

$$Fr, n = \Delta''[\varphi_1'' + \frac{2}{3}(m^2 - 1)\varphi_2''] \quad (41)$$

This expression, enables the calculation of the winding losses due to high frequency currents.

$$P_{loss} = \sum_{n=1}^{N} F_{r,\eta} R_{dc} I_{rms}^2 \quad (42)$$

Remember that Dowell equation (36) is valid under the following assumptions.

1 Flux lines in the winding space are vertical. Hence it ignores magnetization inductance.

2 Windings are modeled as an equivalent foil of conductors

3 Winding curvature is neglected.

4 Capacitive effects are neglected

5 The magnetic field generated by a winding layer is 0 outside that winding.

Ferreira model

In [45] Ferreira make 2 remarks about the porosity factor introduced by Dowell in (41).

1. Skin depth is a physical material constant and cannot be dependent on the geometry as in [*44*]
2. In Dowell equation (36), the average current is reduced by n. Hence, according to Ampere's law the magnetic field should be reduced by the same factor. Therefore, Ferreira modified (36) to

$$Fr, n = \Delta''[\varphi_1'' + \eta^2 \frac{2}{3}(m^2 - 1)\varphi_2''] \quad (43)$$

Additionally, making similar assumptions as Dowell and considering the orthogonality between skin and proximity losses, Ferreira solve Maxwell equation in cylindrical coordinates for round wire conductors in [46] and [47].

$$Fr,n = \frac{\gamma}{2}[\tau_1 + 2\pi\frac{4(m^2-1)}{3}\tau_2] \tag{44}$$

With

$$\tau_1 = \frac{ber(\gamma)bei'(\gamma) - bei(\gamma)ber'}{ber'(\gamma)^2 + bei'(\gamma)^2} \quad \tau_2 = \frac{ber_2(\gamma)bei'(\gamma) - bei_2(\gamma)ber'}{ber'(\gamma)^2 + bei'(\gamma)^2} \tag{45}$$

Where

$$\gamma = \frac{d_r}{\delta\sqrt{2}} \tag{46}$$

In the methods presented up to now uniform distribution of the magnetic field across the conductor cross-sectional area was assumed

Kazimierczuk Initial methods

Analogues to the introduction of the porosity factor by Ferreira in (43). Kazimierczuk et al. in [48] modified Ferreira equation (44) by introducing a porosity factor η for describing losses in round wire windings.

$$Fr,n = \frac{\gamma}{2}[\tau_1 - 2\pi\eta^2\left(\frac{4(M^2-1)}{3} + 1\right)\tau_2] \tag{47}$$

Similarly, in [49] Kazimierczuk et al. based on Ferreira equation (69) introduce two porosity factors in equation (44) for Litz wire ac resistance calculation.

$$Fr,n = \frac{\gamma}{2}[\frac{1}{n_s}\tau_1 - 2\pi\left(\frac{4(M^2-1)}{3} + 1\right)n_s(\eta_1^2 + \eta_2^2\frac{p_f}{2\pi n_s}] \tag{48}$$

Where n_s, η_1 and η_2 are the number of strands in the litz wire, the external porosity factor and the internal porosity factor respectively. With

$$\eta_1 = \frac{d_s}{t_b}\sqrt{\frac{\pi}{4}} \qquad \eta_2 = \frac{d_s}{t_s}\sqrt{\frac{\pi}{4}} \tag{49}$$

tb is the distance between the centers of two adjacent Litz bundles and *ts* is the distance between the centers of two adjacent strands.

Given the complexity of the expressions (47) and (48) almost a decade later after their formulation Kazimierczuk proposed two new methods for the calculation of round wire and litz wire ac resistance in [*50*] and [*51*] respectively. In [*50*, *51*] Kazimierczuk shows that an approximation of dowels could be accurate enough to make a first order approximation of the ac resistance, making [48,49] worthless. Moreover in publications [52, 53] incongruent results were obtained when applying equation (48).

3.1.4 Optimization algorithm for Inductors and Transformers

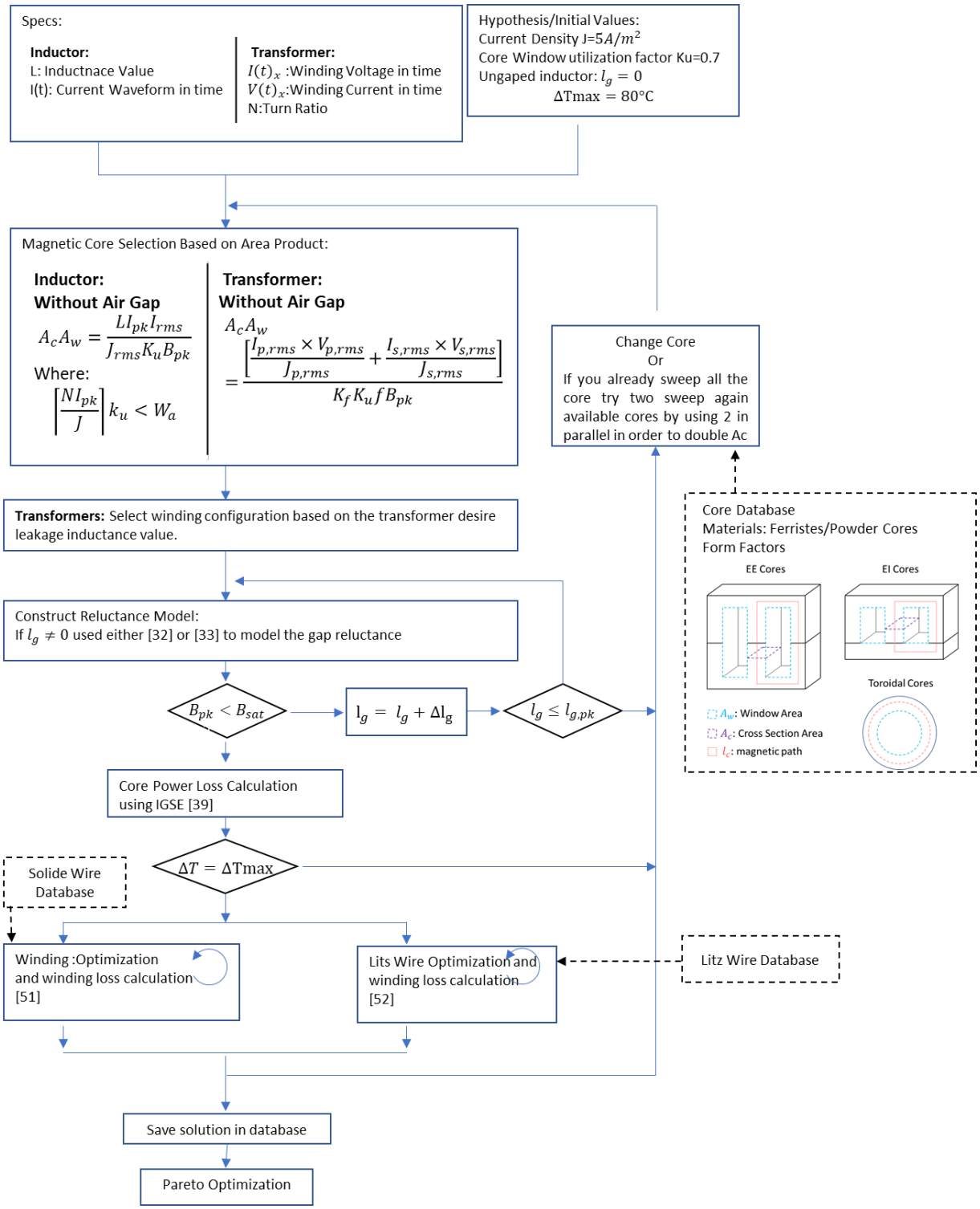


Figure 29: Inductor and Transformer Optimization

3.1.4.1 Magnetic Materials

In the past Ceramic Ferrites (Table 1) were the first choice for power converters designers due to their low cost and better performance with respect to silicon steel. However, Ceramic Ferrites have several shortcomings like low saturation flux density B_{sat} 0.2T to 0.5T , fragility and significant losses over >100kHz that can hinder their use in new power converters designs.

Mn-Zn Power Ferrites				
Name	Manufacturer	μ_r	$B_{sat100}(T)$	Fsw
3C94	Ferroxcube	2300±20%	0.38	<200kHz
R	Magnetics	2300 ± 25%	0.367	<200kHz
N97[1]	TDK	2300± 25%	0.410	<200kHz
PC95	TDK	3300±25%	0.41	<300kHz
PC50	TDK	1400±25%	0.38	300kHz-1MHz
PC200	TDK	800±25%	0.41	700kHz-4MHz

Table 7: Ceramic Ferrites

The arrival of wide band gap devices has enabled to rise the switching frequencies F_{sw} of power converters in order to reduce the size of the magnetic components. For example PFCs F_{sw} have transition from 20kHz-49kHZ for Si based PFCs to 75kHz-150 kHz for SiC based PFCs. Similarly for the DC/DC converters, resonant topologies have enabled F_{sw} in the 120kHz-500kHz range.

At high frequencies Ferromagnetic materials are a better choice due to their limited losses and higher B_{sat}, that enable higher currents through the inductor and

[1] This material was originally fabricated by EPCOS, however TDK acquire EPCOS in October 1, 2009

consequently higher power converters. Moreover, the wide choice of permittivity values of Ferromagnetic cores enables in some case to avoid airgaps (i.e. fringing flux).

Material	Name	Manufacturer	μ_r	B_{sat}
Fe-Al-Si	Kool Mμ	Magnetics	14-125	1
	Sendust	Chang Sung Corporation	26-125	1
Fe-Si	Xflux	Magnetics	26-90	1.6
	Mega Flux	Chang Sung Corporation	26-90	1.6
Fe-Ni	High Flux	Magnetics	14-160	1.5
		Chang Sung Corporation	26-160	1.5
Fe-Ni-Mo	MPP	Magnetics	14-550	0.8
	MPP	Chang Sung Corporation	14-200	0.7

Table 8: Powder Cores

3.1.4.2 Winding Arrangement

The winding arrangement have a direct impact in the leakage inductances of the transformers Figure 30

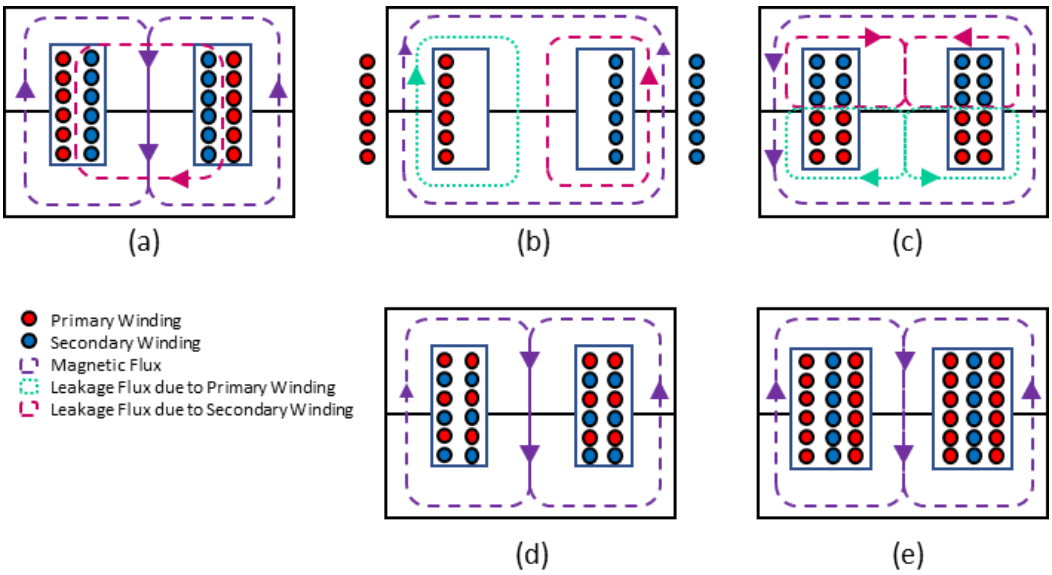


Figure 30: EE Transformer winding configuration (a) Concentric (b) External Leg (c) Split (d) Interleaved Case 1 (e) Interleaved Case 2

Each arrangement has their pros and cons

Winding Arragement	Advantages	Drawbacks
Concentric	• Simple Fabricate • Good for DAB configuration where a small leakage inductance is needed to guaranteed ZVS.	• Even though the leakage inductance is very low sometimes it could be undesirable.
External Leg	• Simple to fabricate • Good thermal properties	• Need of Finite Element Modelling for leakage inductance calculation
Split Case	• Good for LLC transformers where it is feasible to integrate the resonant inductance Lr in the transformer	
Interleaved Case 1 and 2	• Almost negligible leakage inductance • Reduce eddy power losses in the windings	• Complex Fabrication ($) •

Table 9: Advantages and drawbacks of the EE Transformer winding arrangement's

3.2 Capacitors

In general, capacitors constituted a bottleneck in terms of power density, life time and robustness. Contrary to active power devices technologies, capacitor technologies functionality is complementary. Capacitors type are selected based on the application except for power drive inverters where the DC-link is made of both Aluminum Electrolytic Capacitors and Film capacitors in order to exploit the advantages of each technology.

3.2.1 Capacitors Types

There are three types of capacitors:

Aluminum Electrolytic Capacitors (E-Caps):

They have a relative low cost and a high energy storage density. However, their inherent structure, rise concerns in term of the component lifetime as the wet dielectric tend to evaporate with time.

In Inverter application 2 factors should be considered:

- The long tunnel pit structure of anode foils tends to reduce the capacitance at frequencies over 10kHz [54]. Hence, the rated capacitance should be bigger with respect to the low frequency capacitance requirements.
- The Limited Current ripple

Multi-Layer Polypropylene Film Capacitors:

They outperform E-Caps in terms of robustness and life time due to its self-healing capabilities. Moreover, their capacitance is less susceptible to frequency than Electrolytic Capacitors and have a higher ripple current rating than E-Caps.

Multi-Layer Ceramic Capacitors:

They have a high storage energy density, but they are limited to small capacitance values due to its cost and the fragility of ceramic dielectrics.

According to IEC 60384 [55] ceramic capacitors can be classified according to the dielectric Class:

	Characteristics	Relative Permittivity ϵ_r	Application	Example
Class I	-Dielectric constant does not vary with temperature, DC-bias or capacitor wear out.	$\epsilon_r = 15 - 100$	Resonant circuits and precision circuits	NPO
Class II	-Fabricated with Ferroelectric dielectrics. -Dielectric constant varies with applied electric field []	$\epsilon_r = 2000 - 4000$	By-pass Coupling Decoupling Filtering	X7R X8R X5R X6S

Table 10: Capacitor Classification according to IEC 60384

3.2.2 Capacitors Applications

Capacitors have different functions in power converters:

- Voltage Ripple Limitation: In Power Factor Converters and grid tied inverters (e.g. Photovoltaic Inverters) the output power $P_{PFC,OUT}$ have a sinusoidal ripple with twice the line frequency ($2 * F_{line}$), while the load absorbs a constant power P_{Load}. Hence, the instantaneous power mismatch has to be buffered in the DC-Link Capacitors. Similarly, Inverters DC-Link Capacitors buffers the instantaneous power mismatch between the DC and the AC side. In both case there is a voltage ripple in the DC-Link that must be limited to a certain percentage of the average DC-Link voltage. Hence, in these applications the voltage ripple limitation determines the amount of capacitance required for the DC-Link.

-Short-term energy storage: In Telecommunication Systems and Uninterrupted Power Supply (UPS) the DC-Link Capacitors are used as a power backup for a couple of seconds (hold-up time) in the case of a grid outage. During this time, telecommunication system is able to communicate that is going in line-down and UPS starts to produce energy from the energy storage in its battery pack.

-Filter Current Harmonics: Input PFC filters and output inverter filters.

-Energy Buffering for Power Drive Inverters:

In most of the applications the capacitance selection is straightforward except for DC-links for power drives where both E-Caps and Metal film capacitors should be used. In [56] there is a detail procedure for the multi-objective optimization of the DC-link for the latter application.

4 Case Study DC/DC converter for EVs Battery Chargers Multi-objective Optimization Design

Electric Vehicles Battery Chargers are classified based on different electrical vehicles connectors standards (Table 1)

SAE J1772			
Charging Power Levels:	Output Power	Charger Location	Typical Use
AC Charging Level 1 1-Φ 120 Vac (US) 1-Φ 230 Vac (EU)	$P_{OUT} = 1.4kW\ I_{OUT} = 12ADC$ $P_{OUT,max} = 1.9kW\ I_{OUT} = 20ADC$	On-Board	Charging at home or office for low cost EVs
AC Charging Level 2 208-240Vac (US)	$P_{OUT} = 4kW\ I_{OUT} = 17ADC$ $P_{OUT} = 8kW\ I_{OUT} = 32ADC$ $P_{OUT,max} = 19.2kW\ I_{OUT} = 80ADC$	On-Board	Charging at private or public outlets for High-End vehicles
Fast AC Charging Level 3 (208-600 Vac)	$P_{OUT} = 50kW$ $P_{OUT} = 100kW$	Off-Board	Commercial, analogous to a filling station.
DC Charging Level 1 200VDC-450VDC	$P_{OUT} = 40kW\ I_{OUT} = 80ADC$	Off-Board	Dedicated Charging Point
DC Charging Level 2 200VDC-450VDC	$P_{OUT} = 90kW\ I_{OUT} = 200ADC$	Off-Board	Dedicated Charging Point
DC Charging Level 3 200VDC-600VDC	$P_{OUT} = 240kW\ I_{OUT} = 400ADC$	Off-Board	Dedicated Charging Point
IEC 62196			
Charging Power Level	Current	Charger Location	Typical Use
AC Charging Level 1	$P_{OUT} = 4kW - 7.5kW$ $I_{OUT} = 16A$DC	On-Board	Charging at home for High-End vehicles

1-Φ 230 Vac (EU)			
AC Charging Level 2 1-Φ 230 Vac (EU) 3-Φ 400Vac (EU)	$1-\Phi$: $Pmax = 7kW\ I_{OUT} = 16A$ $3-\Phi$: $Pmax = 22kW\ I_{OUT} = 32A$	On-Board	Charging at private or public outlets for high-end vehicles
AC Charging Level 3 3-Φ 400Vac (EU)	$P_{OUT} = 22kW - 43kW$ $I_{OUT} = 32A - 63A$	Off-Board	Commercial, analogous to a filling station.
DC Rapid Charging	$P = 50kW - 240kW$ $I_{OUT,max} = 400A$ $V_{OUT,max} = 500V$	Off-Board	Dedicated Charging Station
CHAdeMo			
Charging Power Level	Current	Charger Location	Typical Use
DC Rapid Charging	$P = 62.5kW$ $I_{OUT} = 125A$	Off-Board	Dedicated Charging Station

Table 11: EVs Battery Charger Classification [*57*,*58*]

In general EVs Battery Chargers are made of two stages. A Power Factor corrector and a DC/DC converter stage.

The topology used for the two stages depends on:

$\boldsymbol{P_{OUT,max}}$**:** Maximum Output Power

Battery Voltage Level: Today, except for the Porsche Taycan with its 800V battery, commercial vehicles have a 400V battery.

Required power density and weight density: For OBC converters these requirements are very stringent and could be as important as the efficiency of the converter. On the other hand, for Off-Board Chargers these requirements are more relaxed, as efficiency is the most important figure of merit.

Standards: Table 11

Governmental Construction Guidelines: For example Chinas 2017 Electric Vehicle Charging Equipment Supplier Qualification Verification Standard [59] (Figure 31).

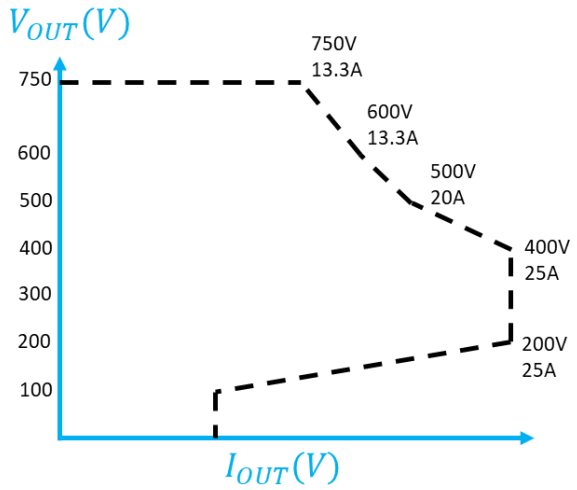


Figure 31: Chinas 2017 Electric Vehicle Charging Equipment Supplier Qualification Verification Standard

For the PFC stage the most common topologies are indicated in *Table 12*:

Topology	Charging Power Level	Benefits	Drawbacks	Literature
1-Φ Boost Interleaved	IEC 62196 AC Charging Level 1, Level 2	-Low Cost -Low Part Count	-Additional Conduction losses due to the diode bridge.	
1-Φ Interleaved Totem Pole	IEC 62196 AC Charging Level 1, Level 2	-High Efficiency -High Power Density -Bidirectional	-Cost: In order to be able to exploit all the benefits of this topology it is compulsory to use SiC Devices.	
3-Φ T-Type Rectifier	IEC 62196 AC Charging Level 3	-High power capability -High Efficiency -Split DC-Link	-Unidirectional	

Table 12: Power Factor Correctors Mainstream Topologies

For the DC/DC Stage the potential topologies are indicated in Table 13:

Topology	Benefits	Drawbacks	Literature
DAB	-Wide Range of output voltage -Bidirectional	-There is a trade-off between reactive current and ZVS. -Large Part Count. Current Sensors and driver in both the primary and secondary side of the converter.	
LLC	-Wide Range of Output Voltage -For Fsw<Fr ZVS for primary side MOSFETs and ZCS for secondary side MOSFETs -Cost	-Complex Control	
CLLC	-Wide Range of output voltage -Bidirectional -Distributed resonant capacitor in the primary and secondary side enables to reduce voltage stress on the resonant capacitors. -Symmetric Gain for both sides of the converter.	-Large Part Count. Current Sensors and driver in both the primary and secondary side of the converter.	

Table 13: DC/DC Stage Mainstream Converter Topologies

Currently, Battery technology is the main bottleneck for the vehicle electrification. Lithium battery have an energy density (200-300Wh/kg) one order of magnitude lower than gasoline (12000Wh/kg) [1] and a limited number of recharging cycles. Hence, a bidirectional topology is counterproductive both for the battery and the overall cost of the Charger. Synchronous rectification in bidirectional converters require extra drivers and current sensors. These are the main reasons, why the LLC converter is the mainstream topology for the DC/DC stage of EV chargers.

Up to know both in the industry and literature LLC converter design guidelines have focus in the boost region (i.e. Fsw<=Fr), where the primary MOSFET and the secondary diodes experience ZVS and ZCS respectively.

The buck region has been undermined given that the boost region is the most efficient region and there was not a need to explore the buck region. However, it is a fact that battery level will increase, hence it will be compulsory to explore the buck region of LLC converters in order to satisfy the future speck of EV Chargers converters. Moreover, enabling the buck region allows to widen the switching frequency of the LLC converter which can be helpful for the inductor/transformer design

In this chapter first the transfer function of the LLC converter will be derived using the Full Harmonic Approximation. Second, it will be illustrated how a variable DC-Link of the PFC stage could narrow the require switching frequency range of the LLC converter, which can be advantageous for the LLC multi-objective optimization. Third, the different operation modes of the LLC will be explained. Forth, possible variation of the LLC converter for power scalability (i.e. increased the output power) will be presented. Finally, a multi-objective-optimization of a LLC converter working in buck region for next generation EV's (i.e. EVs with a battery level of 750V) will be presented.

4.1 LLC Transfer Function: Full Harmonic Approximation

The LLC Converter transfer function is defined by the resonant capacitor C_r, resonant inductor L_r ,the magnetization inductance of the transformer L_m and the switching frequency F_{SW} of the H bridge in the primary side of the LLC converter.

Using the Full Harmonic Approximation (FHA) it is possible to derive the equivalent circuit of the LLC converter (Figure 32)

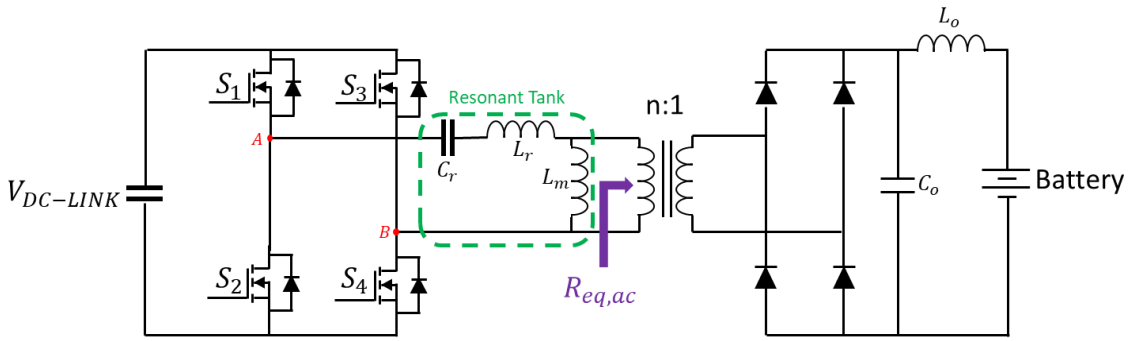


Figure 32: LLC converter topology.

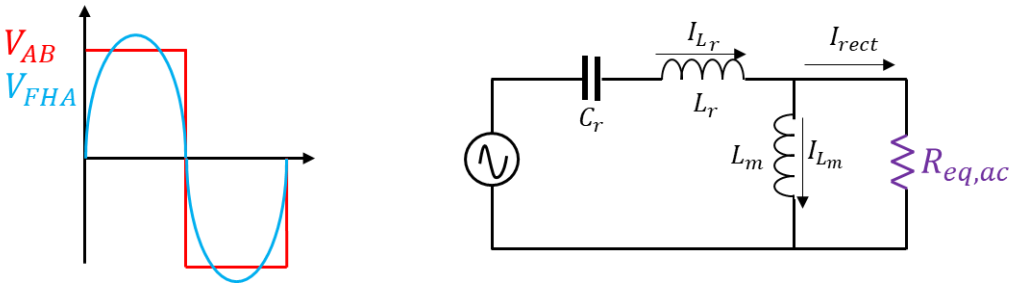


Figure 33: AC Equivalent Circuit of the LLC converter

where $R_{eq,ac}$ is the equivalent load of the rectifier stage reported at the primary side (Figure 33)

$$R_{eq,ac} = n^2 \frac{8}{\pi^2} \frac{V_{OUT}}{I_{OUT}} = n^2 \frac{8}{\pi^2} \frac{V_{OUT}^2}{P_{OUT}} \quad (50)$$

n: Transformer winding ration between the primary and the secondary side.

V_{OUT}: Output Voltage

I_{OUT}: Output Current

P_{OUT}: Output Power

The DC voltage gain ($M = nV_{OUT}/V_{IN}$) of the resonant tank based on FHA is (see Figure 34):

$$M(f_n, l, Q) = \frac{1}{\sqrt{\left(1 + l - \frac{l}{f_n^2}\right)^2 + Q^2\left(f_n - \frac{1}{f_n}\right)^2}} \quad (51)$$

Where

Resonant Frequency: $$F_r = \frac{1}{2\pi\sqrt{L_r C_r}} \quad (52)$$

Characteristic Impedance: $$Z_o = \sqrt{\frac{L_r}{C_r}} \quad (53)$$

	Quality Factor	$Q = \frac{Z_o}{R_{eq,ac}} = \frac{\pi^2 I_{OUT}}{8V_{OUT}}\frac{1}{n^2}Z_0 = \frac{\pi^2 P_{OUT}}{8(nV_{OUT})^2}Z_o$	(54)

Inductance Ratio $$\lambda = \frac{L_r}{L_m} \quad (55)$$

Normalized Frequency $$f_n = \frac{F_{SW}}{F_r} \quad (56)$$

When designing a LLC converter it's important to consider that:

1. F_{SW} is a discrete variable that depends on the clock frequency of the digital signal processor (DSP) used to implement the control. Even though today DSP are very powerful, its important to check that the DSP is compliant with the require switching frequency variation steps require to control the LLC converter in all the working conditions.
2. The inductance ratio λ is the most challenging parameter of the LLC transformer design for the following reasons:
    a. M is very susceptible to λ variations. As λ increases M shrinks. Hence for a given frequency range the gain variation between Fmin and Fmax will increase as λ increases. This could be useful to limit the operation

frequency range of the LLC converter or to be able to satisfy a higher maximum output voltage $V_{out,max}$

b. L_m is not an independent variable of the transformer design. Recall that the magnetization inductance of the transformer can be estimate as

$$L_m = \frac{{n_1}^2}{\mathbb{R}} = \frac{n_1^2 \mu A_c}{l} \quad (57)$$

Where n1, μ, l are the number of turns of the primary winding, the permeability of the core and the mean magnetic path respectively.

Hence, in order to realize a given L_m value, designers should variate either n_1, μ, l or A_c which could rise non-conformities of other transformer specifications. For example, maximum and minimum window utilization area, exceeding core B_{sat} , having a low efficiency or increasing the form factor of the core.

4.2 LLC Operation Modes

There are three operation modes in the LLC converter: Buck mode, Boost mode and Resonance ($F_{sw} = F_r$) (Figure 34).

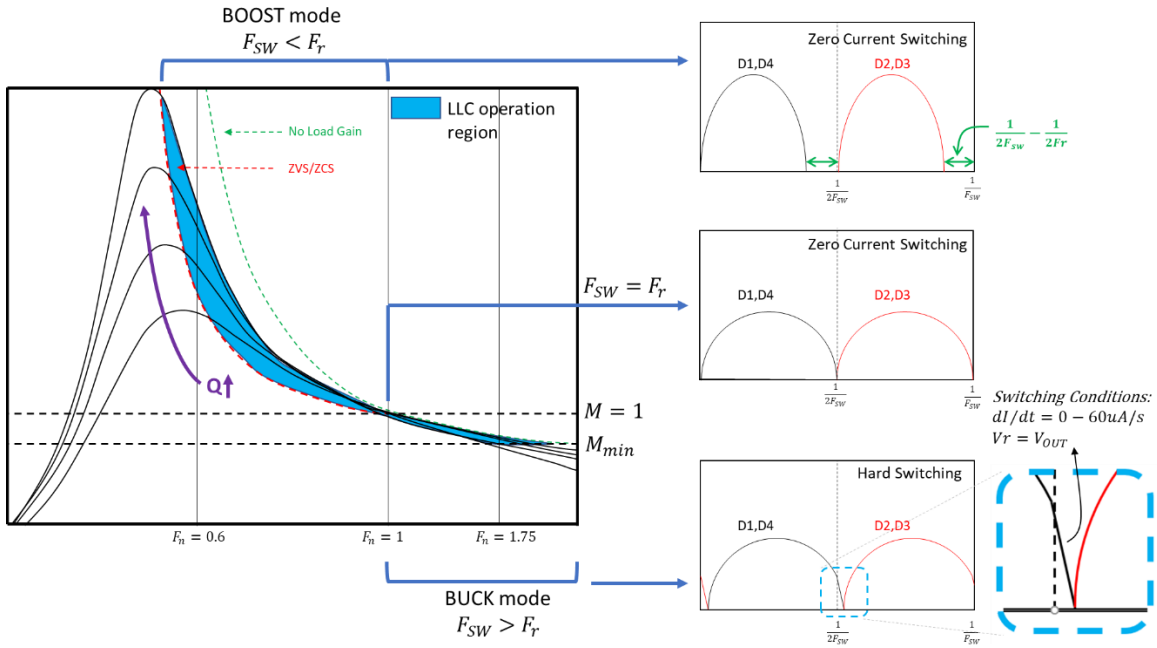


Figure 34: LLC Operation Regions and current waveform in the secondary side.

Boost Mode: In boost mode $F_{sw} < F_r$. Primary side MOSFETs experience ZVS while secondary side diodes experience ZCS. Moreover, there is a time interval equal to $\frac{1}{2F_{sw}} - \frac{1}{2Fr}$ every $\frac{1}{2F_{sw}}$ (see Figure 34) in which the current circulating in the primary side does not deliver power to the load. For a given output power P_{out}, the aforementioned intervals widen while the peak current experienced by the diodes at the secondary side ($I_{s,pk}$) increases as F_{sw} moves away from F_r ; as F_{sw} decreases. (see Figure 35).

Moreover, as:

$$I_s = I_p - I_{L_m} \tag{58}$$

where I_p, I_s, I_{L_m} are the currents at the primary side, secondary side and the magnetization current, as $I_{s,pk}$ increases $I_{p,pk}$ should also increases. Thus, special attention should be paid to avoid exiting the maximum instantaneous dissipation

power of diodes and MOSFETs and avoid saturating the resonance inductance when the LLC operate in boost region. Because, it will require to use diodes and MOSFETS with a larger die size, which translate in a higher cost for components that will not be fully exploited.

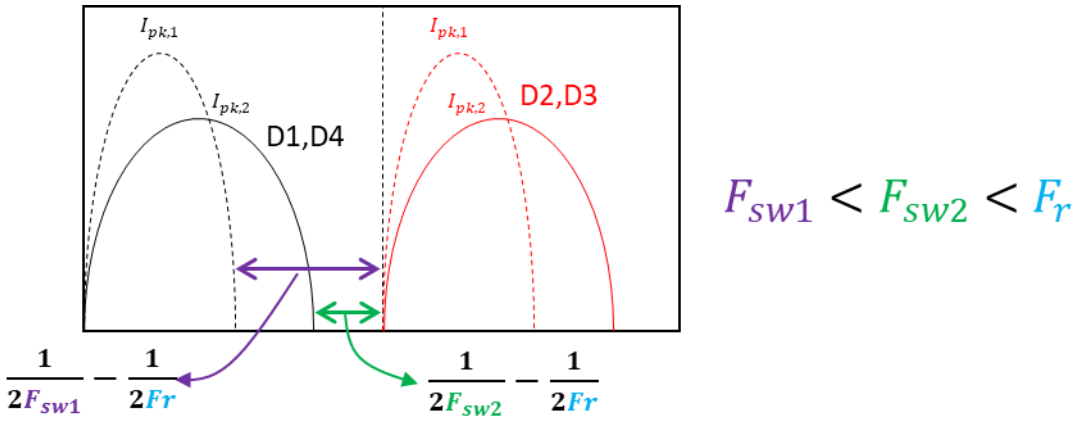


Figure 35: Secondary diodes current comparison for a given output power and two switching frequencies (Fsw1 and Fsw2)

The latter problem, can be coped with a high inductance ration λ , because a small decrease in Fsw causes a significant increase in the output voltage. However, as it will be shown in the case study in section 4.5 it is not always possible to have a high inductance ration.

Resonance: In this condition ($F_{sw} = F_r$). As in the previous case, MOSFETs experience ZVS while diodes ZCS. The LLC converter experiences its maximum efficiency. As $\frac{1}{2F_{sw}} - \frac{1}{2Fr} = 0$, the LLC is always delivering power to the load. The current at the primary side is a perfect sinusoid which simplifies the power dissipation assessment of the LLC inductor and transformer.

Buck Mode: In buck mode $F_{sw} > F_r$. Primary side MOSFETs experience ZVS while secondary side diodes experience Hard-Switching with a very low di/dt value ($0 - 150A/\mu s$).

If Si diodes are used, despite the switching losses generate by the aforementioned switching condition are one order of magnitude smaller than the ones generated in a conventional Hard-Switching application like a PFC, they cannot be ignored. Remember that F_{sw} of an LLC is one order of magnitude higher than a PFC. Hence,

as it is done for conventional hard switching application an energy dissipated map in function of I_F,dI/dt, T_j and V_{rr} could be used to make an accurate assessment of switching power losses and Tj of diodes in an LLC working in buck mode. Expanding the operation range of the converter to this region.

Meanwhile in the case of SiC diodes, switching losses can be neglected in the design phase. Even though it does not mean that they are not present. Consequently, using SiC Diodes enable reaching frequencies of the order of 500kHz which is very convenient for the magnetic components design.

4.3 Variable DC-Link + Frequency Modulation of LLC

The concept of variable DC-Link of the PFC together with the frequency modulation enable to shrink the switching frequency range of the LLC converter and improve the overall efficiency of the converter.

Consider you have a battery which voltage level $V_{Battery}$ oscillates between 350V when is discharged and 800V when it is fully charged.

Figure 36 shows the transfer function of the LLC converter where the x-axis correspond to the normalized switching frequency. In this case the DC-Link voltage level ($V_{DC-link}$) is fixed. Therefore, the normalized switching frequency of the LLC converter swings between 0.6 and 1.75 in order to cope with the $V_{Battery}$ requirements.

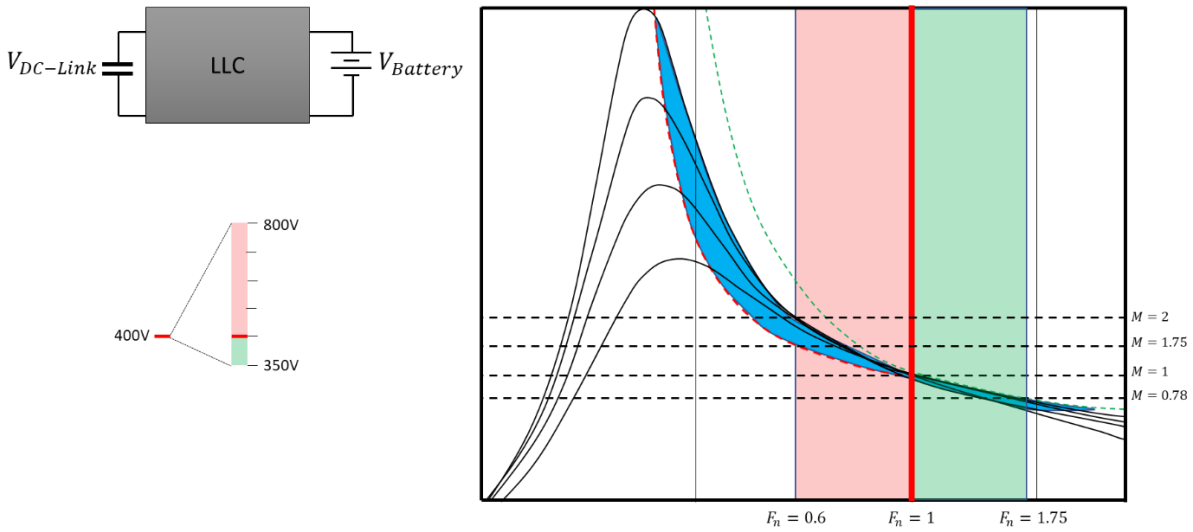


Figure 36:LLC with fixed DC-Link voltage.

In the second case in Figure 37, the variable $V_{DC-link}$ enables to shirk the switching frequency operation region while improving converter efficiency. The latter, is done in two ways.

1st The nearer F_{sw} is to the F_r the converter will be more efficient

2nd When the converter has to supply 400V to 450V to the battery it works in resonance mode where you have the maximum efficiency.

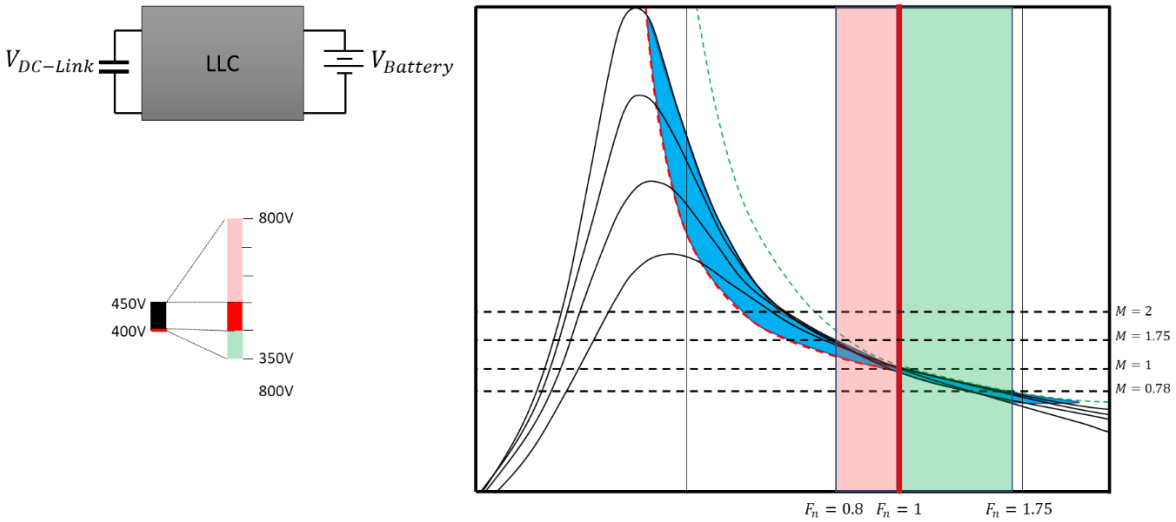


Figure 37: LLC with Variable DC-Link voltage.

4.4 LLC Topology Variations

Additionally, to the low switching losses in semiconductors, LLC converter enables to implement different variations that enable to scale the output power of the converter and reduce the form factor of the converter.

4.4.2 ISOP LLC configuration

Input Series Output Parallel (ISOP) configuration:

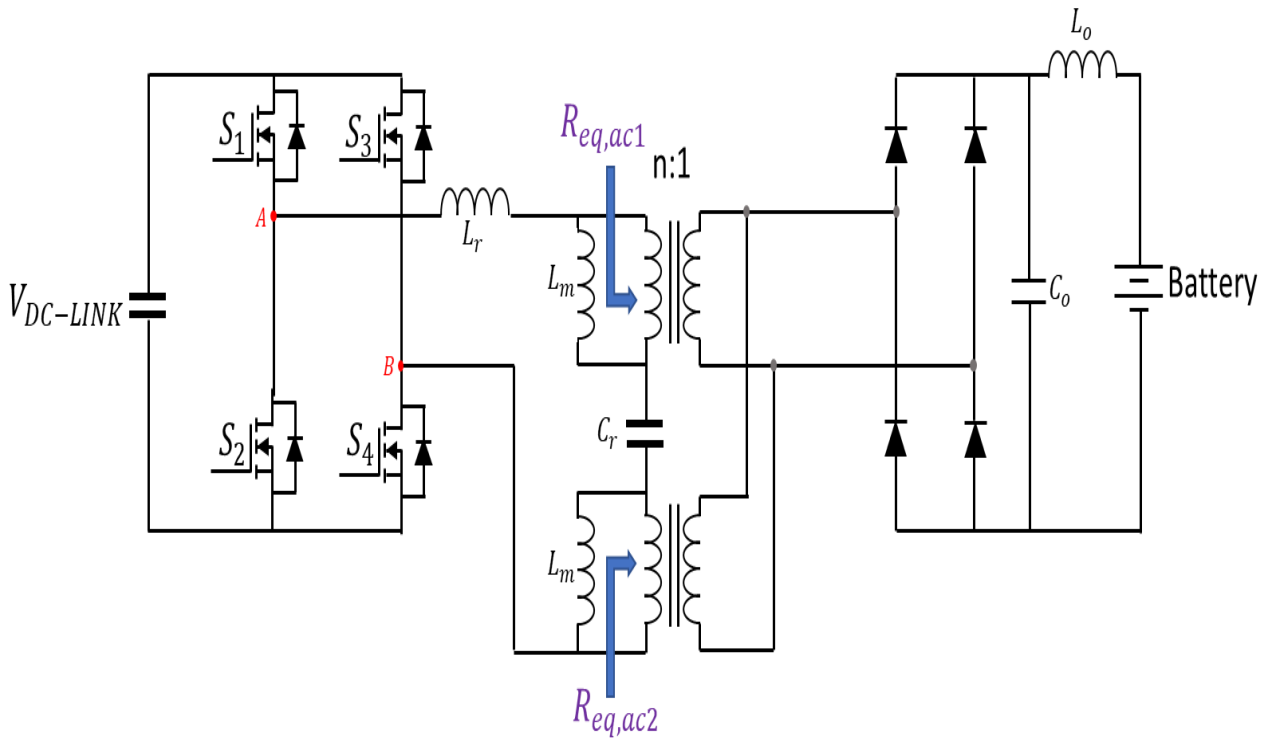


Figure 38: LLC converter in Input Series Output Parallel (ISOP) Configuration

The ISOP configuration presented in Figure 38 can be simplified using the FHA as shown in Figure 39.

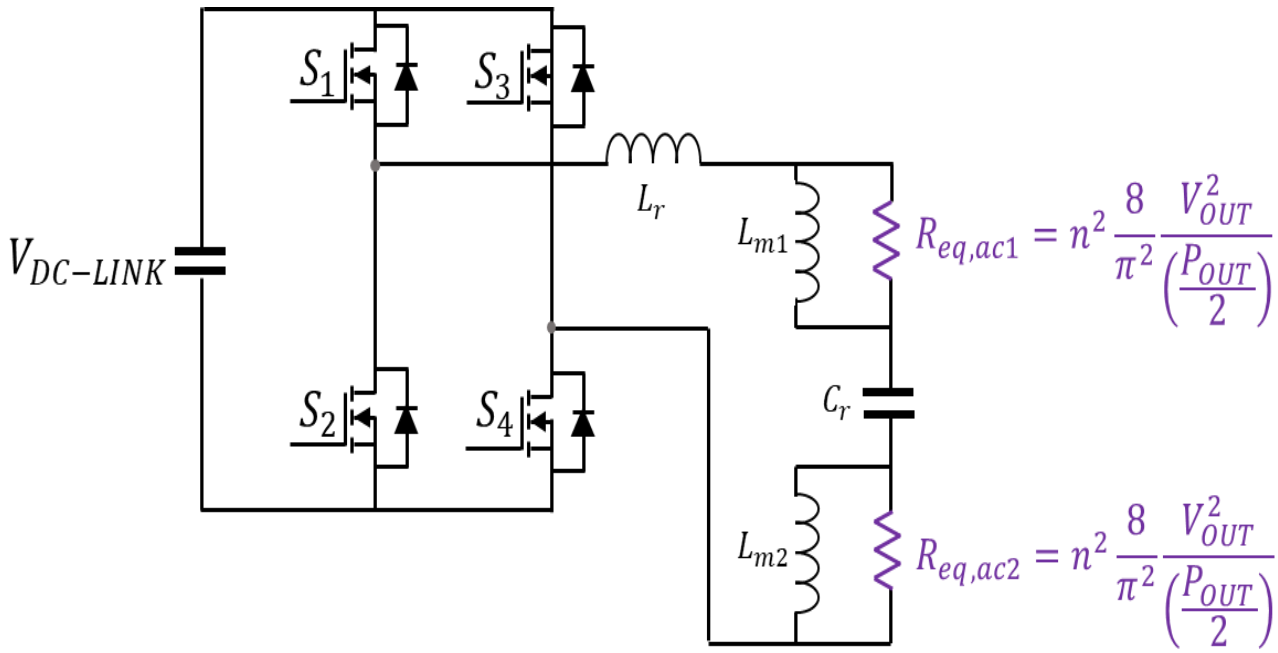


Figure 39: LLC ISOP Configuration equivalent circuit derived with the FHA

Given that the two transformers have the same winding ration n and are connected to an equivalent load that has the same value (i.e. Rac1=Rac2). It is possible to derive the circuit in Figure 32 where the equivalent transformer has a $L_m = L_{m1} + L_{m2}$ and the same winding ration as the individual transformers n. Moreover the equivalent transformer will have an equivalent resistance connected to it equal to :

$$R_{eq,ac} = n^2 \frac{8}{\pi^2} \frac{V_{OUT}^2}{\left(\frac{P_{OUT}}{2}\right)} \tag{59}$$

That means that when evaluating the LLC DC gain M, the Q value correspond to half of the desired output power. For example, if you want to evaluate M for Pout=30kW, you should evaluate the M for Q(Pout=15kW).

Finally, it is important to take in consideration that by Kirchhoff's voltage law at resonance the voltage at the primary of each transformer equals

$$V_{trans,pri} = \frac{V_{DC-LINK}}{\#\ LLC\ transformers} \tag{60}$$

Hence when using this configuration n value must be greater than $\#\ LLC\ transformers$ in order to be able to work as a boost DC/DC converter.

Benefits:

- The magnetization inductance can be distributed between the transformers connected in series. Recall that if two inductors are connected in series the equivalent inductance equals the sum of the two inductances. Hence if it is not feasible to reach the desired magnetization inductance while being compliant with the rest of the transformer's specs (e.g. turn ration), this topology could be helpful.
- Reduce winding losses. Transformer connected in series enable to reduce the amount of turns in the primary winding N1, see equation (59)

$$V_{in,p} = \frac{V_{in,LLC}}{TN} \qquad L_{m,transf} = \frac{L_m}{TN} \tag{61}$$

Where $V_{in,LLC}$, $V_{in,p}$, L_m, $L_{m.transf}$ and TN are the LLC input voltage, input voltage at the primary side of a transformer connected in series, magnetization inductance of the LLC circuit and magnetization inductance of a transformer respectively.

- Increase the power density by reducing the form factor of the transformers. Having a single transformer is bulkier than having a series of transformers, especially the height. Recall that the bottle neck of power density are capacitors. Hence, you want magnetic components with a high minor or equal to the required capacitors height.

Drawbacks

- This topology is power limited by the maximum feasible current flowing in the primary side, that depends both on the available MOSFETs current rate and the maximum current allowed by the magnetic components (resonant inductor and transformers) before they start to saturate.
- For a wide voltage gain control in a small frequency range it is compulsory to have a high λ .

4.4.2 IPOP LLC configuration

The IPOP LLC configuration (Figure 40) is the mainstream topology for rectifier with a split bus like the Vienna Rectifier or the T-Type Rectifier. Moreover it can be used for rectifier with a single bus.

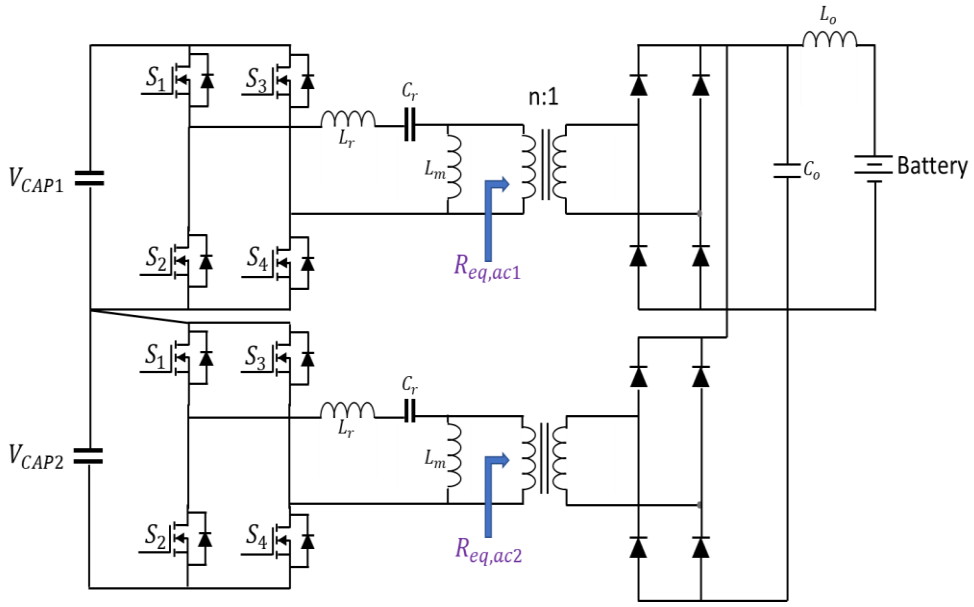


Figure 40: LLC Converter in Input Parallel Output Parallel (IPOP) Configuration

Using FHA approximation, it is possible to derive the equivalent circuit in Figure 41.

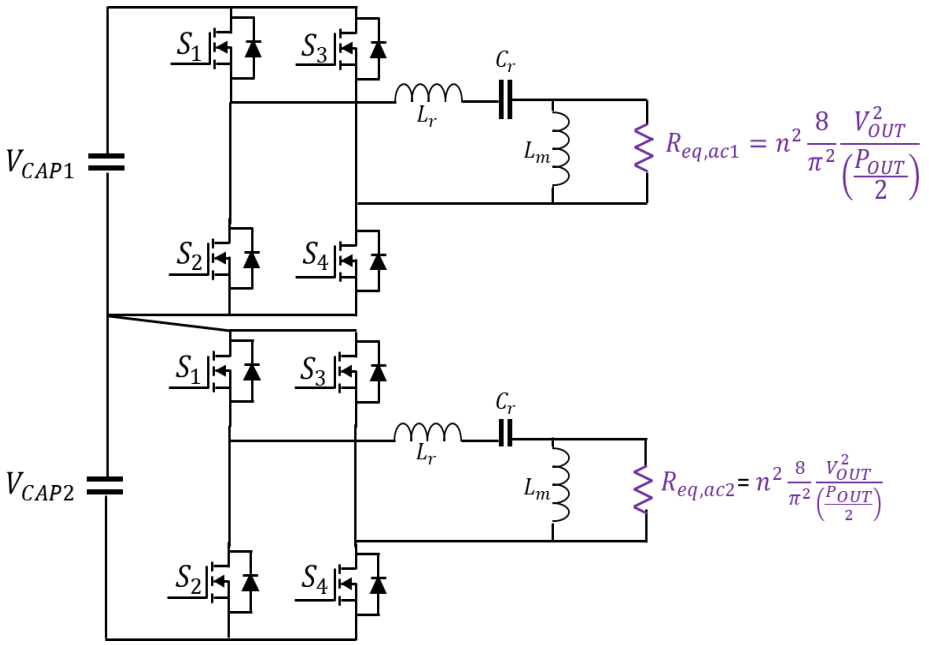


Figure 41: LLC IPOP Configuration equivalent circuit derived with the FHA

Dividing the circuit in Figure 41 in two it is possible to arrive the circuit in Figure 32.

4.4.2 LLC Transformers parallel configuration

In order to further reduce Lm value while halving the power rating, two transformers connected in parallel at the primary side and at the secondary side (Figure 42) can be used instead of one.

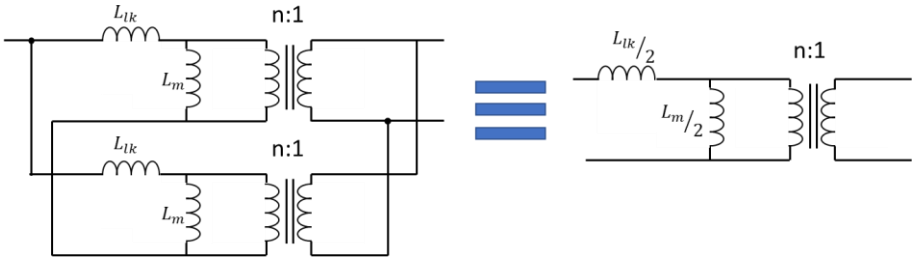


Figure 42: Two transformers connected in parallel at the primary and the secondary side

Finally, it is important to remark that for high out power 22kW a combination of the ISOP and IPOP can be used to increase power density, efficiency and improve thermal management.

4.5 Multi-Objective Optimization of LLC converter for an Onboard Charger

In the following section the design of the LLC converter for the DC/DC stage of a level 2 Onboard Charger with a maximum output voltage $P_{OUT,max} = 22kW$ and a maximum output voltage of 750V will be presented.

4.5.1 Specifications

The working conditions of the LLC stage are dictated by the battery charging profile that determines the amount of maximum current that should be feed to the battery for a given battery voltage level. The latter can be represented either with a charging profile graph as in Figure 31 or in tabular form.

Moreover, remember that the LLC converter is connected to a PFC stage hence the feasible input voltages for the LLC stage $V_{IN,LLC}$ depends on the output voltage value the PFC stage $V_{OUT,PFC}$ is able to provide.

For the following example: $V_{OUT,PFC} = 400V - 500V$

4.5.2 LLC Topology definition

1. **Choose the number of Transformers (TN).**

   The number of transformers present in the LLC circuit (TN) for IXOP where X could be S/P should comply with the following equation.

   $$P_{transfo,max} \times TN = P_{OUT,max} \quad (62)$$

   Where $P_{trasnfo,max}$, is the maximum power each transformer is able to transfer to the output. Given that at resonance the output current contribution of each transformer is equal to the secondary diodes RMS currents $I_{Diode,RMS}$.

   In order to define the initial TN value First, we hypothesizing diodes nominal current $I_{diodes,n}$.

   - In this case $I_{diodes,n} = 30A$

   Second, assuming the converter operates in resonance mode for all the working condition, select a TN value using equation (63)

	$I_{out,LLC}/TN < I_{Diode,n}$	$with\ TN = 1,2,3, \ldots$	(63)

   - If Pout=22kW and Vout=350,300V,200V for TN=2, $I_{out,LLC}/TN > I_{Diode,n}$ (see Table 14)

$P_{out}\ (kW)$	$V_{out}\ (V)$	$I_{out,LLC}$ (A)	$\frac{2 \times I_{outLLC}}{TN}\ (A)$
22	700	31.43	15.71
22	650	33.85	16.92
22	600	36.67	18.33
22	550	40.00	20.00
22	500	44.00	22.00
22	450	48.89	24.445
22	400	55.00	27.50
22	350	60	31.00
22	300	60	39.66
22	200	60	55.00

Table 14: LLC converter secondary diodes maximum current control with TN=3

There are two alternatives:

- use diodes with a higher current rate (e.g. 60A).
-make a power derating by fixing $I_{outLLC,max} = 60A$. Hence if $V_{out} = 200V \rightarrow P_{out,max} = 12kW$

Consequently, recalling equation (62) $P_{transfo,max} = 5.5kW$ for $V_{out} > 350V$

2. **Topology selection:**
   - Given the high-power rate its better an IPOP configuration as initial condition.

3. **Define the transformer winding ration N by hypothesizing M_{min} and $V_{in,LLC,min}$**

$$N = \frac{V_{in,LLC,min} \times M_{min}}{V_{out,LLC,min}} \quad (64)$$

In order to avoid having a very high F_{sw} in buck mode, the minimum DC gain (M_{min}) should be limited. Moreover, given that the input voltage of the LLC stage equals the output voltage of the PFC stage ($V_{in,LLC} = V_{out,PFC}$), the minimum feasible and reasonable value for $V_{out,PFC,min}$ should be defined.

- In this with $M_{min} = 0.8$ and $V_{in,LLC} = 350V$ @ $Vout = 200V \rightarrow N = 1.4$

4. Select Fr

Given the high switching frequencies of LLC converters, it is compulsory to use litz wire to avoid eddy losses in the winding. Typically type 1,2 or 8 litz wire are used.

Litz wire fabricator design guidelines, council a certain wide gauge for a given frequency range.

For Type 1 and 2 see *Table* 15

Frequency	Recommended Wire Gauge
60Hz to 1kHz	28 AWG
1kHz to 10kHz	30 AWG
10kHz to 20kHz	33 AWG
50kHz to 50kHz	38 AWG
100kHz to 200kHz	40 AWG
200kHz to 350kHz	42 AWG
850kHz to 1.4MHz	46 AWG
1.4MHZ to 2.8MHz	48 AWG

Table 15: Design Guidelines recommendation for New England Wire Technologies Type 1 and Type 2 Litz Wire single strand wire gauge

Type 8 enable full performance with a winding occupation of $\approx 90\%$ and it can be used from 1kHZ to 400kHz. Given its cost we should avoid it as first choice. Hence, when selected the resonant frequency, we should make a projection of $F_{sw,max}$ so that both Fr and Fsw are inside one of the frequency range of litz wire design guidelines.

For this design Fr=250kHz and $F_{sw,max} = 300kHz$ was chosen as initial condition.

5. Calculate the transformers L_m, Lr, Cr values.

During the no load condition, the current flowing through L_m I_{L_m} should be high enough to charge and discharge the junction capacitance of the MOSFETs at the primary side, enabling ZVS.
For $F_{sw} \leq F_r$:

$$I_{L_m,min} \geq \frac{N_{MOS} C_{oss} V_{in,LCC}}{T_{dead}} \qquad L_{m,max} \leq \frac{V_{in,LLC}}{2\pi F_r I_{L_m,min}} \tag{65}$$

Where N_{MOS} stands for the number of switches, C_{oss} is the MOSFET effective output capacitance (time related) and T_{dead} is the dead time interval of the MOSFETs gate drivers.
For $F_{sw} > F_r$:

In buck mode the voltage through L_m is smaller than Vin and the worst-case condition is found at $F_{sw,max}$.

$$I_{L_m,min} = \frac{V_{in} \times N \times M_{min}}{4 \times F_{sw,max} \times L} \qquad L_{m,max} \leq \frac{T_{dead} M_{min}}{16 F_{sw} C_{oss}} \tag{66}$$

Given that the converter must work in buck region (66) should be used.

The C_{oss} value depends on the MOSFET choice (Table 16)

MOSFET Technology	Conduction Losses	Coss(tr)	Cost
SJ MOSFET	Lowest	Intermediate	Cheapest
SiC DMOS (Cree)	Moderate	Lowest	Moderate
SiC Trench	Low	Highest	Moderate

Table 16: MOSFET performance tradeoffs for ZVS in an LLC circuit

If Infineon IPP65R045C7 SJ MOSFET with Coss(tr)= 1630pF is selected.
Hypothesizing $F_{sw,max}$=300kHz and $T_{dead} = 300ns$

$$L_{m,max} \leq \frac{300 \times 10^{-9} \times 0.8}{16 \times 300 \times 10^3 \times 2584 \times 10^{-12}} = 19.34\ \mu H$$

At first glance, given the wide output voltage requirement designers will tend to increase $\lambda > 3$, which translates in a minimum feasible L_m value. However, there is a tradeoff between L_m and the current at the primary side of the transformers in an LLC circuit. Recalling equation (58), $L_m \propto \frac{1}{I_{L_m,pk}} \rightarrow L_m \propto \frac{1}{Ip}$.

On the other hand, for the resonance capacitor as there is a sinusoidal waveform flowing through it, the relation between the peak current $I_{Cr,max}$ and the peak voltage $V_{C_r,max}$ is given by equation

$$V_{C_r,max} = \frac{I_{Cr,max}}{2\pi F_{sw} Cr} \tag{67}$$

Therefore, during operation $V_{cr,max}$ increases either as the current in the primary side increases or as F_{sw} decreases. Hence, Cr should be as high as possible in order to prevent the converter from exceeding the maximum Vac value of the capacitors used for Cr.

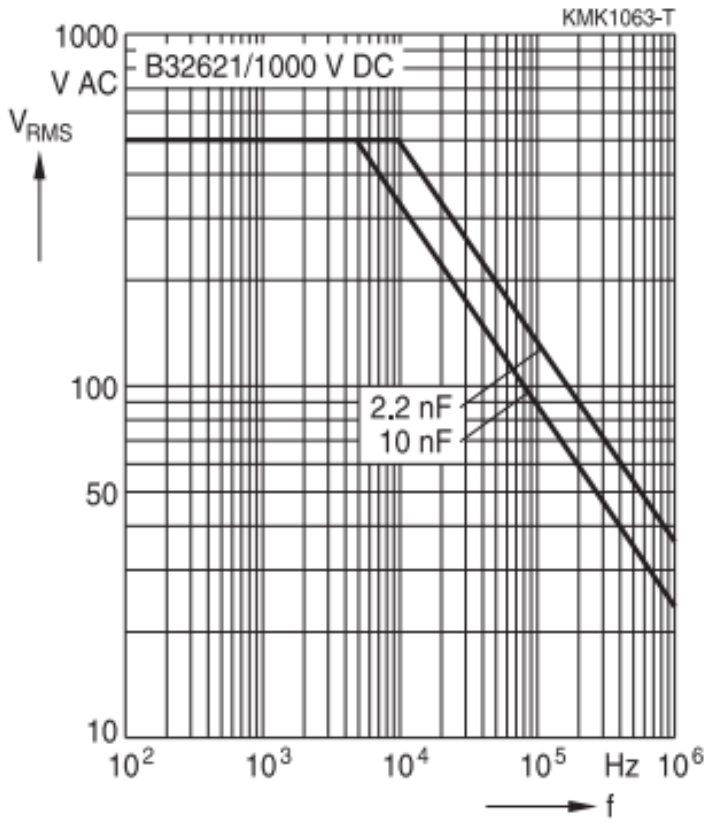


Figure 43: Frequency derating of capacitor maximum Vac Value (TDK-Lambda)

Hence the following algorithm should be used in order to define L_m, L_r and C_r.

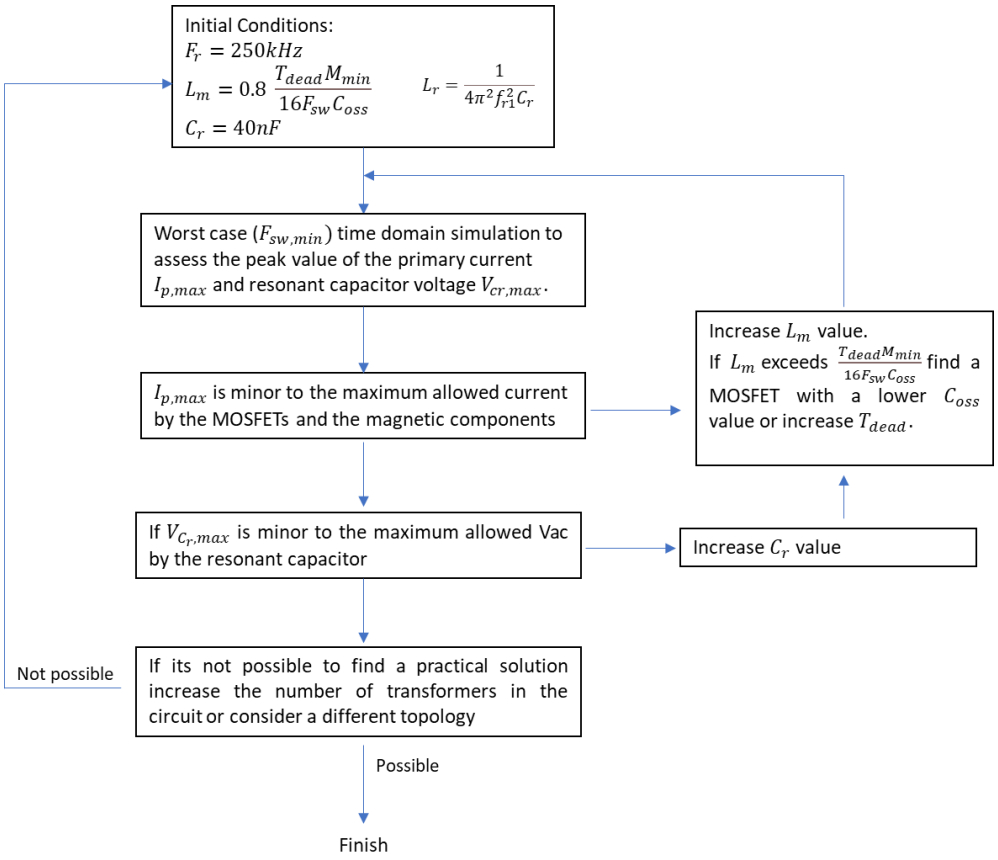


Figure 44: Algorithm used to define L_m,L_r and C_r

6. Choses between Si and SiC diodes

Based on the battery voltage level, the target cost and power density of the LLC. NOTE: The best practice is to use as initial condition Si. However, in this case as power density should be maximized it is evident that SiC devices should be used.

Moreover, the empirical frequency range in Table 17 can be also useful for diodes technology selection.

Secondary Side Diodes:	
Si	SiC
Fr=120kHz – 220kHz	Fr=200kHz – 500kHz

Table 17: Resonant frequency Fr definition, based on the semiconductor technology of the secondary side diode

7. **Chose transformer and inductor core material based on the converter requirements.**

   For LLC converter powder core materials are used.
   - If full performance is required a Fe-Ni-Mo alloy powder core (MPP) should be a must. Given, that at the moment MPP cores are not available in E core shape, a Fe-Ni alloy powder core (High Flux) should be used instead.
   - If the converter must comply with a performance-cost tradeoff, either Fe-Si or Fe-Ni should be used.
   - If the application is cost sensitive a Fe-Al-Si alloy should be used.

   - Following the aforementioned criteria's:
     - Fe-Al-Si with EE and EI form factor were considered for the transformers
     - Fe-Al-Si with EE, EI and toroidal form factor were considered for the transformers

8. **Identify the maximum height of the electrolytic capacitors used for the DC-Link both at the output of the PFC and the DC/DC stage ($Height_{E-CAP}$) and filter core materials database.**
   In order to increase the power density of the converter all the magnetics components should have a height less or equal to the electrolytic capacitor height $Height_{E-CAP}$. This is a practical way to decimate the core material database.

9. **Design the magnetic components following the algorithm presented in section 3.1.4**

Output Power	P_{out}	22kW	Devices
Resonant Capacitor	C_r	$50nF$	5X 10nF 2000VDC / 700VAC C823D102-90
Transformer magnetizing inductance	L_m n	$15\mu F$ 0.7	Magnetic Kool Mμ E core 00K4317E024
Resonant Inductance	L_r	$8.10569\mu F$	
Mosfets	Q		8 X IPP65R045C7
Diodes	D		8 x E4D20120D 1200V 20A

Table 18: 22kW OBC Converter Specs

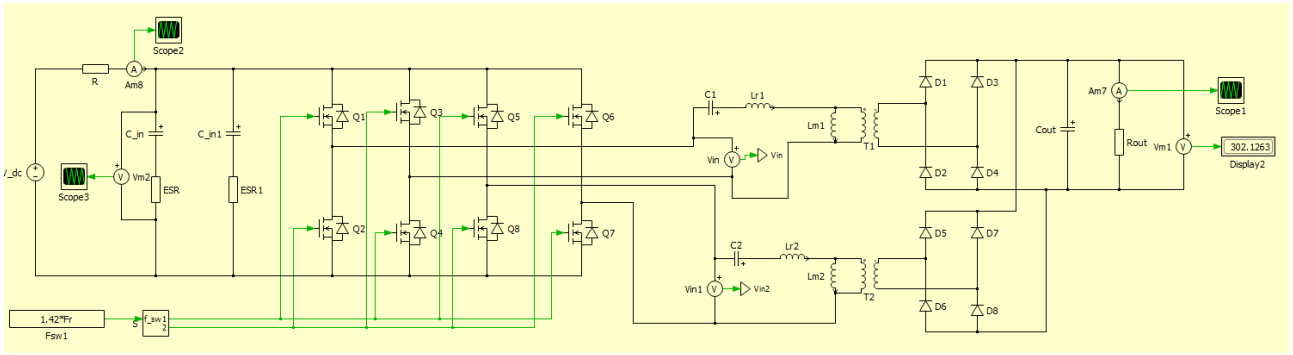


Figure 45: PLECS time domain simulation of the 22kW LLC converter for OBC

In the graph below (*Figure 46*):

Ip1: Current at the primary side of the transformer T1

ILm1: Magnetization current in transformer T1

Vin: Input Voltage to the LLC circuit

ID1: Current through diode D1

ID2: Current through diode D2

VD1: Voltage in diode D1

VD2: Voltage in diode D2

VCr: Voltage in resonant capacitor C1

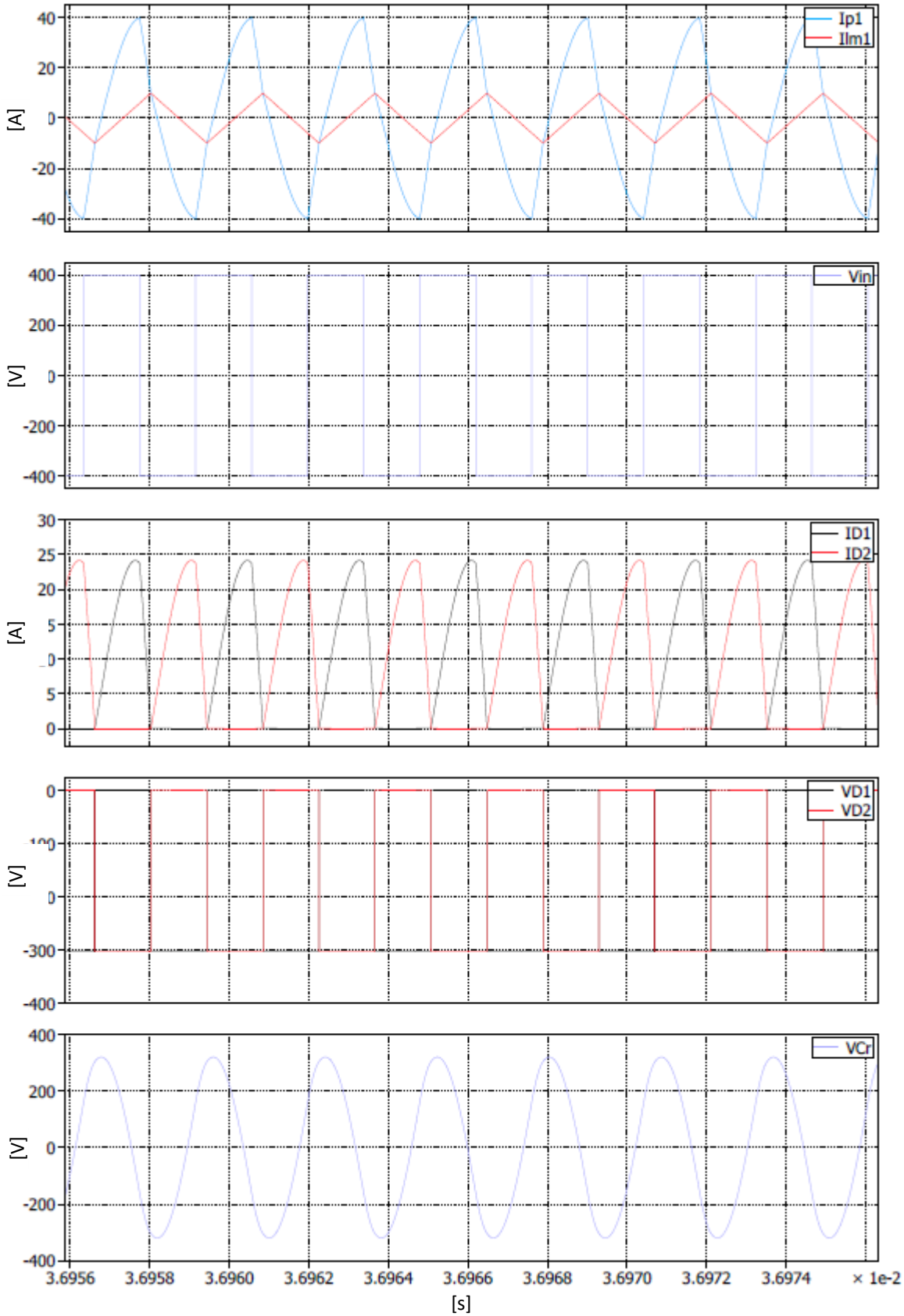


Figure 46: Current waveforms for Fsw=1.42 Vin=400V Vout=300V Iout=30A Pout=6kW

5 Conclusions

Recalling the Multi-Objective optimization framework in Figure 1, in this chapter conclusion are presented:

In Chapter 1:

The context and the motivation for this work was presented.

In Chapter 2:

First, the correlation of the semiconductor technology (Si, SiC and GaN) and their structures with their devices characteristics were explained in the first part of the chapter.

Second, it was shown that due to dynamic $R_{DS,on}$ and the lack of avalanche rate, GaN devices should be over dimension and until the vertical devices are not available, they will be exclusively used in the scientific world.

Third, it was illustrated how using the parameters listed in *Table 1* it is possible to improve the overall efficiency, power density and reliability of a converter at a Material-Component level of the optimization framework.

Fourth, the tradeoff between conduction and switching losses was explained and a graphical tool to select devices with and optimum tradeoff was presented.

Finally, a multi-objective optimization algorithm for semiconductor and heatsink selection was presented. This algorithm take in to account datasheet information of the components in order to make an initial screening. Follow by a measurement of static and dynamic parameters that enable to identify the ideal switching condition of each devices, instead of doing a 1 to 1 comparison of the candidates in the same switching condition.

In Chapter 3

First, pros and cos of the different reluctance and power loss model for the magnetic components were discussed. Then, based on the aforementioned analysis a multi-objective optimization algorithm for the inductor and transformer design was presented.

In Chapter 4

A case study of a 22kW LLC On Board Charger design was presented. The design was based on the methodology presented in Chapter 2 and 3 in order to be able to optimize both at component and material level the figures of merits of the converter. Using this case study a procedure for the design of next generation OBC converter was illustrated. This methodology enables to find the boundary condition between Si diodes and SiC diodes in this particular application. Moreover, it shows that wide

output voltage LLC converters have a frequency limitation due to the AC voltage of the resonant capacitor Cr and the DC bias of the magnetic components. The fact that in literature there are several LLC converters with an $F_r > 300kHz$, could be misleading for the Fr selection of a wide output voltage LLC converter. This thesis illustrates that the aforementioned converter can work at this frequency because they work exclusively at resonance. Finally, the case study also shows that the inductance ration λ of the LLC converter is inversely proportional to frequency. Therefore, it is compulsory to use DC-Link Voltage modulation in order to provide the desired range of output voltages.

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