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Full Digital Control and Multi-Loop Tuning of a Three-Level T-Type Rectifier for Electric Vehicle Ultra-Fast Battery Chargers †

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Abstract: The rapid development of electric vehicle ultra-fast battery chargers is increasingly demanding higher efficiency and power density. In particular, a proper control of the grid-connected active front–end can ensure minimum passive component size (i.e., limiting design oversizing) and reduce the overall converter losses. Moreover, fast control dynamics and strong disturbance rejection capability are often required by the subsequent DC/DC stage, which may act as a fast-varying and/or unbalanced load. Therefore, this paper proposes the design, tuning and implementation of a complete digital multi-loop control strategy for a three-level unidirectional T-type rectifier, intended for EV ultra-fast battery charging. First, an overview of the operational basics of three-level rectifiers is presented and the state-space model of the considered system is derived. A detailed analysis of the mid-point current generation process is also provided, as this aspect is widely overlooked in the literature. In particular, the converter operation under unbalanced split DC-link loads is analyzed and the converter mid-point current limits are analytically identified. Four controllers (i.e., dq-currents, DC-link voltage and DC-link mid-point voltage balancing loops) are designed and their tuning is described step-by-step, taking into account the delays and the discretization introduced by the digital control implementation. Finally, the proposed multi-loop controller design procedure is validated on a 30 kW, 20 kHz T-type rectifier prototype. The control strategy is implemented on a single general purpose microcontroller unit and the performances of all control loops are successfully verified experimentally, simultaneously achieving low input current zero-crossing distortion, high step response and disturbance rejection dynamics, and stable steady-state operation under unbalanced split DC-link loading.

Keywords: digital control; grid-connected converters; three-level T-type rectifier; VIENNA rectifier; active front-end; power factor corrector; battery charging; ultra-fast charging; electric vehicles

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1. Introduction

Despite the steady performance improvement of Li-ion batteries, their weight and cost still impair mass-market vehicle electrification [1]. A widespread DC ultra-fast charging (UFC) infrastructure could alleviate the limited range issue of electric vehicles (EVs), by enabling charging times comparable with the refueling of internal combustion engine (ICE) vehicles. As the pace of adoption of EVs is rapidly increasing and thousands of DC fast-charging stations are being installed around the world [2,3], ultra-fast battery charging is currently a key research topic in both industry and academia. In fact, several challenges have yet to be addressed, including the potentially negative impact on the grid of a fast charging station [4–6], the need for high-performance power electronics technology [7], the presence of competing industry standards, and battery health/thermal degradation issues related to high charging speeds [8].

State-of-the-art EV UFCs are typically rated above 150 kW [7] and are normally connected to the low-voltage grid, mainly to leverage the existing industrial power electronics knowledge and availability [7,9–11]. The basic structure of a DC off-board charger is schematically illustrated in Figure 1 and consists of two conversion stages [7,10]. The first stage is connected to the grid and is referred to as active front–end (AFE). The main role of this stage is to ensure input unity power factor and sinusoidal current shaping [12]. The second stage is an isolated DC/DC converter which provides galvanic isolation from the grid and controls the charging process by regulating the current fed into the battery [13]. The present work only focuses on the AFE stage.

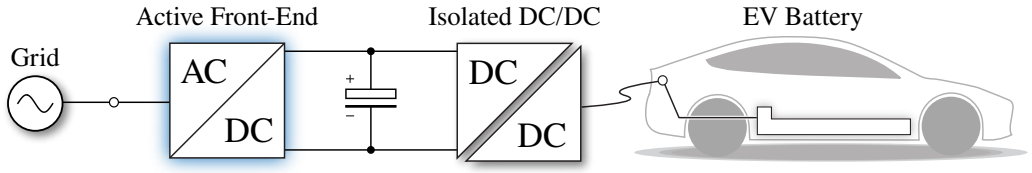

Figure 1. Schematic overview of an electric vehicle (EV) ultra-fast battery charger.

As of today, the two-level inverter represents the most adopted solution for general active rectification, as it is simple, reliable and intrinsically bidirectional. Nevertheless, the overall performance of this topology is strongly limited by its two-level output voltage waveform (i.e., requiring large AC-side filtering elements) and the high voltage rating of the semiconductor devices (i.e., characterized by limited conduction and switching performance) [14–16]. These limitations translate into a severe performance trade-off between achievable efficiency and power density, which may prove to be insufficient for the targeted UFC application. The most effective approach to enhance the overall performance of the converter is by adopting multi-level topologies, which simultaneously reduce the stress on the AC-side filter components and allow to employ semiconductor devices with lower voltage rating and thus better figures of merit [17].

Since DC fast chargers usually require unidirectional power flow from the grid to the vehicle, three-level rectifiers represent excellent candidates for active rectification [18–20]. These converter topologies trade higher efficiency and power density for a slight complexity increase, thus achieving improved performance with respect to two-level inverters [14–16].

In addition to high efficiency and high power density, the main requirements of an AFE for battery charging applications may be summarized in (1) sinusoidal input current shaping (i.e., with low distortion and harmonics); (2) DC-link voltage regulation according to the optimal DC/DC operating point [13]; (3) minimization of the DC-link mid-point third-harmonic voltage oscillation, that is typical of three-level converters [21,22]; and (4) control of the mid-point voltage deviation under unbalanced split DC-link loading [23], which may occur when separate DC/DC units are connected to the two DC-link halves [24]. All of these tasks require a proper converter control strategy with adequate dynamical performance, which is therefore the subject of this work. In particular, (1) can be achieved with a high-bandwidth current control loop (i.e., to limit low-frequency harmonics) and a purposely designed grid-side filter (i.e., to attenuate high-frequency harmonics) [25,26]. Tasks (2) and (4) are managed with a DC-link voltage and a mid-point voltage balancing loops having sufficient dynamics to ensure low voltage deviation under load or unbalance steps. Finally, (3) is achieved with an appropriate selection of the converter modulation strategy [22,27]. It is worth highlighting that the elimination of the low-frequency mid-point voltage ripple is of utmost importance, as the DC/DC stage may not be able to reject it [13]. Battery chargers, in fact, cannot allow significant charging current ripple, as this would cause the premature aging and shorter lifetime of the battery itself [28].

The digital control implementation of power converters has recently become an industry standard, mainly due to the advent of modern, powerful, reliable and low-cost digital signal processors (DSPs). The well-known benefits of digital controllers reside in excellent reproducibility, noise immunity and flexibility, allowing for the implementation of

complex control strategies [29]. Despite these advantages, the digital implementation of the control is also affected by limited computational capabilities and sampling, quantization and zero-order hold (ZOH) effects that may negatively impact the control itself.

Specifically, the control of three-level rectifiers is characterized by unique challenges. First, due to their unidirectional nature, rectifiers are characterized by discontinuous conduction mode (DCM) operation around the current zero-crossings, leading to low-frequency current distortion [30]. Moreover, the presence of a split DC-link translates into an additional system state variable, requiring a supplementary control loop with respect to two-level inverters. Primarily for these reasons, several works dealing with the control of unidirectional three-level rectifiers have been published in the literature [31–35].

In particular, ref. [31] is the first proposing a multi-loop control strategy for a three-level unidirectional rectifier. The three phase currents are regulated by means of hysteresis controllers, while the DC-link voltage and the mid-point voltage deviation are regulated with traditional proportional (P) or proportional–integral (PI) regulators. While the mid-point voltage balancing loop acts on the common-mode current reference, no clear quantitative relation between this reference and the resulting mid-point current is provided. Therefore, no clear tuning of this control loop is achieved.

In [33], a digital multi-loop control strategy is implemented for a VIENNA rectifier operated at 1 MHz. However, the focus of the work is limited to the current controllers and their practical implementation, in order to improve the phase current distortion around the zero-crossings. No details on the DC-link voltage and mid-point voltage balancing control loops are provided.

A complete system small-signal model of the unidirectional three-level rectifier is derived in [32]. This model is then leveraged to design and tune four control loops, namely regulating the dq currents, the DC-link voltage and the mid-point voltage deviation. Nevertheless, the tuning coefficients are extremely complex and a straightforward expression linking the zero-sequence voltage injection with the mid-point current formation is not provided.

This expression is derived in [34], where the mid-point current formation process is analyzed and a simple link between the zero-sequence voltage injection and the resulting mid-point current is found. This link is exploited for the tuning of the mid-point voltage balancing loop, leading to predictable dynamical performance. Nevertheless, the actual converter mid-point current limits are not derived and no limitation on the zero-sequence voltage injection is enforced, possibly leading to uncontrolled phase current distortion for significant load unbalance values.

The instantaneous mid-point current limits of a unidirectional rectifier are obtained in [35], where a multi-loop control scheme is also implemented. The current controllers are tuned taking into account the delays related to their digital implementation. However, no tuning of the DC-link voltage and mid-point voltage balancing loops is provided. Moreover, even though the zero-sequence voltage injection is dynamically limited within its feasible window, no mid-point current limitation is implemented, leading to the uncontrolled wind-up of the PI regulator in the case of large load unbalances.

Even though the complete state-space model of three-level rectifiers has been analyzed in the literature and multi-loop control strategies have already been proposed, to the best of the authors' knowledge, a simple, clear and exhaustive control loop design and tuning procedure has yet to be provided. In particular, no implementation of the DC-link mid-point voltage balancing loop taking into account the converter mid-point current limits has been proposed to date.

Therefore, this paper proposes a complete multi-loop control strategy for a unidirectional three-level rectifier, with the main goal of providing a straightforward design and tuning procedure of all controllers. The major contributions of this work are summarized in: (1) the design, tuning, simulation and experimental verification of a multi-loop digital control scheme for unidirectional three-level rectifiers; (2) the formal derivation of the converter instantaneous zero-sequence voltage limits and their implementation in the closed-loop control; and (3) the analytical derivation of the converter mid-point current

limits, which are exploited for the implementation of an anti-wind-up scheme within the DC-link mid-point voltage balancing control loop. It must be noted that this work is an extension of [12], where the proposed control strategy has been briefly introduced. The analysis is here extended and verified with the inclusion of exclusive experimental results.

This paper is structured as follows. In Section 2, the operational basics of three-level rectifiers are described and the system state-space model is derived. In Section 3, the proposed multi-loop control strategy is reported and all controllers are analytically tuned, leveraging the system state-space equations. In Section 4, the small-signal transfer functions of the closed-loop controllers are verified in simulation, and both steady-state and dynamical performance of all control loops are verified experimentally on a 30 kW T-type converter prototype, leveraging a general purpose microcontroller unit (MCU) for the digital control implementation. Finally, Section 5 summarizes and concludes this work.

2. System Model

The system considered herein consists of a three-level unidirectional rectifier fed from the three-phase grid and two independent equivalent current source loads, as illustrated in Figure 2. It is worth noting that, even though the T-type converter topology is specifically selected in the present analysis, the following considerations remain valid for all unidirectional three-level topologies with a split DC-link, i.e., for all the implementations of the VIENNA rectifier [36]. Furthermore, to simplify the analysis, no inner grid impedance and no AC-side filter are considered. Both elements do not affect the general control considerations of this work, particularly when the filter is properly damped [25,37,38].

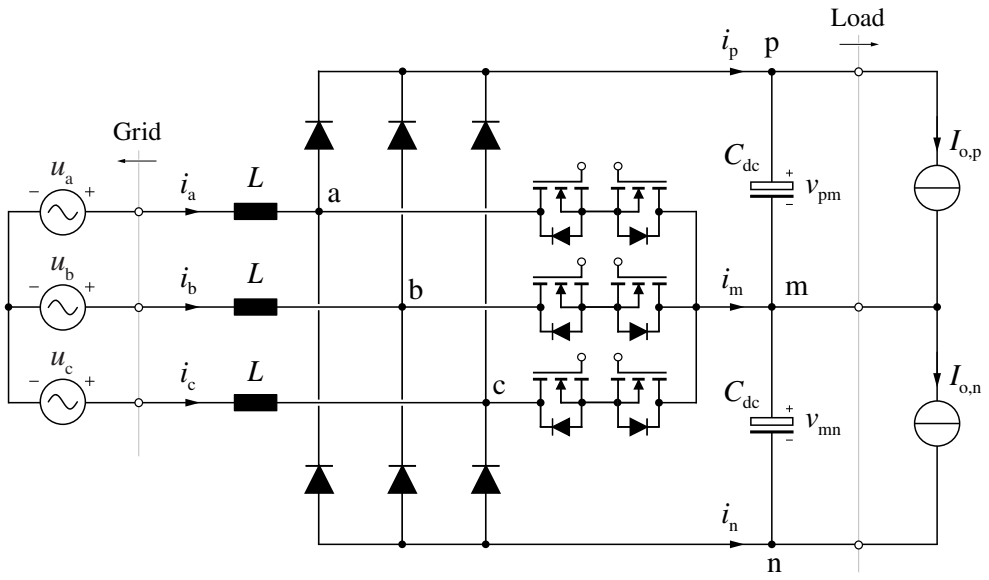

Figure 2. Schematic of the considered system, consisting of an ideal grid, a three-phase three-level unidirectional T-type rectifier and two independent equivalent current-source loads.

The AC-side and DC-side passive components define the system state-variables, namely the boost inductor currents i_a, i_b, i_c and the DC-link capacitor voltages v_{pm} and v_{mn}. In particular, the three-wire nature of the system (i.e., lacking the neutral conductor) implies:

$$i_a + i_b + i_c = 0, \tag{1}$$

such that only two inductor currents are independent. Furthermore, the two capacitor voltage state variables are better expressed by

$$v_{dc} = v_{pm} + v_{mn}, \tag{2}$$

$$v_m = v_{pm} - v_{mn}, \tag{3}$$

where v_{dc} is the full DC-link voltage and v_m represents the mid-point voltage deviation (i.e., $v_m = 0$ in nominal operating conditions, being $v_{pm} = v_{mn} = v_{dc}/2$).

With the adoption of a dq reference frame synchronized with the grid voltage vector $\vec{u}$ (i.e., in the direction of the d-axis), the system state-space equations can be expressed in a compact form, as

$$\begin{cases} L\,\dfrac{di_d}{dt} = u - v_d + \omega L i_q \\ L\,\dfrac{di_q}{dt} = -v_q - \omega L i_d \\ \dfrac{C_{dc}}{2}\,\dfrac{dv_{dc}}{dt} = \dfrac{i_p - i_n}{2} - \dfrac{I_{o,p} + I_{o,n}}{2} \\ C_{dc}\,\dfrac{dv_m}{dt} = -i_m - (I_{o,p} - I_{o,n}) \end{cases} \tag{4}$$

where i_p, i_m, i_n are the DC-link rail currents (with $i_p + i_m + i_n = 0$), $I_{o,p}$, $I_{o,n}$ are the split DC-link load currents and v_d, v_q are the phase voltages applied by the rectifier in the dq reference frame. The derived state-space equations can be expressed with an equivalent circuit representation, as illustrated in Figure 3.

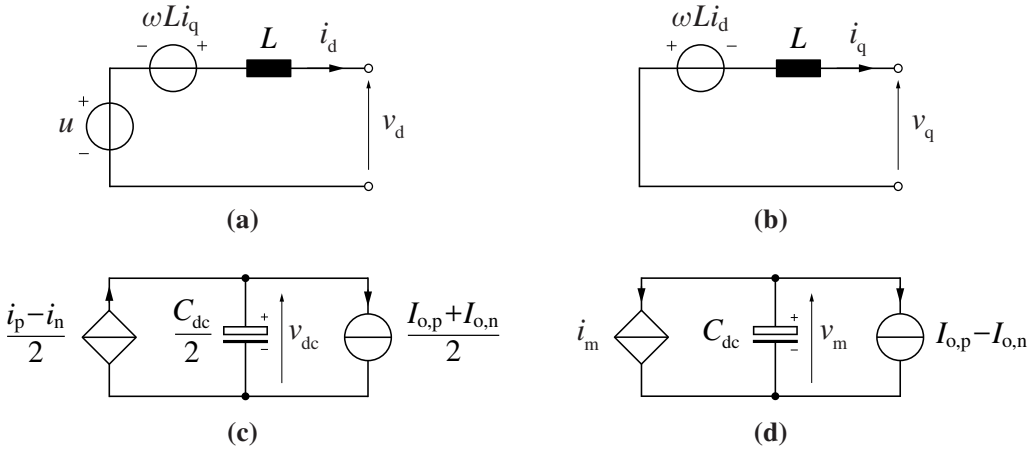

Figure 3. Equivalent circuit representation of the system state-space equations: (**a**) d-axis current; (**b**) q-axis current; (**c**) DC-link voltage; and (**d**) mid-point voltage deviation.

In order to solve the state-space system (4), the relationship between the DC-side currents i_p, i_m, i_n and the state variables must be identified.

Assuming balanced DC-link voltages (i.e., $v_{pm} = v_{mn} = v_{dc}/2$), a first relation between AC-side and DC-side quantities is obtained leveraging the input/output power balance as

$$P = v_a\,i_a + v_b\,i_b + v_c\,i_c = \frac{3}{2}\,(v_d\,i_d + v_q\,i_q) = v_{pm}\,i_p - v_{mn}\,i_n \approx \frac{1}{2}\,v_{dc}\,(i_p - i_n). \tag{5}$$

The DC-link voltage state-space equation can therefore be expressed as

$$\frac{C_{dc}}{2}\,\frac{dv_{dc}}{dt} = \frac{3}{2}\,\frac{v_d\,i_d + v_q\,i_q}{v_{dc}} - \frac{I_{o,p} + I_{o,n}}{2}, \tag{6}$$

which is non-linear with respect to v_{dc}.

A second relation between AC-side and DC-side quantities can be derived leveraging the mid-point current i_m generation process. Several past works have investigated and described this process as being governed by the zero-sequence voltage component v_o injected by the converter [21,23,34]. In particular, v_o does not affect the phase currents (assuming a three-phase three-wire system); nevertheless, this voltage component modifies

the duty cycle of the mid-point switches, thus affecting the mid-point current local average value, expressed by

$$i_{\mathrm{m}} = \tau_{\mathrm{a}}\, i_{\mathrm{a}} + \tau_{\mathrm{b}}\, i_{\mathrm{b}} + \tau_{\mathrm{c}}\, i_{\mathrm{c}}. \tag{7}$$

τ_{x} represents the relative ON-time (i.e., duty cycle) of the mid-point switches of phase x = a, b, c and is determined by the ratio between the desired reference bridge-leg voltage $v_{\mathrm{xm}} = v_{\mathrm{x}} + v_{\mathrm{o}}$ and the DC-link voltage v_{dc} as

$$\tau_{\mathrm{x}} = 1 - \frac{2}{v_{\mathrm{dc}}}\,|v_{\mathrm{xm}}| = 1 - \frac{2}{v_{\mathrm{dc}}}\,|v_{\mathrm{x}} + v_{\mathrm{o}}| \qquad \mathrm{x} = \mathrm{a},\, \mathrm{b},\, \mathrm{c}. \tag{8}$$

Recalling that $i_{\mathrm{a}} + i_{\mathrm{b}} + i_{\mathrm{c}} = 0$, the expression of the mid-point current local average becomes:

$$i_{\mathrm{m}} = \sum_{\mathrm{x}=\mathrm{a},\mathrm{b},\mathrm{c}} \left(i_{\mathrm{x}} - \frac{2}{v_{\mathrm{dc}}} |v_{\mathrm{x}} + v_{\mathrm{o}}|\, i_{\mathrm{x}} \right) = \sum_{\mathrm{x}=\mathrm{a},\mathrm{b},\mathrm{c}} -\frac{2}{v_{\mathrm{dc}}} |v_{\mathrm{x}} + v_{\mathrm{o}}|\, i_{\mathrm{x}}. \tag{9}$$

Moreover, since the voltage applied by a bridge-leg of a unidirectional rectifier can only have the same sign as the current flowing in it (i.e., $v_{\mathrm{xm}} = 0$ when the mid-point switch is ON and $v_{\mathrm{xm}} = \mathrm{sign}(i_{\mathrm{x}})\, v_{\mathrm{dc}}/2$ when the switch is OFF), the following relation holds:

$$|v_{\mathrm{xm}}|\, i_{\mathrm{x}} = |v_{\mathrm{x}} + v_{\mathrm{o}}|\, i_{\mathrm{x}} = (v_{\mathrm{x}} + v_{\mathrm{o}})\, |i_{\mathrm{x}}| \quad \mathrm{x} = \mathrm{a},\, \mathrm{b},\, \mathrm{c}. \tag{10}$$

Therefore, substituting (10) into (9), the mid-point current local average can be expressed as

$$i_{\mathrm{m}} = \sum_{\mathrm{x}=\mathrm{a},\mathrm{b},\mathrm{c}} -\frac{2}{v_{\mathrm{dc}}} (v_{\mathrm{x}} + v_{\mathrm{o}})\, |i_{\mathrm{x}}| = -\frac{2}{v_{\mathrm{dc}}} \left[\sum_{\mathrm{x}=\mathrm{a},\mathrm{b},\mathrm{c}} v_{\mathrm{x}}\, |i_{\mathrm{x}}| \; + v_{\mathrm{o}} \sum_{\mathrm{x}=\mathrm{a},\mathrm{b},\mathrm{c}} |i_{\mathrm{x}}| \right]. \tag{11}$$

To obtain a quantitative evaluation of i_{m}, the phase voltage and phase current expressions are required. Neglecting the voltage drop at fundamental frequency across the boost inductance L, the phase voltages applied by the rectifier are:

$$\begin{cases} v_{\mathrm{a}} \approx u_{\mathrm{a}} = M\, \dfrac{v_{\mathrm{dc}}}{2}\, \cos(\vartheta) \\ v_{\mathrm{b}} \approx u_{\mathrm{b}} = M\, \dfrac{v_{\mathrm{dc}}}{2}\, \cos(\vartheta - \frac{2}{3}\pi) \\ v_{\mathrm{c}} \approx u_{\mathrm{c}} = M\, \dfrac{v_{\mathrm{dc}}}{2}\, \cos(\vartheta - \frac{4}{3}\pi) \end{cases}, \tag{12}$$

where $\vartheta = \omega t = 2\pi f t$ is the phase angle and $M \in [0,\, 2/\sqrt{3}]$ is the converter modulation index. The phase currents, assuming unity power factor operation, are therefore:

$$\begin{cases} i_{\mathrm{a}} = I\, \cos(\vartheta) \\ i_{\mathrm{b}} = I\, \cos(\vartheta - \frac{2}{3}\pi) \\ i_{\mathrm{c}} = I\, \cos(\vartheta - \frac{4}{3}\pi) \end{cases}. \tag{13}$$

By averaging the value of i_{m} over one-third of the fundamental period (i.e., the DC-side current periodicity), the expression of the mid-point current periodical average can be derived. Furthermore, subdividing v_{o} into a third-harmonic component $v_{\mathrm{o},3}$ representative of the selected modulation strategy and an additional component $v_{\mathrm{o},\delta}$ reserved for control purposes, the following expression is obtained:

$$I_{\mathrm{m}} = \frac{3}{2\pi} \int_0^{2\pi/3} i_{\mathrm{m}}\, \mathrm{d}\vartheta = -\frac{3}{\pi\, v_{\mathrm{dc}}} \int_0^{2\pi/3} \left[\sum_{\mathrm{x}=\mathrm{a},\mathrm{b},\mathrm{c}} v_{\mathrm{x}}\, |i_{\mathrm{x}}| \; + v_{\mathrm{o},3} \sum_{\mathrm{x}=\mathrm{a},\mathrm{b},\mathrm{c}} |i_{\mathrm{x}}| \; + v_{\mathrm{o},\delta} \sum_{\mathrm{x}=\mathrm{a},\mathrm{b},\mathrm{c}} |i_{\mathrm{x}}| \right] \mathrm{d}\vartheta. \tag{14}$$

Since the first two terms are characterized by $2\pi/3$ periodicity, their integral is null, therefore:

$$I_{\mathrm{m}} = -\frac{3}{\pi\, v_{\mathrm{dc}}} \int_{0}^{2\pi/3} v_{\mathrm{o},\delta} \sum_{\mathrm{x}=\mathrm{a,b,c}} |i_{\mathrm{x}}|\, \mathrm{d}\vartheta. \tag{15}$$

This equation can be used to estimate the effect of a constant $v_{\mathrm{o},\delta}$ contribution (i.e., added to all phase voltage references) on the generated average mid-point current. However, the solution of (15) is not straightforward, as the instantaneous zero-sequence voltage $v_{\mathrm{o}} = v_{\mathrm{o},3} + v_{\mathrm{o},\delta}$ is dynamically limited with a $2\pi/3$ periodicity, directly affecting the applied $v_{\mathrm{o},\delta}$. The upper and lower v_{o} limits can be derived from the well-known current-dependent bridge-leg voltage limits, meaning that:

$$\begin{cases} 0 \le v_{\mathrm{xm}} \le +\dfrac{v_{\mathrm{dc}}}{2} & i_{\mathrm{x}} > 0 \\ -\dfrac{v_{\mathrm{dc}}}{2} \le v_{\mathrm{xm}} \le 0 & i_{\mathrm{x}} < 0 \end{cases} \qquad \mathrm{x} = \mathrm{a,\ b,\ c}, \tag{16}$$

which may be rewritten as

$$\begin{cases} v_{\mathrm{xm}} \le \dfrac{\mathrm{sign}(i_{\mathrm{x}}) + 1}{2}\, \dfrac{v_{\mathrm{dc}}}{2} \\ v_{\mathrm{xm}} \ge \dfrac{\mathrm{sign}(i_{\mathrm{x}}) - 1}{2}\, \dfrac{v_{\mathrm{dc}}}{2} \end{cases} \qquad \mathrm{x} = \mathrm{a,\ b,\ c}. \tag{17}$$

Leveraging $v_{\mathrm{xm}} = v_{\mathrm{x}} + v_{\mathrm{o}}$, the following maximum and minimum zero-sequence voltage limits are obtained:

$$\begin{cases} v_{\mathrm{o,max}} = \min\left[\dfrac{v_{\mathrm{dc}}}{4}(\mathrm{sign}(i_{\mathrm{x}}) + 1) - v_{\mathrm{x}}\right] \\ v_{\mathrm{o,min}} = \max\left[\dfrac{v_{\mathrm{dc}}}{4}(\mathrm{sign}(i_{\mathrm{x}}) - 1) - v_{\mathrm{x}}\right] \end{cases} \qquad \mathrm{x} = \mathrm{a,\ b,\ c}. \tag{18}$$

These limits are graphically illustrated in Figure 4 for two different values of DC-link voltage and assuming unity power factor operation (i.e., $\mathrm{sign}(i_{\mathrm{x}}) = \mathrm{sign}(v_{\mathrm{x}})$). It is shown that a v_{dc} increase (i.e., a reduction in M) widens the feasible zero-sequence injection region, thus increasing the mid-point current control capability of the converter.

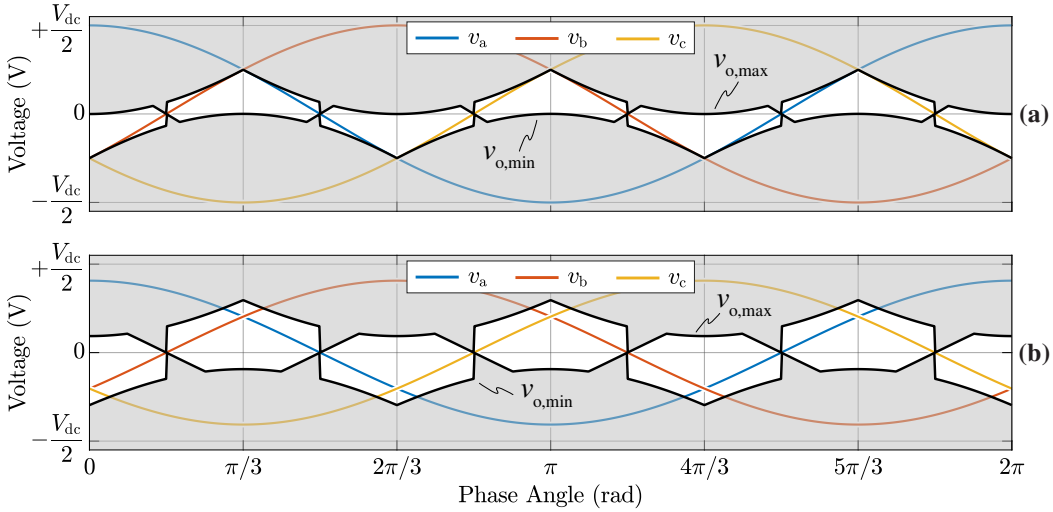

Figure 4. Zero-sequence voltage limits $v_{\mathrm{o,max}}$, $v_{\mathrm{o,min}}$ for $v_{\mathrm{dc}} = 650\,\mathrm{V}$ (**a**) and $v_{\mathrm{dc}} = 800\,\mathrm{V}$ (**b**), assuming a 400 V line-to-line grid voltage and unity power factor operation.

Even though $v_{o,max}$ and $v_{o,min}$ modify the shape of the applied $v_{o,\delta}$, i.e., effectively reducing its average value, a simple expression of I_m can be obtained by neglecting the zero-sequence voltage limits and solving (15):

$$I_m \approx -\frac{12}{\pi}\frac{i_d}{v_{dc}}v_{o,\delta}. \tag{19}$$

It is worth noting that this expression overestimates the mid-point current value, particularly for high values of $v_{o,\delta}/v_{dc}$. Nevertheless, (19) sets an upper limit for I_m, which is of practical interest in ensuring the stability of the mid-point voltage control loop. The state-space equation of the DC-link mid-point voltage deviation v_m can therefore be expressed as

$$C_{dc}\frac{dv_m}{dt} = \frac{12}{\pi}\frac{i_d}{v_{dc}}v_{o,\delta} - (I_{o,p} - I_{o,n}), \tag{20}$$

which is the last equation to practically solve system (4).

The validity of (19) can be extended if a zero-sequence third-harmonic component $v_{o,3}$ is added to the reference signals. This component is defined by the adopted modulation strategy, which directly affects the stresses on the active and passive components of the converter (e.g., AC inductors, DC-link capacitors, semiconductor devices) [22,27]. To minimize the size of the split DC-link capacitors and ensure minimum mid-point voltage ripple, the zero mid-point current modulation (ZMPCPWM) is adopted herein. This modulation ensures a zero mid-point current local average over the whole fundamental period by injecting a specific low-frequency zero-sequence voltage waveform, which may be directly derived from (11), setting $i_m = 0$:

$$v_{o,3} = -\frac{v_a|i_a| + v_b|i_b| + v_c|i_c|}{|i_a| + |i_b| + |i_c|}. \tag{21}$$

A comparison between the average mid-point current obtained with sinusoidal modulation (SPWM), i.e., without low-frequency zero-sequence component injection, ZMPCPWM and expression (19) is reported in Figure 5. It is immediately observed that the addition of a $v_{o,3}$ component ensures a wider validity of (19); however, it does not affect the maximum I_m value, as explained in Appendix A.

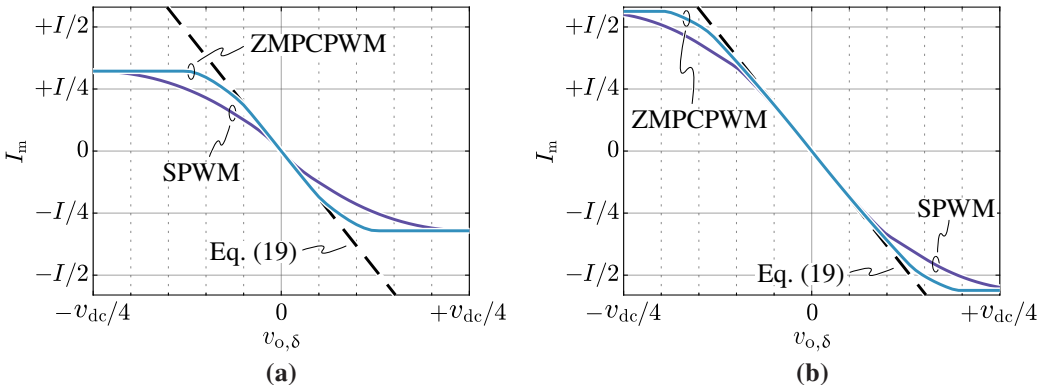

Figure 5. Mid-point current periodical average I_m as a function of the zero-sequence voltage injection $v_{o,\delta}$ for $v_{dc} = 650$ V (**a**) and $v_{dc} = 800$ V (**b**). Results obtained with sinusoidal modulation (SPWM) and zero mid-point current modulation (ZMPCPWM) are compared to (19).

3. Controller Design

In this work, a 30 kW T-type unidirectional rectifier operating with a 20 kHz switching frequency is considered (see Section 4). The converter is connected to the European low-voltage grid (i.e., 50 Hz, 400 V line-to-line) and the DC-link voltage can be varied between 650 V and 800 V to narrow the regulation region of the following DC/DC conversion stage,

thus simplifying its design [24] and control [13]. The most relevant parameter values for control purposes are $L = 150\,\mu H$ (i.e., at the peak phase current $I = 61.5\,A$) and $C_{dc} = 4080\,\mu F$.

The converter is controlled by means of a cascaded multi-loop structure consisting of four loops, which correspond to the state-space variables in (4), namely the DC-link voltage loop, the mid-point voltage balancing loop and the phase current loops in the dq frame, as illustrated in Figure 6. A conventional voltage-oriented control is adopted [25]: the grid synchronization is obtained by means of a phase-locked loop (PLL) [39], aligning the d-axis of the rotating dq frame with the phase voltage vector $\vec{u}$ measured at the point of common coupling (PCC). The outer v_{dc} loop is responsible for controlling the DC-link capacitor voltage according to the reference value required by the DC/DC stage, forcing the power balance between the grid and the load. As a consequence, the output of this controller is the d-axis current reference (i.e., responsible for the power transfer), while the q-axis current reference is set to zero to ensure unity power factor operation. Ultimately, the role of the v_m loop is to control the mid-point voltage deviation to zero, thus ensuring the voltage balance between the two series-connected DC-link capacitors. The v_m loop operates in parallel to the cascaded v_{dc}, i_{dq} loops (i.e., without interference), since it acts on the zero-sequence voltage injection, which does not affect the phase currents and thus the overall power transfer. It is worth highlighting that the v_m loop allows for the steady-state operation with a certain degree of load unbalance between the two DC-link halves (i.e., $I_{o,p} \neq I_{o,n}$).

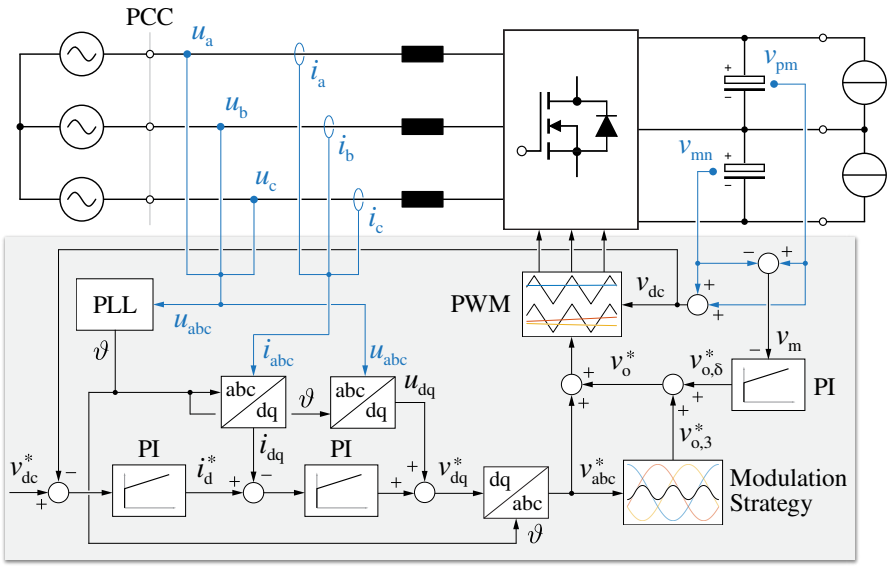

Figure 6. Simplified schematic overview of the converter control, including the dq current i_{dq}, DC-link voltage v_{dc} and mid-point voltage v_m controllers. Detailed schematics of the control loops are provided in Figures 7–9, respectively.

The main goals of the proposed control scheme are (1) sinusoidal input current shaping, ensuring low THD and low-frequency harmonics; (2) strong disturbance rejection of the DC-link voltage against load steps; and (3) low steady-state and dynamical mid-point voltage deviation, even under unbalanced split DC-link loads.

3.1. dq Current Control Loops

The current control is implemented in the rotating dq frame to achieve zero steady-state tracking error with a simple proportional–integral (PI) regulator and maximize the disturbance rejection performance of the loops. The measured PCC voltages (see Figure 6) are fed into the PLL, achieving the reference frame synchronization with the grid (i.e., angle ϑ). Even though only two-phase currents are independent, all three of them are measured for redundancy reasons, enhancing the measurement offset and gain compensations. The d-axis reference current i_d^*, responsible for the active power transfer, is provided by the DC-link voltage control loop, while the q-axis reference i_q^* is set to zero for unity power

factor operation. The digital sampling and update is performed once per switching period (i.e., $f_s = f_{sw} = 20\,\text{kHz}$).

Due to the unidirectional nature of the rectifier, the phase currents encounter discontinuous conduction mode (DCM) operation around the current/voltage zero-crossings [30]. In particular, DCM operation poses two major control challenges, which may lead to steady-state and dynamical issues, if not properly addressed [40]. First, conventional synchronous/asynchronous sampling does not provide the average phase current value under DCM conditions, due to the discontinuous nature of the current ripple. This may lead to noticeable current distortion around the zero crossings, due to the variable current feedback error. The second challenge is represented by the system transfer function (i.e., duty-to-current) becoming non-linear in DCM and thus translating in a variable open-loop gain. The gain is typically much lower than in continuous conduction mode (CCM) and thus reduces the control-loop bandwidth, inevitably leading to additional input current distortion. The first issue is tackled by oversampling the measured currents and averaging the sampled values, thus obtaining a moving average of the phase currents. The second issue, instead, is not directly addressed, nevertheless, the system gain drop in DCM is managed by maximizing both the control bandwidth and the low-frequency open-loop gain (i.e., by means of the integral part of the PI regulator).

The digital implementation of the current control loop introduces three main delay components, which negatively affect the achievable control bandwidth and/or decrease the closed loop stability margin [41,42]. The current oversampling and averaging process introduces the first delay component, i.e., a moving average delay of $T_s/2$ (where T_s is the sampling period). The second delay contribution is related to the digital processing, which yields a pure delay of one sampling period T_s between the measured quantities and the control signal output. Finally, the PWM modulator introduces a zero-order hold (ZOH) effect of one sampling period, which may be treated as a $T_s/2$ delay if the control bandwidth is sufficiently lower than the Nyquist frequency. Overall, the total resulting delay of $2T_s$ can be expressed with the transfer function:

$$G_{d,i}(s) = e^{-s\,2T_s} \approx \frac{1 - sT_s}{1 + sT_s}, \tag{22}$$

where the exponential term is rationalized with a first-order Padè approximation.

The voltage-to-current plant transfer functions in the dq frame can be derived from (4) by disregarding the disturbance components (i.e., easily compensated by suitable feed-forward terms) as

$$G_{p,i}(s) = \frac{i_d(s)}{v_d(s)} = \frac{i_q(s)}{v_q(s)} = \frac{1}{sL}. \tag{23}$$

The integral nature of the plant allows for a zero steady-state tracking error with a proportional regulator. Nevertheless, a PI controller is adopted to achieve better disturbance rejection performance and higher low-frequency open-loop gain, especially required to counteract the DCM-induced distortion around the current zero-crossings. Therefore, the controller transfer function is:

$$G_{c,i}(s) = k_{P,i} + \frac{k_{I,i}}{s}. \tag{24}$$

To improve the dynamical performance of the control loops and ensure the small-signal operation of the PI regulator, the phase voltages and the current cross-coupling terms are fed forward. The complete current closed-loop control schematic is illustrated in Figure 7. The open-loop control transfer function is therefore:

$$G_{ol,i}(s) = G_{d,i}(s)\,G_{p,i}(s)\,G_{c,i}(s). \tag{25}$$

Since simplified rational transfer functions have been derived for every component of $G_{ol,i}(s)$, the tuning of the PI regulator can be performed in the continuous time domain leveraging conventional techniques. A phase margin criteria is adopted in this work. The

open-loop 0 dB cross-over frequency $\omega_{c,i}$ is obtained by substituting (22)–(24) into (25) and setting $|G_{ol,i}(j\omega_{c,i})| = 1$, resulting in:

$$\omega_{c,i} = \frac{1}{T_s} \frac{\sqrt{[1+k_z^2]\left[1+\tan^2\left(m_\varphi\right)\right]} - k_z - \tan\left(m_\varphi\right)}{1 - k_z \tan\left(m_\varphi\right)} \tag{26}$$

where m_φ is the desired open-loop phase margin (i.e., expressed in radians) and k_z is the ratio between the PI zero $\omega_{z,i} = k_{I,i}/k_{P,i}$ and $\omega_{c,i}$. If $\omega_{z,i}$ is located sufficiently below $\omega_{c,i}$ (i.e., $k_z \ll 1$), the following approximate relation holds:

$$\omega_{c,i} \overset{k_z \ll 1}{\approx} \frac{1}{T_s}\left[-\tan(m_\varphi) + \sqrt{1+\tan^2(m_\varphi)}\right], \tag{27}$$

Therefore, the PI parameters are directly obtained as

$$\begin{cases} k_{P,i} = \omega_{c,i} L \dfrac{1}{\sqrt{1+k_z^2}} \overset{k_z \ll 1}{\approx} \omega_{c,i} L \\ k_{I,i} = \omega_{z,i} k_{P,i} \end{cases}. \tag{28}$$

In this work, $m_\varphi = 60°$ and $k_z = 1/5$ are assumed, ensuring a good compromise among reference tracking speed, step response overshoot and disturbance rejection capability. For the system considered herein (i.e., with $f_s = 20$ kHz), a 850 Hz open-loop cross-over frequency is obtained, which roughly corresponds to the closed-loop control bandwidth.

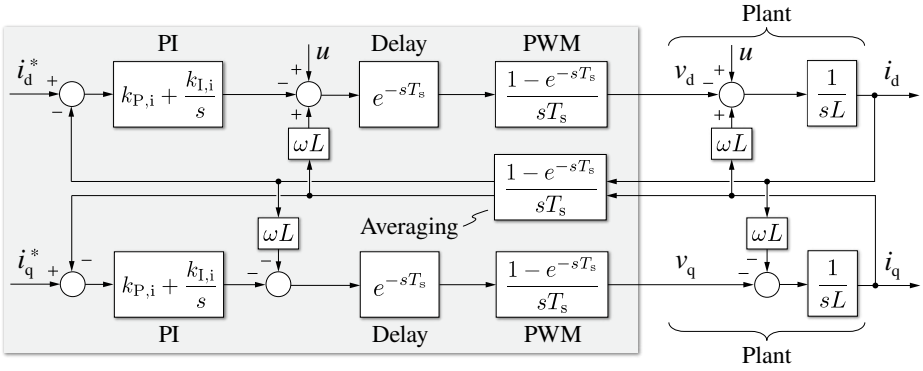

Figure 7. Detailed equivalent block diagram of the i_d and i_q current control loops.

It is worth mentioning that, since soft-saturating powder core inductors have been adopted for the experimental prototype (see Section 4), the worst-case value of L used in (28) corresponds to the minimum inductance value at the nominal peak current (i.e., $L = 150$ µH at $I = 61.5$ A). This approach ensures that the maximum closed-loop control bandwidth is never exceeded; however, it does not compensate for the differential inductance variation, leading to variable control bandwidth along the grid fundamental period (i.e., depending on the instantaneous phase current value) and lower dynamical performance at low current levels. Another approach is to control the three phase currents in the abc stationary frame and compensate for the phase inductance variation with three independent time-varying open-loop gain adjustments, as in [43]. Nevertheless, this approach lacks the benefits related to the dq frame current control implementation (e.g., ideally zero steady-state reference-tracking error) and has therefore not been adopted in this work.

3.2. DC-Link Voltage Control Loop

In general, the DC-link voltage controller of an active rectifier is responsible to adjust the active power absorbed from the grid to balance the power absorbed from the load. In the present case, the load is represented by the isolated DC/DC stage of the ultra-

fast battery charger, which sets the v_{dc} loop reference according to an optimal operating efficiency criterion [24]. To regulate the DC-link voltage, this control loop acts on the d-axis current reference, which directly adjusts the active power transfer. Assuming the DC-side load currents $I_{o,p}$, $I_{o,n}$ as disturbance components and considering $i_q = i_q^* = 0$ for unity power factor operation, the current-to-voltage plant transfer function is obtained from (6) as

$$G_{p,v}(s) = \frac{v_{dc}(s)}{i_d(s)} = \frac{3}{2}\frac{v_d}{v_{dc}}\frac{2}{sC_{dc}}, \tag{29}$$

which is non-linear with respect to v_{dc}.

The DC-link voltage control structure is illustrated in Figure 8. The control loop consists of a PI regulator, an optional feed-forward contribution, two gain adjustment blocks, the current control loop and the plant transfer function.

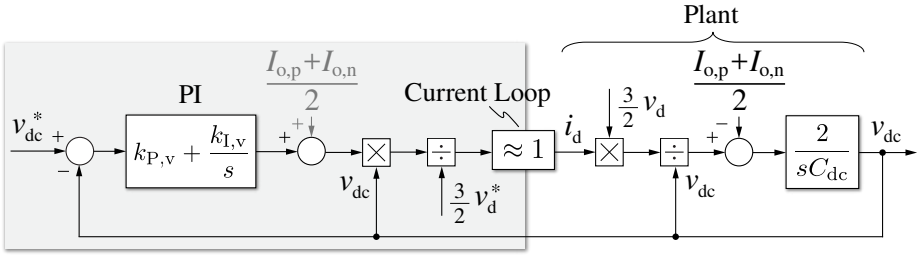

Figure 8. Detailed equivalent block diagram of the v_{dc} voltage control loop.

Even though the plant has an integral behavior, a PI regulator is selected to improve the controller load disturbance rejection capabilities. Therefore, the controller transfer function is:

$$G_{c,v} = k_{P,v} + \frac{k_{I,v}}{s}. \tag{30}$$

As the power absorbed by the DC/DC stage is generally known with reasonable accuracy (i.e., the reference charging power), $I_{o,p}$ and $I_{o,n}$ can easily be estimated and their values can be fed forward to unburden the integral part of the PI regulator. The plant non-linearity highlighted in (29) is compensated by multiplying the regulator output with the measured DC-link voltage v_{dc}. Moreover, the controller gain is adjusted to compensate for the dependence of the plant transfer function on the applied d-axis voltage v_d. The output of the regulator is then saturated to the maximum rectifier current I_{max} and becomes the reference for the inner d-axis current control loop. Since this loop is characterized by much faster dynamics with respect to the voltage control one, the current loop can be considered as an ideal actuator (i.e., a unity gain block). Therefore, the v_{dc} control open-loop transfer function is expressed by

$$G_{ol,v} = \frac{2}{3}\frac{v_{dc}}{v_d} G_{p,v}(s)\, G_{c,v}(s) \tag{31}$$

The tuning of the PI regulator is performed assuming that the cross-over frequency of the voltage control loop $\omega_{c,v}$ is set sufficiently low compared to the current control loop one $\omega_{c,i}$. With this assumption, the inner loop does not dynamically affect the outer one, leading to simple tuning expressions:

$$\begin{cases} k_{P,v} = \omega_{c,v}\dfrac{C_{dc}}{2} \\ k_{I,v} = \omega_{z,v}\, k_{P,v} \end{cases}. \tag{32}$$

In this work, $\omega_{c,v}$ is set to $\omega_{c,i}/10$, resulting in a 85 Hz open-loop cross-over frequency. Moreover, the PI zero $\omega_{z,v}$ is set to $\omega_{c,v}/2$, to maximize the disturbance rejection capabilities of the control loop.

3.3. DC-Link Mid-Point Voltage Balancing Loop

Since three-level rectifiers are characterized by a split DC-link (see Figure 2), a voltage unbalance between the upper and lower capacitors may either appear under normal operating conditions, due to device and/or control non-idealities, or under unbalanced load conditions (i.e., $I_{o,p} \neq I_{o,n}$). In particular, a steady-state and/or dynamical load unbalance can appear in battery charging applications when separate DC/DC units are connected to the two DC-link halves, as in [24]. In all cases, the closed-loop control of the DC-link mid-point voltage deviation v_m is required, both to limit the voltage stress on the semiconductor devices to $v_{dc}/2$ and to ensure the symmetry between the AC-side voltages applied by the rectifier during the positive and negative grid half-cycles. The control of v_m is achieved by acting on the zero-sequence voltage injection level to vary the mid-point current periodical average I_m, as explained in Section 2. Since the zero-sequence voltage v_o does not affect the AC-side currents, and thus the active power transfer, the v_m control loop does not directly interfere with the other closed-loop controllers. The plant transfer function is therefore obtained from (20), by considering the DC-side load currents $I_{o,p}$, $I_{o,n}$ as disturbance components:

$$G_{p,b}(s) = \frac{v_m(s)}{v_{o,\delta}(s)} = -\frac{12}{\pi}\frac{i_d}{v_{dc}}\frac{1}{sC_{dc}}. \tag{33}$$

The DC-link mid-point voltage balancing control structure is illustrated in Figure 9. The control loop consists of a moving average filter (MAF), a PI regulator, two gain adjustment blocks, the zero-sequence voltage saturation, and the plant transfer function.

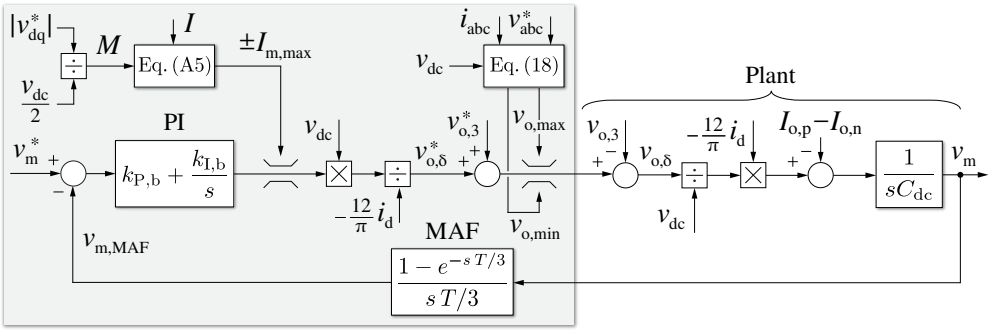

Figure 9. Detailed equivalent block diagram of the v_m voltage control loop.

The DC-link mid-point voltage deviation is obtained by the v_{pm}, v_{mn} measurements and is passed through an MAF running at three times the grid frequency, to prevent any feedback of the 150 Hz voltage oscillation that is obtained when ZMPCPWM is not adopted [21,27]. Therefore, v_m is sampled at the sampling frequency $f_s = 20$ kHz and averaged with three times the grid periodicity, introducing a moving average delay of $T/6$, where $T = 1/f$ is the grid fundamental period. The resulting delay transfer function is therefore expressed as

$$G_{d,b}(s) = \frac{1 - e^{-s\,T/3}}{s\,T/3} \approx e^{-s\,T/6} \approx \frac{1 - s\,T/12}{1 + s\,T/12}. \tag{34}$$

Also for this control loop, a PI regulator is adopted, to improve its disturbance rejection capabilities:

$$G_{c,b}(s) = k_{P,b} + \frac{k_{I,b}}{s}. \tag{35}$$

The output of the regulator corresponding to the desired mid-point current is saturated according to the minimum/maximum mid-point current limits expressed by (A5) (see Appendix A). In this way, a successful anti-wind-up scheme can be implemented, so that the integral action of the regulator is stopped once the current limits are hit. Since the plant transfer function $G_{p,b}$ depends on other state variables (i.e., i_d, v_{dc}), these are actively

compensated by adjusting the open loop gain with the measured quantities. In this way, stable controller dynamics are maintained for all operating conditions. Finally, the resulting reference is added to the zero-sequence third harmonic component $v_{o,3}$ derived from the selected modulation strategy, and is then saturated according to the upper and lower zero-sequence voltage limits reported in (18). This saturation process is of extreme importance, as a large input current distortion would arise without it (see Section 4). Overall, the v_m open-loop control transfer function is expressed by

$$G_{ol,b}(s) = -\frac{\pi}{12}\frac{v_{dc}}{i_d} G_{d,b}(s)\, G_{p,b}(s)\, G_{c,b}(s). \tag{36}$$

To prevent dynamical interference with the MAF, the DC-link mid-point voltage balancing loop cross-over frequency $\omega_{c,b}$ is set one decade lower than $3f$ (i.e., 15 Hz). The PI regulator coefficients are thus obtained as

$$\begin{cases} k_{P,b} = \omega_{c,b}\, C_{dc} \\ k_{I,b} = \omega_{z,b}\, k_{P,b} \end{cases}, \tag{37}$$

where the PI zero $\omega_{z,b}$ is set to $\omega_{c,b}/2$.

4. Simulation and Experimental Results

The controller design procedure described in Section 3 is here applied to a 30 kW unidirectional T-type rectifier operated at 20 kHz. This converter has been designed to take part in a modular and scalable ultra-fast battery charger consisting of N identical modules operated in parallel [38]. The specifications and the nominal operating conditions of the converter are summarized in Table 1. To validate the theoretical assumptions, the converter control small-signal behavior is tested in simulation environment and both steady-state and dynamical performances of all control loops are experimentally assessed on a converter prototype.

Table 1. Three-level unidirectional T-type rectifier specifications and nominal operating conditions.

Parameter	Description	Value
f	grid frequency	50 Hz
P	nominal active power	30 kW
V	peak phase voltage	325 V
I	peak phase current	61.5 A
V_{dc}	DC-link voltage	650–800 V
L	boost inductance	150–190 µH
C_{dc}	DC-link capacitance	4080 µF
f_{sw}, f_s	switching, control frequency	20 kHz

4.1. Simulation Results

A complete simulation of the system is set up in the PLECS environment, where the proposed multi-loop control strategy is implemented with a custom C-code script. The discretized execution of the MCU is simulated by triggering the control block once per sampling period (i.e., at $f_s = 20$ kHz) and making the outputs available at the following triggering instant. Furthermore, the current oversampling and averaging process is performed with 32 samples per period.

The analytical tuning of the control loops described in Section 3 is here verified. A set of circuit simulations is performed by providing sinusoidal references with different frequencies to each controller, measuring the system response, and deriving its magnitude and phase with a discrete Fourier transform (DFT). To comply with the unidirectional nature of the rectifier, a DC offset is added to the dq current references.

The closed-loop small-signal transfer function results, expressed as magnitude/phase Bode plots, are reported in Figure 10 and compared to the analytical transfer functions derived in Section 3. The analytical open-loop transfer functions are also shown for completeness. It is observed that the results of the simulation closely match the analytical expectations, thus providing a first validation of the proposed controller design procedure.

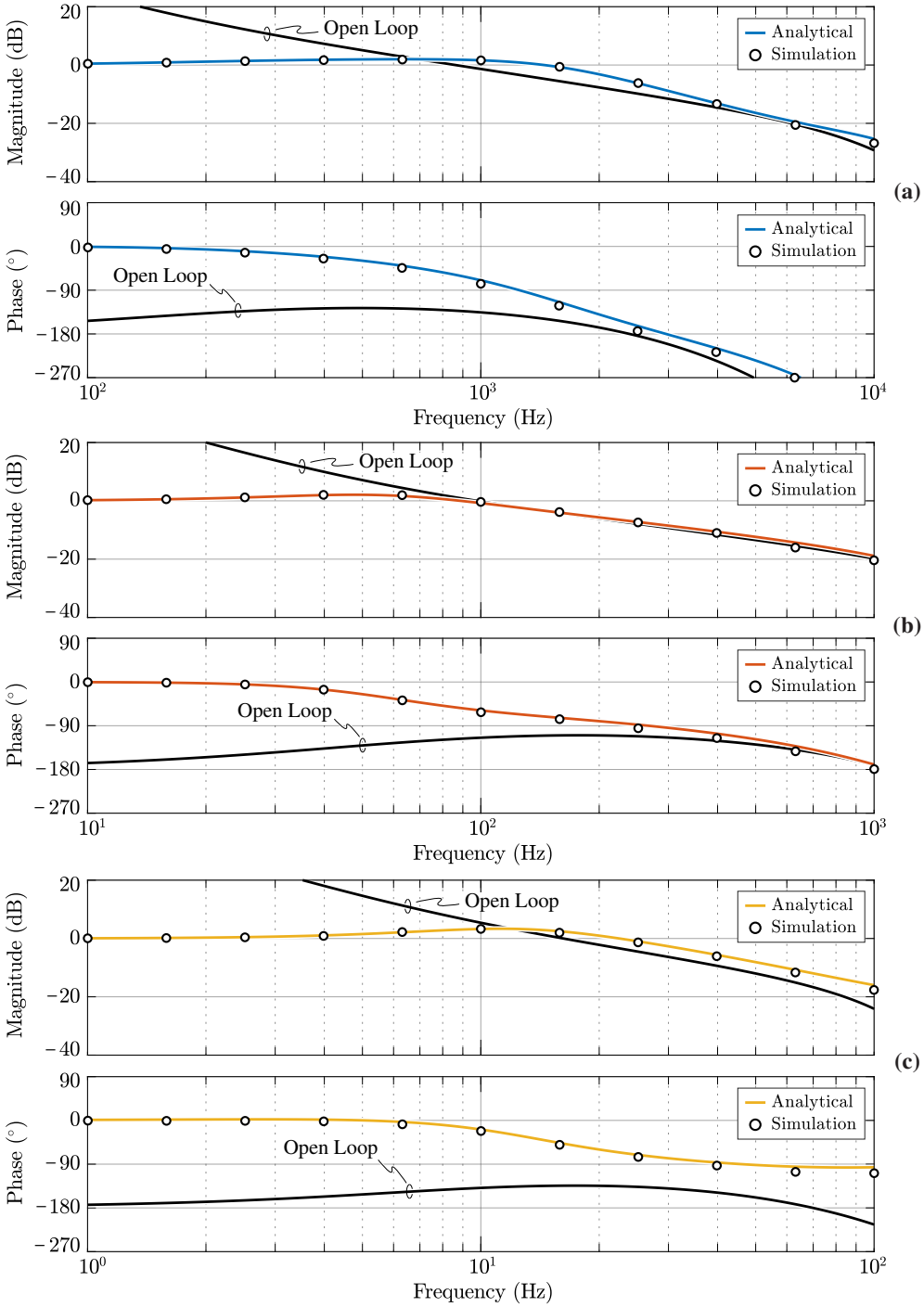

Figure 10. Comparison between analytically derived and simulated closed-loop transfer functions of (**a**) the dq axis current control loops; (**b**) the DC-link voltage control loop; and (**c**) the DC-link mid-point voltage balancing control loop. The analytical open-loop transfer functions are also shown.

4.2. Experimental Results

The steady-state and dynamical performance of the proposed control strategy are tested on the T-type rectifier prototype shown in Figure 11. This prototype employs 650 V

Si MOSFETs switching at 20 kHz and 1200 V Si fast-recovery diodes. Even though the rectifier consists of two three-phase 30 kW units connected in parallel, only one unit is operated for the experimental validation. The complete converter multi-loop control is implemented on a STM32G474VE MCU from ST Microelectronics [44] with an interrupt service routine running at $f_s = 20$ kHz.

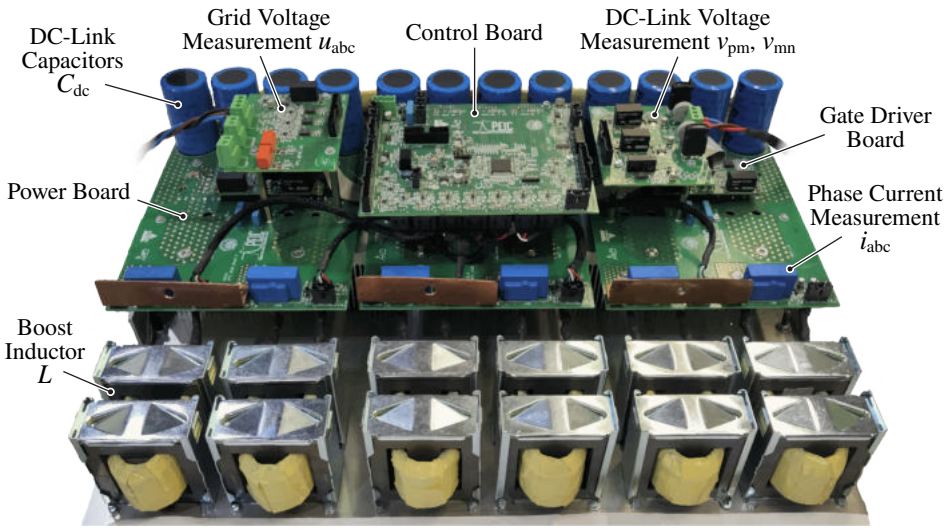

Figure 11. Overview of the 3-level unidirectional T-type rectifier prototype utilized for the experimental tests. The converter consists of two paralleled 30 kW units.

It is worth noting that the converter boost inductors (i.e., L) are designed according to the optimization procedure presented in [45] and employ XFlux 60µ powder cores from Magnetics [46], which feature a soft-saturating B–H characteristic. As already mentioned in Section 3, this property induces a variation in the differential inductance value during the grid period (i.e., following the average phase current value), translating into a variable plant gain and thus a variable current control bandwidth. Therefore, to ensure the control stability over the complete operating range of the rectifier, the worst-case value of L corresponding to the minimum inductance value at the nominal peak current (i.e., $L = 150$ µH at $I = 61.5$ A) is adopted for tuning. The detailed characteristics of the inductor design are reported in [38].

The experimental tests are performed using a grid emulator at the input side of the rectifier, emulating the European low-voltage grid (i.e., 50 Hz, 400 V line-to-line), and two independent electronic loads connected to the two DC-link halves, emulating a modular DC/DC converter stage as in [24]. All measurements are carried out with a Teledyne LeCroy 500 MHz, 12-bit, 10 GS/s, 8-channel oscilloscope, employing isolated high-voltage differential probes for voltage measurements and standard current probes for current measurements.

4.2.1. Steady-State Performance

The rectifier operation in stationary conditions is illustrated in Figure 12, where the measured grid voltages u_{abc} and phase currents i_{abc} are shown for different values of transferred power at $v_{dc} = 800$ V. It is observed that the phase currents are in all cases in phase with the grid voltages (i.e., unity power factor operation) and the current quality improves for higher loads. At 10% of the rated power, as shown in Figure 12b, the large ripple-to-average current ratio and the unidirectional nature of the rectifier lead to pronounced zero-crossing distortion. Nevertheless, even under these conditions, the current waveforms remain pseudo-sinusoidal, thanks to the high current control bandwidth (i.e., high open-loop gain at low frequency) and the feed-forward contributions illustrated in Figure 7. The current waveform quality improves dramatically at 50% and 100% of the rated power, as the relative current ripple decreases and the DCM-related zero-crossing distortion becomes negligible. Since no AC-side LCL filter is considered in this work (i.e., for the sake of simplicity), the actual THD of the current absorbed from the grid cannot

be directly evaluated. Nevertheless, this is done in [38], where a THD lower than 5% is achieved for power levels as low as 20% of the rated power (i.e., 6 kW), therefore validating the claimed control performance in terms of low input current distortion.

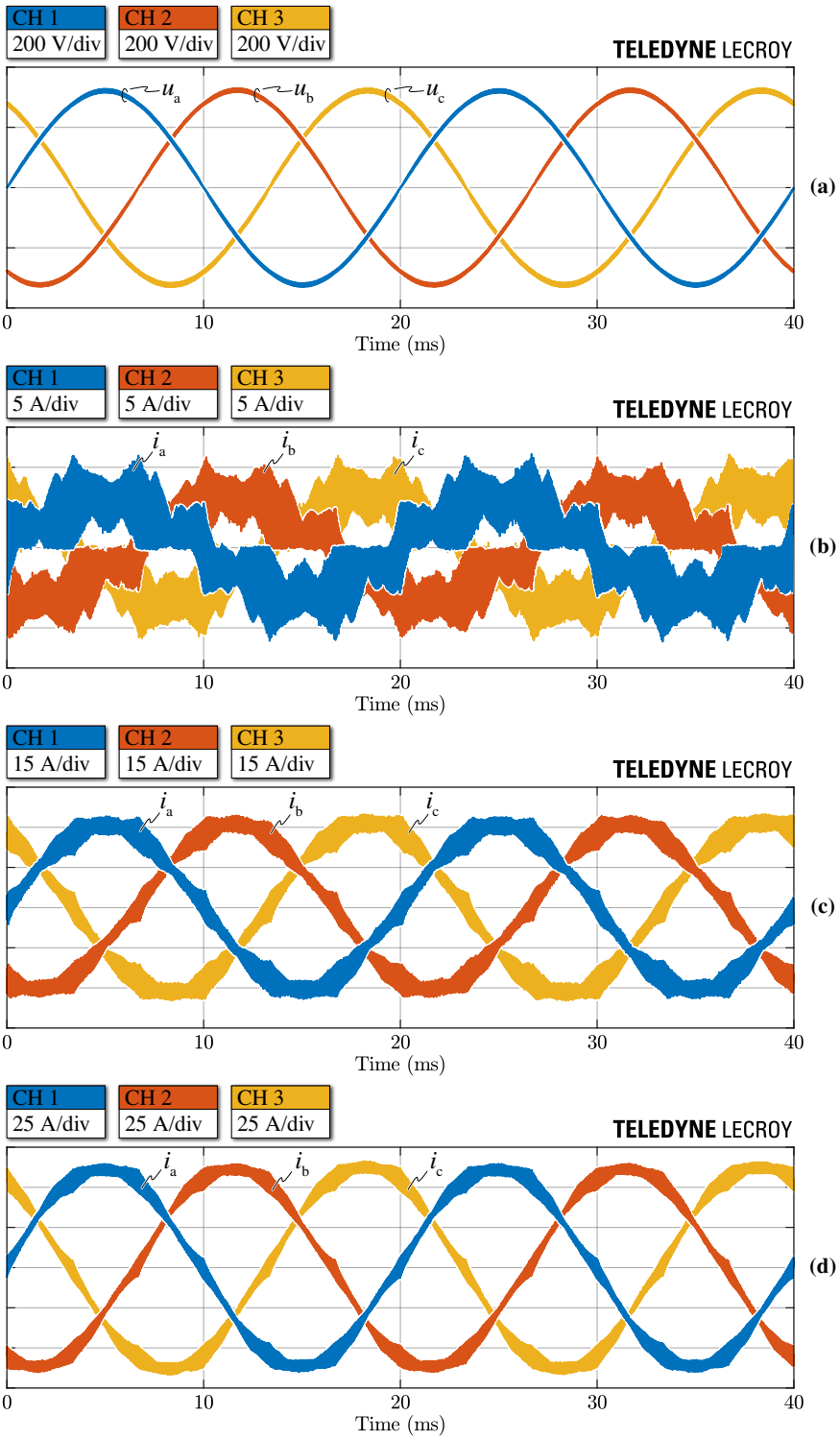

Figure 12. Experimental waveforms under steady-state conditions with $v_{dc} = 800$ V and ZMPCPWM. Measured grid voltage waveforms u_{abc} (**a**) and phase current waveforms i_{abc} at 10% (**b**), 50% (**c**) and 100% (**d**) of the nominal power (i.e., $P = 30$ kW).

The steady-state reference bridge-leg voltages v^*_{am}, v^*_{bm}, v^*_{cm} and zero-sequence voltage v^*_o are illustrated in Figure 13 with $v_{dc} = 800$ V and adopting ZMPCPWM. Figure 13a high-

lights the pure zero-sequence third-harmonic injection of ZMPCPWM, with $v_{o,\delta} = 0$ and thus $v_o = v_{o,3}$. Figure 13b,c, instead, show the effect of the addition of a $v_{o,\delta}$ contribution to the third-harmonic component (i.e., $v_o = v_{o,3} + v_{o,\delta}$). In particular, the $v_{o,\delta}$ contribution shifts upwards the bridge-leg voltage and zero-sequence voltage references, hitting the zero-sequence voltage limit $v_{o,max}$ expressed in (18) and thus causing the saturation of the voltages themselves.

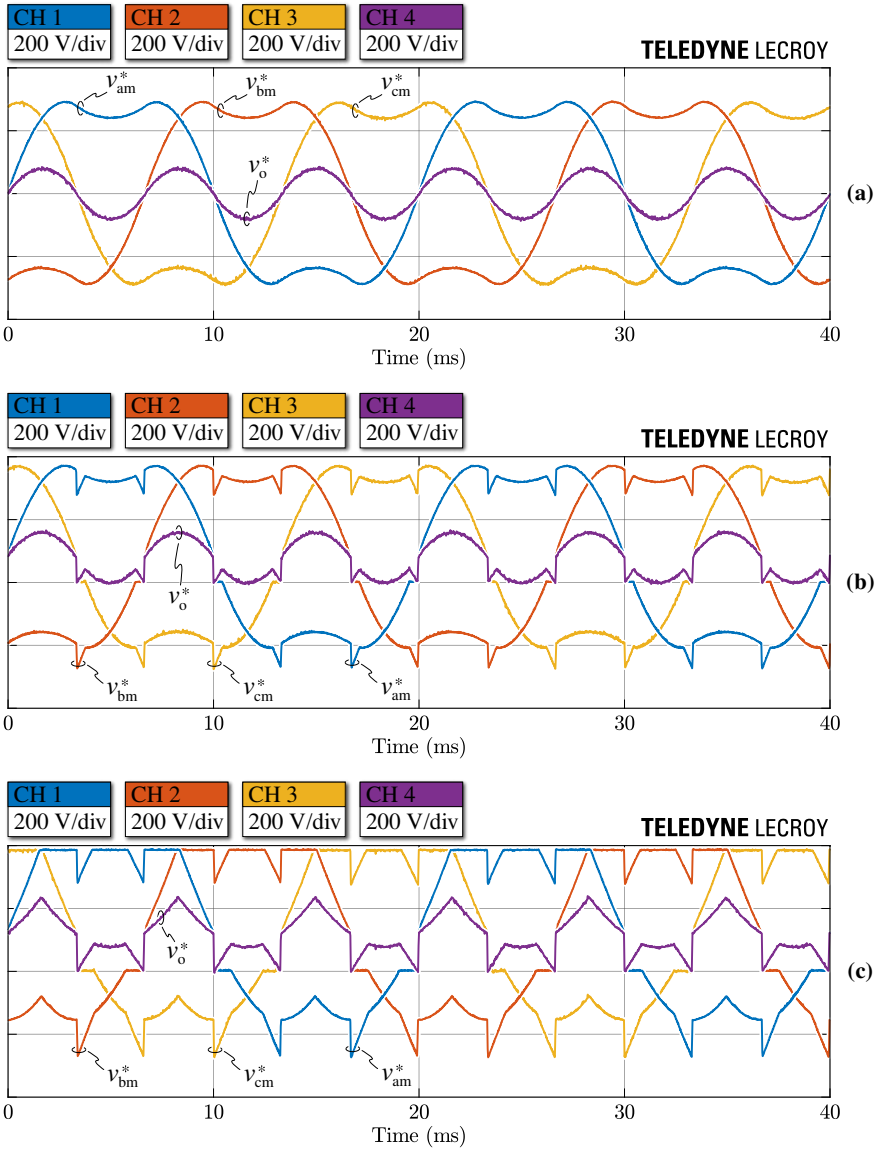

Figure 13. Experimental waveforms in steady-state conditions with $v_{dc} = 800\,V$ and ZMPCPWM. Reference rectifier bridge-leg voltages v^*_{am}, v^*_{bm}, v^*_{cm} and zero-sequence voltage v^*_o for $v_{o,\delta} = 0$ (**a**), $v_{o,\delta} = 0.1\,v_{dc}$ (**b**) and $v_{o,\delta} = 0.2\,v_{dc}$ (**c**). The waveforms are obtained from the digital-to-analog converter (DAC) of the MCU (i.e., with a 0–3.3 V measurement range), therefore they are rescaled.

It is worth noting that the zero-sequence voltage saturation is of utmost importance, since it ensures that only feasible bridge-leg voltages are applied (i.e., considering the sign of the phase currents) and avoids the asymmetrical saturation of the voltage references, which would lead to large and uncontrolled phase current distortion. The rectifier phase currents i_{abc} and mid-point current periodical average I_m with $v_{o,\delta} = 0.2\,v_{dc}$ are illustrated with and without the zero-sequence voltage saturation in Figure 14a,b, respectively. It is observed that, without the zero-sequence voltage saturation, the current controllers are no longer able to ensure sinusoidal current shaping, as the reference phase voltages cannot

be applied by the rectifier and get distorted. This in particular proves the ability of the proposed control scheme to provide stable and undistorted operation under split DC-link loading (i.e., $I_m \neq 0$). Finally, Figure 14 also highlights that the injection of a positive zero-sequence voltage component $v_{o,\delta}$ yields a negative mid-point current periodical average I_m.

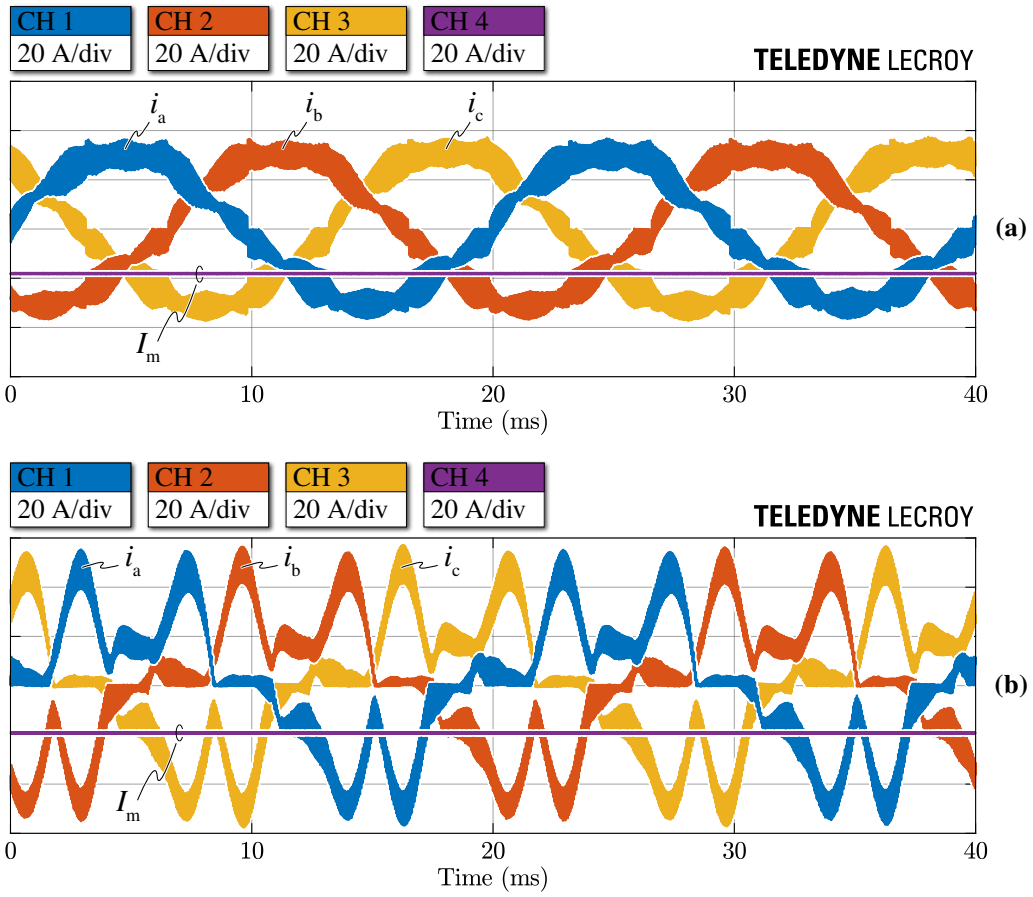

Figure 14. Experimental waveforms in steady-state conditions at $P = 15\,\text{kW}$ with $v_{dc} = 800\,\text{V}$, $v_{o,\delta} = 0.2\,v_{dc}$ and ZMPCPWM. Measured phase current waveforms i_{abc} and mid-point current periodical average I_m with zero-sequence voltage limitation $v_{o,max/min}$ enabled (**a**) and disabled (**b**).

The mid-point current generation capabilities of the rectifier are assessed by varying the injected zero-sequence voltage $v_{o,\delta}$ for different DC-link voltage v_{dc} values. The obtained mid-point current periodical average I_m is illustrated in normalized form (i.e., divided by the phase peak current I) in Figure 15a,b, where the results for both ZMPCPWM and SPWM are reported, respectively. It is observed that the injection of a zero-sequence third harmonic component $v_{o,3}$ (i.e., ZMPCPWM) extends the linear $I_m(v_{o,\delta})$ trend to lower DC-link voltage values (i.e., higher modulation index M), as previously pointed out in Section 2. In particular, the measurements reported in Figure 15 closely match the results from simulation (e.g., see Figure 5), with a maximum error of 2% over the complete evaluation range.

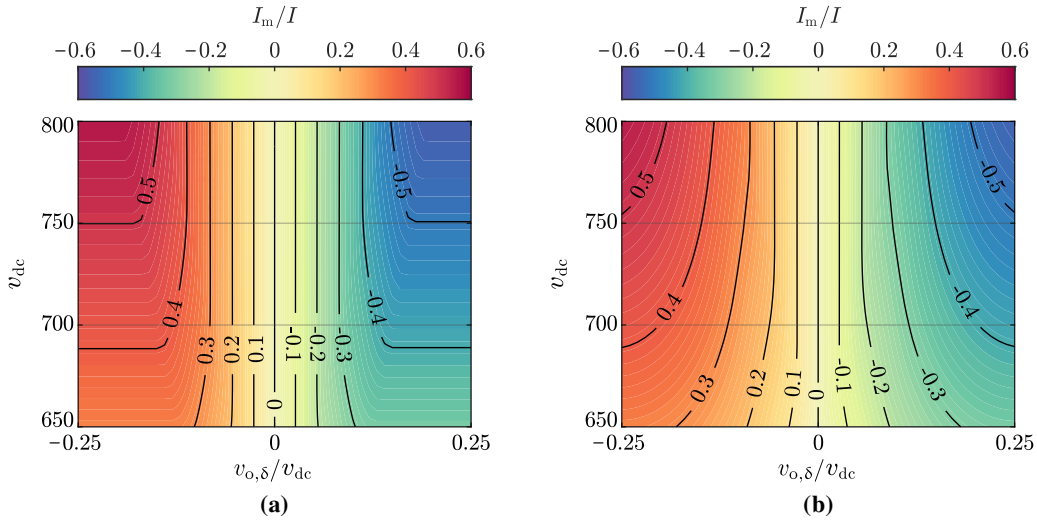

Figure 15. Experimental mid-point current periodical average I_m (i.e., normalized with respect to the phase peak current I) as a function of $v_{o,\delta}/v_{dc}$ and v_{dc}, adopting ZMPCPWM (**a**) and SPWM (**b**).

4.2.2. Dynamical Performance

The large-signal dynamical performance of the current control loop is verified by testing the system response to a d-axis current reference i_d^* step. The measured phase currents i_{abc} and d-axis current i_d for a current step between 50% and 100% of the nominal rated current $I = 61.5\,A$ are shown in Figure 16. A fast rise-time of ≈0.4 ms and a ≈15% overshoot are observed, validating the tuning procedure proposed in Section 3. It is worth noting that i_d is discretized in time, since it is measured at the output of a digital-to-analog converter (DAC) of the MCU and is updated once per control period (i.e., $T_s = 50\,\mu s$).

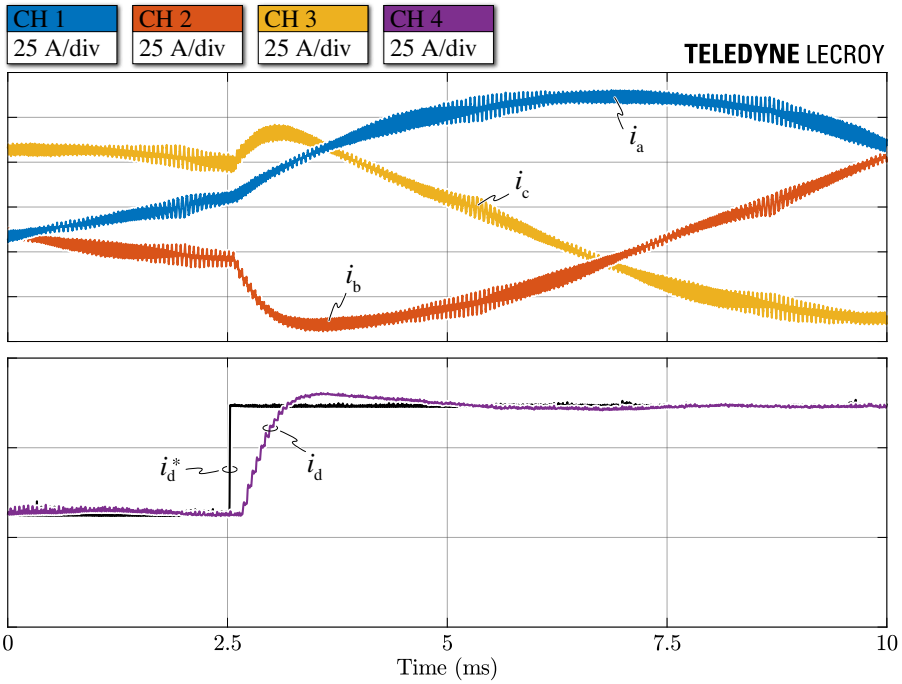

Figure 16. Experimental current control loop reference step response between 50% and 100% of the nominal current (i.e., $I = 61.5\,A$) with $v_{dc} = 800\,V$ and ZMPCPWM. Measured phase currents i_{abc}, d-axis current reference i_d^* and d-axis current i_d. The d-axis quantities are obtained from the DAC of the MCU (i.e., with a 0–3.3 V measurement range), therefore they are rescaled.

The dynamical performance of the DC-link voltage control loop is verified with two different tests.

First, the system response to a v_{dc}^* reference step is evaluated. Figure 17 shows the DC-link voltage control loop response to a reference step change between $v_{dc} = 650\,V$ and $v_{dc} = 800\,V$. Due to the large DC-link voltage variation, the PI controller output saturates at the maximum converter current limit I_{max} and v_{dc} rises linearly, avoiding overshoots. It is observed that the two cascaded control loops (i.e., outer v_{dc} loop and inner i_d loop) are well decoupled due to the 10 times different bandwidth (see Section 3); therefore, they do not interfere.

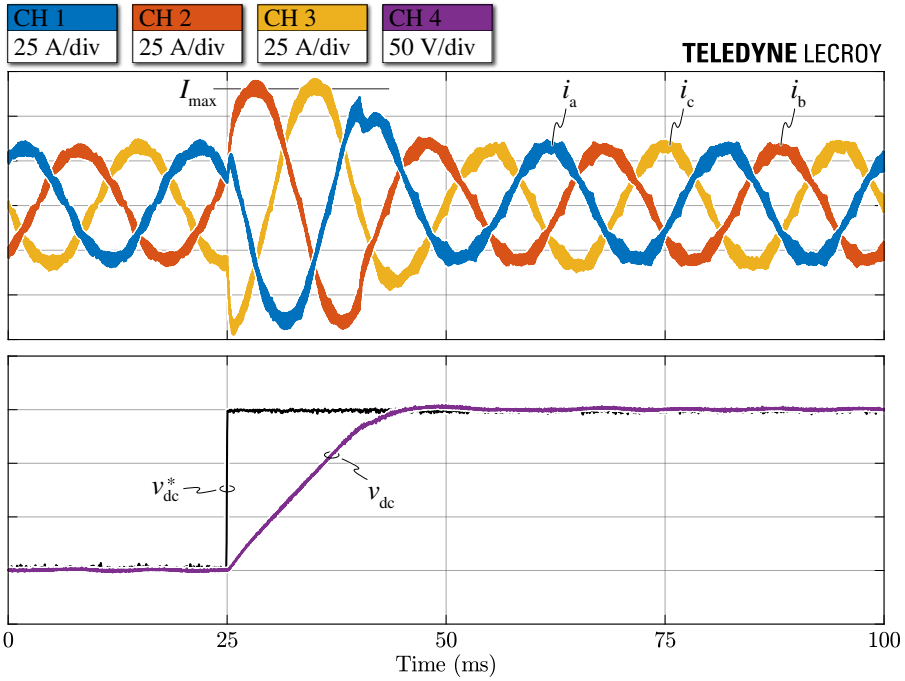

Figure 17. Experimental DC-link voltage control loop reference step response between $v_{dc} = 650\,V$ and $v_{dc} = 800\,V$ with a constant load power $P_o = 15\,kW$ and ZMPCPWM. Measured phase currents i_{abc}, DC-link voltage reference v_{dc}^* and DC-link voltage v_{dc}. The DC-link voltage reference is obtained from the DAC of the MCU (i.e., with a 0–3.3 V measurement range); therefore, it is rescaled.

The second test evaluates the disturbance rejection capability of the control loop, by assessing the DC-link voltage deviation following a load step. To strictly evaluate the dynamical performance of the controller, the feed-forward contribution $(I_{o,p} + I_{o,n})/2$ shown in Figure 8 is disabled. Figure 18 shows the system response to a 10 kW load step between $P_o = 22.5\,kW$ and $P_o = 12.5\,kW$. A maximum voltage deviation of $\approx$15 V is observed, mostly counteracted by the large low-frequency open-loop gain of the controller, which ensures the desired high disturbance rejection performance. It is worth noting that, since the rectifier is unable to reverse the power transfer, the currents are temporarily controlled to zero in reaction to the DC-link voltage overshoot. During this time interval, the DC-link voltage decreases almost linearly due to the constant power absorbed by the load, and the system dynamics are therefore uncontrolled (i.e., they are dictated by the load).

Therefore, with these two tests, the DC-link voltage control loop is successfully verified, featuring the desired fast large-signal control dynamics and strong disturbance rejection capabilities.

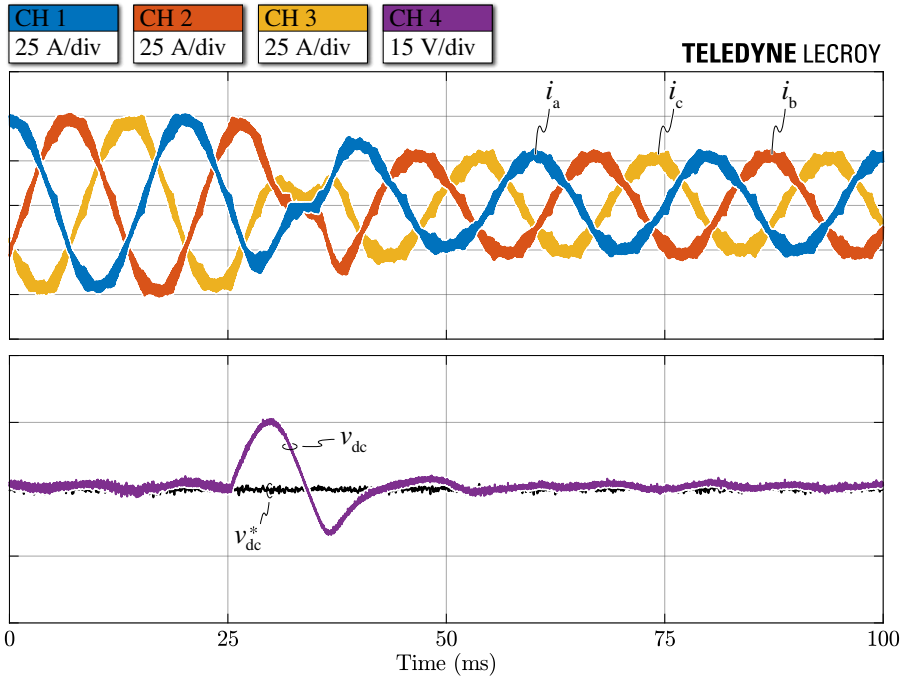

Figure 18. Experimental DC-link voltage control loop response to a 10 kW load step between $P_o = 22.5$ kW and $P_o = 12.5$ kW with $v_{dc} = 800$ V and ZMPCPWM. Measured phase currents i_{abc}, DC-link voltage reference v^*_{dc} and DC-link voltage v_{dc}. The DC-link voltage reference is obtained from the DAC of the MCU (i.e., with a 0–3.3 V measurement range); therefore, it is rescaled.

Ultimately, the dynamical performance of the DC-link mid-point voltage balancing control loop is assessed by evaluating the mid-point voltage deviation following a load unbalance step. As previously illustrated in Figure 9, the v_m control loop regulates the mid-point current I_m by acting on the zero-sequence voltage injection $v_{o,\delta}$. Since the zero-sequence voltage does not affect the phase voltages applied by the rectifier, the v_m loop ideally does not interfere with the phase currents and/or the total power transfer. Figure 19 shows the system response to a 3 kW load unbalance step, performed by changing the power absorbed by the electronic load connected to the lower DC-link half between $P_{o,n} = 10.5$ kW and $P_{o,n} = 7.5$ kW. The results for both ZMPCPWM and SPWM are shown in Figure 19a,b, respectively. It is worth noting that both an unbalance step and a load step are performed simultaneously, as only one DC-link half is affected by the load step (i.e., for simplicity of the test realization). In this case, both the v_{dc} and v_m control loops act at the same time, nevertheless, their response is completely decoupled. In particular, it is observed that the action of the v_{dc} loop is restricted to few ms after the step (i.e., visible by the amplitude change of the phase currents), while the response of the v_m loop lasts tens of ms, due to its lower bandwidth. A maximum mid-point voltage dynamical deviation of 18 V is obtained, as the PI regulator zero $\omega_{z,b}$ has been tuned to maximize the disturbance rejection capability of the controller (see Section 3). Furthermore, the comparison between Figure 19a and Figure 19b shows the fundamental role of the MAF applied to the measured v_m (see Figure 9) in achieving similar control performance when adopting either ZMPCPWM or SPWM, i.e., despite the low-frequency 150 Hz voltage ripple induced by SPWM.

In conclusion, both the steady-state and dynamical performance of all control loops can be considered successfully verified, as supported by the provided experimental results.

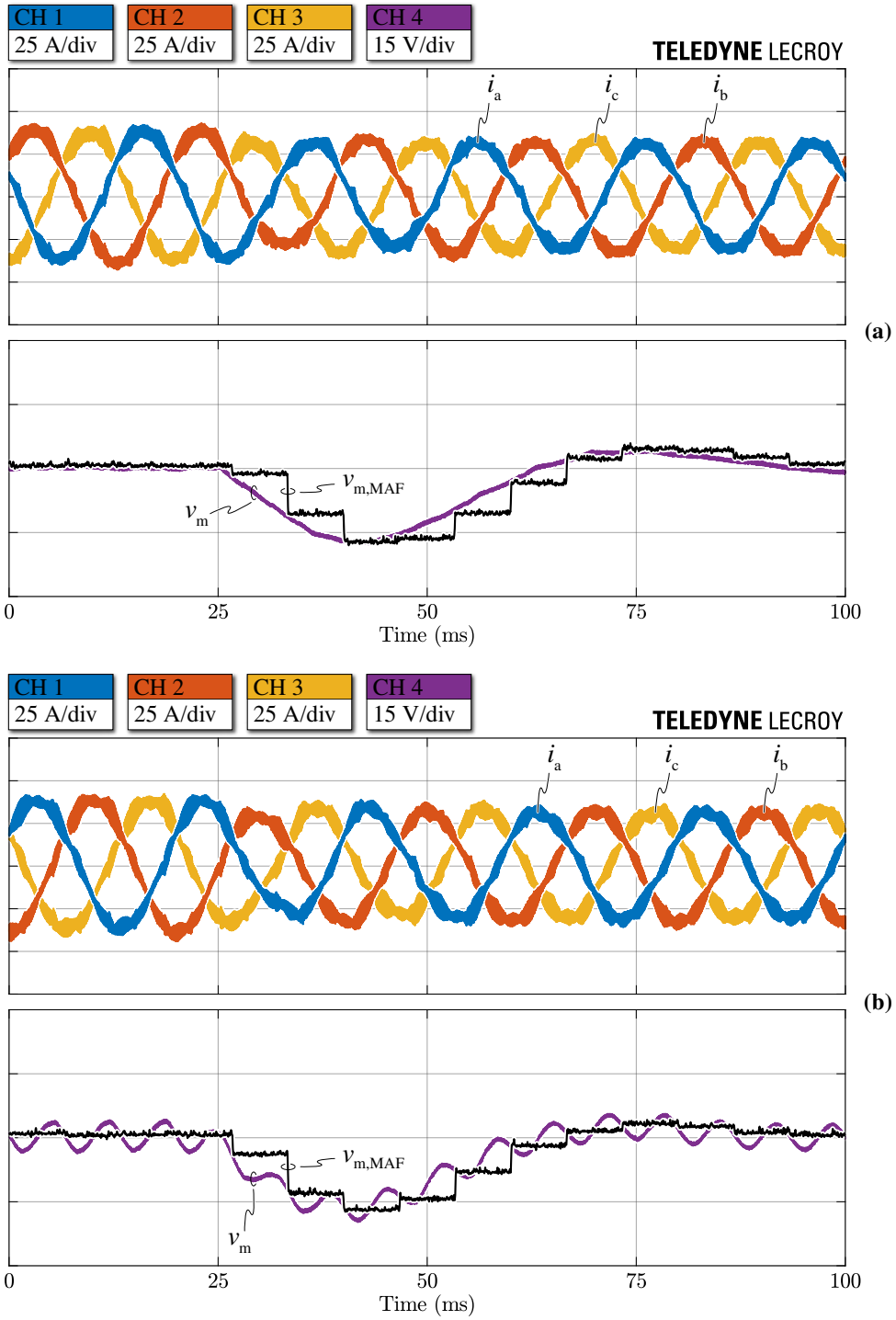

Figure 19. Experimental DC-link mid-point voltage balancing loop response to a 3 kW load unbalance step with $v_{dc} = 800\,V$: the load connected to the lower DC-link half performs a step between $P_{o,n} = 10.5\,kW$ and $P_{o,n} = 7.5\,kW$, while the load connected to the higher half absorbs a constant power $P_{o,p} = 7.5\,kW$. Measured phase currents i_{abc}, DC-link mid-point voltage deviation v_m and DC-link mid-point voltage moving average $v_{m,MAF}$ with ZMPCPWM (**a**) and SPWM (**b**). The mid-point voltage moving average is obtained from the DAC of the MCU (i.e., with a 0–3.3 V measurement range); therefore, it is rescaled.

5. Conclusions

This work has presented the design, tuning and implementation of a digital multi-loop control strategy for the three-level unidirectional active front–end of an EV ultra-fast battery charger. The main properties and the operational basics of three-level rectifiers have been recalled, and the fourth order state-space model of the considered system has been derived. Major attention has been reserved to the mid-point current generation process and its relation with the zero-sequence voltage injection, identifying the instantaneous zero-sequence voltage limits and the maximum mid-point current capability of the converter by analytical means. Four control loops, namely the dq currents, DC-link voltage and mid-point voltage balancing loops, have been designed taking into account the main delay components and compensating for the plant non-linearities. Therefore, an analytical tuning procedure of all loops has been provided, leveraging the system state-space model previously derived. Finally, the proposed controller design procedure has been applied to a 30 kW three-level T-type rectifier operated at 20 kHz (i.e., switching and control frequency). The small-signal transfer functions of the designed control loops have been simulated and found in excellent agreement with their analytical derivations. The complete multi-loop control strategy has been implemented on a general purpose MCU and both the steady-state and dynamical performances of all controllers have been experimentally verified on a purposely built converter prototype. Overall, the designed control loops have achieved all requested features, namely low input current zero-crossing distortion, high step response and disturbance rejection dynamics and stable steady-state operation under unbalanced split DC-link loading.

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Appendix A. Mid-Point Current Limits

The mid-point current local average i_m is dynamically limited by the maximum and minimum zero-sequence voltage limits reported in (18). The upper and lower i_m limits can therefore be derived by substituting the expressions of $v_{o,max}$ and $v_{o,min}$ into (11), obtaining:

$$\begin{cases} i_{m,max} = -\dfrac{2}{v_{dc}}\left[\displaystyle\sum_{x=a,b,c} v_x\,|i_x| + v_{o,min}\sum_{x=a,b,c}|i_x|\right] \\ i_{m,min} = -\dfrac{2}{v_{dc}}\left[\displaystyle\sum_{x=a,b,c} v_x\,|i_x| + v_{o,max}\sum_{x=a,b,c}|i_x|\right] \end{cases}. \tag{A1}$$

These limits are illustrated in Figure A1 for two different values of DC-link voltage.

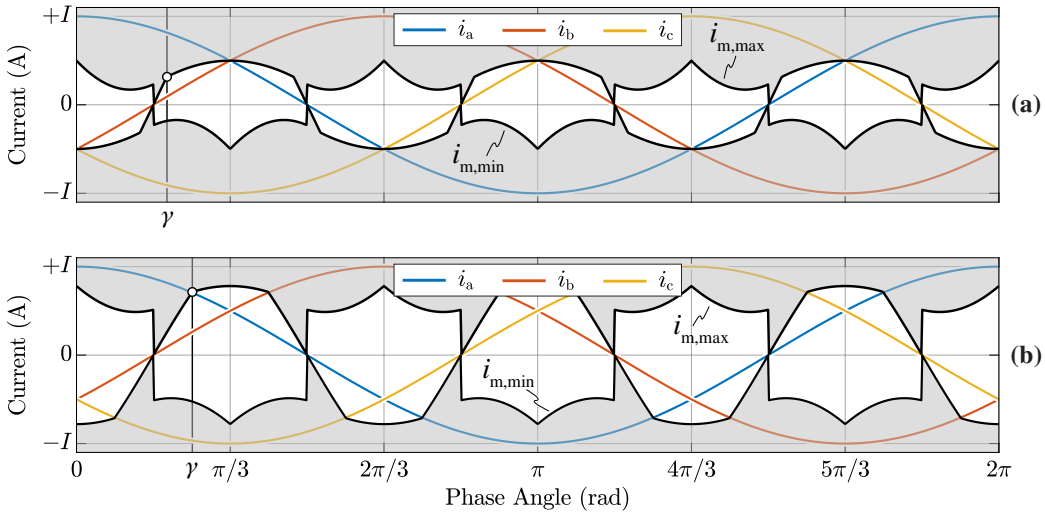

Figure A1. Mid-point current local average i_m limits for $v_{dc} = 650\,V$ (**a**) and $v_{dc} = 800\,V$ (**b**), assuming a 400 V line-to-line grid voltage and unity power factor operation. Angle γ, identifying the intersection between v_b and $v_c + v_{dc}/2$ within $[0, 2\pi/3]$, is highlighted.

Since (A1) expresses the maximum and minimum feasible envelopes of i_m along the grid period, the boundaries of the mid-point current periodical average I_m can be derived integrating (A1) over $2\pi/3$. In particular, with the integrals of $i_{m,max}$ and $i_{m,min}$ being identical (i.e., with opposite signs), the I_m limits are symmetrical:

$$I_{m,max} = -I_{m,min} = -\frac{3}{\pi\, v_{dc}} \int_0^{2\pi/3} v_{o,min}\left(|i_a| + |i_b| + |i_c|\right) d\vartheta. \tag{A2}$$

To facilitate the solution of (A2), it is worth observing that $i_{m,max}$ is characterized by even symmetry within $[0, 2\pi/3]$ (see Figure A1). Therefore, the integration may be restricted to $\vartheta \in [0, \pi/3]$. Moreover, leveraging the expression of $v_{o,min}$ and the signs of i_a, i_b, i_c within the considered window, the following is obtained:

$$I_{m,max} = \frac{12}{\pi\, v_{dc}} \left[\int_0^{\pi/6} i_a \left(v_c + \frac{v_{dc}}{2} \right) d\vartheta - \int_{\pi/6}^{\gamma} i_c\, v_b\, d\vartheta - \int_{\gamma}^{\pi/3} i_c \left(v_c + \frac{v_{dc}}{2} \right) d\vartheta \right]. \tag{A3}$$

The angle γ identifies the intersection between v_b and $v_c + v_{dc}/2$ (see Figure A1) and is thus expressed by

$$\gamma = \sin^{-1}\left(\frac{1}{\sqrt{3}M} \right) \qquad M \geq \frac{2}{3}, \tag{A4}$$

where the validity range of (A4) is derived from the integration limits in (A3) (i.e., $\gamma \leq \pi/3$). Finally, substituting (12), (13), (A4) into (A3) and solving the integral terms, the following analytical expression is obtained:

$$I_{m,max} = \frac{3}{\pi}\, I \left[1 + \frac{1}{2M} \left(\sqrt{3M^2 - 1} - \frac{1}{\sqrt{3}} \right) + \frac{M}{2} \left(3 \sin^{-1}\left(\frac{1}{\sqrt{3}M} \right) - \pi - \frac{\sqrt{3}}{2} \right) \right], \tag{A5}$$

which is only valid within $2/3 \leq M \leq 2/\sqrt{3}$. Expression (A5) is graphically illustrated in Figure A2, where it is also compared to experimental results achieving a maximum error of 1% over the complete operating range. It is worth noting that (A5) corresponds to what was found in [23] by means of a space-vector-based approach.

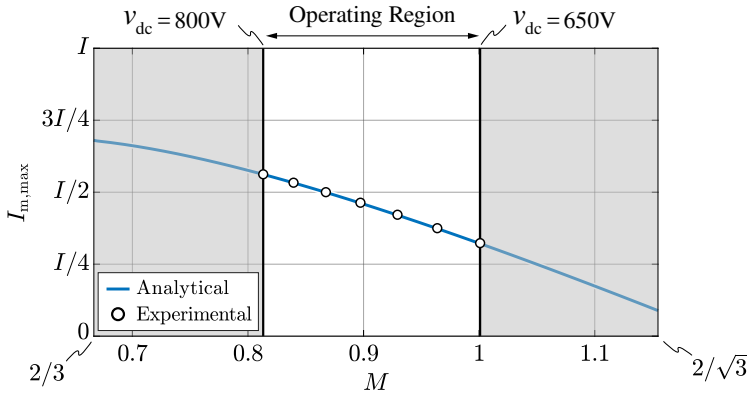

Figure A2. Maximum mid-point current periodical average $I_{m,max}$ as a function of the modulation index M. The converter operating region (i.e., v_{dc} = 650–800 V) is highlighted. The analytical expression (A5) is compared to experimental results, showing excellent agreement.

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