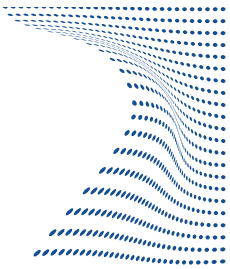
Polytechnic University of Turin

Doctoral School - 33rd Cycle



Dissertation for the doctoral program in:

Electrical, Electronics and Communications Engineering with curriculum in "Electronic Devices"

Enhanced Electrical and Reliability Testing of Power Semiconductor Devices

---

Author:
Davide Cimmino

Supervisor:
Prof. Candido Pirri
Co-Supervisor:
Prof. Sergio Ferrero

Thesis Sponsorship:
Vishay Intertechnology, R&D Power Diodes Division, Borgaro, Italy

---

March 15, 2021

"*My life story is the story of everyone I've ever met.*"

Jonathan Safran Foer

Abstract

Enhanced Electrical and Reliability Testing of Power Semiconductor Devices

by Davide Cimmino

Before the last two decades, power electronics was strictly related to electrical engineering, and relegated to applications ranging from medium to high powers, such as industry drives, railway traction and power supplies. But with the increasing demand for electricity and the diffusion of modern consumer products related to power management, the whole grid comprehending generation, transmission, distribution and use of electric energy, gained remarkable visibility along with the engineering field of power electronics, with the goal of maximizing the efficiency, versatility and reliability of the supply chain, as well as the integration of renewable power sources into this continuously evolving organism. This PhD thesis, carried out at the Polytechnic of Turin and sponsored by a Vishay Intertechnology Inc. scholarship, focuses on the performance and lifetimes of power semiconductor devices, when electrical and environmental testing conditions apply high stress to the devices beyond current standards, especially in terms of reliability. Part I gives a brief introduction on the major definitions in the field of reliability testing, focusing on the terms involved in the following sections, along with an overview of current and possible future trends in the field of reliability testing. In part II, the standard High Temperature High Humidity Reverse Bias (H3TRB) reliability test for power semiconductor devices, also known as Temperature Humidity Bias (THB) test, is performed at high voltage in order to investigate and analyze peculiar failure modes generated by the combination of high reverse bias voltage and humidity. The results led to the publication of 3 research papers during the doctoral program. The main topic of part III is the study and development of a high-current on-wafer Forward Voltage Drop (VF) drop measurements system for power semiconductor diodes. The methodology involves the design, characterization, evaluation and further improvement of a dedicated testing setup with the objective of performing measurements without inducing any degradation in the devices under test. Eventually, part IV is dedicated to the evaluation of the cosmic ray ruggedness of power semiconductor devices. The testing has been performed in agreement with the JEDEC standard JEP151, and the experimental work involved the development of dedicated testing boards, for the following test campaign at the “ISIS Neutron and Muon Source” of the “Rutherford Appleton Laboratory” in Didcot, United Kingdom.

Acknowledgements

At the moment of writing this acknowledgment section, a lot of mixed feelings spiral inside my head as I conclude this doctoral program and my thesis manuscript. It is indeed a very complicated period of modern history. If I think about the difference from how everything changed from the beginning of these three years to the present, it really feels like a incredible amount of time. I have changed a lot as a person and as a professional, and I believe I owe most of what I have achieved to a multitude of individuals whose consciousness, presence, grit, determination, kindness, patience, charisma, friendship, involvement and love, have let me understand how much we need to grow up everyday as workers, students and human beings in order to evolve toward a better future, for us in our daily life, and for everyone else with our legacy.

First of all I want to say thanks to the two institutions that made my doctoral program possible, which are the Polytechnic University of Turin on the academic side, and Vishay as the company who issued the scholarship for my research. In particular I am grateful to my supervisor Prof. Candido Pirri from the Department of Applied Science and Technology (DISAT), and Rossano Carta from Vishay, head of the Power Diodes R&D group, who represented for me these two worlds during my daily experience. When I first arrived at the company to start my research, Rossano welcomed me and followed my first steps in a territory which was unknown to me, as I started my very first experience after the master degree. I can say that his dedication and resolution really helped in shaping my approach to research, my experience in a company and my attitude as a young professional.

I am sure I would never change my co-supervisor Prof. Sergio Ferrero to anyone else. He has seen me in the best and worst moments, and I am proud and grateful of the human relationship that we naturally formed. He successfully supported me through the complex world of research publications, as well as being my point of reference at the Polytechnic of Turin. I want to say thanks to all my colleagues at Vishay, from all the laboratories and departments, for the great support and effort they dedicated to me and my projects, in particular to Nabil El Baradai who became my supervisor at the company in the last year, for his knowledge, dedication and friendship, as we fought side by side to achieve our objectives. I am also grateful to Giovanni Richieri and Roberta Busca for the great synergy that we established together, in order to gave birth to two of the publications from this thesis, I would have never reached this goal without them.

In conclusion I would like to say thanks to my friends, family, my parents and in particular my brother and my girlfriend Roberta, for how much they have done for me in this period. Your encouragement, your strength and affection, have helped me in the hardest moments to reset and start again with all my enthusiasm, you are the foundations holding the temple of my spirit.

Davide Cimmino
Turin, Italy
March 15, 2021

Table of Contents

List of Figures

List of Tables

List of Abbreviations

BV . . . . . .Breakdown Voltage

CDF . . . . . .Cumulative Distribution Function

CR . . . . . .Cosmic Ray

DC . . . . . .Direct Current

DMM . . . . . .Digital Multimeter

DUT . . . . . .Device Under Test

EDX . . . . . .Energy-Dispersive X-ray spectroscopy

EECR . . . . . .Extreme Energy Cosmic Ray

FIB . . . . . .Focused Ion Beam

FIT . . . . . .Failures In Time

FR . . . . . .Floating Ring

H3TRB . . . . . .High Temperature High Humidity Reverse Bias

HALT . . . . . .Highly Accelerated Life Test

HASS . . . . . .Highly Accelerated Stress Screening

HTGB . . . . . .High Temperature Gate Bias

HTGS . . . . . .High Temperature Gate Stress

HTRB . . . . . .High Temperature Reverse Bias

HTS . . . . . .High Temperature Storage Test

HV-THB . . . . . .High Voltage Temperature Humidity Bias

IGBT . . . . . .Insulated Gate Bipolar Transistor

JTE . . . . . .Junction Termination Extension

LTJ . . . . . .Low Temperature Joining

LTS . . . . . .Low Temperature Storage Test

MOSFET . . . . . .Metal Oxide Semiconductor Field Effect Transistor

MS . . . . . .Mechanical Shock

MTBF . . . . . .Mean Time Between Failures

MTTF . . . . . .Mean Time To Failure

NYC . . . . . .New York City

PC . . . . . .Power Cycling

PDF . . . . . .Probability Density Function

PECVD . . . . . .Plasma-Enhanced Chemical Vapor Deposition

PSD . . . . . .Power Semiconductor Device

PSU . . . . . .Power Supply Unit

RESURF . . . . . .Reduced Surface Field

SAM . . . . . .Scanning Acoustic Microscopy

SEB . . . . . .Single Event Burnout

SEE . . . . . .Single Event Effects

SEGR . . . . . .Single Event Gate Rupture

SEM . . . . . .Scanning Electron Microscopy

SOA . . . . . .Safe Operating Area

TC . . . . . .Thermal Cycling

THB . . . . . .Temperature Humidity Bias

Tj . . . . . .Junction Temperature

TST . . . . . .Thermal Shock Test

UHECR . . . . . .Ultra High Energy Cosmic Radiation

USB . . . . . .Universal Serial Bus

VF . . . . . .Forward Voltage Drop

VLD . . . . . .Variation Lateral Doping

VT . . . . . .Vibration Test

In loving memory of my grandmother Maria ...

Part I

Introduction

Chapter 1

Introduction

1.1 Thesis Framework and Outline

The following doctoral thesis work has been carried out at the Polytechnic University of Turin, with an industrial scholarship offered by Vishay Intertechnology Inc. and carried out at Vishay Semiconductor Italiana S.P.A., a power semiconductor company located in Borgaro Torinese, Italy. This research work has been focused on better understanding the effects of enhanced electrical and reliability testing conditions on state-of-the-art Power Semiconductor Devices (PSDs). Given the nature of the research activity, this manuscript has been divided accordingly in 3 main parts.

Part I gives a brief introduction on the major definitions in the field of reliability testing, focusing on the terms involved in the following sections, as well as an overview of current and possible future trends in the field.

In part II, the standard High Temperature High Humidity Reverse Bias (H3TRB) reliability test for power semiconductor devices also known as Temperature Humidity Bias (THB) test, is performed at high voltages in order to investigate and analyze peculiar failure modes generated by the combination of high reverse bias voltage and humidity, which led to the publication of 3 articles from the PhD candidate [1–3] during the doctoral program.

The main topic of part III is the study of on-wafer forward voltage drop measurements of power semiconductor diodes at high current. The methodology involves the design, characterization, evaluation and further improvement of a dedicated testing setup with the objective of performing measurements without inducing any degradation in the Devices Under Test (DUTs).

Part IV is dedicated to the evaluation of the Cosmic Ray (CR) ruggedness of power semiconductor devices. The testing has been performed in agreement with the JEDEC standard JEP151 "Test Procedure for the Measurement of Terrestrial Cosmic Ray Induced Destructive Effects in Power Semiconductor Devices"[4] and the experimental work involved the development of a dedicated testing board and the following test campaign at the ISIS Neutron and Muon Source located at the Rutherford Appleton Laboratory in Didcot, United Kingdom. The experimental work has been carried out under the supervision of the Reliability and Radiation Effects on Advanced CMOS Technologies (RREACT) group from the University of Padova, Italy.

1.2 Introduction

In recent years, Power Electronics has become a crucial part of modern electronic systems and applications in a wide range of fields, such as electric power generation and transmission, home appliances, heavy industry and transportation. Each one of these system relies on the performances and properties of the underlying components in order

to operate for the required period of time. We can rephrase this statement by recurring to the definition of Reliability, which is defined for instance as "the ability of a system or component to perform its required functions under stated conditions for a specified period of time" [5–7]. For this reason, differently from what happened until the first half of the XXI century, high reliability has become nowadays one of the key requirement of modern systems and consequently of their components, which in turn need to pass a broad set of screening and reliability tests before moving to mass production and distribution. In the following sections, an brief overview of reliability testing and current standards for power semiconductor devices is presented, as well as some necessary definitions.

1.2.1 Power Devices and Global Trends

Before the last two decades, power electronics was strictly related to electrical engineering, and relegated to applications ranging from medium to high powers, such as industry drives, railway traction and power supplies. But with the increasing demand for electricity and the diffusion of modern consumer products related to power management, the whole chain comprehending generation, transmission, distribution and use of electric energy, gained remarkable visibility along with the engineering field of power electronics, with the goal of maximizing the efficiency, versatility and reliability of the above mentioned electricity chain, and the integration of renewable power sources into a continuously evolving electrical power grid, including electric mobility [8]. Figure 1.1 shows the trend of power modules market for mainstream applications [9].

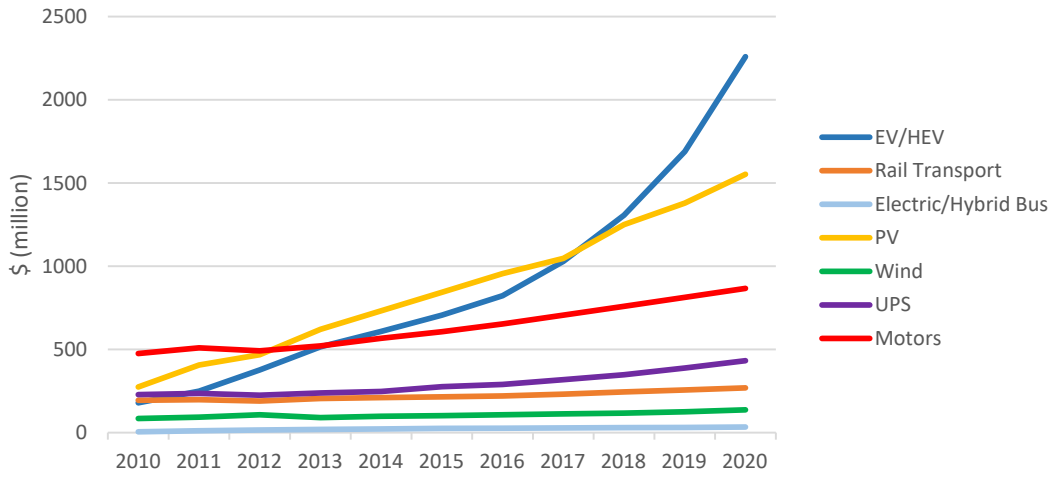


FIGURE 1.1: Trend of power modules market for mainstream applications. © 2019 IEEE [9].

There are several reasons for which power electronics is and will be a key technology, and according to some analysts [10] these reasons are strictly related to several global trends driving our present. One of the main drivers is the global increase of population yielding to an increase in the demand of natural resources needed for primary industries and for the sustenance in new urban areas. In order to satisfy this demand, the consumption of energy increases inevitably, along with the demand of water and rare earth minerals. Nonetheless, the byproduct of this ascending exploitation is the increase of greenhouse gases, and temperature on a global scale, with the impossibility for the earth to sustain itself and replenish its resources in a short circuit leading to inevitable

consequences. It then becomes necessary to implement major changes to the electrical power conversion chain in order to greatly increase its capabilities, in order to drive society towards a new paradigm of interconnection between humans and their environment, which can one day allow to achieve an equilibrium between human needs and the environment. Main power electronic applications will drive the sustainable energy revolution with the integration of renewable sources, including photovoltaics and wind power, into the existing grid. This integration will then need an improvement of transmission efficiency and power distribution, which will be achieved thanks to enhanced high voltage lines and local distribution strategies, including energy storage, bidirectional power flow strategies, and other smart grid approaches. The improve in efficiency will then require improvements at the component level, with the increasing diffusion of wide band gap power devices, or at the circuit level, with the adoption of new converter topologies to reduce parasitic effects and efficiency and eventually at the size level thanks to the miniaturization of power circuits, leading to the substitution of voluminous and expensive legacy systems with newer and smaller counterparts. Moreover, the diffusion of new generation full electric vehicles is leading the mobility revolution thanks to the popularity of electric bikes, scooters, cars, trucks, trains, ships and air transport [8, 11].

1.2.2 Reliability: basics concepts and definitions

The definition of reliability exposed at the beginning of section 1.2 is not unique and it is continuously evolving through the years, as well as other reliability related concepts are. In this section, the most significant reliability definitions are listed in order to introduce the necessary terminology used in the next sections. A more complex definition of reliability comes from the IEC 60050-191 standard:

- **Reliability**: The ability of a product to perform required functions, under given environmental and operational conditions and for a stated period of time. [12, 13]

Following this definition, the concept of failure of a device is described for instance as:

- **Failure**: The termination of the ability of an item to perform a required function [12, 13]

The state of a failed device is defined “Fault”:

- **Fault**: “a fault is the state of an item characterized by its inability to perform its required functions” A fault is therefore the state resulting from a failure.[12, 13][1]

A way to describe a fault is what is defined as Failure mode:

- **Failure mode**: is the description of a fault. In other words, is how one observes the fault, generally as a deviation from the expected function of a device or system.

Closely related to the concept of failure mode, is the Failure Cause:

- **Failure Cause**: “is the circumstances during design, manufacture or use which have led to a failure” [12, 13].

Understanding the failure cause is of paramount importance for device engineers in order to improve their designs and prevent failures. Failure causes are generally coming from design, intrinsic weaknesses, manufacturing, aging and misuse of a system [13]. In order to understand a failure cause, it is important to analyze the Failure Mechanism:

[1] It is important to notice that this definition excludes temporary situations in which a system is temporarily unavailable due to programmed maintenance or other voluntary interruptions of working operation.

- **Failure Mechanism**: The physical, chemical or other processes that may lead to a failure [12, 13].

Considering the framework and the topics treated in this thesis, it is necessary to extend these definitions, considering power electronic devices as the target. Device Failures can be generally categorized in several layered ways, considering the time span, the entity, the manifestation and the type of stress.

First of all, a failure can be Intermittent or Extended:

- **Intermittent**: when the failure has a limited duration in time;
- **Extended**: failure continues indefinitely until, when possible, some corrective action restores the fault.

When the entity of the fail is taken into account, there are two possible definitions:

- **Complete**: when failure results in a total loss of functionality;
- **Partial**: when some functionalities are not lost.

Moreover, failures can be also identified according to the way they manifest in time:

- **Sudden**: when failure occurs suddenly, without or with limited warning in time;
- **Gradual**: when failure occurs in a longer time frame, generally accompanied by specific signals that can be monitored in time.

Two common terms used to describe failures are a sub-classes of the latter definitions, these terms are:

- **Catastrophic**: failure is complete and sudden;
- **Degraded**: failure is gradual and partial.

Moreover, considering the condition under which failure occurs, failures can be classified as:

- **Primary**: when failure is due to the natural aging of the device in normal use conditions and stresses as specified by the manufacturer (e.g. datasheet conditions).
- **Secondary**: when failure is caused by device overstress. An overstress is the use of a device outside its datasheet conditions or its specific Safe Operating Area (SOA).

It is important to highlight that ovestresses can cause failure when either the device is deliberately used outside its normal use conditions (i.e. voluntary overstress) or when the use conditions do not fit the specifications of the device. Furthermore, while secondary failures can be avoided by using the device in conditions allowed by design and specifications, primary failures can only be solved by changing the device's design.

In order to describe the time behavior of device failure it is important to introduce the definition of Failure Rate, and the "bathtub curve".

- **Failure Rate**: the frequency with which failures occur in time, generally expressed in number of failures per second [14].

The bathtub curve is essential to reliability, since it well models the failure behavior versus time of a wide class of items, including power semiconductor devices. This model is schematized in 1.2 and can be divided in 3 main sections:

- **Infant Mortality**: early failures region, where failures occur with a rapidly decreasing failure rate
- **Normal Usage** also called "normal life": a region where failure rate has a minimum and is approximately constant.
- **Wear Out Failures**: also known as "end of life" region, where failure rate is increasing due to long term device wear-out.

In the first region, failures are highly undesirable and their origin is attributed to issues related to the manufacturing phase. This region gives rise to "dead-on-arrival" devices [15], with obvious consequences for both the manufacturer and final customer's point of view. In the infant mortality region, the failure rate generally has an exponential decreasing behavior, which can last from hours to even years depending on the specific product, before moving to the normal life phase [15]. The occurrence of failures in the infant mortality period can be lowered significantly thanks to the so called burn-in tests, accelerated tests where devices are stressed for a small period of time, and only the passed devices are distributed to the final user.

In the Normal life period, when devices are operated in datasheet conditions, the failure rate encounters a minimum. In this region, device failure happens mostly due to excess stress. This period is the one considered in the design phase.[16].

Eventually, in the wear-out period, wearing and aging of the product determines material degradation, the failure rate increases progressively and eventually leads to the failure of the whole population of devices after a given time ($t \to \infty$).

Interestingly, electronic devices failure rate can be generally modeled by the bathtub curve behavior, so failure rate curves can be fitted accordingly [17] by achoosing the appropriate model for the failure rate, as it will be shown in the next section.

1.2.3 Mathematical Definitions

The following section gives a brief overview of the main mathematical definitions and models involved in reliability evaluation [19]. If the cumulative distribution function or "failure distribution" F(t) (or "unreliability") represents the fraction of failed samples at time t, then the reliability function (or survival function) can be defined as follows:

$$R(t) = 1 - F(t) \tag{1.1}$$

This function represents the fraction of survived devices at time t, which allows to define the Probability Density Function (PDF) f(t):

$$f(t) = \frac{dF(t)}{dt} \tag{1.2}$$

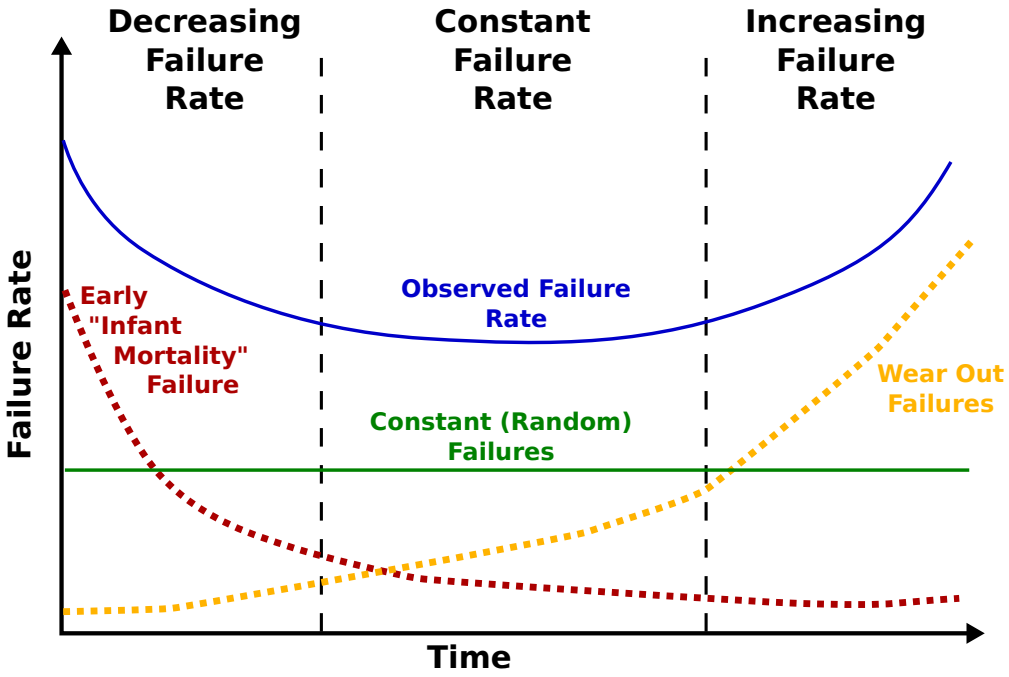


FIGURE 1.2: Bathtub failure rate distribution curve [18].

representing the variation of failed devices at time t. The latter definition allows to write the **hazard function** or "instantaneous" failure rate:

$$h(t) = \frac{f(t)}{R(t)} = -\frac{1}{R(t)}\frac{dR(t)}{dt} \tag{1.3}$$

The hazard function describes how the failure rate changes in time for a population of devices [16]. Eventually, all these definitions allow to describe also the Mean Time To Failure (MTTF):

$$MTTF = \int_0^\infty t f(t) dt = \int_0^\infty R(t) dt \tag{1.4}$$

which is the expected value of the PDF f(t), denoting the average time to failure for a non-repairable system.

1.2.3.1 Weibull Distribution

The weibull distribution is a very useful model, which can describe all three regions of the bathtub curve presented in the previous section. Its reliability function is:

$$R(t) = e^{-\left(\frac{t}{\alpha}\right)^{\beta}} \tag{1.5}$$

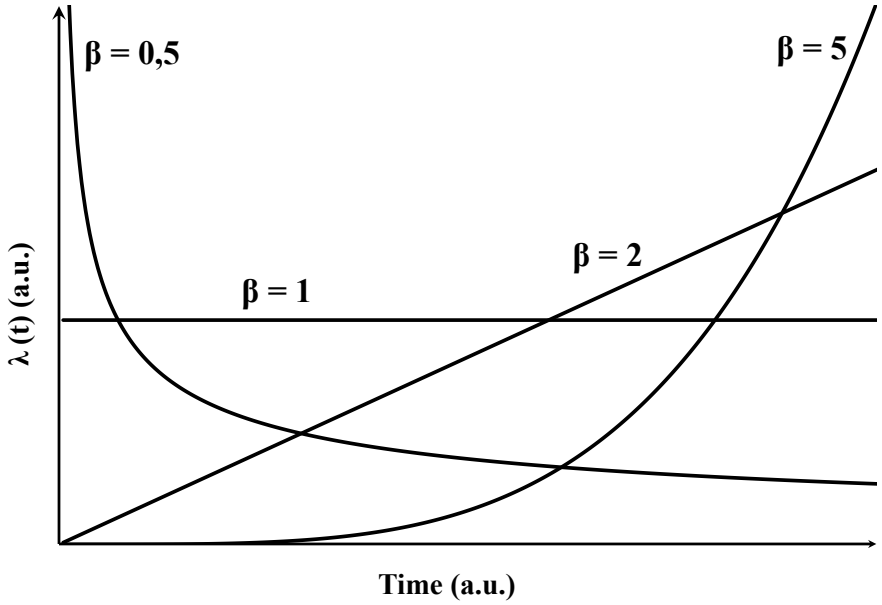


FIGURE 1.3: Weibull Failure Rate Curve versus Beta Values. The variation of β allows the modeling of each section of the bathtub curve: infant mortality, normal life and wear-out regions.

The consequent Cumulative Distribution Function (CDF) is then:

$$F(t) = 1 - R(t) = 1 - e^{-\lambda t} \tag{1.6}$$

Which allows to determine the relative PDF:

$$f(t) = -\frac{dF(t)}{dt} = \frac{\beta}{\alpha^{\beta}} t^{\beta-1} e^{-\left(\frac{t}{\alpha}\right)^{\beta}} \tag{1.7}$$

As a consequence, the hazard function is:

$$h(t) = \frac{\beta}{\alpha^{\beta}} t^{\beta-1} \tag{1.8}$$

As said at the beginning of this section, thanks to this function it is possible to model device failure rate in all the three regions of the bathtub curve by changing the value of β, as reported in 1.3.

1.3 Overview of Power Semiconductor Reliability Testing

1.3.1 Reliability Test Standards for Power Semiconductor Devices

Given the current level of diffusion and their continuously widening market, there can be several motivations to evaluate the reliability of power semiconductor devices [11].

The first reason is the increase of power density, which is a measure of how much power is dissipated in the volume unit (W/m^3). Higher power density requirements, often related to package downsizing and increasing currents per chip, yield to a global increase of temperatures and significant temperatures differences between different points in being it a discrete package or power module.

In terms of environment temperatures, state-of-the-art power applications face increasingly hard conditions. For instance, modern hybrid automotive systems involve working operation of power electronic circuit in proximity of the combustion engine, with heat-sink temperatures which can be as high as 120°C, in order to control the temperature of the control circuitry. This temperature requirement has been increasing through the years moving up to 175°C as a specification limit for the junction temperature.

The same consideration can be done regarding the humidity of the environment. For instance modern offshore wind power farms, include power converters which can be exposed to oscillating environmental conditions, including high humidity peaks during working operation [20]. In this case, and as we will see in II, the combined effect of high humidity and high voltage operation can yield critical failures on the field, lowering the harvesting efficiency of the system and in critical cases to power production.

Another interesting trend is the increasing number of interlinked frequency inverters per system, a significant trend in the industrial automation field. When multiple systems are linked, the total Mean Time Between Failures (MTBF) is the sum of each inverter's MTBF divided by the total number of inverters:

$$MTBF_{Total} = \frac{\sum_{i=0}^{n-1} MTBF_i}{n} \tag{1.9}$$

Where n is the number of interlinked inverters, which can significantly lower the total MTBF.

With respect to those listed in section 1.2.1, these latter are two more practical examples of driving forces in the world of power electronics, but they are a major focus continuing from the past which will continue to be followed also in the coming years. With these considerations and knowing that some high-demanding mainstream applications, such as it happens in the automotive field, require working operation and stable performance for service times of 30 years.

Therefore, testing and assuring reliability in order to have an acceptable time to market deeply relies in what is called "Accelerated Reliability Testing". Several kind of accelerated stress tests for reliability have been developed in the last 40 years, and are nowadays accepted as the basis for product qualification in several fields, of which automotive represents one of the main the references.

The most common qualification test considered by manufacturers are reported in the following list [6]:

- **HTRB**: High Temperature Reverse Bias (HTRB) Test

- **HTGS** (or **HTGB**): High Temperature Gate Stress (or Bias) Test
- **THB** (or **H3TRB**): Temperature Humidity Bias Test
- **LTS**: Low Temperature Storage Test
- **HTS**: High Temperature storage test
- **TST**: Thermal Shock Test
- **TC**: Temperature Cycling
- **PC**: Power Cycling
- **VT**: Vibration Test
- **MS**: Mechanical Shock

The normatives behind the definition of these test are always changing, but the general approach, setup and requirements in terms of test limits and lifetime requirements are converging towards a common structure, even if several manufacturers can present slight differences in their testing methods.

As main reference, we can consider the AECQ-101 normative "Stress test qualification for automotive grade discrete semiconductors" from the Automotive Electronic Council [21], which is being continuously updated, or the more recent ECPE directive AQG 324 "Qualification of Power Modules for Use in Power Electronics Converter units in Motor Vehicles" [22]. With these two guidelines, a comprehensive set can be retrieved in terms of testing methods, failure criteria and requirements covering the topics considered in this thesis and beyond, given that the main subjects are power diodes but the normative include definitions for other common power devices such as Insulated Gate Bipolar Transistors (IGBTs), power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), etc...

These tests can qualify the device both at the chip level and at the level of the package, by stressing the interaction with properties related to the assembly process such as the kind of package, the bonding method, the type of molding compound, the passivation gel in power modules, the effect resistance to humidity and several other mechanical and thermal properties related to the assembly materials. In addition, several tests consider also package stability in defined environmental conditions of storage, such as fixed high or low temperature stress, cyclic temperature variation, vibration and mechanical shock test.

Before moving to the next section it is useful to give two more definitions:

- **Stressor**:the physical conditions to which a component is exposed during testing (e.g. Voltage, power, temperature, humidity, pressure, etc...) [23].
- **Accelerated Stress Test**: A test in which the applied-stress level is chosen to exceed that stated in the reference conditions, in order to shorten the time required to observe the stress responses of the item, or magnify the response in a given time. To be valid, an accelerated test shall not alter the basic modes and/or mechanisms of failure, or their relative prevalence [23].

The following sections will introduce the listed reliability tests, which are valid for both discrete plastic packages and power modules, except for the vibration test and mechanical shock test which can be considered out of the scope of this thesis.

1.3.1.1 High Temperature Reverse Bias test (HTRB)

The High Temperature Reverse Bias (HTRB) applies both temperature and reverse bias stressors to the device, in order to evaluate the stability of leakage through time. The applied bias is a Direct Current (DC) voltage forcing each DUT in reverse bias conditions, generally up to 100% of their nominal Breakdown Voltage (BV) or blocking voltage, and the temperature of the environment chamber or hot plate is set in order to bring the devices close to their maximum Junction Temperature (Tj) but avoiding thermal runaway effects.

This test has the main objective of highlighting degradation or critical failures appearing not in the bulk, but in the edge termination structure and in the passivation stack of the power device, independently on the field spreading technique exploited to reduce the field at the surface of the chip, which can be for instance, Floating Ring (FR), Junction Termination Extension (JTE), Variation Lateral Doping (VLD), Reduced Surface Field (RESURF), etc...

As a consequence, these surface fields induce ions migration and can cause charge accumulations in critical points, leading to local increased leakage current, unwanted local inversion in regions with low doping, BV reduction and even short-circuit filaments through pn junctions.

The sources of mobile ions can be several, and can be due to impurities accumulated during the front-end and even the assembly process of the device, eventually leading to performance degradation or failure, and highlighted in a shorter time thanks to the acceleration factor given by high temperatures.

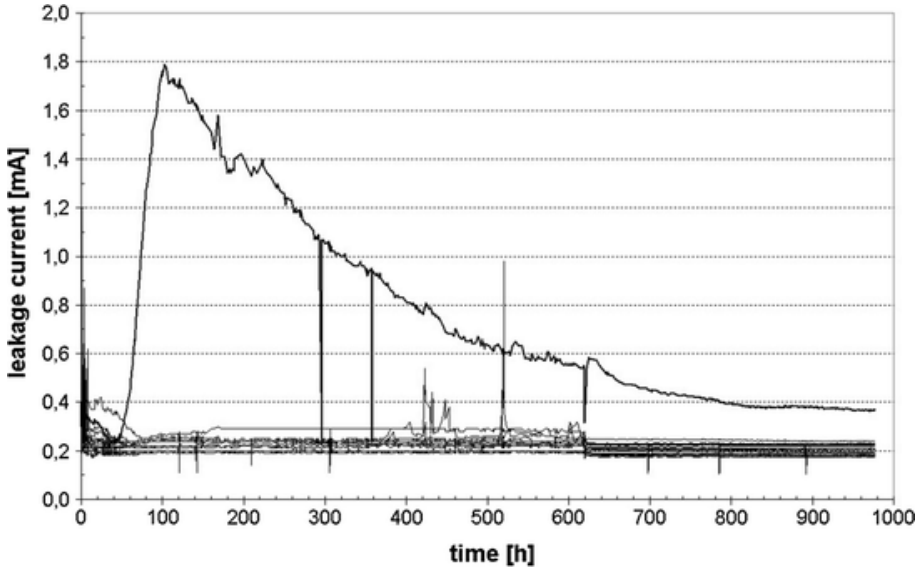


FIGURE 1.4: Example of HTRB leakage monitoring curve. One device exhibits unstable behavior, but then re-enters in the limits before the end of the test, revealing a design issue in the bonding diagram which can has then been addressed by the designers.Picture reproduced with permission from [6].

At each test checkpoint, the bias and temperature stressors are removed, and the DUTs are left at room temperature until they reach thermal equilibrium conditions, allowing electrical measurements comparable with the initial test conditions. The test

limits, or failure criteria for High Temperature Reverse Bias (HTRB) focus on the increase of leakage current at room temperature, with a limit of 5 times the initial leakage value of the DUT [21].

As we will see in part II for other tests such as the High Temperature High Humidity Reverse Bias (H3TRB), or in the case of some research or manufacturers standards, leakage monitoring can be performed throughout the whole duration of the test, which can last beyond 1000h in the case of automotive qualifications. In this way, also the stability of the leakage current is taken into account as an additional observable of test. Some authors even suggest an advanced method to monitor each device singularly, and perform intermediate electrical verification on the single device under test without removing it from the test apparatus, thanks to a dedicated local heating system and control circuit [24].

Sometimes, even if the above stated characteristics of the device (e.g. passivation stack, quantity of mobile ions, etc..) fulfill the requirements, some package level issues can arise and be highlighted by the HTRB test. For instance, Figure 1.4 , shows the monitored evolution of the leakage current during HTRB test for an IGBT.

It can be seen that without monitoring, the outlier device rising above the initial value and then coming back into limits before intermediate tests, would have resulted in an "Pass" after test. Thanks to monitoring, this single device was analyzed and showed a non-conformity in the bonding diagram, with a wire lying open loop above the IGBT guard ring. This analysis allowed designers to correct the bonding geometry and eliminate this issue on the final design, as confirmed by further HTRB testing [6].

It has been shown [25] that new silicon carbide devices allow higher robustness thanks to the higher critical surface field up to $3\,MV/cm$, but with respect to silicon, higher margin are considered, so that critical fields are held below the $1MV/cm$ limit, which is approximately one order of magnitude higher than the safe limit of Silicon ($100\,kV/cm \div 150\,kV/cm$) [6].

Moreover, even with these margin, SiC device processing [26] can induce charge accumulation and change locally the BV with respect to the expected nominal value, which can localize in higher field positions causing device failure [25]. It is important to highlight that the electrical failure modes of HTRB can be similar to those observed in the Temperature Humidity Bias (THB) test, which is the main subject of the next section, and of II.

1.3.1.2 High Temperature Gate Stress (HTGS) Test

The High Temperature Gate Stress (HTGS) or High Temperature Gate Bias (HTGB), focuses on the evaluation of the gate leakage current stability of power transistor devices (e.g. MOSFETs, IGBT, etc. . .).

The gate voltage is set to a maximum value of $\pm 20\,V$, for devices with gate oxide thickness higher than $100\,nm$, resulting in an electric field of generally $2\,MV/cm$. This high field is influenced by surface charges and defects, which combined with the accelerating effect of temperature allows to evaluate not only the stability of the leakage current but also the influence of surface cleanliness, especially for power modules, where the dice are only protected by a silicone soft gel [6].

1.3.1.3 Temperature Humidity Bias (THB) Test

The Temperature Humidity Bias (THB) test or High Temperature High Humidity Reverse Bias (H3TRB), evaluates the ruggedness of DUTs against 3 combined stressors:

humidity, high voltage, and high temperature, the last of which is used as an acceleration factor. According to current standards for testing [21, 22, 27] describing the testing protocol and requirements, the following values for temperature, humidity and bias are shown as reference:

- **Temperature**: 85°C
- **Humidity**: 85% R.H.
- **Reverse Voltage (DC)** : $80\% \cdot V_{nom}$ (100V max)

Discrete packages are supposed to be hermetically sealed against humidity, and when no defects are present, devices perform as expected in terms of BV and leakage current.

Since this condition is not always trivial to achieve in a manufacturing platform, THB testing is always included in the qualification plan of power semiconductor devices, and it will be explained in part II, the general approach is to remove the bias limitation and test the devices at the true 80% of their nominal blocking voltage [1–3, 28–30].

Furthermore, humidity penetration is more critical to power modules, where the only protection is a silicone soft gel, the type and deposition of which can even introduce contaminant ions, yielding to can local changes in the behavior of the device in terms of BV and leakage current, or even long term reliability failure.

Moreover, another main aspect of silicone soft gel is the high humidity absorption causing humidity to reach the surface of the chip. In this way voltage-humidity phenomena such as corrosion, electrochemical migration, and ion transport can be triggered causing BV and leakage current degradation. For these reasons, Temperature Humidity Bias (THB) is considered the main test to evaluate the reliability of the passivation stacks and terminations in power semiconductor devices.

In the case of power modules, additional protective layers on top of the silicone soft gel have been proposed, but with the risk of lowering humidity diffusion outwards the module when the external value of humidity is lower than the inside's value, for this reason if humidity absorption cannot be lowered such as in the case of advanced epoxy rosin materials, the only choice is to remove humidity faster to avoid moisture trapping thanks to high diffusive non-hermetical compounds.

A more extended review of THB testing will be treated in part II, since one of the main topic of this work is related to the high voltage version of this test, with the aim of testing devices without limiting voltage to the $100\,V$ value, in order to understand their performance in terms of reliability.

1.3.1.4 High Temperature and Low Temperature Storage Tests

High temperature and low temperature storage tests have been implemented in order to test material integrity, focusing on rubber, plastic, and organic passivation materials, as well as typical module soft mold gels and glues.

The term "storage", refers to the device being not in operation [6], so the term is referring to the maximum and minimum temperature limits out of which the device will be undergo permanent damage due to the environmental temperature, which for the purpose of this test is static.

For instance, typical silicone gels involved in module production have high temperature limits of 180°C and low temperature limits of -55°C, which are in the range of automotive applications (-40°C to 150°C range), but may result inappropriate in the case of e.g. space applications or high temperature applications such as oil and gas drilling [31].

Below their critical temperatures, cracks will appear in soft molds and rubbers so that when the temperatures goes back to normal their elastic properties will not be restored. Similarly, degradation of some materials happens at high temperatures, but when the temperature is back into operational limits. In both cases, these kind of the damages cannot be restored, yielding to performance and integrity loss for the device, both in terms of humidity and mechanical properties.

In conclusion, it is clear how these requirements will be harder to satisfy when future application will require extended operative ranges, thus making these temperature tests a crucial step for qualification.

1.3.1.5 Temperature Cycling and Temperature Shock Test

Temperature excursions are a remarkable stress for power semiconductor devices and their packaging, depending on their final application, for these reasons the Temperature Cycling and Temperature Shock test are key qualification tests which emulate the variations of temperature during working operation.

Depending on the entity of the temperature wings (i.e. °C per minute), these tests can be divided in two typologies: fast and slow temperature swing. The first type, involving temperature swings of around $10 \div 40$ °C/min, is generally called temperature cycling test, and the DUTs are translated repeatedly between two separate environments representing temperature extremes, with typical chamber temperatures of - 40 °C to + 125 °C [32].

Oppositely, in the second testing method, higher temperature swings are applied. This test is generally performed by changing the heat transfer method from air to liquid in order to increase the heat transfer rate, for instance involving liquid baths of hot oil at more than 150 °C and liquid nitrogen on the other extreme at a temperature of -196 °C, allowing higher thermal "shock" to the devices.

Moreover, at the beginning of the test and after each step of the cycling sequence, having a 1000 cycles requirement, devices undergo electrical testing in order to detect material and performance degradation.

The above described tests have the objective of evaluating the whole device assembly in order to highlight possible criticalities between materials having different thermal expansion coefficients, including both functional and interconnection layers. It has been shown that bi-metal strain can be reduced by designing proper heat-sinks allowing proper heat transfer rates, in order to reduce bending and increasing the lifetime of the device [33].

The typical failure mode involves crack formation and layer delamination, which can be detected by Scanning Acoustic Microscopy (SAM), X-Ray imaging, and Scanning Electron Microscopy (SEM) imaging. Given the nature of the failure mode, it is important to highlight that package having small size are less sensitive to thermal shock failure with respect to large assembly (e.g. Power modules) given the compactness of the assembly and lower bending thanks to the smaller size of their lead frame and interconnects.

1.3.1.6 Power Cycling Test

In a power cycling test, the DUTs are self-heated by an intermittent current flow in forward conducting conditions. The quantity of the dissipated heat flow is proportional to the area of the device and the device technology.

The general setup involves a battery of DUTs mounted on a heat-sink emulating application conditions, while the devices are set in DC conduction with proper timing in order to obtain a well defined temperature curve. During the ON time the device self-heats until the maximum target temperature, detected by a sensing current, is reached. At that point, the load current is switched OFF and the device is cooled until it reaches the selected minimum temperature and ends the cycle, which is then repeated for the required amount of times.

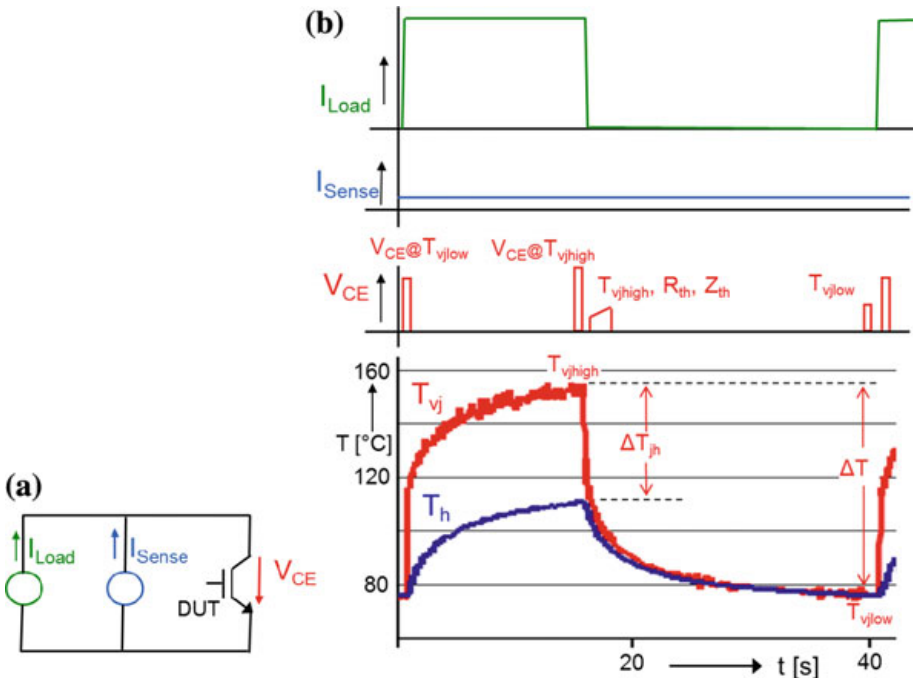


FIGURE 1.5: Power cycling typical circuit schematic (a) and time evolution of a single power cycle, highlighting the load current, the sense current, the voltage drop on the device (i.e. IGBT) and the temperature evolution. © 2018 Reproduced with permission from [6].

The lower limit is set by the heat-sink temperature T_h, and represents the lower limit in which the device is back to its initial temperature conditions. The main parameters of this test are:

- ΔTj: the temperature delta between the maximum and minimum junction temperature of the DUT
- T_m: the average temperature of the DUT
- t_{ON}: the ON time of the load current

If we define the ΔTj as in the following formula:

$$\Delta T_j = T_{high} - T_{low} \tag{1.10}$$

The value of the average temperature T_m can be defined as:

$$T_m = T_{low} + \frac{T_{high} - T_{low}}{2} = T_{low} + \frac{\Delta T_j}{2} \tag{1.11}$$

Moreover, depending on the value of t_{ON}, which is the other important testing parameter, it is possible to stress the device in different ways depending on the duration of the load current pulse. Normative IEC 60749-34:2010 [34] defines a short and a long pulse test, with $t_{ON} < 5\,s$ in the first case and $t_{ON} > 15\,s$ in the second.

On the one hand, the short pulse power cycling, the self heating is mostly limited to the interconnects and wires and is very useful to highlight possible design issues related to the quality of the bonding and of the metallization.

On the other hand, the long pulse test applies a much higher stress and allows to evaluate the overall strength and resistance of the assembly materials to thermal fatigue, simulating possible harsh intermittent behavior of real applications. [6]

Typical failure mechanisms include, wire bond lift-off (see Figure 1.6, metallization degradation or reconstruction, solder fatigue or wire bonding heel cracks. These latter can be interlinked, thus requiring accurate failure analysis in order to determine the root cause of the failure and improve device reliability.

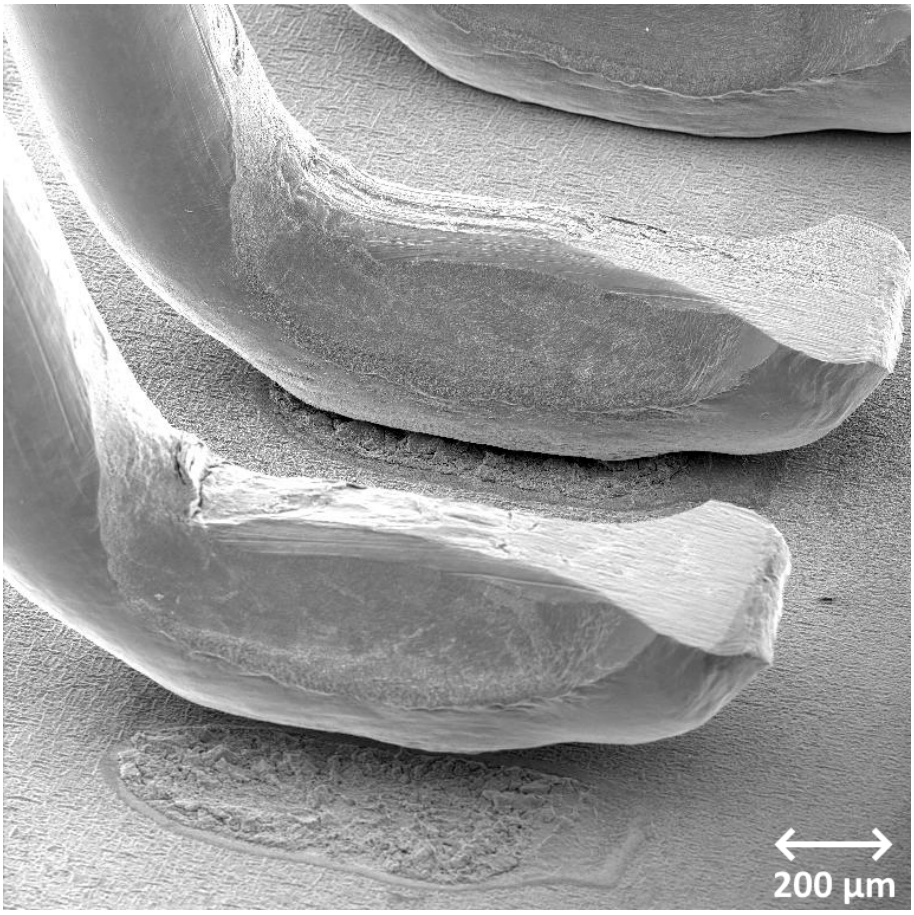


FIGURE 1.6: Example of wire bonding lift-off due to power cycling

In general, the detection of failure is achieved through the monitoring of the forward voltage drop of the DUT, with typical limits of 5% and 20% increase with respect to the initial value. Moreover, failure can also be determined by final electrical characterization by showing an increase of Rth or parameteric degradation of BV, leakage current or ather typical parameters. For further reference please consider the following publications [6, 22, 34, 35].

1.3.1.7 Cosmic ray Testing

Even if this test is not yet included in the main qualification standards, the importance of electronic equipment sensitivity to cosmic radiation, in particular for power electronic devices, has been gaining importance among device manufacturers since the observation of early failures in the first years of the 1950's decade.

High-energy phenomena including high energy radiation bursts and particles, can induce the formation of particle "showers" in the earth's atmosphere. These particle showers are composed mostly of high energy neutron and protons, which can interact with electronic circuits and cause either digital disturbances or critical failure depending on the kind of application [6]. In the particular case of power electronics, when a device is in reverse bias, and for voltage levels above 200 V, a so called Single Event Effects (SEE) caused by single particle collisions, can induce local breakdown phenomena yielding to a sudden device failure called Single Event Burnout (SEB).

The nature of this phenomenon, the related normatives and the testing methods will be discussed in Part IV.

1.3.2 Current and future challenges of reliability testing

1.3.2.1 Current approaches to enhanced reliability

Following from the testing methodologies listed in section 1.3, it is possible to do several consideration to shed a light on the current approaches and testing methodologies. First of all, these tests generally involve the use of new, randomly chosen devices from production or samples, in order to perform a single reliability test. But another approach could be, in order to improve the reliability level of the devices, to perform more than one test on the device, defining a test chain where each device undergoes a sequence of several test conditions, increasing the number of possible testing methods It is indeed hard to have a reference literature of such testing approach, which generally is adopted internally by companies for what is called design for reliability, with the aim of improving the design from the reliability point of view and reducing the management cost of solving reliability issues when the design is frozen and already in production. An example of this kind of approach, has been materialized in the concept of sequenced Highly Accelerated Life Test (HALT) and Highly Accelerated Stress Screening (HASS)), testing. When a device undergoes HALT testing, the testing levels are increased progressively, and even beyond, the datasheet conditions until the failure of the DUT. Some examples of this kind of test can be for instance the step-by-step increase of voltage during insulation testing, or a progressive increase of temperature swing during the power cycling test. After the HALT test, and by using the same enhanced limits coming from the latter procedure, the stress conditions of the HASS can be defined. These new conditions are generally set higher than the datasheet conditions, but with a guard-band to let the device operate below the destruction level. The defined HASS conditions are then applied to production devices, in order to perform a screening of the weak devices which could result on a failure on arrival or failure on the field faster than expected. In general, in the stress sequence, a combination of stress levels can be applied. This is what happens, for instance, for power modules, when both high load currents, variable ambient temperature and vibration are combined and applied simultaneously to simulate working operation in the final applications.

A further development of the testing approaches is defined in [5], and denominated "robustness validation", where all the knowledge from testing and device simulations is combined together, in order to define dedicated specification limits and "mission profiles"

to improve the reliability of the devices. Real mission profiles are not easily defined, and sometimes even the measurement of real stress in the final application requires a significant amount of time, as it is for instance the case when humidity and temperature is monitored throughout the four season of the year in a wind power farm, or even defining a "reference" mission profile for automotive applications when the vehicles are used in the most various environmental conditions across the globe. A way to address this issue is to implement monitoring strategies, in order to perform more realistic measurements to better outline the stress requirements, and perform active evaluation on particular device parameters with the objective of avoiding sudden failure of the system in use [36–39].

1.3.2.2 Future Challenges

Last developments in research and market trends, show how wide bandgap power devices are the present and future of power electronics, thanks to their superior material characteristics, which makes them the most suitable successors of silicon devices. For this class of devices, properties such as superior thermal conductivity, high breakdown fields and high saturation drift velocity, will enable the development and deployment of new highly reliable and efficient technologies in a wide variety of fields, such as communications, energy harvesting, electric mobility and many others [40]. The two main protagonists of this transition into the wide bandgap world, are SiC and GaN [41–43], for which a summary of their characteristics and most suitable applications is shown in Fig. 1.7 with respect to Silicon.

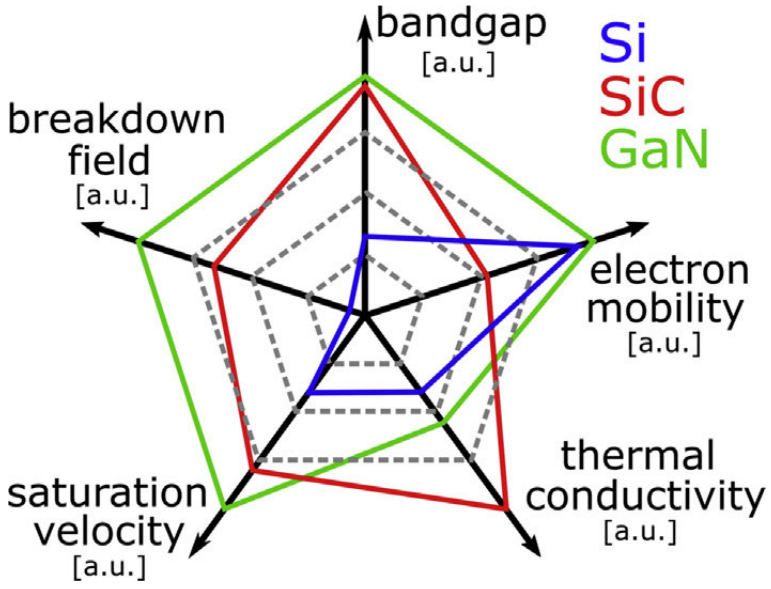


FIGURE 1.7: Wide Bandgap Materials Properties Diamond Chart [44].

The main peculiarity of these new generation of devices, is that with the improvements in terms of bulk materials and front end processing, proceed at a faster pace with respect to the development of the packaging technologies, and this holds for both discrete packages and power modules [45]. In order to close this gap, and allow the full deployment of these new technologies, reliability testing will be a key requirement with respect to the following trends related to the improvement and qualification of the assembly technologies.

The first is the increase of current density, which can be obtained only by lowering the voltage drops at the package level, accounting to a significant amount at rated current, which can be lowered by reducing the series resistance from the package contacts down to the metallization of the chip. The second aspect is the continuously increasing trend of the power density requirements per unit area, requiring dedicated systems for heat dissipation. The third factor is the maximum junction temperature of the devices, which is set by the material and for classical silicon devices can reach a maximum of 200 °C, only with a considerable amount of development in terms of leakage current and passivation reliability. This point can be addressed thanks to SiC and GaN technologies thanks to their superior thermal conductivities, but a true improvement can only be achieved with enhanced package thermal design, especially in terms of power cycling capabilities. Eventually, the fourth factor is the minimization of parasitic inductances and capacitances, which need to be controlled in order to be assimilated into functional elements, and not just an intrinsic issue of the circuits. Moreover, all these factors are interconnected, and a dedicated solution must be tailored to each application in order to obtain the wanted performance, which is a remarkable challenge for researchers and designers around the world [6].

For instance, the substitution of the classical wire bonding with flat metallic foils (e.g. Ag) is one kind of proposal to address the increase of current density by allowing a better contact with reduced DC resistance, improved heat dissipation, optimized current flow distribution, as well as reduced inductance and electrical parasitics [46, 47]. In addition, several kinds of interconnects are under evaluation such as ceramic-based structures [48]. This solution works very well when complemented by another interesting proposal, which is the inclusion of a liquid cooling circuit inside the base plate of power modules. This solution can yield very high heat transfer rates, removing the need of the intermediate thermal grease layer, thus significantly lowering the overall thermal resistance [49]. Furthermore, in order to achieve higher power cycling capabilities at maximum Tj, it is possible to exploit the low Low Temperature Joining (LTJ) process. In this sintering technique, a silver particle powder is deposed between two plated surfaces which are protected with an organic film to avoid the diffusion of Ag. Then the combination of pressure and temperature up to 250°C removes the protective layers allowing the diffusion and densification of Ag, yielding a highly reliable interconnection sintered layer [50]. This technique also improves the thermal conductivity up to four times with respect to standard SnAg soldering with very thin layers measuring even less than $20\mu m$, reducing the substrate-chip thermal resistance, while having a very high melting temperature. Moreover, new pressureless sintering techniques are under evaluation [51].

Part II

High Voltage Temperature Humidity Bias (HV-THB) Test

Chapter 2

High Voltage Temperature Humidity Bias (HV-THB) Test

2.1 Introduction

The problem of humidity and its effect on power circuits has been, is, and will remain a topic of great importance in the field of power electronics. Modern qualification standard for power semiconductor devices, from Si to wide band gap alternatives, always include at least the standard Temperature Humidity Bias (THB) test to highlight possible design and assembly issues with the reliability of the final product causing performance degradation or even critical failure on the field when the device is in operation in its final application. Moreover, the high-voltage version of this test is becoming the de-facto standard to intercept possible reliability issues in state-of-the-art power devices, as it will be shown in the following sections.

For this reason, one of the main objective of this industrial PhD work has been the development of a dedicated High Voltage Temperature Humidity Bias (HV-THB) testing setup, control software and methodology, to perform and analyze the sensitivity of a set of sample devices against humidity using 650V power diodes as testing vehicle, assembled in standard MTP packages.

In the first part of this chapter, an overview of current methodologies for HV-THB testing is reported as a complete review work from the author [2]. The second part of the chapter is then complemented by a description of the methodologies, including the control software and measurement boards, followed by the experimental results and discussions related to the analyzed samples, which led to the publication of two papers by the candidate [1, 3].

2.2 Review and state of the art of HV-THB

The main objective of this section is to present an in-depth overview of current HV-THB testing in order to give the reader a broad representation of current approaches to setups and methodologies for the reliability assessment of combined voltage and humidity effects, for the qualification and analysis of power semiconductor devices.

As already mentioned in Part I, this is one of the main topic of the thesis, which led to the publication of 3 peer reviewed papers [1–3], of which reference [2] is exactly the topic of this section.

For this reason the content of this section will be reproduced as-is, in compliance with the publisher's (MDPI - `https : / / www . mdpi . com/`) open access license (`https : / / www . mdpi . com / openaccess`). The following material of section 2.2 is reproduced with permission from the paper entitled "High-Voltage Temperature Humidity Bias Test (HV-THB): Overview of Current Test Methodologies and Reliability

Performances" [2], located at `https://doi.org/10.3390/electronics9111884`. The policy excludes the copyright of the figures, for which the author obtained dedicated permissions for reuse, in order to keep the original form of the whole paper and safeguard the integrity of the work.

2.2.1 Introduction

The last few years have seen a remarkable drive toward the use of alternative energy sources, and the transition from fossil fuels to electric energy in several fields. For these reasons, the efficiency and reliability of power semiconductor applications have become critical focuses of the industry, along with the increasing of performances [52]. Therefore, researchers and designers in the field of power electronics are challenged to find new solutions and adapt current designs to achieve the expected transition into an electric world, while allowing all new technologies to meet and go beyond current safety and reliability requirements [30]. The only way to achieve this target is to intercept possible failures not only by following current regulations, but also going a step forward and testing devices and systems with increased stress, in order to broaden the spectrum of application for each piece of technology.

The presence of humidity is one of the most critical factors for the reliability of power semiconductor devices and circuits [6], and each component has its own sensitivity to this stressor, especially when high-voltage designs are considered [53, 54], so that proper design rules must be implemented to avoid failure. Common power semiconductor devices are generally deployed in either plastic packages, where usually one or two devices are encapsulated in molding compound, or power modules, in which several power devices with a given topology are integrated into a single case filled with gel. In plastic packages, the penetration of moisture is very slow when compared to modules [3], since plastic packages offer a higher level of protection with respect to gel. That happens in the case of power module packages, easily allowing moisture penetration toward active areas of the devices [28].

When power devices are biased in humidity conditions, the co-presence of high-electric fields and moisture can trigger failure mechanisms which are different with respect to cases where each stressor is applied singularly, alongside with the temperature of the environment in which the device is operated. The high voltage temperature humidity bias (HV-THB) test is a device test which can be applied to power devices both in plastic packages and power modules [1, 3, 55, 56]. In this kind of accelerated test, the devices undergo triple stress due to the simultaneous application of high-voltage reverse bias, high-humidity and temperature for a pre-determined period of time. In this review, we will focus on HV-THB testing, comparing the methodologies, acceleration models, failure modes and passivation materials, in order to give an overview of state-of-the-art voltage-humidity testing for power semiconductor devices.

2.2.1.1 Current Normatives

As highlighted in the previous paragraph, the most tested vehicles are power modules and plastic packages. In the case of plastic packages, the current normative for discrete active electronic components is the AEC-Q101 [21] by the Automotive Electronics Council, entitled "Failure mechanism based stress test qualification for discrete semiconductors in automotive applications" defining the minimum stress test requirements and conditions for automotive applications. This normative defines several tests in both static and dynamic environmental and electric conditions, including the humidity bias

testing, named the high humidity high temperature reverse bias, or H3TRB. The test requires the devices to pass 1000 h test with an ambient temperature (Ta) of 85 °C and relative humidity (R.H.) of 85%, while reverse biased at 80% of rated blocking voltage (V_{nom}) up to a maximum of 100 V DC. Moreover, the devices must be electrically tested at least before and after H3TRB as a minimum requirement. In real qualification tests, devices under test (DUTs) are evaluated at defined times—for instance, 0 h, 168 h, 500 h and 1000 h—in order to record the evolution of the electrical parameters in a more detailed way. It is important to notice that the current standard does not require continuous monitoring of any electrical parameters. In the case of power modules, the reference normative is the ECPE AQG 324, "Qualification of Power Modules for Use in Power Electronics Converter Units in Motor Vehicles" [22]; the H3TRB test is described in section QL-07. The static conditions of 85 °C and 85% R.H. are the same as those seen in AEC-Q101, while the maximum V_{nom} has a lower limit of 80 V. It should be noticed that this $80 \div 100\,V$ limitation was set in order to satisfy the maximum temperature increase and maximum power dissipation required respectively by the IEC 60068-2-67 [57] and IEC 60749-5 [27], on which the latter regulations were based, in order to avoid unwanted self-heating that would drive away moisture [58] or the additional failure modes which are instead investigated by the HV-THB version of the test. For both power modules and plastic packages, the DUTs must be electrically characterized before and after each test iteration until the 1000 h requirement is satisfied, and they need to be DC biased in blocking conditions for the whole duration of the test. Table 2.1 shows a summary of the most important differences between current HV-THB parameters versus standard H3TRB, the details of which will be discussed in the following section.

Table 2.1: Generic stress parameters of standard versus high-voltage Temperature Humidity Bias (THB) test. The HV-THB is not limited in voltage, while the standard H3TRB has a maximum reverse bias voltage of 100 V [2].

Parameter	Standard THB (or H3TRB)	High Voltage THB
Temperature	85 °C	85 °C
Relative Humidity	85%	85%
Reverse Bias	$80\% \cdot V_{nom}$	Up to $90\% \cdot V_{nom}$
Bias Limitation	Max. $80 \div 100$ V	Unlimited
Leakage Monitoring	Not required	Continuous

2.2.2 Comparison of Test Methodologies

2.2.2.1 Test Setup and Procedures

Performing a high voltage test in high humidity conditions requires a dedicated setup, in most cases capable of continuous active monitoring of the DUTs [1, 3, 53, 59–61], and with high voltage design rules requirements. A general schematic of the HV-THB test setup is shown in Figure 2.1 [1]. The DUTs are positioned on a high voltage biasing board or a dedicated rack inside a climatic chamber, allowing both environmental and electrical isolation with respect to the external environment. A high-voltage power supply unit (PSU) applies the voltage bias to the devices in the chamber and is controlled by a monitoring and control unit, usually a dedicated computer with ad hoc control software. Moreover, a measurement board with a dedicated active or passive circuit reads the

leakage current values flowing through each device. Where possible, the control software can be also linked to the test chamber, in order to continuously monitor both humidity and temperature levels, which must be kept under control during the whole duration of the test. Moreover, an overcurrent limit is usually set to prevent extended damage in case of DUT failure [62], and active leakage monitoring can also be configured in order to remove device bias in cases of high leakage drift beyond a previously set value, so that critical failure is avoided and fine failure analysis can be carried out on the samples [1].

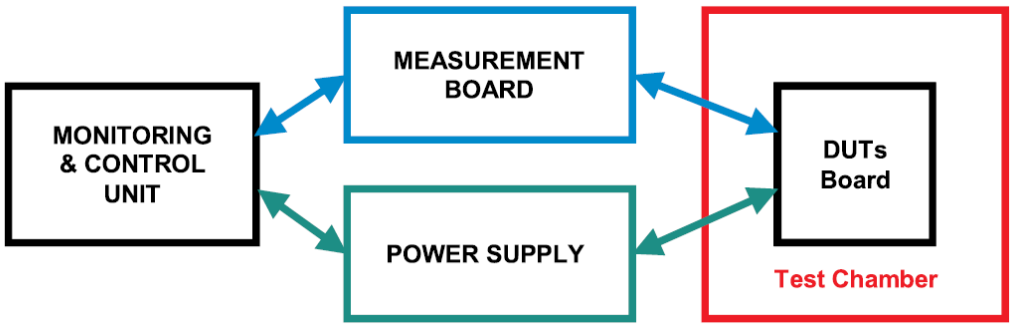


FIGURE 2.1: Schematics of a generic HV-THB test architecture. Figure reproduced with permission from [1].

The testing procedure is generally performed as follows: the DUTs are tested with a curvetracer in order to obtain their reverse I-V characteristics, and are then positioned in the climatic chamber and integrated in the test circuitry. In order to avoid condensation, the chamber is ramped up to 85 °C and 85% R.H., and only after reaching stable conditions is the voltage applied. The devices are then monitored continuously, and the test is halted in order to perform intermediate reverse I–V characteristics to evaluate the status of the DUTs at desired checkpoints (0 h, 168 h, 500 h, etc.) up to their nominal blocking voltage V_{nom} or below their Breakdown Voltage (BV). At these checkpoints, the devices are left outside the testing chamber [1, 3] or baked [29] in order to drive out moisture before testing at room temperature.

2.2.2.2 Leakage Current Monitoring

Leakage monitoring is a key feature when performing HV-THB, especially in the first hours of testing. In this period, the leakage curves usually show a peculiar transitory behavior that must be taken into account to properly set the test limits. This behavior is depicted in Figure 2.2. The leakage curve has an initial steep increasing trend, later evolving into an asymptotic decreasing behavior, which is probably caused by charge relocation inside the DUT and is not related to the typology of the device—for instance, there are metal oxide semiconductor field effect transistors (MOSFETs), insulated gate bipolar transistors (IGBTs), power diodes, etc. [1, 28, 56, 62, 63]. This behavior is always present, but no literature specifically addresses a model for this phenomenon.

In order to address this behavior, it is not possible to stick to the usual strategy of setting a rigid percentage limit to discriminate between test pass and fail. The general approach is to leave the DUTs to follow their evolutions, and after reaching the maxima

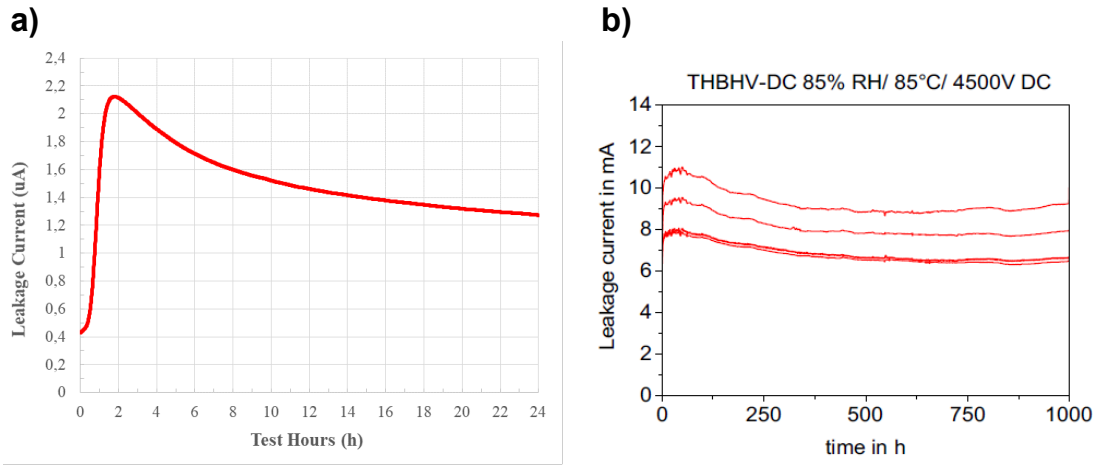


FIGURE 2.2: Typical leakage monitoring curves for a single 650 V power diode in the first 24 h of HV-THB testing at 85 °C and 85% R.H.—reverse biased at 80% V_{nom} (a). Evolution of HV-THB testing for a set of 4 power modules with 24 IGBTs and 12 diodes each, tested at 85 °C and 85% R.H. with a reverse bias at 4500 V (b). (a) Reproduced with permission from [1] and (b) reproduced with permission and adapted from [63].

of their respective curves, constantly read the minimum values of the curves and set those as the references for classical rigid limits in the form of:

$$I_{monitored} < \alpha \cdot I_{reference} \tag{2.1}$$

where $\alpha > 1$ is a chosen positive constant defining the maximum limit with respect to the reference value [1, 60]. It is important to notice that sometimes, during the asymptotic phase of the test, some devices could exhibit an unstable behavior (Figure 2.3). It can be seen that the DUTs overcome the fixed limit and subsequently go back to their asymptotic regime [55, 60, 64]. In this case, there is no clear agreement coming from the authors on whether to consider this behavior a pass or a fail, but its effect is something that needs to be considered when designing the final circuit.

A similar recovery behavior has been observed also during the HV-THB testing of SiC MOSFETs. In this case a DUT showed a temporary reduction in blocking voltage capability at 6000 h of testing, and later fully recovered its blocking voltage at the 9000 h checkpoint measurement [64]. Another point that should be examined regarding leakage current monitoring is the sampling time during the test. Considering the general evolution of a HV-THB monitoring curve, it is hard to define a standardized value for the sampling interval, which depends on the behavior of the technology under examination. For this reason, since a single sampling value cannot be defined, future standards will need to take this into account when defining the guidelines of the HV-THB testing in order to set a minimum monitoring frequency. For instance, authors report sampling rates ranging from 1 s [59] to 5 min [61]. Moreover, the presence of higher frequency peaks on the monitored signal [55] implies that the choice of a longer sampling time has to be considered only if the presence of these peaks is not meaningful with respect to the trend of the curve for the technology under examination, since these peaks could not be detected and averaged out by the longer sampling time. For this reason, it is also important to have stable temperature and humidity conditions inside the chamber,

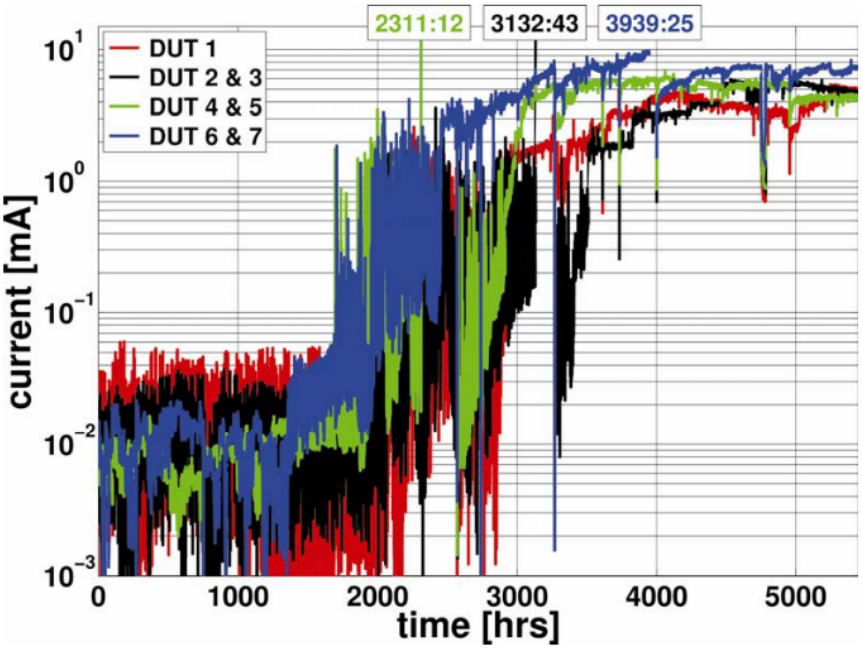


FIGURE 2.3: Example of an HV-THB test monitoring for 1.2 kV devices tested at 65% V_{nom}. Failure timestamps are reported at the top of the picture. Figure reproduced with permission from [56].

in order to remove secondary effects such as the periodic oscillation of the curves, which may be related to the thermostat and hygrostat cycle times inside the test chamber.

2.2.2.3 Intermediate Testing and Electrical Degradation

As already specified in section 2.2.2.1, intermediate measurements are performed in order to evaluate device degradation at each checkpoint of the HV-THB testing. The observable degradation of characteristics generally occurs in two ways, as represented in Figure 2.4.

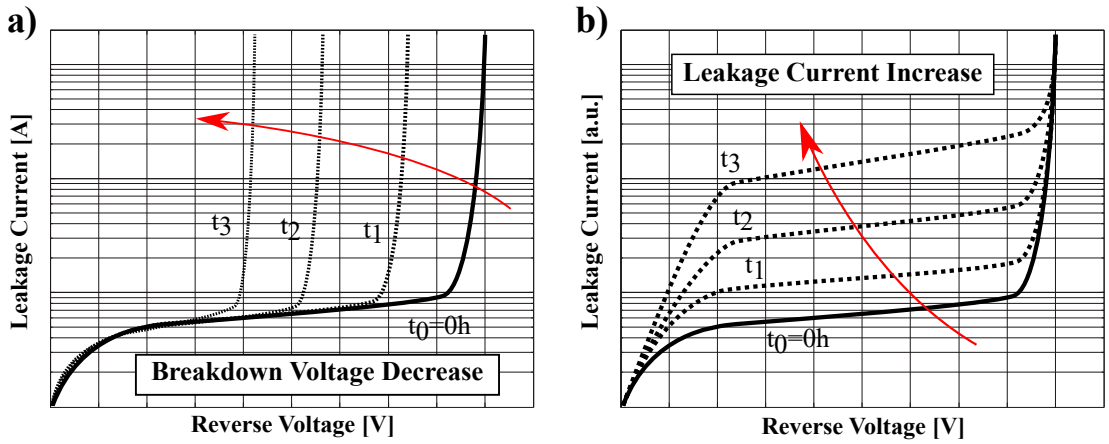


FIGURE 2.4: The two main types of electrical degradation of I–V characteristics after HV-THB: Breakdown voltage decrease (a), and leakage current increase (b) in a generic power semiconductor device [2].

The first type of degradation is a decrease in breakdown voltage (Figure 2.4a), where the knee of the characteristic moves toward lower voltages, but without increasing the leakage values below the Breakdown Voltage (BV) voltage. The second kind of degradation is the gradual increase of leakage on the whole characteristic (Figure 2.4b), but without significantly impacting the BV value. Both these electrical degradation mechanisms can happen at the same time, and have direct effects on the leakage current measured by the monitoring system. It is important to highlight that the observable degradation of the characteristics, involving either an increase of leakage current or a decrease of BV, is mostly due to the wear out of passivation stacks in the junction termination regions, where voltage–humidity-related phenomena are generally localized [1, 3, 28, 56]. These phenomena will be described in the following sections.

2.2.2.4 Accelerated Test Models

In order to define a model for the accelerated stress of the HV-THB, as proposed by several authors [28, 29, 56, 61], it can be useful to list previously defined models in order to see which are the most suitable for the calculation of the acceleration factor. First, we have the DiGiacomo model, a physical model developed to describe the behavior of metallic migration in encapsulated packages. This latter is defined in equation 2.2 [65]:

$$t_f = \frac{Q_c}{\beta \cdot J_{tip}} \tag{2.2}$$

In this equation, t_f is the time to failure for dendritic growth between the two biasing electrodes, Q_c represents the critical amount of migrating metal ions required to achieve dendrite formation across the space between the electrodes, β is the degree of oxidation or fraction of active surface (which is metal dependent) and J_{tip} is the current density at the dendrite tip [66]. This model, which is based on Butler–Volmer's equation relating electrode potential to current density [67], is indeed well defined from a physical point of view and gives good insights into the nature of the phenomenon, but it is not applicable to HV-THB testing because it needs to be related to the stressors of the test: temperature, humidity and voltage. For this reason, several models can be integrated in order to extrapolate the acceleration factor. The first step is to consider the Arrhenius equation, linking temperature and reaction rate, described in equation 2.3:

$$t_f = A_1 \cdot \exp\left(\frac{E_A}{k \cdot T}\right) \tag{2.3}$$

where t_f is the median time to failure, A_1 is a fitting parameter, k is the Boltzmann's constant, T is the absolute temperature and E_A is the activation energy for the chemical reaction. The Arrhenius equation only considers the effect of temperature, so the model must be extended in order to include multiple stressors. A first approach to this extension could be achieved with the Eyring equation [66, 68], but with the drawback of increasing the complexity of the equation. For this reason, the Hornung model is preferred [69], and its equation was developed to describe dendritic growth based on the

Arrhenius model [66] by adding the effect of voltage to the term A_1 from equation 2.3:

$$t_f = \frac{\alpha \cdot d}{V} \cdot \exp\left(\frac{E_A}{k \cdot T}\right) \tag{2.4}$$

In this equation, α is a fitting parameter, d represents the spacing between the electrodes and V is the applied voltage [66, 69]. Furthermore, it is possible to consider the effect of humidity by considering Peck's model [70]. This model extends the Arrhenius equation by including relative humidity to the Arrhenius model [70–73]:

$$t_f = A_3 \cdot RH^{-x} \exp\left(\frac{E_A}{k \cdot T}\right) \tag{2.5}$$

where A_3 and x are fitting coefficients, and RH is the relative humidity. In this way, by combining Hornung's and Peck's models (Equations 2.4 and 2.5), it is possible to derive an acceleration factor for the stressors of the THB test [28, 74–76]:

$$a_f(RH, T, V) = \left(\frac{RH_a}{RH_u}\right)^x \cdot \exp\left(\frac{E_A}{k} \cdot \left[\frac{1}{T_u} - \frac{1}{T_a}\right]\right) \cdot \left(\frac{V_a}{V_u}\right)^y \tag{2.6}$$

where the indices a and u refer respectively to the accelerated and usage conditions. However, this approach does not include the interaction between the stressors. For reference purposes, additional details regarding each model (Equations 2.2 to 2.6) can be found in the work by Zorn et al. from 2014 [28]. Voltage can indeed be a strong acceleration factor; in fact, let us consider the example from [29]. Here a standard 80 V THB test is compared to a HV-THB test with a bias of 65% V_{nom} (780 V) applied to 1200 V IGBT module devices. In this case, the substitution of the latter values into Equation 2.6 gives an acceleration factor of 150, meaning that the standard 80 V value from AECQ101 applies a significantly lower amount of stress at fixed 85 °C/85% R.H. conditions. Moreover, due to the nature of the test, long runners make it hard to estimate the effective acceleration of the test and the validity of the model, especially at voltages below 60% V_{nom}. In order to overcome this issue and estimate the effect of acceleration, one option [28] is to measure the reduction of the breakdown voltage. For instance, as reported in Figure 2.5, it has been shown that by passing from a 65% to 90% V_{nom} reverse bias, the experiments show an acceleration factor of 2.1 [56], which is not a huge increase but significant for a test that can last for several thousands of hours.

2.2.3 An overview of the failure modes

In section 2.2.1, it was anticipated that different package technologies could behave differently with respect to humidity intake. For instance, it has been shown that power modules and small plastic packages (e.g., standard TO-247) have significantly different moisture uptakes. In fact, for a standard MTP power module, a weight increase of 1.9 g has been measured after 24 h at 85 °C/85% R.H, mostly absorbed by the silicon gel, while it is not possible to measure a significant change in weight for a TO-247 package exposed to the same conditions [3]. The presence of humidity together with the applied bias can activate a chain of chemical reactions, leading to corrosion and consequently device degradation and failure.

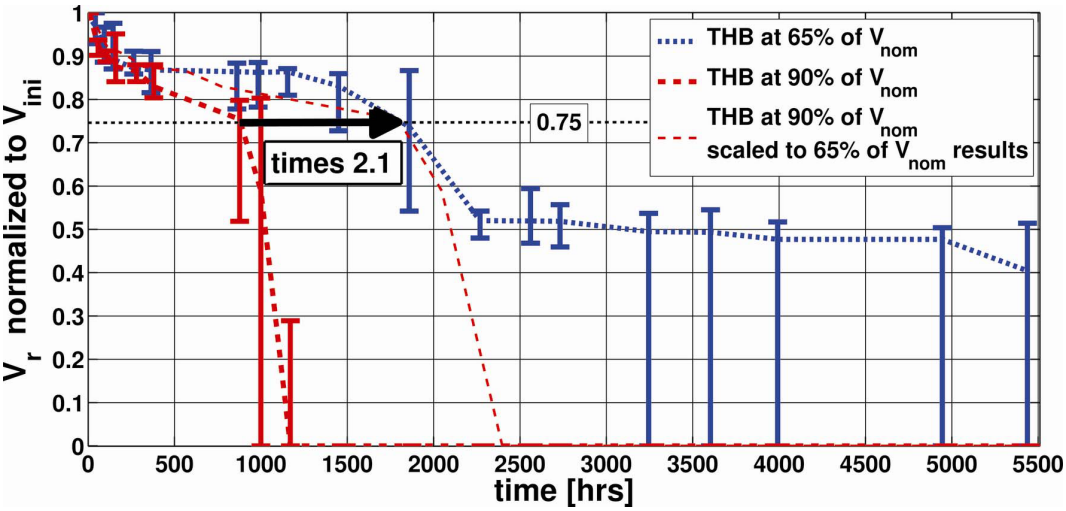


FIGURE 2.5: The effect of acceleration due to bias voltage with respect to the initial breakdown voltage (BV) values versus test time. Figure reproduced with permission from [56].

2.2.3.1 The Corrosion Cell

The corrosion process starts with the hydrolysis of water adsorbed by the surface between the biased electrodes, forming a so called "corrosion cell." This happens on the anode's surface, with the formation of hydrogen, according to the following oxidation reaction:

$$2\ H_2O\ \rightarrow\ O_{2(g)} + \ 4H^+ + \ 4e^- \tag{2.7}$$

Differently, the cathode side presents a reduction reaction with the formation of hydroxide ions and hydrogen gas [29, 77–80]

$$\begin{aligned} 2H_2O\ +\ 2e^-\ &\rightarrow\ H_{2(g)}\ +\ 2(OH)^- \\ 2H_2O\ +\ O_2\ +\ 4e^-\ &\rightarrow\ 4(OH)^- \end{aligned} \tag{2.8}$$

In this way, the anode side process yields a locally acidic solution, and the cathode side a basic one. Thus, a pH gradient is formed between the electrodes.

2.2.3.2 Aluminum Corrosion

Aluminum is very reactive and Al(OH)3 forms at its surface when in presence of water, yielding a high oxidation resistance at pH values between 4 and 9 [81–84]. Outside this range, the aluminum hydroxide can react as an acid or a base depending on the properties of the solution (i.e., pH and equilibrium potential). In the case of an acid solution, $Al(OH)_3$ is oxidized as follows:

$$Al(OH)_3\ +\ 3H\ \leftrightarrows\ Al^{3+}\ +\ 3H_2O \tag{2.9}$$

These ions are very unstable in solution, so the probability of them reaching the cathode by migration is very low. Oppositely, on the cathode side, the $Al(OH)_3$ can form aluminates following the reaction:

$$Al(OH)_3 \ + \ OH^- \ \leftrightarrows \ [Al(OH)_3]^- \tag{2.10}$$

Differently from Al^{3+} ions, these aluminates are very stable and can migrate in the solution, form a precipitate on the anode side or even form complex salt ions on their migration path. In addition, an alternate source of gaseous H2 with respect to water hydrolysis can be the following:

$$Al \ + \ 3H_2O \ \rightarrow \ Al(OH)_3 \ + \ \frac{3}{2}H_2 \tag{2.11}$$

This gaseous hydrogen, and the product of Equation 2.8, can lead to blistering and delamination of the upper passivation layers [3, 85]. The whole reaction is represented schematically in Figure 2.6 [56], where the process is described schematically in Figure 2.6a, while a real example of aluminum corrosion is shown in Figure 2.6b.

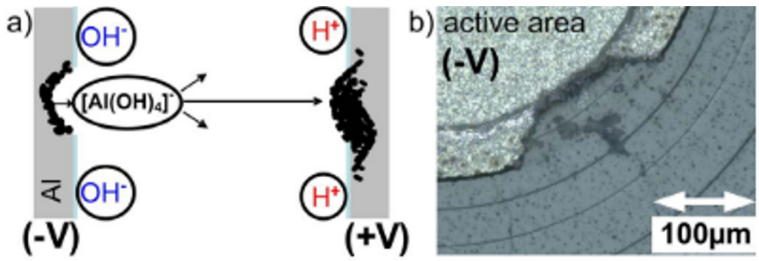


FIGURE 2.6: Schematic process of aluminum corrosion and accumulation (a). An example of an eroded metallization edge on the junction termination of a diode chip after HV-THB testing (b). Figure reproduced with permission from [56].

2.2.3.3 Electrochemical Migration (ECM)

Section 2.2.3.2 has shown how aluminum has a peculiar migration behavior when a corrosion cell is built, but not all metals have the same behavior with respect to transport under an electric field. For instance, for Cu and silver, which are common materials involved in powered device manufacturing, failure due to ECM can be observed since the native metal oxides of these materials can be easily decomposed, and due to local acid conditions, metal ions are produced by corrosion at the anode, following the reaction [56, 86]:

$$M \ \rightarrow \ M^{n+} \ + ne^- \tag{2.12}$$

The metal ions produced at the anode are then accelerated by the electric field toward the cathode. It is here that they can recombine back to neutral atoms and deposit on the cathode:

$$M^{n+} + ne^{-} \rightarrow M \tag{2.13}$$

This behavior is described schematically in Figure 2.7 [56]: here the Cu and Ag metal ions progressively build a dendrite structure following the direction of the electric field, starting from the anode side.

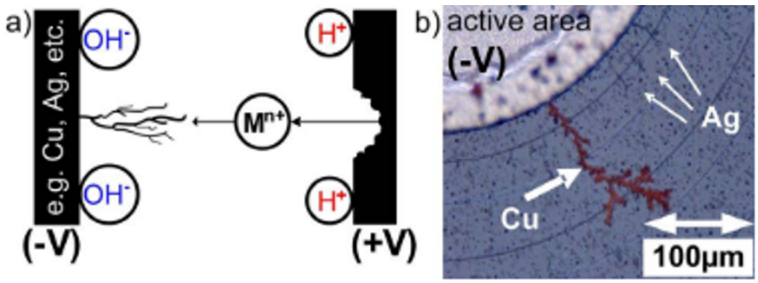


FIGURE 2.7: Schematic process of ECM dendrite formation (a) and an example of Cu and Ag dendrite formation on the junction termination of a 1.7 kV diode chip after HV-THB testing (b). Figure reproduced with permission from [56].

2.2.3.4 Device Failure Analysis

As a combination of the three mechanisms highlighted in section 2.2.3.1, 2.2.3.2 and 2.2.3.3, the entity of failure and degradation can manifest in several ways, which generally involve charge accumulation; a mix of polyimide blistering and lifting; and metal or nitride corrosion. An example of polyimide blistering is shown in Figure 2.8 for an HV-THB power diode at 80% V_nom [3]. The top view shows the presence of darker spots, where outgassing and lifting of the inner layers give rise to the presence of "blisters" or "bubbles" on the upper polyimide layer.

In the internal layers of the passivation, underneath the polyimide bubble, other layers showed significant degradation. In Figure 2.9a, the aluminum field plate of a power diode HV-THB tested at 80% V_{nom} is revealed with a focused ion beam (FIB) cross-section. The top polyimide layer was lifted, leaving a gap from the underlying metal field plate showing high degradation both in shape and composition. The change in composition was confirmed by energy-dispersive X-ray spectroscopy (EDX) at two points (Figure 2.9b), showing (1) no degradation and (2) compositional and shape degradation.

Moreover, it has been shown that even simple charge accumulation at the interfaces of the passivation stacks of HV-THB tested IGBTs [87] can lead to the electrical degradation of characteristics, as shown previously in Figure 2.4a. In this case, even if no morphological degradation is observed on the surface of the device, a significant reduction in BV voltage is reported, with negligible effect on the leakage current of the device. In this specific situation, localizing the point of degradation on the device is very hard and can only be achieved by getting accurate Focused Ion Beam (FIB) cross-sections of the DUTs [1, 3].

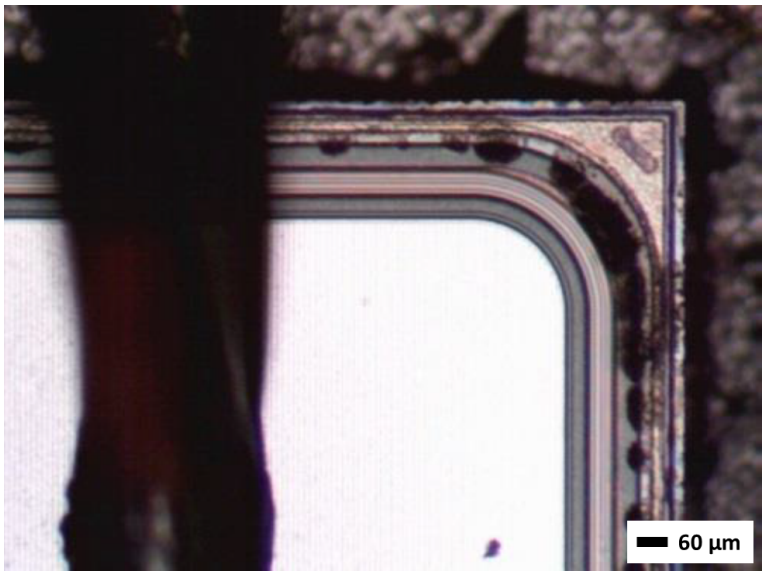


FIGURE 2.8: Top view of a decapsulated MTP module showing polyimide blistering (darker spots) after HV-THB testing. Device degradation is concentrated on the surface of the junction termination. Figure reproduced with permission from [3].

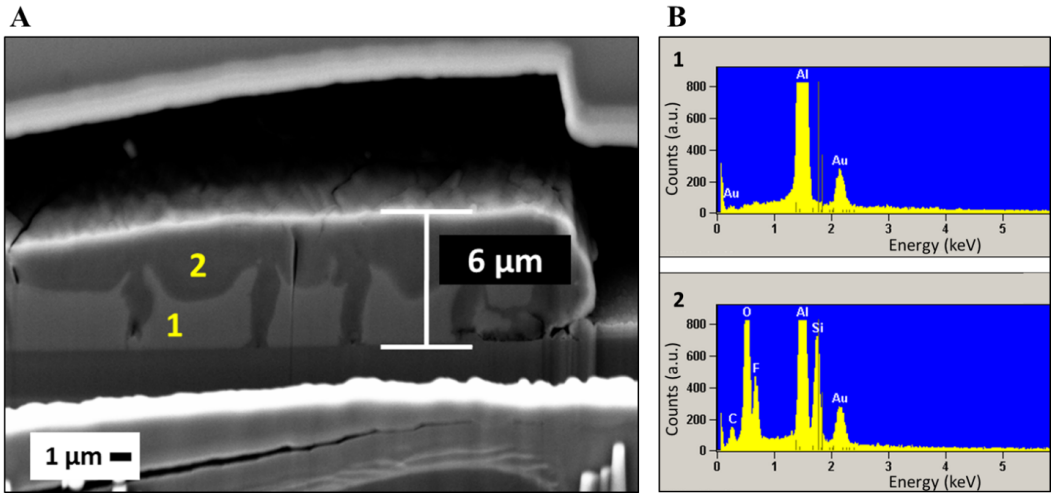


FIGURE 2.9: FIB cross-section of a degraded aluminum field plate for an HV-THB tested diode after 200 h of testing at 80% V_{nom} (a). The capping layer (polyimide) was lifted, revealing a gap and the underlying metal field plate, showing 2 different phases (b). The change in composition was confirmed by energy-dispersive X-ray spectroscopy (EDX) analysis at 2 points, showing: (1) no degradation and (2) compositional and shape degradation. Figure reproduced with permission from [3].

2.2.4 Materials and Accelerated Testing Performances

As seen in the previous sections, HV-THB applies a strong stress to the DUTs, and as highlighted by several studies [3, 30, 55, 63, 80, 88–92] the optimization of power semiconductor devices against humidity-voltage phenomena is strictly related to the intertwined roles of both the passivation stack and the structure of the junction termination, where field peaks are generally localized and can trigger humidity related

degradation processes [3, 88, 89, 93]. This section presents current developments in silicon and silicon carbide power semiconductor devices and their relative performances under HV-THB. In addition, it is important to highlight that humidity and reliability studies regarding other wide bandgap semiconductor power devices such as GaN and GaAs are currently ongoing, and can be already found in the literature; see, for instance, [94, 95]. Nonetheless, such studies will not be included in this review, since these latter are still at an early stage and do not yet present extensive results regarding HV-THB.

2.2.4.1 Passivation and Termination Materials

Moisture related degradation is strictly dependent on the materials of the passivation structure. Several solutions are possible, but in some cases a complex multi-material passivation stack becomes necessary to achieve superior roughness, as will be explained in the following sections. Table 2.2 shows key characteristics of a series of passivation materials for the manufacturing of power semiconductor devices. In Table 2, it is important to notice the differences in relative dielectric constant and critical electric field among the listed materials, in particular, for 4H-SiC, Si_3N_4, SiO_2, AlN and HfO_2, since these materials will be objects of discussion in the following sections.

TABLE 2.2: Dielectric constant, band-gap, and critical electric field for several dielectric materials with Si and 4H-SiC as reference. Table adapted from [2, 96].

Material	**Relative dielectric constant**	**Band-gap (eV)**	**Critical electric field (MV/cm)**	**Thermal conductivity (W/cmK)**
Al_2O_3	8	8.8	> 5	$0.02^{\#}$
AlN	9.14	6.03	$1.2 \div 1.8$	11.7
CaF_2	6.81	12.3	14.44	0.1
HfO_2	~ 30	6	8.5	$0.015^{\#}$
LiF	9	11.6	12.24	$0.15^{\#\#}$
Si_3N_4	7.4	5.3	10	0.3
SiO_2	3.9	9	10	$0.015^{\#}$
TiO_2	$24 \div 57$	3.05	2.7	$0.07^{\#}$
ZrO_2	15	5.8	$15 \div 20$	0.02
Si	11.7	1.12	0.3	1.5
4H-SiC	9.66	3.23	$3 \div 5$	3.7

\# - thermal conductivity data for sputtered material, otherwise for bulk

\#\# - thermal conductivity at 77K

Passivation coatings in silicon devices are generally divided into two categories: primary and secondary passivation layers. Primary layers are generally in contact with the bulk single crystal silicon, while secondary layers are generally separated from the bulk by at least one dielectric layer [97]. Both layers are important with respect to humidity related issues, since local immobile and mobile charges at their interfaces can have great impacts on device reliability. Historically, SiO_2 was generally the standard primary passivation material, grown by thermal oxidation in a dry or wet oxidizing atmosphere [97–103], which was generally followed by an annealing step to improve layer stability and overall electrical properties of the device [97, 103–107]. The deposition of secondary

passivation layers can have significant impacts on the electrical characteristics of the underlying layers. Thus, the deposition of a further layer becomes critical in order to obtain the desired electrical and reliability performances, since the application sequence of the passivation layers in power semiconductor devices is generally primary (generally SiO_2), secondary (SiO_2, Si_3N_3, etc.), upper organic passivation layer (polyimide, etc.) and a final capping silicone gel or epoxy in the case of power modules, or molding compound in the case of plastic packages [97].

2.2.4.2 Silicon Nitride as a Passivation Material

Silicon nitride Si_3N_4 is generally involved in the fabrication of high-reliable devices, due to its multiple advantages. In fact, silicon nitride can act both as a getter and alkali barrier [97], and at the same time have great resistance with respect to humidity. Silicon nitride layers are usually formed by the reaction of either SiH_4 or $SiCl_4$ in an NH_3 atmosphere at 800–900 °C, or at lower temperatures by plasma enhanced chemical vapor deposition (PECVD) or even by atomic layer deposition (ALD). Several works show significant HV-THB performance improvements when silicon nitride layers are included in the passivation stack. [1, 3, 55]. In such cases the nitride layer has been deposited by plasma PECVD [3, 55], and even variations to the stoichiometry of the deposited layer can lead to consequent variations in the performances of the devices [55]. Moreover, in the presence of high electric fields, silicon nitride itself can undergo a corrosion process [63, 108] leading to the penetration of humidity, and eventually to the critical failure of the device. It has been shown that the addition of a further semi-insulating layer on the passivation structure of the device, and the optimization of the polyimide material [3, 55, 63], allows to achieve improved HV-THB capabilities without activating other failure modes.

2.2.4.3 Silicon Carbide Devices

SiC technologies are bound to become the standard in the coming years; therefore, this section has been devoted to current advances in the study of their performances when evaluated under HV-THB test. In particular, actual HV-THB testing of SiC power devices is in its early stages, and few studies are currently available, but these results are already meaningful with respect to HV-THB capabilities and other classes of reliability tests of silicon carbide power devices. One line of research related to possible voltage-humidity issues is the investigation of charge accumulation, an important topic in the case of SiC devices. For instance, in the case of 4H SiC power diodes, a breakdown voltage instability due to charge accumulation has been observed [89]. Two different charge accumulation phenomena have been described, both connected to metal contaminants. The first one induced by temperature and bias, and the second one due to humidity [89]. A second study from the same author [93] investigated the effects of several passivation stacks with the aim of reducing charge accumulation in the termination area of 4H-SiC power diodes. In this study, a customized capacity measurement method [109] was used to identify, among the proposed ones, the structures which suppress positive charge accumulation, leading to BV instability in the termination [110]. In addition, another aspect related to the testing of HV-THB SiC devices is the presence of very low leakage current values, as in the case of SiC MOSFETs. As shown in Figure 2.10, monitoring can be challenging since leakage values are extremely low and many devices must be monitored at the same time [30, 59].

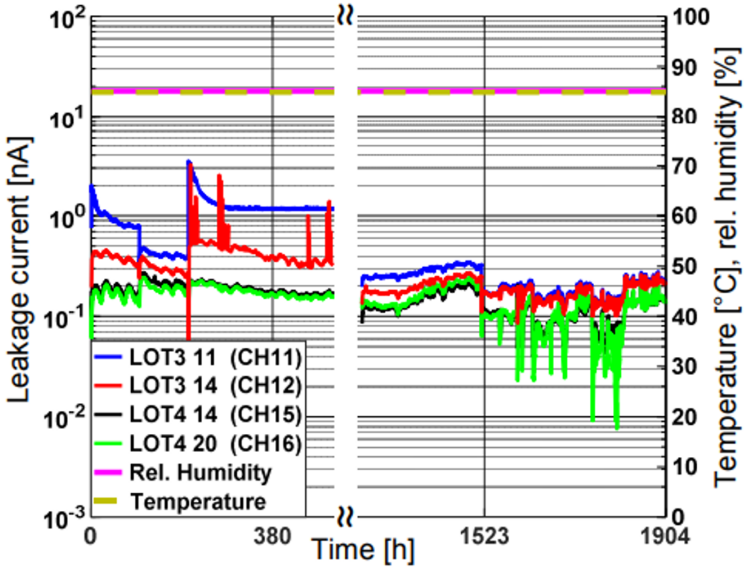


FIGURE 2.10: Leakage current monitoring during THB test on four 1200 V SiC-MOSFETS in plastic package. The right axis shows both temperature and relative humidity, having constant values throughout the whole duration of, respectively, T_amb = 85 °C and R.H. = 85%. Current reading is so low that it is mostly determined by noise and offset correction. Figure reproduced with permission from [30].

Passivation stacks for SiC devices show promising results with the use of AlN and HfO_2 due to their high dielectric constants and higher critical electric fields [88, 96]. The device simulations reported in Figure 2.11 show a comparison of three different passivation materials applied to a SiC device.

In this simulation work, a good reduction of the electric field peak was achieved with an HfO_2 layer applied to the termination region. In this way enhanced shrinking of SiC power devices becomes viable not only for their thermal performances, which are ensured by the physical properties of silicon carbide, but also with respect to THB performances, since local peaks in critical junction termination points can be reduced significantly. In conclusion, several studies reveal that SiC devices show superior robustness [30] and outstanding humidity capabilities with respect to silicon devices [59, 111]. Whenever reported, device failures are supposedly triggered by chip imperfections or by the preparation process, shifting the focus of reliability improvement, in these cases, more to the packaging and manufacturing process than the device itself.

2.2.5 Review Conclusions

Several aspects of the High Voltage Temperature Humidity Bias (HV-THB) test have been investigated. Firstly, current regulations and standards have been described and compared to the HV-THB characteristics, and the main features of the test setup have been outlined, discussing also the main issues related to the testing of the DUTs, followed by the description of the acceleration models of the three main stressors: temperature, humidity and voltage. Secondly, the main failure modes triggered by the interaction of humidity and high voltage have been described, and examples of the physical degradation have been given. Indeed, the literature shows that HV-THB testing is a valuable source of information for the evaluation of reliability performances of power semiconductor

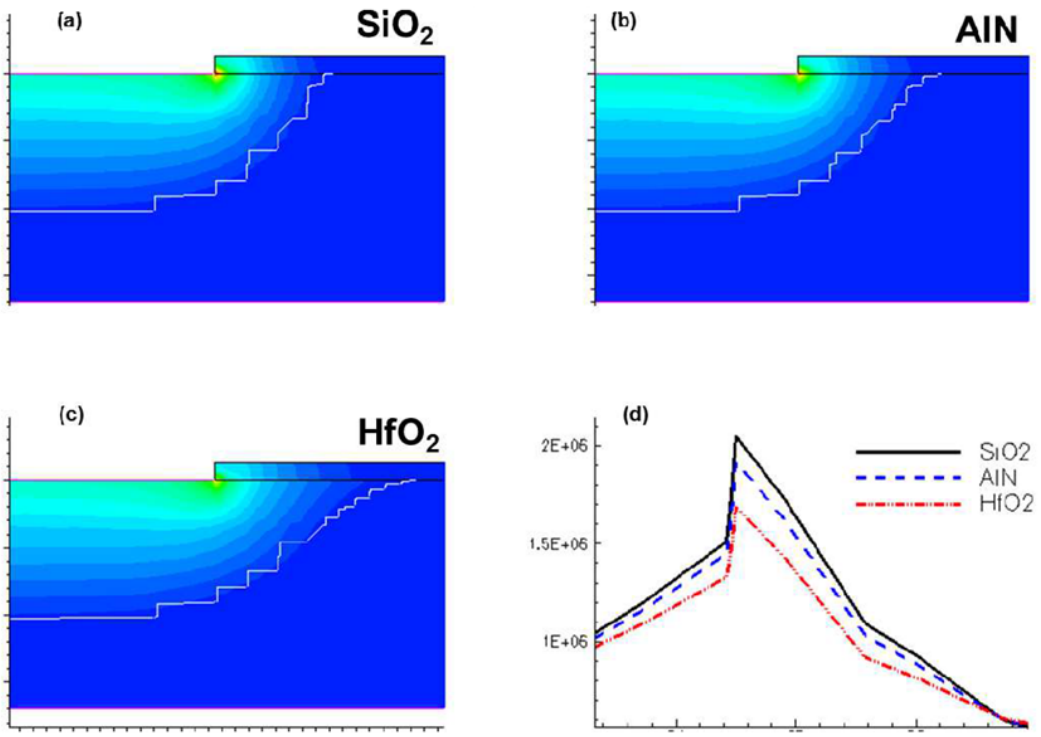


FIGURE 2.11: Cross-section electric field distribution of SiC Schottky diodes, including SiO_2 (a), AlN (b) and HfO_2 (c). On the right side (d), horizontal cut line of the electric field close to the passivation layer. Figure reproduced with permission from [88].

devices when high bias and humidity are applied simultaneously at fixed temperature. Moreover, HV-THB will remain a remarkable reliability test even for new generations of wide band-gap power semiconductor devices. In particular, it has been highlighted how several authors already use this test for the evaluation of multiple class of SiC power MOSFETs, IGBTs and diodes, and how the use of these new materials will enable further studies and application development. Eventually, it is important to notice that this improvement will come only by further optimization of materials and architectures of both passivation and junction termination structures, in order to control local electric fields, moisture absorption, and unlock the maximum potential of these new materials by improving their reliability in harsh environment applications.

2.3 Methodology

The main objectives of this methodology section are to develop a dedicated system setup for the monitoring of the leakage current during HV-THB, validate the testing results, and finally enable further studies on power semiconductor devices passivation improvement, as a part of a wider study in collaboration with Roberta Busca and Giovanni Richieri. These studies eventually resulted in the publication of two papers during this PhD program, and several parts of the next section are reproduced in part from these 2 publications [1, 3]. Moreover, permission for reuse of this material and images have been obtained by the author for both articles [1, 3]. In the first part of this section, a description of the system setup is provided, as well as the logic and features of the dedicated measurement software. In the second part, the results and approach of this methodology are analyzed from an electrical point of view, including leakage monitoring curves and I-V characteristics of the sample Devices Under Test (DUTs). These results are then analyzed by standard failure analysis techniques, including dedicated Scanning Electron Microscopy (SEM) and FIB analyses performed on passivation structures after HV-THB testing, aiming to better understand the failure modes and obtain insights on the improvement of passivation structures and materials.

2.3.1 Design of the measurement system

2.3.1.1 System Architecture

In order to achieve continuous monitoring of the DUTs, these latter need to be biased and exposed to humidity and high-temperature inside a climactic chamber, with a dedicated power supply system and measurement board. This setup is described schematically in Figure 2.12, while a picture of testing equipment is reported in Fig. 2.13

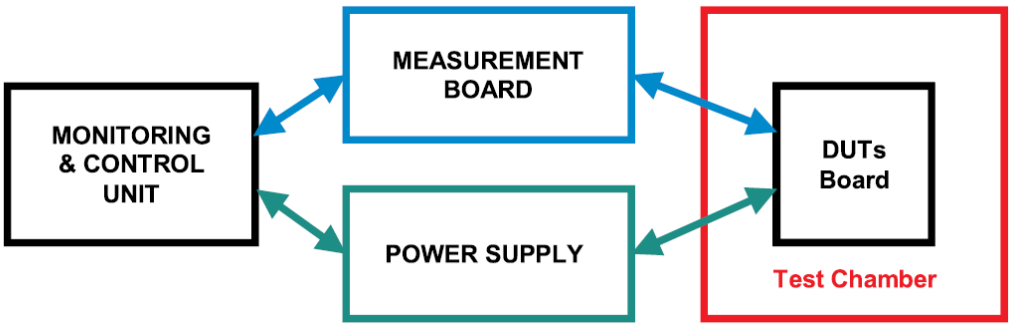


FIGURE 2.12: Schematics of a generic HV-THB test architecture. Figure reproduced with permission from [1].

The core of the system is the control unit, which has been realized with a National Instruments PXIe equipped with a PXIe 4081 Digital Multimeter (DMM) unit, and four high speed PXIe 2527 switch modules. Each switch is capable of reading either 32 dual ended channels or 64 single ended channels in common ground configuration, allowing for a large sample size. The operating system of the control unit supports the LabVIEW™environment, which will be used to control and configure both the leakage current monitoring and the power supply. The control software has been written by the author and will be described in the following sections.

The second part of the system is the Power Supply Unit (PSU), realized with an Elektroautomatik PS9000, having a maximum DC voltage of 750 V, covering the biasing

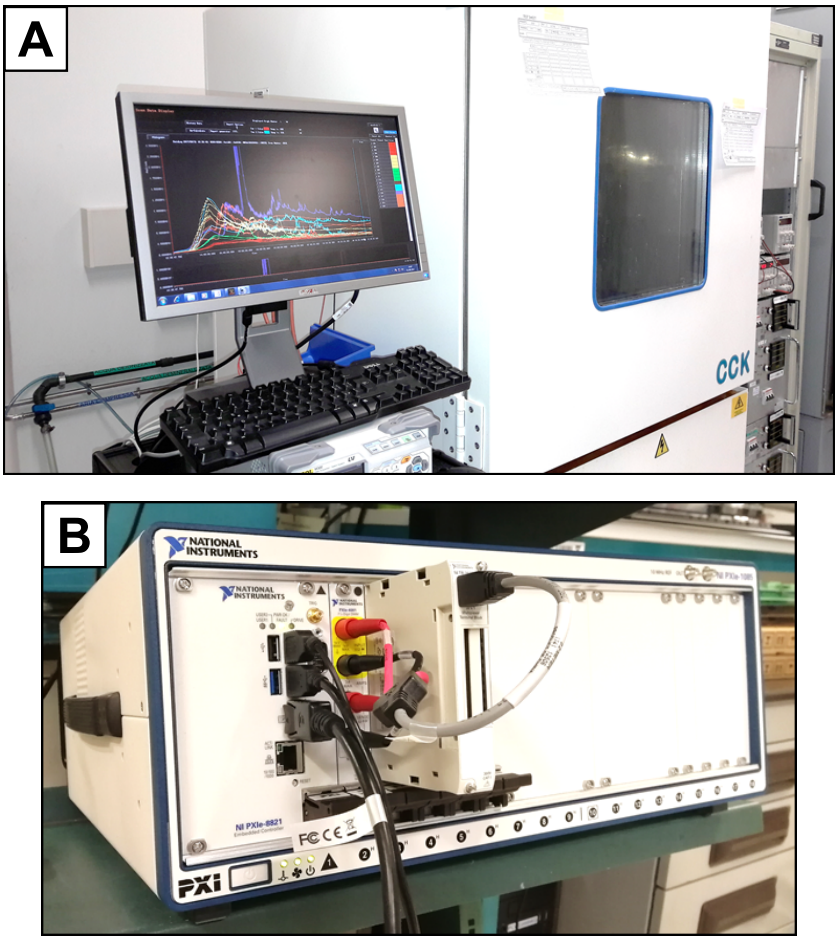


FIGURE 2.13: HV-THB Experimental Setup.

requirement of the samples involved in this research. The PSU can be controlled and configured through standard USB serial connection by the monitoring unit, allowing the setup of current and power maximum limits in order to avoid excessive damage to the DUTs in case of critical failure.

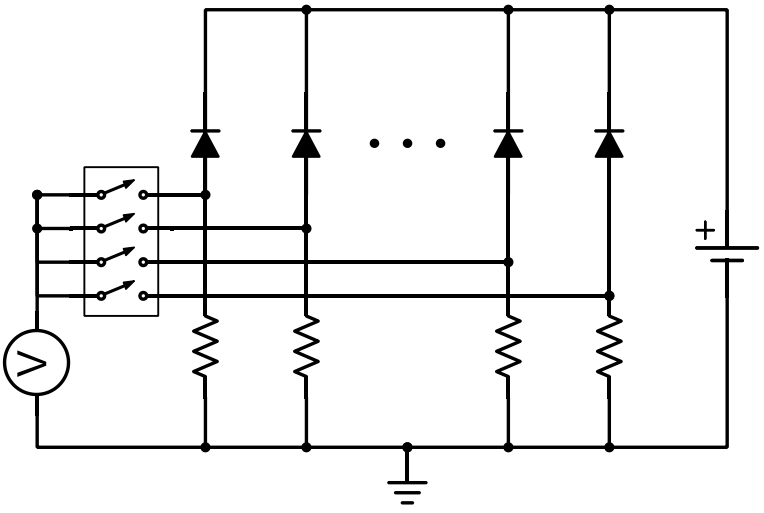


FIGURE 2.14: Schematic of the HV-THB measurement circuit.

The last main part of the system is the measurement board. This latter is positioned outside the environmental chamber and is generally an active board including operational amplifiers current-to-voltage conversion circuits, or simple high value resistors on which the very small leakage currents of a power diode, which can go down to the value of a few nA, can be measured thanks to proper dimensioning of the resistor's value.

Figure 2.14 [1] shows the schematics of the resistor measurement circuit, and the working principle can be described as follows. The PSU is activated by the control unit, and for each channel the DMM performs a voltage measurement on the selected resistor in order to determine the value of the leakage current on each branch of the board. The chosen value of the resistors for this circuit has been set to $100\,k\Omega \pm 1\%$ ceramic type, with the purpose of reading current values down to the order of a few tenths of nA.

Eventually, at each cycle, all data are shown on a dedicated graph on the monitoring interface's screen and saved in a dedicated log file. This configuration allows to continuously scan the leakage current on all selected channels, and to monitor the evolution of the test both online and offline thanks to the data-logging capabilities of the control software, which will be thoroughly described in the next section.

2.3.1.2 Programming of the Control System

Due to the nature of the DUTs and the test, some custom features have been implemented in order to achieve monitoring and control of the HV-THB test. The core loop of the LabVIEW™ program performs a measurement of all the selected channels with the defined speed and resolution, which are both fully adjustable for multiple class of devices. The real time data is then processed and visualized at each measurement, so that changes in the behaviour of the devices can be identified right from the beginning of the test[1] [1].

The user interface of the control software is reported in Fig. 2.15, showing the main user controls and configuration options.

The left column is dedicated to channel selection and allows the user define the channels to be monitored on the 4 DMM units, which can be enabled singularly. After the selection of the channels, the total number of these latter is reported on the top left in a dedicated box. At the center of the interface, two more columns allow the configuration of both the switch and DMM. The switch setup includes options to select the switch configuration (e.g. dual ended 32 channel mux, 64 single ended mux, etc...), the slot position of each switch unit, and the sync trigger configuration allowing the control software to cycle through all channels at each iteration. The DMM configuration section allows to set the measurement range in volts, the resolution of the DMM, the type of measurement (which for the purpose of this study is always set to DC voltage), the trigger and measurement destination which enables the single channel measurement and sync with the switches, the sampling time value, and an acquisition timeout in order to automatically free the system and stop the measurement in case the selected sampling time is too long. On the right side, the other main part is the monitoring graph, showing the evolution of the leakage current, allowing the individual selection of the channels to be visualized, and showing the elapsed time in hours on the top left corner.

In the center top side section of the interface, several option are available to configure the power supply, including the software configuration of the Power Supply Unit (PSU), the voltage bias level, the emergency "STOP" button, the board resistor value and

[1] this paragraph is reproduced as-is from [1]. The policy excludes the copyright of the figures, for which the author obtained dedicated permissions for reuse.

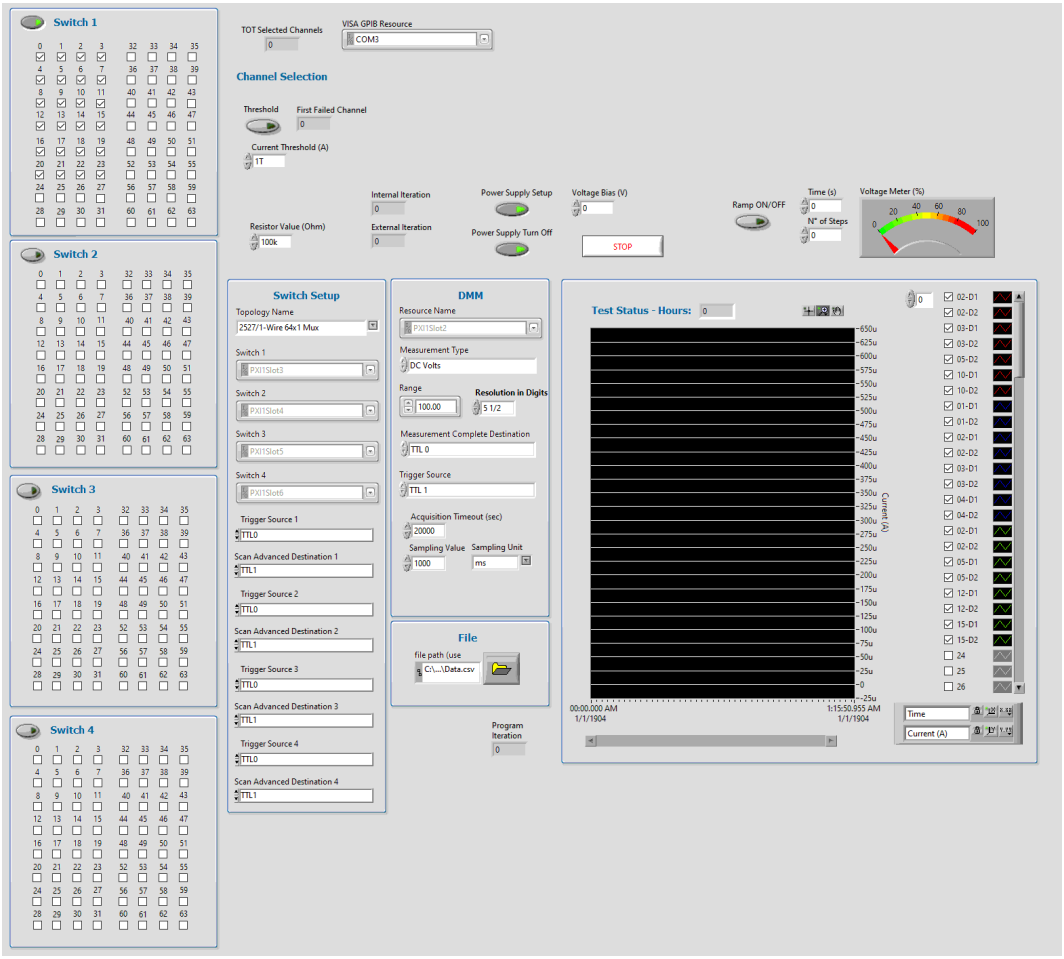


FIGURE 2.15: View of the user interface of the control software developed in LabVIEW™ environment.

the threshold configuration. The voltage ramp setup is located on the top right corner, allowing the selection of the ramp rise time, the number of steps and a dedicated voltage meter. Eventually, the log file configuration is positioned at the bottom center of the page, and allows to set the log file directory and file name, with the data output in ".csv" format including the times and leakage values for each selected channel.

The back panel and control logic is summarized in Fig. 2.16, where the channels, power supply, ramp and log file configuration inputs are sent to the a first level configuration box, where the DMM is configured and synchronized with the switch as they enter the main loop to start the leakage monitoring. The main loop controls the graphing, data-logging, visualization and control on the measured data, updates the main status variable and performs the control on the selected threshold level. When the threshold criteria is fulfilled, the program is halted and the flow exits from the loop moving to the setup exit configuration, deactivating the power supply and closing the data stream of the log file.

The two main control features of the system are the percentage threshold and absolute threshold of the measured current value. Both these options have the possibility to interrupt the test when the actual leakage value of the device overcomes the selected limit, thus saving them from critical damage. These controls act on each individual channel, and as soon as one channel triggers the condition its number is returned to

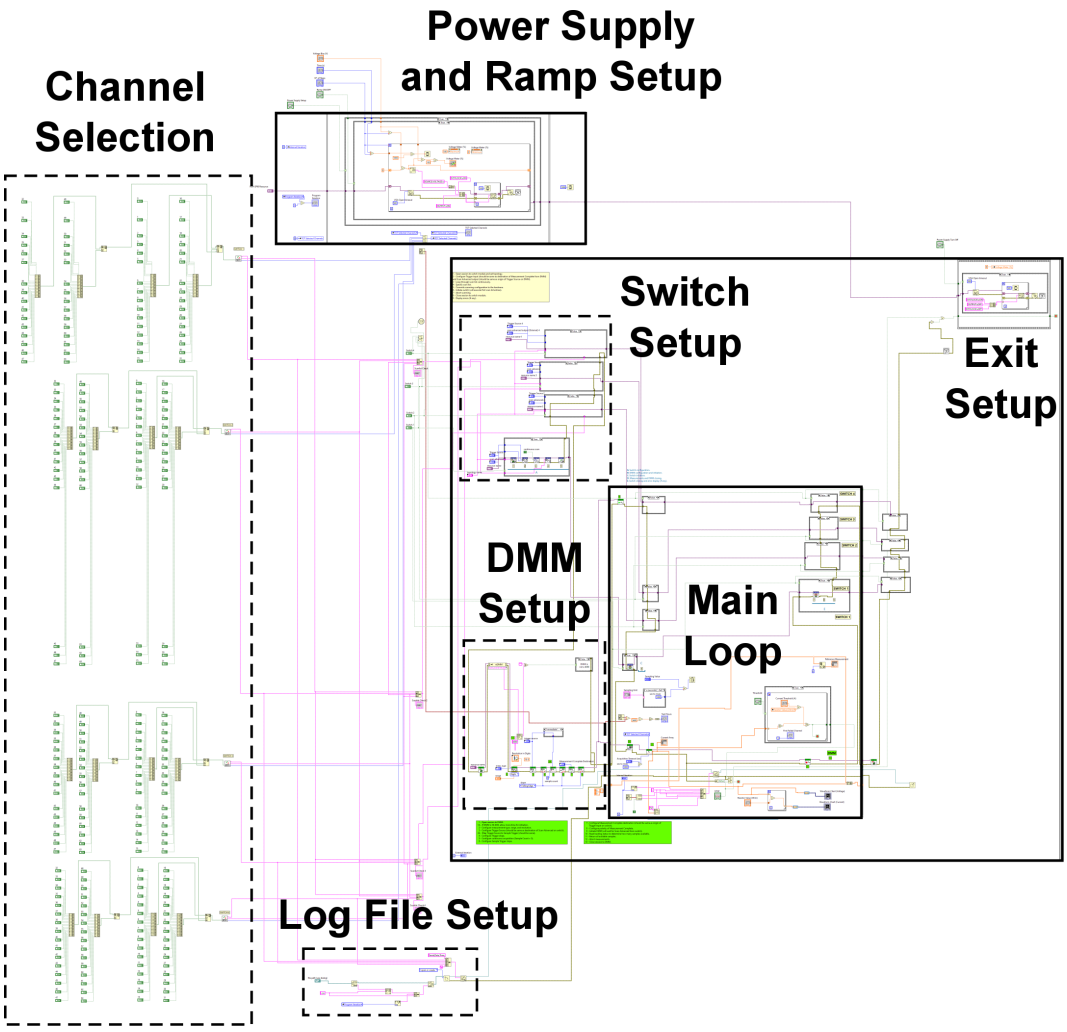


FIGURE 2.16: View of the back panel of the control software developed in LabVIEW™ environment.

the user, the bias is removed and the test is stopped. Apart from monitoring and high voltage, an additional feature has been added to the system, in order to study the effects of how the voltage is initially applied to the DUTs, which is not part of the standard H3TRB methodology. This additional feature is the possibility to ramp the voltage up to the target DC bias of the test. The voltage ramp brings all devices to the desired bias level, and the duration and the step increase of the voltage can be controlled individually. Eventually, in order to avoid condensation, the DUTs are inserted into the chamber at ambient temperature, and then the chamber is ramped up to the nominal conditions of humidity and temperature, only at that point bias is applied [63]. As such, with the use of a ramp, an additional control has been implemented to evaluate the test methodology and its effects on the devices[2][1]. All the features and programming blocks are described in the next section and the programming is performed in LabVIEW™ environment.

[2]this paragraph is reproduced as-is from [1]. The policy excludes the copyright of the figures, for which the author obtained dedicated permissions for reuse.

2.3.1.3 Test conditions and DUTs

Firstly, before the test, all DUTs undergo a curvetracer measurement at room temperature, determining the initial conditions of the reverse IV characteristics. The DUTs are positioned in the climatic chamber, which is then ramped up to 85 °C and 85% R.H. conditions. After waiting for 30 min, the voltage ramp is applied with a duration of 30 min. When the ramp reaches the selected voltage level, the test is officially started, and the regime conditions are shown in 2.3. At selected time steps of 168, 500, 1000 h (or more if needed) all DUTs are removed from the chamber, and after 12 h of rest at room conditions, a curvetracer measurement is performed. This process is repeated at each time step until a device exceeds the selected threshold criteria, or the test is deemed as over. Each DUT has been tested after each test step, with a Keysight B1505A curvetracer, assessing the actual status of the I-V reverse characteristics, and allowing for highly detailed electrical and failure analysis evaluations. All tested DUTs are 650 V power diodes in standard MTP dual die power modules. These samples were prepared with the purpose of evaluating the nature of the failure mode and several termination passivation schemes[3] [1].

Table 2.3: Set of stressors applied during the test. [1]

Parameter	**Value**
Temperature	85 °C
Relative humidity	85%
Voltage	80% V_{nom}

[3]this paragraph is reproduced with some editing from [1]. The policy excludes the copyright of the figures, for which the author obtained dedicated permissions for reuse.

2.3.2 System Evaluation

2.3.2.1 Monitoring of the leakage current

A typical curve of 650 V with 80% voltage rating applied is reported in Fig. 2.17. At the beginning of the test, all devices exhibit a slow initial increasing and decreasing evolution of the leakage current. This phenomenon can be attributed to moisture penetration and interface charge relocation, and in particular to local charge distribution inside the termination of the devices, when interacting with the applied electric field. After the initial phase, typically lasting around 10 hours, all devices stabilize asymptotically toward a stable current level.

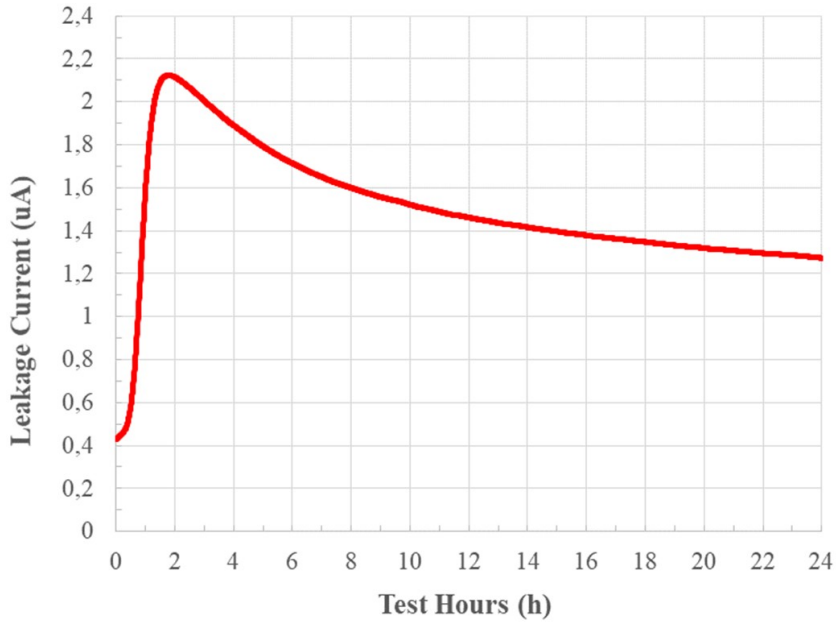


FIGURE 2.17: Leakage current evolution in the first 24 h of the test for a 650 V diode polarized at 80% V_{nom}. Figure reproduced with permission from [1].

At this point, as indicated in Section 2.3.1.2, control can be switched to percentage threshold mode. In this way the reference value is set to the regime level, and control is performed more coherently with the testing methodology and the nature of the DUTs. This kind of phenomenon is mostly present only at the first start of the test, and thanks to our software implementation, the use of an optimized voltage ramp has helped the devices reach the regime level with a smooth evolution. Moreover, an example of monitoring up to 1000h is reported in fig. 2.18, showing the evolution in time of leakage for 8 DUTs under HV-THB, the negative peaks are due to momentary opening of the test chamber for other test run in parallel in the same chamber or electrical supply interruption[4] [1]..

[4]this section is reproduced with some editing from [1]. The policy excludes the copyright of the figures, for which the author obtained dedicated permissions for reuse.

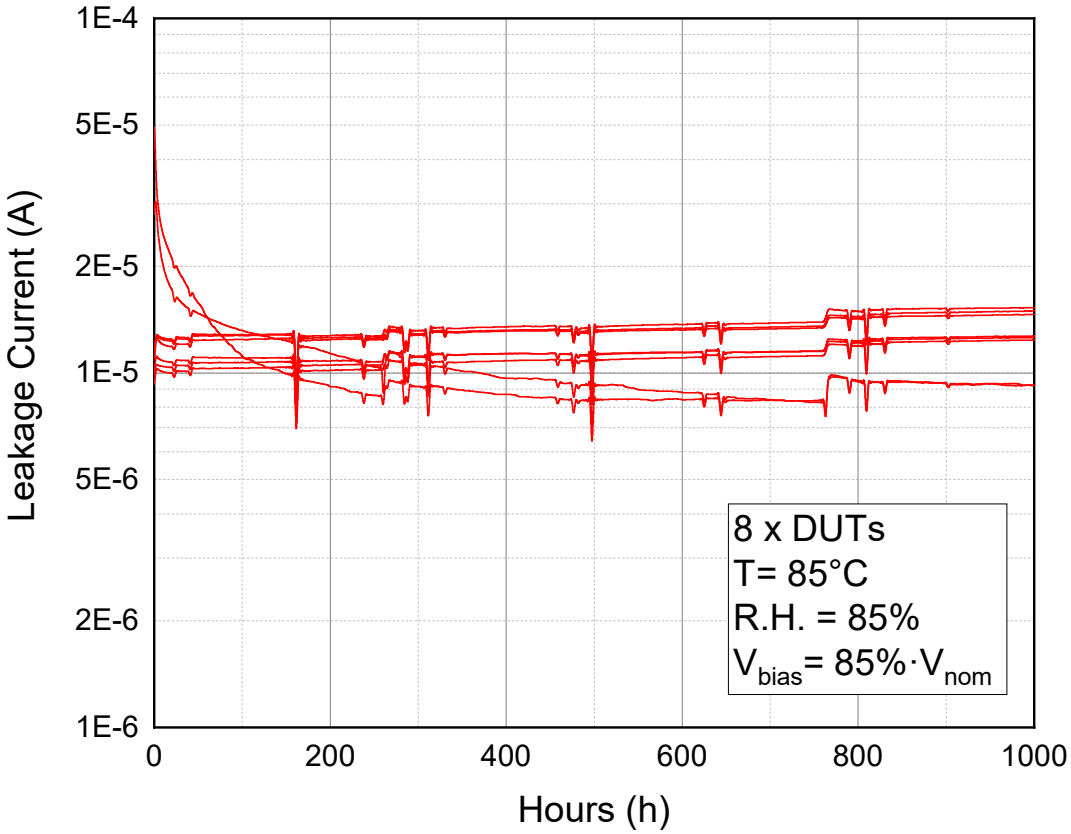


FIGURE 2.18: Leakage current evolution of 650 V diodes polarized at 80% V_{nom}.

2.3.2.2 Curvetracer analysis

As discussed in section 2.3.1.3, in order to identify and understand the kind of degradation that affects the devices, each test is complemented with an I-V analysis of the reverse characteristics of the diodes, before and after each step of the test session. Fig. 2.19 shows an example where the electrical characteristics of the DUTs are mostly unaffected by the stress conditions. During the test, the monitoring presents a stable leakage current level up to 1000 h. This stability is then confirmed by the curvetracer analysis, the shape of the characteristic remains the same even after 1000 h of testing[5] [1]..

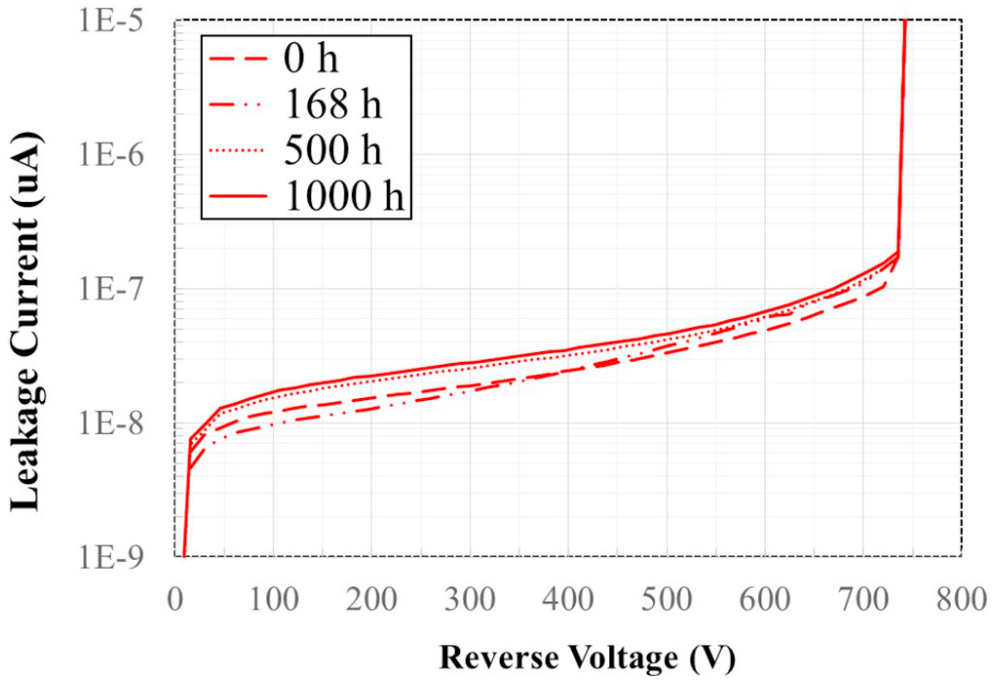


FIGURE 2.19: reverse characteristic of a 650 V diode, tested at 0 h, 168 h, 500 h and 1000 h, exhibiting no electrical degradation

2.3.2.3 Device Failure Analysis

As already highlighted, thanks to the threshold control, device degradation is intercepted in time, allowing for a more accurate failure analysis of the DUTs. After the initial testing, the analysis flow continues with an optical inspection of the selected DUTs, followed by a FIB/SEM analysis.

One example of optical inspection is reported in 2.20, performed on a DUT failed at 168 h. In such case, the leakage monitoring shows electrical degradation, but only thanks to the inspection we can link this phenomenon to the consistent morphological variation of the surface. The curvetracer analysis also confirms a significant variation of the BV limit of the reverse I-V characteristic. This variation can be identified as the cause of leakage drift observed during the monitoring phase, confirming what has been evidenced in previous studies [28]. The actual nature and entity of degradation induced by the test is then analysed through FIB and SEM in order to complete the methodology flow.

[5]this paragraph is reproduced with some editing from [1]. The policy excludes the copyright of the figures, for which the author obtained dedicated permissions for reuse.

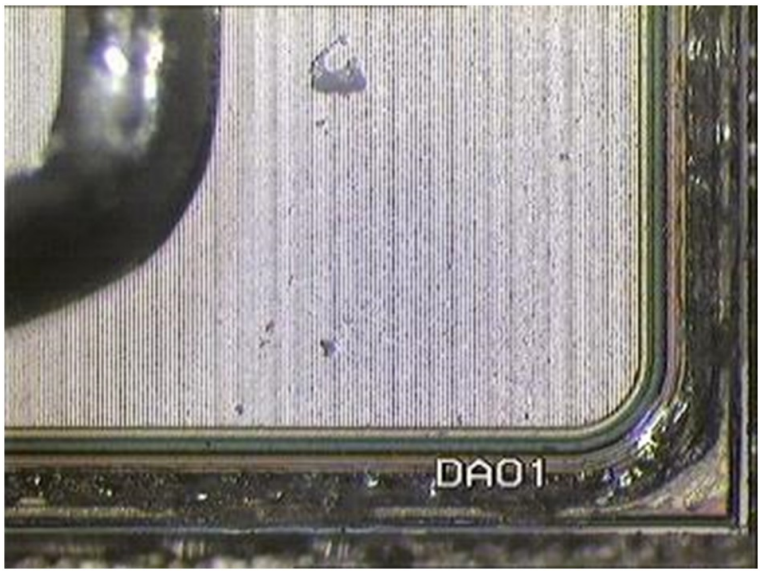


FIGURE 2.20: Device Optical Inspection after HV-THB test.

A set of 3 different groups of 650 V sample power diodes, with blocking voltage of 650 V and an floating ring termination structure was used to validate the HV-THB system. The structures are listed in Fig. 2.21. Group A presents a simple passivation structure composed of oxide, a silicon resistive layer as primary passivation, and an additional polyimide layer as secondary passivation. Group B and C have been reinforced with dedicated capping layers deposed by Plasma-Enhanced Chemical Vapor Deposition (PECVD) to complete the passivation structure. For this purpose, these diode having the same secondary passivation structure, were produced by adding either a silicon dioxide (sample B) or a silicon nitride (sample C) interlayer with the same thickness.

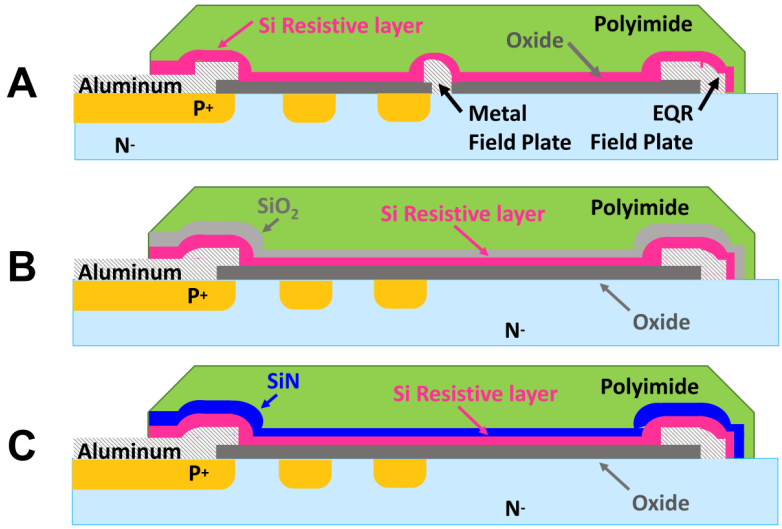


FIGURE 2.21: Passivation details: Polyimide only base sample (A), SiO2 capping layer sample (B) and Si_3N_4 capping layer sample (C) on a typical planar FR termination design.

After fabrication and assembly in MTP power modules, the devices were stressed by performing HV-THB tests at 85 °C, 85% RH, with 520 V applied bias (Vr at 80% of rated voltage capability). Before and after each step of the HV-THB test, the DUTs were subjected to I–V analysis of the diode reverse characteristics and a summary of leakage degradation by sample group is reported in 2.22.

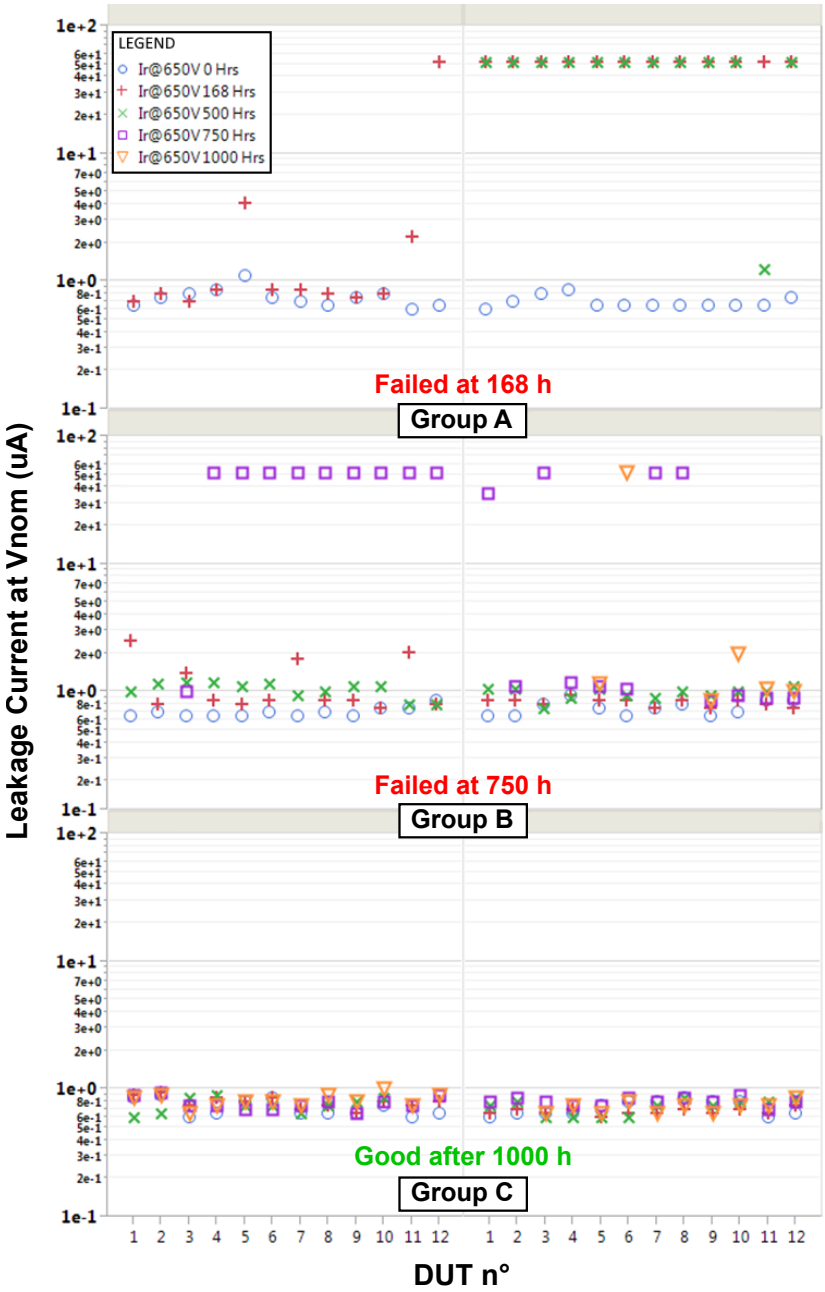


FIGURE 2.22: Leakage Current Degradation Summary after HV-THB test: Polyimide only base sample (A), SiO_2 capping layer sample (B) and Si_3N_4 capping layer sample (C) on a typical planar FR termination design. The samples show signs of failures respectively at 168 (A), 750 (B), while no failures are detected for sample C even after 1000 h of HV-THB test.

For sample A, after silicone gel removal, optical microscope inspection revealed polymer degradation with bubble formation in all three passivation materials. An SEM image from an FIB cross section performed on a bubble in the failed termination area, highlights that the organic materials have not degraded but have instead been lifted, possibly as a result of the corrosion of the underlying layer of resistive silicon and of the aluminum field plate [63]. Indeed, the aluminum field plate appears swollen, with a change in conformity close to the edges (Fig. 2.23). Moreover, from SEM imaging, the polyimide seems to maintain its adhesion with a very thin portion of the underlying film, but any deterioration in the latter could have induced a detachment, probably stimulated by the gas formation that caused the swelling.

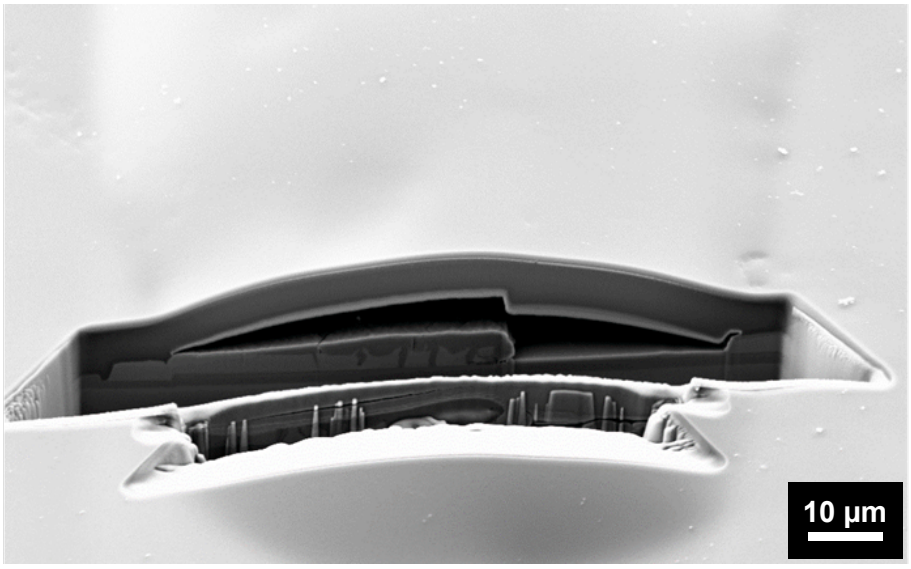


FIGURE 2.23: SEM image of an FIB cut of a bubble in the failed termination area of sample A device. The polyimide is lifted and the aluminum layer is severely degraded.

Further Energy-Dispersive X-ray spectroscopy (EDX) analysis is then performed to evaluate the change in composition along the aluminum field plate. Comparing data acquired from untouched aluminum portions and on degraded ones, it is possible to observe the appearance of different peaks. The presence of silicon can be explained by migration from the upper silicon resistive layer with the formation of aluminum silicide. Instead, the oxygen peak demonstrates the formation of aluminum oxide species (Fig. 2.24).

These species derive from a combination of humidity penetration, electrochemical phenomena, and the high chemical reactivity of aluminum with water. More specifically, when water is adsorbed and an external bias is applied, a pH gradient forms due to the separation of H^+ and OH^- ions. In this environment, different types of reactions can occur. As evidenced in section 2.2.3.1 the general behavior for metal atoms in these conditions is the following:

$$M \rightarrow M^{n+} + ne^- \ (anode) \tag{2.14}$$

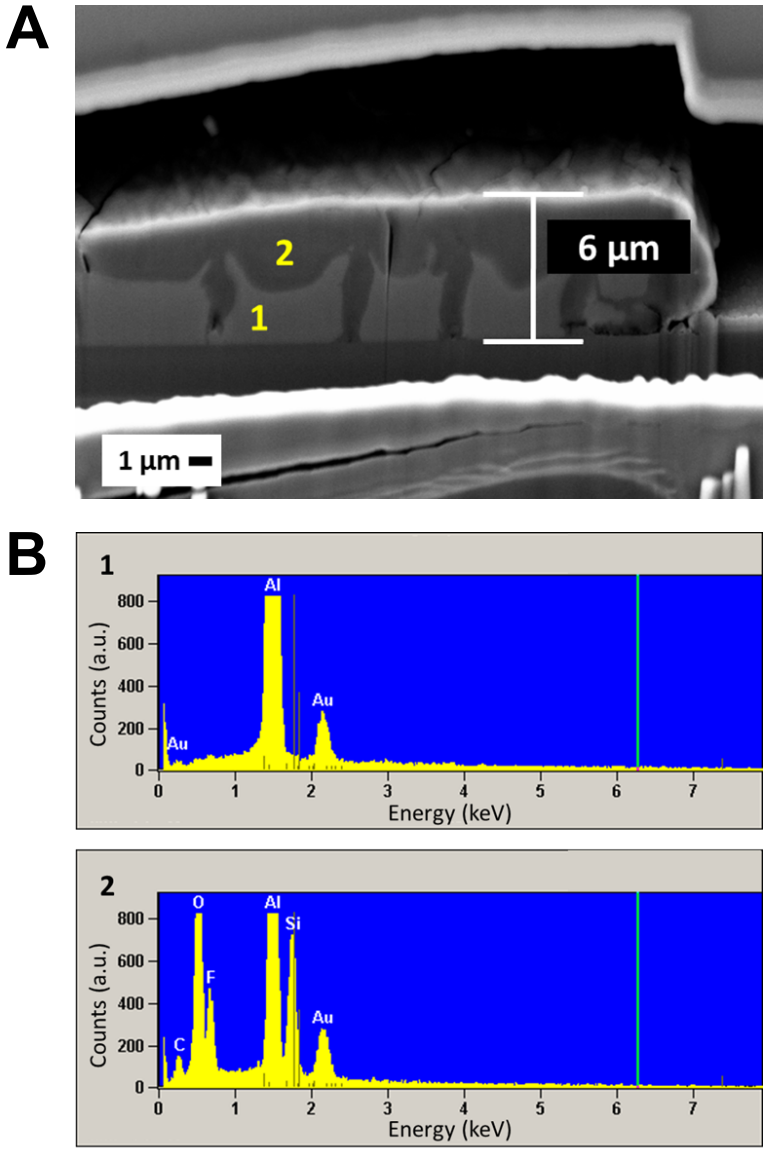


FIGURE 2.24: (A) SEM image of an FIB cut across the aluminum field plate, for a Group A sample DUT failed after 168 h. (B) EDX analysis on two different points of the aluminum field plate: (1) untouched portion (2) degraded portion. EDX spectra comparison reveals AlO_x and aluminum silicide formation (migration from resistive layer). Peaks of fluorine and carbon can be attributed to previous plasma etching (with SF6) or cleaning (diluted HF) processes and to the presence of organic materials such as polyimide.

$$M^{n+} + ne^- \rightarrow M\ (cathode) \tag{2.15}$$

Reaction 2.15 is usually accompanied by dendrite formation along the surface of the material involved in the metal transportation. Aluminum, which is typically used as a contact metal in this type of device, is known to be particularly reactive in the conditions previously explained. In fact, aluminum easily forms hydroxides when in contact with

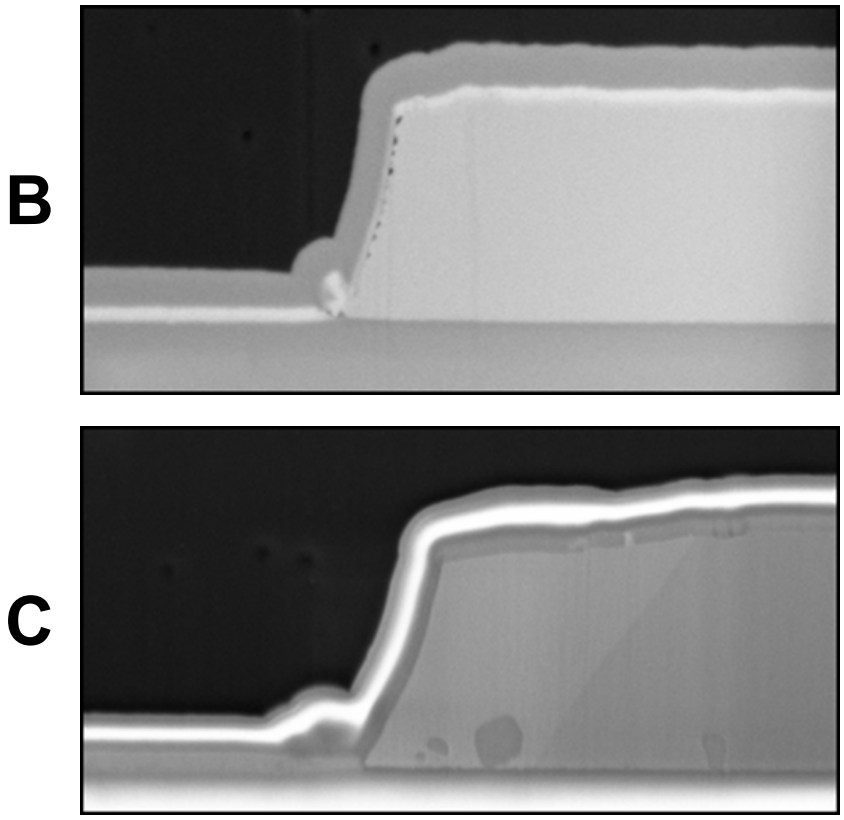


FIGURE 2.25: (B) SEM image of an FIB cut of SiO_2 DUT that failed after 750 h. Small voids on the Si resistive layer and on the oxide capping interface are evident. (C) SEM image of an FIB cut of silicon nitride DUT showing good electrical characteristics after 1500 h of HV-THB testing. No signs of degradation are present between passivation layers.

water. These compounds are quite stable in neutral solutions, but in the presence of acids or bases, they dissolve rapidly, resulting in layer corrosion.
The proposed reactions occur as follows (overall reaction of aluminum with water):

$$Al \ + \ 3H_2O \ \rightarrow \ Al(OH)_3 \ + \ 3/2 \ H_2 \tag{2.16}$$

In neutral environments, $Al(OH)_3$ (amorphous) is transformed to the stable hydrated oxide:

$$Al(OH)_3 \ \rightarrow \ Al_2O_3 \ \cdot \ H_2O \tag{2.17}$$

which has a free energy of formation of -436.3 kcal and acts as a passivated barrier. Alkaline solutions are able to destabilize this protective oxide that forms AlO_2^- [112] and can cause rapid dissolution of aluminum at room temperature, which continues to react and consume water following Eq. 2.16. In high-humidity conditions, this equilibrium is completely right-shifted, causing H_2 formation, which could explain the spongy appearance of the aluminum layer and polyimide bubble formation.

Furthermore, thanks to FIB analysis for sample B and C it is possible to extract

some additional results. In fact, as seen in Fig. 2.22, the devices with a silicon nitride capping layer do not exhibit any shift or significant electrical characteristic variation, presenting a stable leakage current level beyond 1000 h. In contrast, the devices with a SiO_2 capping layer display a leakage shift above the imposed threshold after 750 h, and so the test is stopped before further device degradation. After device decapsulation, failure analysis proceeded with an optical inspection of the selected DUTs. SiO_2 samples, which failed after 750 h, seemed to evidence no physical damage in the device structure. As expected, the same result was obtained for the silicon nitride samples, which were still presenting good electrical characteristics at 1500h, when the test was considered finished with no degradation or failure of the latter devices.

However, an in-depth observation performed with SEM on an FIB cut of the DUTs that failed after 750 h, highlighted small voids in the Si resistive layer and on the capping oxide (Fig. 2.25B). After further inspections, we can link the leakage degradation to the morphological variation of the interface between the oxide capping layer and the silicon resistive layer. (Fig. 2.25C) shows the SEM image of an FIB cut of a silicon nitride sample which still showed good electrical characteristics after 1500 h of the HV-THB test, confirming the absence of physical degradation[6] [1].

[6]several parts of section 2.3.2.3 are reproduced with some editing from [1]. The policy excludes the copyright of the figures, for which the author obtained dedicated permissions for reuse.

2.4 Summary

The High Voltage Temperature Humidity Bias (HV-THB) highlights particular failure modes due to the interaction of high voltage with humidity by using temperature as an acceleration factor. This kind of test is of great importance in the reliability assessment of power semiconductor devices.

Firstly, this chapter gives an overview of the existing test methodologies and approaches to HV-THB, as well as current developments in the field as an introduction to the methodology section, coming from a published review paper by the author in [2].

Secondly, in the methodology section, a dedicated system setup is successfully developed and described. The control software has been customized in order perform a non-invasive analysis, by continuously monitoring the electrical evolution of the leakage current in the Devices Under Test (DUTs), and allowing automatic test stop in case of progressive degradation of the devices. Moreover, the functionalities of this system and its dedicated methodology, are then exploited to show results related to the testing of power diode modules, showing the capabilities of the test to enable significant reliability evaluation in the study of semiconductor passivation materials. This achievement is then also confirmed by failure analysis of the devices including Scanning Electron Microscopy (SEM) and Focused Ion Beam (FIB) characterization of the internal structures, and giving remarkable insights and enabling further studies on the reliability of power semiconductor device passivations. The results coming from the studies in this chapter have been published resulting in 2 papers from the author [1, 3].

Part III

On-Wafer High Current Forward Voltage Drop (V_F) Test of Power Semiconductor Diodes

Chapter 3

On-Wafer High Current V_F Test of Power Semiconductor Diodes

3.1 Introduction

3.1.1 Research Framework and objectives

The wafer sell market of power semiconductor devices represents an important business for device manufacturers all over the world, and accurate product information is important for the final customer in order to select the best devices for their application.

In the case of power diodes, wafer sell datasheet require several key parameters including the Forward Voltage Drop (VF) measured at the datasheet "nominal current" value. This kind of measurement at the wafer level, requires proper setup and methodology in order to avoid chip damage or degradation, and as a consequence can be increasingly challenging depending on the maximum current rating of the chip.

The main objective of this chapter is to design, implement and evaluate a wafer-level high current VF measurement setup on a pre-existing production apparatus, in order to extend the initial low current testing level up to $100\,A$.

As a side note, the content of this chapter involves a purely experimental work, thus it does not include a literature review section.

3.1.2 Forward Voltage Testing of Power Diodes

The Forward Voltage Drop (VF) test is a standard test performed both during the front end manufacturing phase and assembly of power semiconductor diodes. This test is performed by imposing an external current pulse to the Device Under Test (DUT), in order to measure the voltage drop between the anode and cathode of the device in forward bias conditions.

One of the key datasheet parameter for power diodes, useful for circuit designers to select the correct device for their application, is the "Nominal Current" or "Current Rating". This value, usually represented as $I_{F(AV)}$, represents the maximum average current that a diode can handle in forward bias operation, which basically describes a thermal limitation for the junction and is thus directly related to the maximum Junction Temperature (Tj) and the maximum power dissipation of the device.

The VF datasheet value is another key datasheet parameter, and is generally reported at the current rating of the diode. In the case of assembled device in standard packages (e.g. TO220, TO247, MTP modules and other packages), the wires allow easy access to the anode and cathode terminals, allowing safe contacting for the test. Oppositely, testing at the wafer level is generally performed at lower currents, and the VF value can only be correlated to the assembly value in order to determine production and assembly limits. This approach can be a problem in the case of wafer-sell products,

since the actual statistical limits of the product do not represent significant information for the final customer.

For these reasons it is crucial to obtain accurate high current VF measurement in order to provide this key wafer-level parameter to the final customer, without introducing damage to the chips, which can be then safely shipped to the final customer allowing high quality standards.

Taking into consideration the case of a common p-i-n junction power diode, we can describe the current characteristics determining the forward I-V characteristic of the device, as reported in Fig. 3.1.

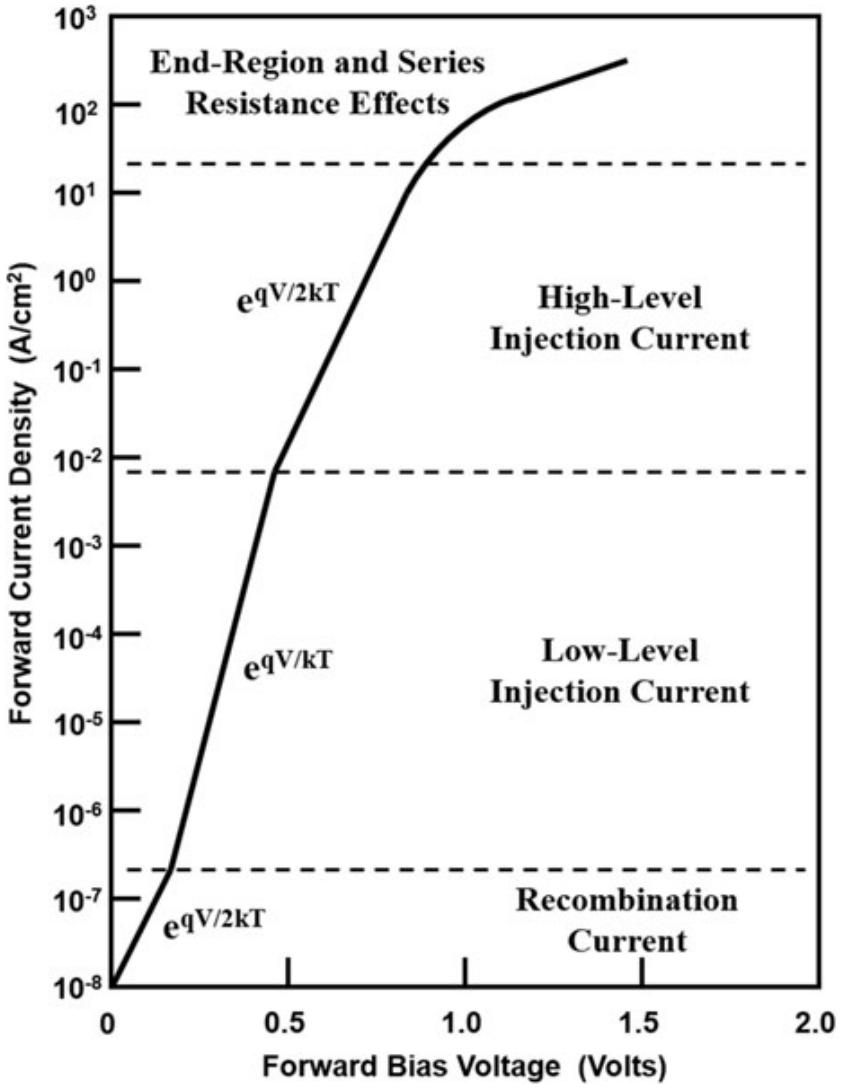


FIGURE 3.1: Typical Forward Characteristic of a p-i-n diode, divided by working operation regions./, © Springer, 2018. Reproduced with permission from [113].

In the lower region, the conduction current is determined by generation and recombination in the space-charge region, and the proportionality rate is $\frac{qV}{2kT}$, where q is the unit charge, V the forward bias voltage, k the Boltzmann constant and T the temperature of the device. In the Low-level injection region, with bias level of $0.1 \div 0.5\,V$, the conduction is dominated by the diffusion of minority charge into the n^- region, also called drift region. In these conditions, the carrier injected carrier density is still below

the background levels and the proportionality with respect to the bias voltage is $\frac{qV}{kT}$, increasing faster than the recombination current region. When the injection charge level rises above the background doping limit, the diode is in High-Level Injection conditions. The current density in this operation region is proportional to $\frac{qV}{2kT}$ and the voltage drop across the drift region can be considered constant thanks to the conductivity modulation effect. At higher current levels, the forward voltage drop increases faster due to recombination in the end regions of the device, resulting in a carrier density decrease in the n^- region, and series resistance effect become dominants [113].

The area of interest of this study falls between the two upper end operation region of series resistance and high injection level, since the final measurement of the VF also includes series effects "outside" the chip, given by the contact resistance of the measurement terminals (for reference see Figure 3.3).

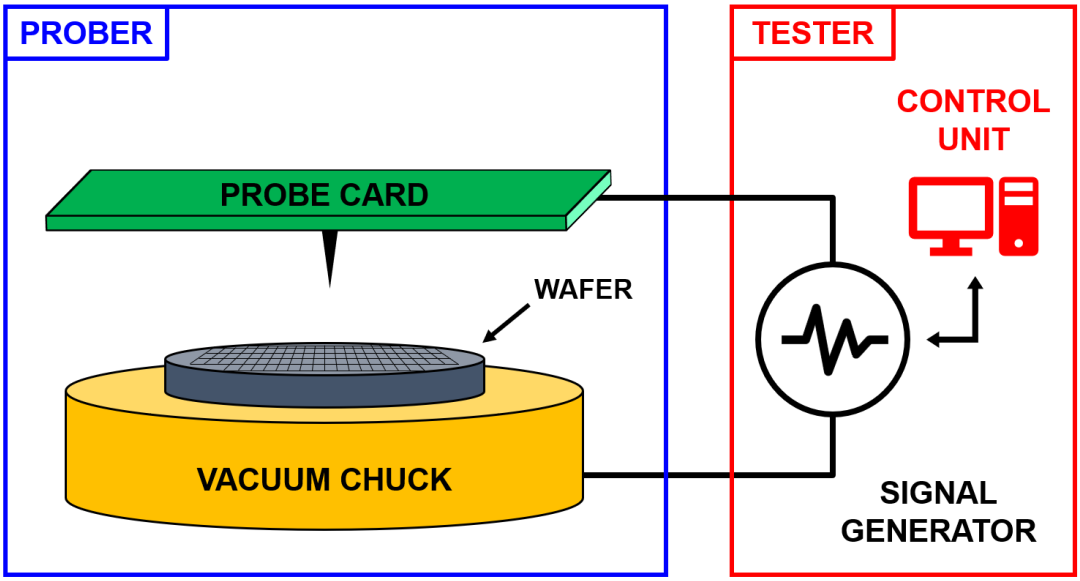


FIGURE 3.2: Diagram of the VF measurement system, showing the Prober and Tester assembly. The Prober system allows the movimentation and contacting of each chip, while the Tester generates both the measurement signal and control signal for the probe.

The schematic of the measurement setup is represented in Fig. 3.2, and can be divided in Prober and Tester. The tester machine is the main control unit and coordinate both the testing process and the test signal generation, for the testing several diode electrical parameters such as leakage current, Breakdown Voltage (BV) and VF low current VF. The Prober allows the movimentation and alignment of wafers from a dedicated cassette to the surface of the vacuum chuck, which has both the functions of keeping the wafer in place and contacting the back side of the wafer, representing the "common cathode" of all the diode chip on the wafer's front. The anode contact is performed for each chip through a "probe card", whose main function is the routing of the generated signal from the tester unit to the contact needles, which are positioned on the back of the probe card. The probing system allows the contacting of each die through an user defined wafer map, and the inking of "failed" devices, which resulted non-compliant with respect to the defined test limits.

Figure 3.3 shows a schematic electrical representation of the testing setup. The measurement is performed between terminal A and B, where Rp1 and Rp2 represent respectively the equivalent resistance of the probe tip and the resistance of the back

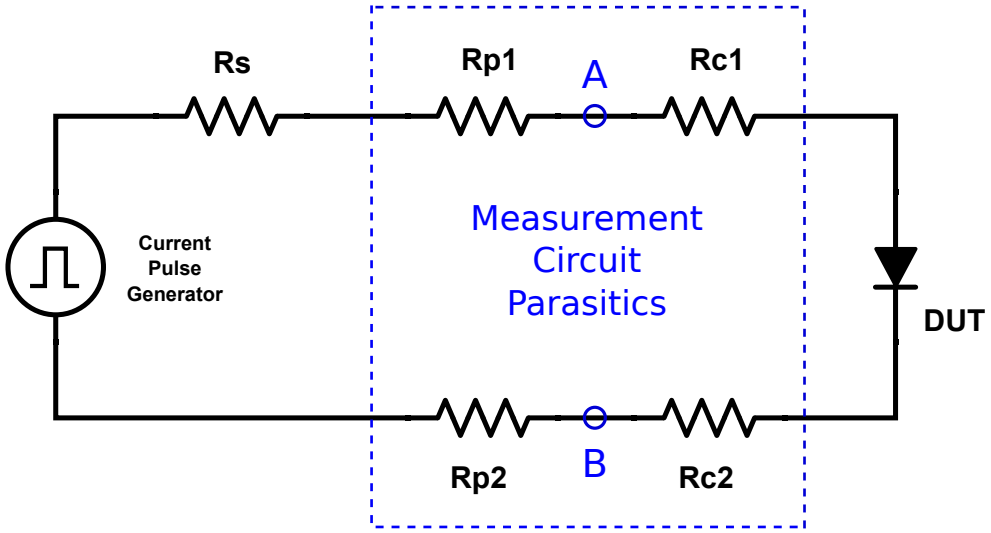


FIGURE 3.3: VF Measurement Electrical Schematic. The measurement is performed between terminal A and B, where Rp1 and Rp2 represent respectively the resistance of the probe tip and back contact, Rc1 and Rc2 define respectively the contact resistances between the tip and the DUT at the anode and the contact resistance between the DUT and the back vacuum chuck at the cathode. Rs is the source internal resistance of the current pulse generator.

terminal (vacuum chuck), which can be considered as negligible given the high conductivity of the constructing materials (Be-Cu alloys for the probe tips and Au plating for the vacuum chuck). Moreover, Rc1 and Rc2 define respectively the contact resistance between the tip and the DUT at the anode side and the contact resistance between the back of the DUT and the vacuum chuck at the cathode.

The structure of the probe card needles and routing allow to have separated "power" and "sensing" needles, in order to perform a current force/voltage sense measurement between the points A and B shown in Fig.3.3.

3.2 Preliminary Evaluations

3.2.1 Benchmark Analysis of High-current VF Measurements

In the first part of this work, the internal capabilities at the research site have been evaluated in order to define the starting point of this analysis. The maximum current level tested at the in-site front-end manufacturing resulted being $5\,A$, while other company sites reported values up to $25\,A$, with currents per needle as high as $5\,A/needle$ considered as a safe limit with the chosen needle shape.

Table 3.1: High Current VF: Device Manufacturers Benchmark.

Device Manufacturer	Source Type	Current Rating (A)	Voltage Rating (V)	Needle Traces	Estimated Current per Needle (A)
A	Assembled	18	1200	16	1,13
	Assembled	30	1200	17	1,76
	Die	75	1200	22	3,41
	Die	75	1200	22	3,41
B	Assembled	60	1200	3	-
C	Assembled	60	1200	5	-
D	Assembled	75	1200	48	1,56
	Die	200	650	105	1,90
E	Assembled	75	1200	7	10,71
F	Assembled	20	1200	16	1,25
G	Die	200	650	16	12,5
	Die	8	1200	4	0,50
Internal	Die	5	200-1200	-	1,25

Moreover, in order to achieve setup capabilities in-line with the main manufacturers, a product benchmark analysis has been performed in order to select the desired maximum current capabilities to be implemented in the final system. This analysis went through more than 200 commercially available products from major power diode manufacturers, showing that the highest current level for testing VF on-wafer, were as high as $300\,A$ as declared in their datasheets.

The second part of this benchmark addressed the actual testing trace on reverse engineered devices from several manufacturers, in order to estimate some key information related to the shape and number of probe marks on a variety of commercially available power diodes. The results of this analysis is reported in Table 3.1, where it is possible to notice how different manufacturers have different testing approaches, especially in terms of number of probe needles, and thus in the maximum current level per needle at fixed current rating.

Another interesting difference is the positioning of the needles, which varies from one manufacturer to the other, depending on their testing methodology. Figure 3.4 shows two examples of opposite approaches for probe mark positioning. Fig. 3.4a shows the typical centered testing pattern, where all needles touch the chip covering a wide area on the device, from manufacturer A. On the right an example of perimeter contacting, following the inner edge of the whole chip's active area, from manufacture D. Both

these approaches are valid, and choosing one with respect to the other depends on the requirements of the assembly process.

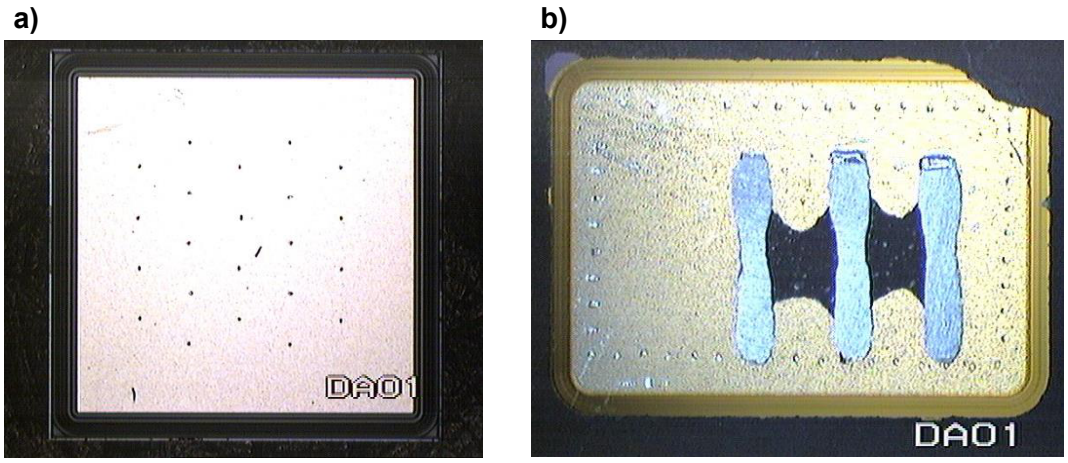


FIGURE 3.4: Example of Probe Marks from two different Manufacturer. From Table 3.1, Manufacturer A on the left (a) and manufacturer D on the right (b)

3.2.2 Baseline Setup for VF testing and Limitations

The testing setup involving the tester system described in section 3.2.1, presents a pulsed test with well defined characteristics, which will be described in order to have the full starting picture on which the high current system will be defined in the following sections.

The VF measurement is a square-pulse current test, with the following main characteristics set on the tester's control unit, and defined in the test program file:

- **Peak Current**: $5\,A$ (standard, native capability up to $200\,A$)
- **Pulse width**: $380\,\mu s$
- **Upper and Lower Voltage Limits**: representing the defined test limits, inside of which the device is considered "good".

It is important to notice that the native capability of the tester allows currents peaks as high as $200\,A$, a good reason to implement changes only in the prober section of the system (Fig. 3.2).

Eventually, a cost evaluation for the purchase of a dedicated new tool from a test machine manufacturer, revealed a required investment of $1\,M\$$, which is well beyond the stated limit for this project, thus the decision to follow a challenging lower investment solution.

3.3 Methodology: Phase 1

In this first phase of the methodology, an overview of the main design and evaluation steps for the new setup are proposed, as well as a wide set of preliminary electrical and mechanical testing, in order to understand the performance and capabilities of the new system with respect to the stated requirements. The testing vehicles for this section are $600\,V$ power diode sample wafers with several current ratings up to $250\,A$.

3.3.1 High Current Probe Card Designs

In this section, two probe card design are proposed following the requirements listed in the previous sections. The two design can be differentiated based on their needle shape and structure, which are **Vertical** and **Cantilever** probe cards, and will be referenced in this way throughout the whole chapter.

Before going into the detail of each probe card, it is useful to describe the probe card circuit schematic, which is the same for both the two high-current probe cards designs. This latter is reported in Figure 3.5 showing the current "equalization" circuit and probe needles contacting on the DUT chip's surface for a number n of branches. Each branch include its corresponding fuse F_i and $1\,\Omega$ equalization resistor R_i, and all branches are driven by the current generator.

The contact resistance, which includes the tip resistance and can be variable during the whole lifetime of the needles due to the mechanical wear-out of the probe material, requires a current equalization circuit in order to ensure that the current flows equally in each branch of the circuit and eventually through the probe needle. The contact resistance can be estimated in a magnitude range between $\sim 10 \div 100\,m\Omega$, thus the choice of a $1\,\Omega$ resistor, being one order of magnitude higher than the worst case value.

Table 3.2: Probe card summary table, showing the characteristics of the Cantilever and Vertical design.

	Cantilever Probe Card	**Vertical Probe Card**
Power Needles	40	33
Sense Needles	2	2
Tip Profile	Flat	Round
Needle Diameter (mils)	15	5
Needle Material	Be-Cu Alloy	
Maximum Current (A)	100	

Table 3.2 includes a summary of the two proposed designs, in terms of number of power needles, sense needles, maximum current and dimensions, while Fig. 3.6 shows the main structural differences between the two designs. The Cantilever structure is a rigid beam design with flat tip touching on the surface of the chip, while the vertical design includes a spring suspension system with the purpose of reducing the mechanical wear-out of the needle's tip, improving the total lifetime of the needles and reducing both contact pressure and scratch damage on the DUT.

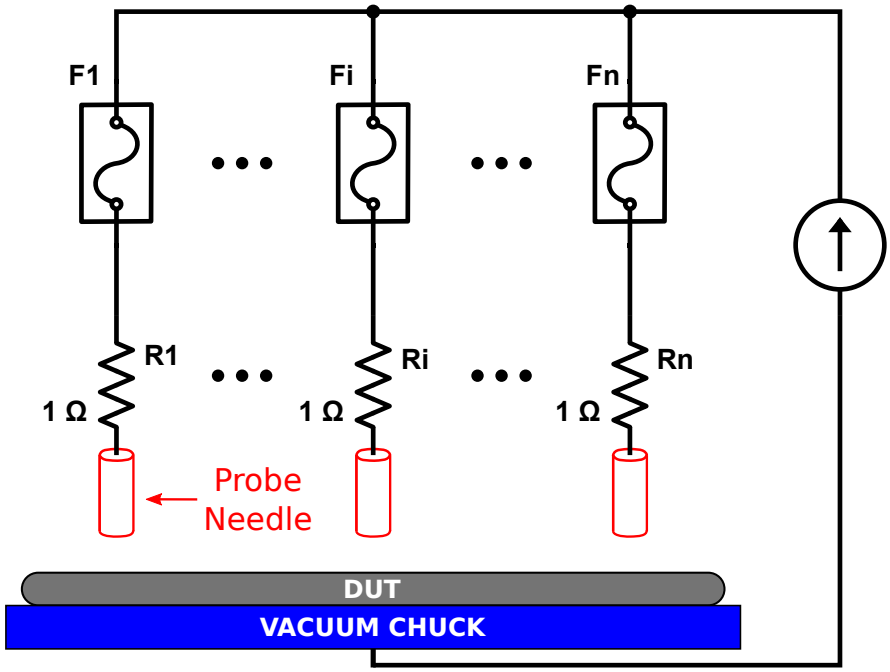


FIGURE 3.5: Probe Card Circuit Schematic, showing the current equalization circuit and probe needles contacting on the DUT chip's surface for a number n of branches. Each branch include its corresponding fuse F_i and $1\,\Omega$ equalization resistor R_i, and all branches are driven by the current generator.

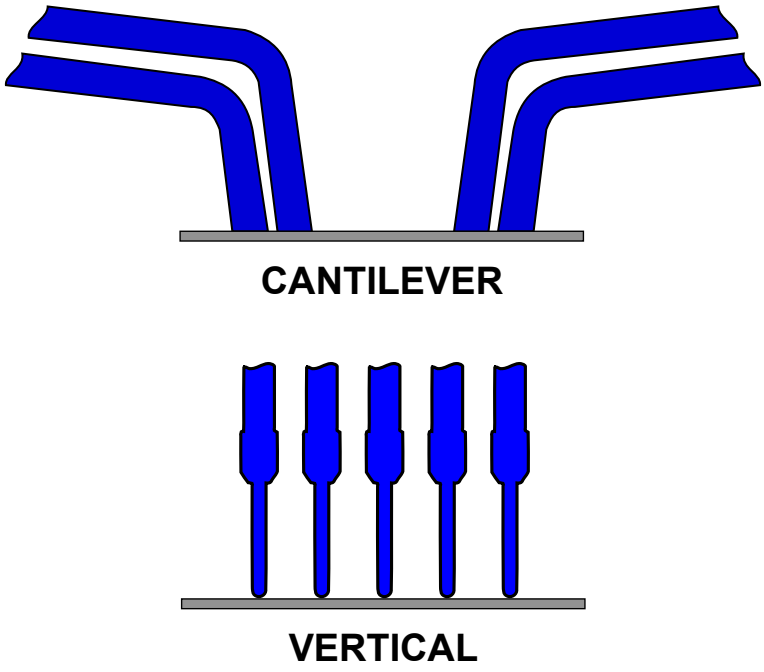


FIGURE 3.6: High-Current probe card designs, showing the side Structure of the Cantilever and Vertical designs.

3.3.2 New Probe Card Evaluation and Preliminary Testing

3.3.2.1 Optical Inspection

Both design, with chosen specification, have been built by a probe card manufacturer and provided for optical inspection, mechanical and electrical evaluation. The bottom optical view of both prototypes is shown in Fig.3.7, where the Cantilever design is reported on the left (a) and the Vertical probe card on the right (b). From the initial inspection both probe cards present the expected dimensions and type of needles, but the vertical distribution of needles tips is more regular in the Cantilever probe card than in the Vertical one. This condition is determined by the spring system of the vertical probe card, and a proper **Overdrive** can compensate the differences in height between the needles by lowering the distance between the probe card and the surface of the wafer under test.

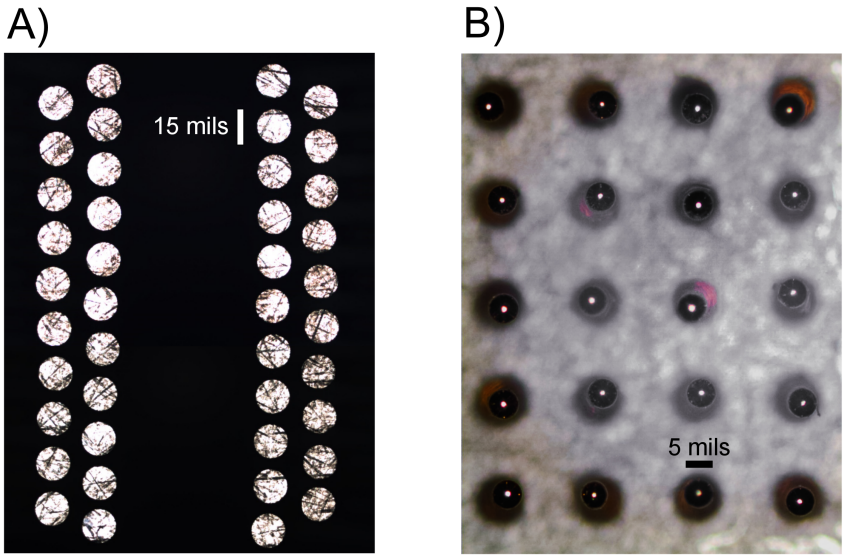


FIGURE 3.7: High-Current probe card designs: bottom view optical view of Cantilever (a) and Vertical (b) probe card needles assembly.

For both probe cards, probe mark analysis at the SEM (Fig.3.8, A1 and B1), profilometer measurements, and silicon surface check after contact metal delayering (Fig.3.8, A2 and B2), all performed after VF testing up to $100\,A$, show no damage to the device.

3.3.2.2 Mechanical Overdrive Evaluation

In order to determine the proper overdrive for each probe card, several mechanical and electrical tests have been performed for the sake of determining an optimal value with good contact on the wafer, good probe mark shape and depth in line with the initial setup, low impact on the value of the median and standard deviation of the final statistical VF measurements.

An analysis has been performed on the values of the VF standard deviation and VF median with respect to the chosen overdrive sweep range, and the results are shown in Fig. 3.9 and Fig.3.10. In particular for both probe cards, a minimum value for the VF standard deviation has been found, and this evidence increases with the current level of the test. For the cantilever design, the optimal value of the overdrive has been found to

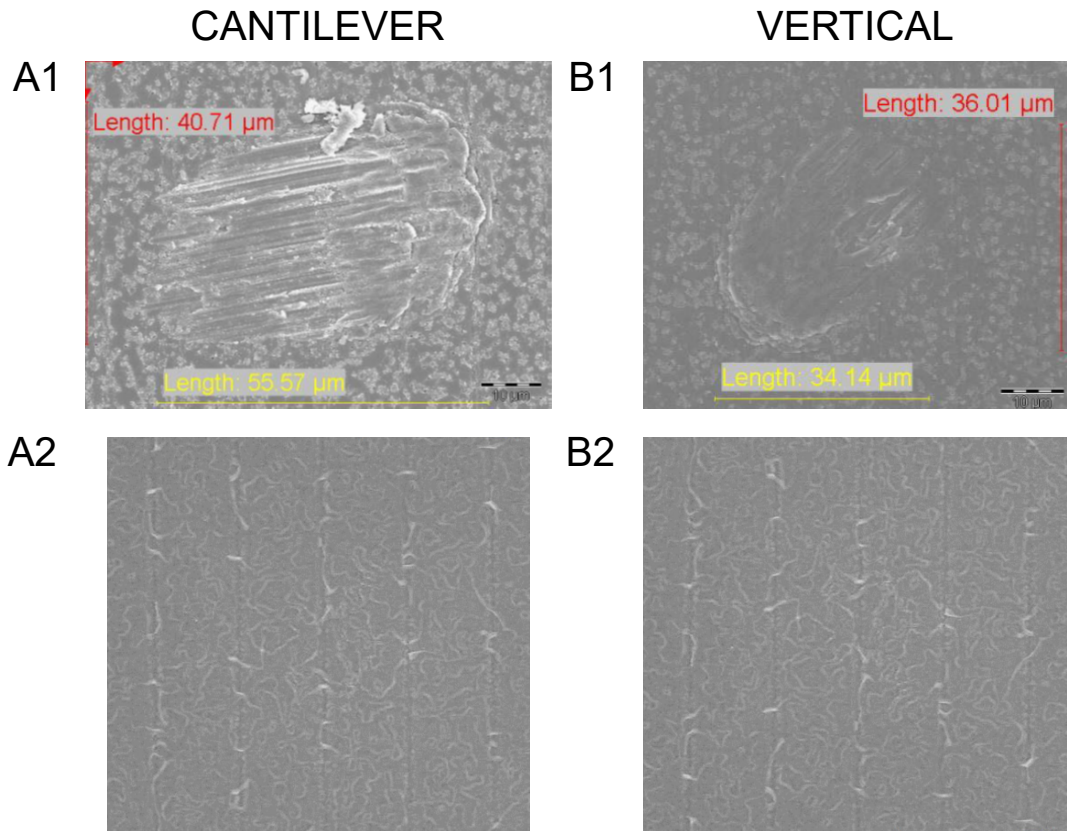


FIGURE 3.8: SEM Probe Mark Inspection for Cantilever (A1) and Vertical high current probe card (B1). Image taken at same location after top metal delayering, showing no damage on the silicon surface for Cantilever (A2) and Vertical (B2) probe cards.

be $100\,\mu m$ while for the vertical probe card this value has to be in the range between $300 \div 400\,\mu m$.

Furthermore, in the case of the Vertical design, needle contacting is not uniform due to the native difference in height of the needles, caused by the spring suspension system. In the range $450 \div 500\,\mu m$ the probe marks show no variation and good contact, even if the standard deviation is slightly affected, while below $400\,\mu m$, not all needles show good contact in terms of uniformity, repeatability and definition of the probe marks. For these reasons, the overdrive value has been chosen as the minimum value for which all needles were contacting the surface of the device in the analysed range, and as close as possible to the standard deviation minimum, resulting in an overdrive value of $400\,\mu m$. A final assessment on the overdrive value has been done also in collaboration with the probe card manufacturer. From this confrontation, the suggestion to increase the overdrive to $700\,\mu m$ emerged, but the capabilities of the prober only allow a maximum value of $500\,\mu m$, thus the decision to proceed with the latter value for all the following evaluations. As a side note, it is important to consider that lower overdrive values are preferred in order to reduce the mechanical wear-out of the needles and increase the lifetime of the probe card, which results in an increase of the maximum number of touchdowns before maintenance.

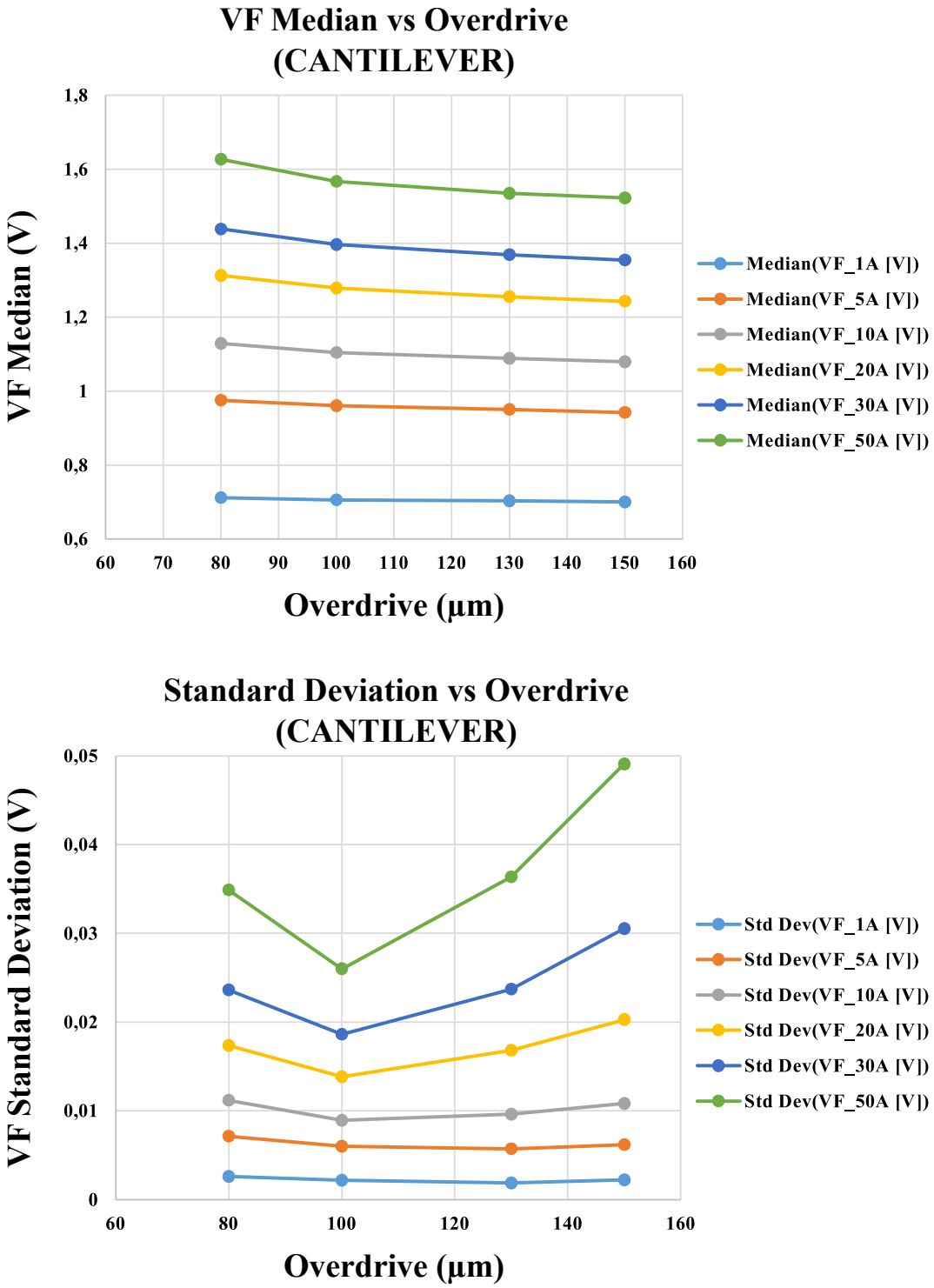


FIGURE 3.9: Cantilever Probe Card VF Median and standard deviation versus Overdrive, measured at different current levels from 1 A up to 50 A.

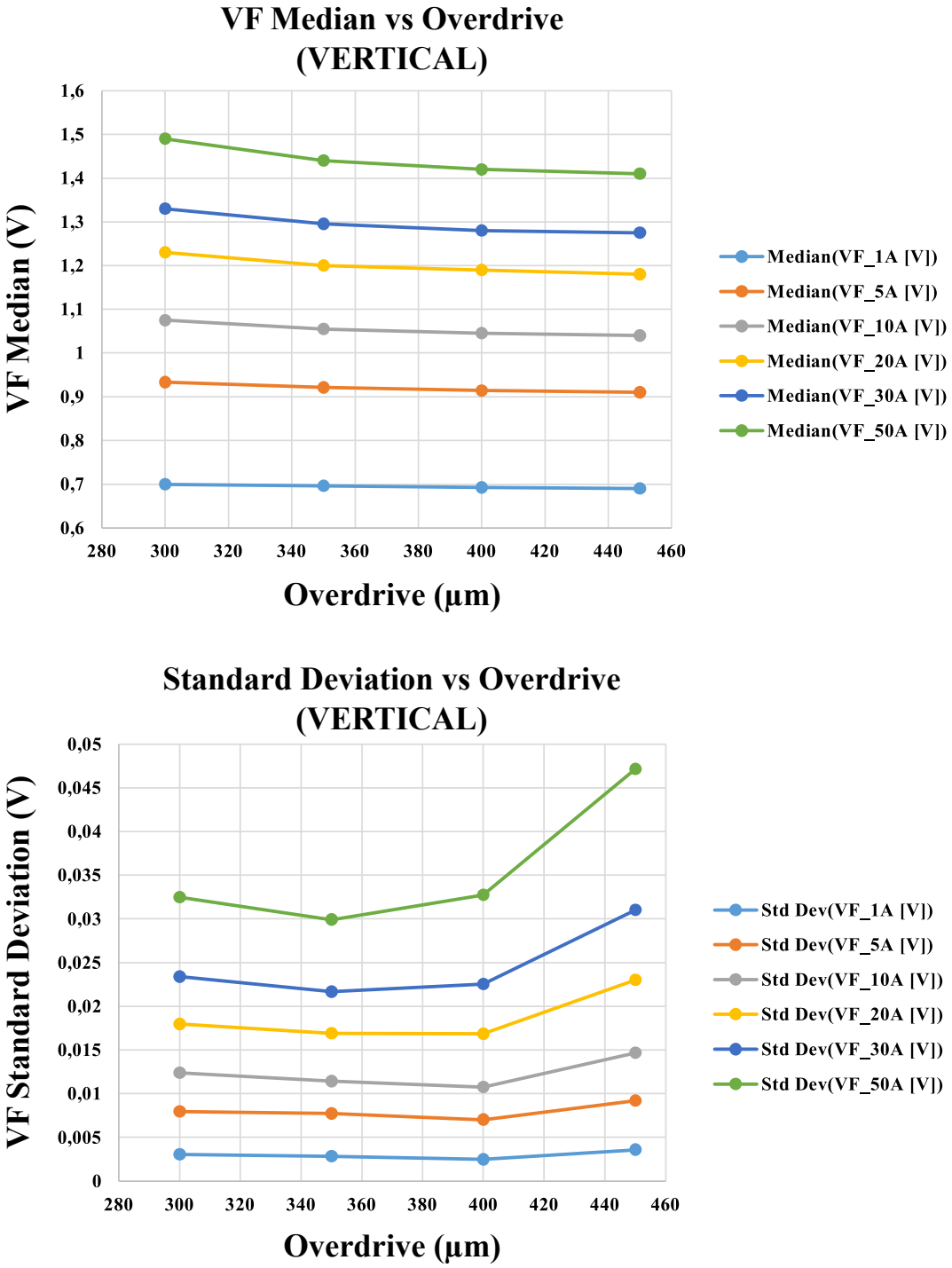


FIGURE 3.10: Vertical Probe Card VF Median and standard deviation versus Overdrive, measured at different current levels from 1 A up to 50 A.

3.3.2.3 Mechanical Marathon Test

Another significant test is the so called "marathon" test, evaluating the degradation of needles in time due to repeated touchdown on the metal surface of the wafer under test. The test has been performed on a selection of dummy device test wafer, and at defined checkpoints (0, 5k, 10k touchdowns), both probe card design have been been evaluated separately on a dedicated wafer, in order to monitor the degradation of the probe marks after repeated mechanical stress of the needles.

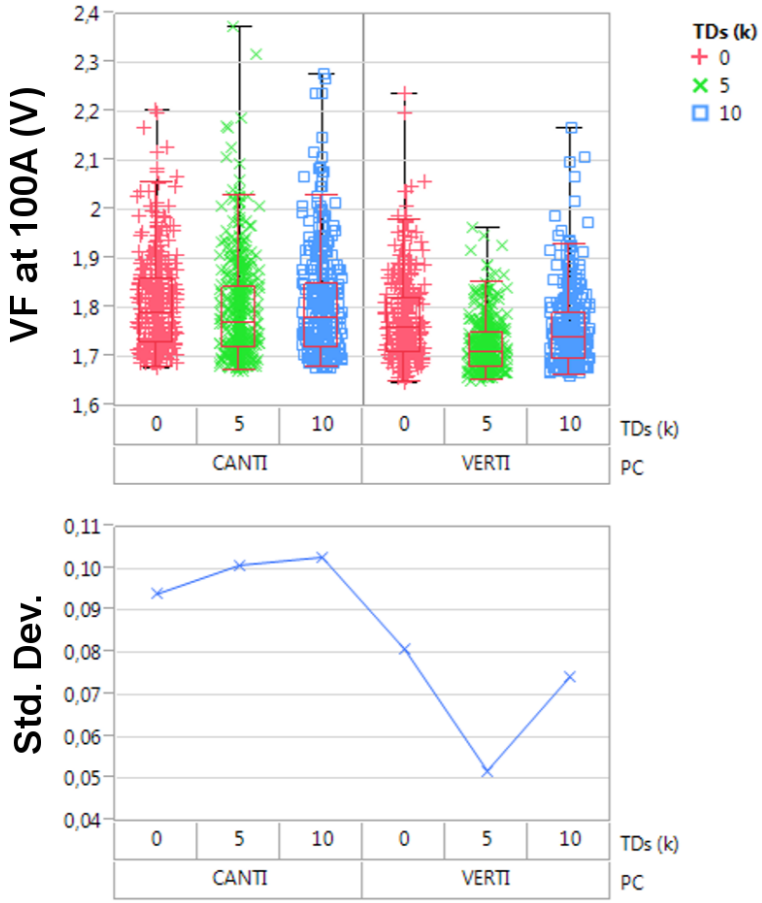


FIGURE 3.11: VF Marathon Test Statistical Analysis.

The statistical analysis and probe mark analysis is reported in figure 3.11, showing discording effects for the 2 probe card designs. For the cantilever probe card, the median is almost unaffected, while the graph shows a slight linear increase in time for a total of $\simeq 10\,mV$. This is not true for the vertical probe card, where the standard deviation reaches a minimum at $5\,k$ touchdowns ($\simeq 50\,mV$), and then rises back up ($\simeq 75\,mV$) to reach a final value which is lower than the initial one, showing a final absolute decrease of $\simeq 5\,mV$.

The optical monitoring and evaluation of the probe marks is reported in Fig. 3.12 and 3.13, while the profilometer analysis is reported in Fig. 3.14 and 3.15. These results confirm the phenomenon observed from the statistical observation (3.11), for which the wearing of the needle in the first $10\,k$ touchdowns gives a slight linear increase in depth for the cantilever (measured on at least 3 different needles), while for the vertical probe card this increase is not constant and shows an unstable behavior for which the stability of the probe mark is affected. This phenomenon is probably due to the combined effect

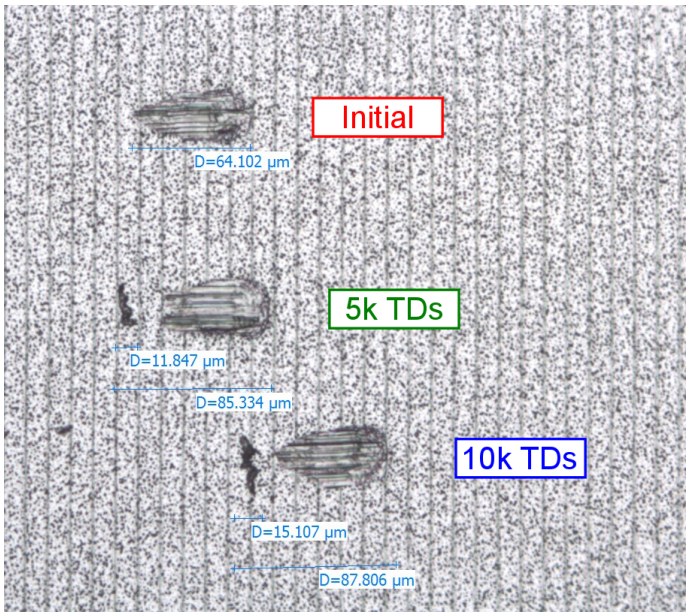


FIGURE 3.12: Probe Card Cantilever Marathon Test Analysis of the Probe Mark, showing the initial conditions and the status of the probe mark at 5k and 10k touchdowns.

of the overdrive (maximum possible $500\mu m$ opposed to the suggested $700\mu m$), and the wearing of the needle during the marathon test. It is important to consider that $10\,k$ is a first "seasoning" for a probe card, which generally has maximum limits in the range of $100\,k \div 1\,M$ touchdowns of expected lifetime before maintenance, so a further analysis would require longer times and resource investments, which are out of scope for this prototype evaluation, focusing more on the feasibility of the measurement system and the stability of the probe cards in their activity.

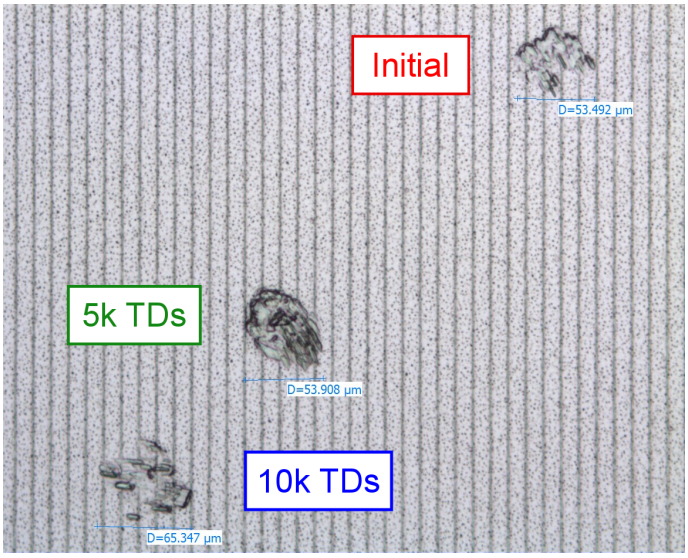


FIGURE 3.13: Probe Card Vertical Marathon Test Analysis of the Probe Mark, showing the initial conditions and the status of the probe mark at 5k and 10k touchdowns.

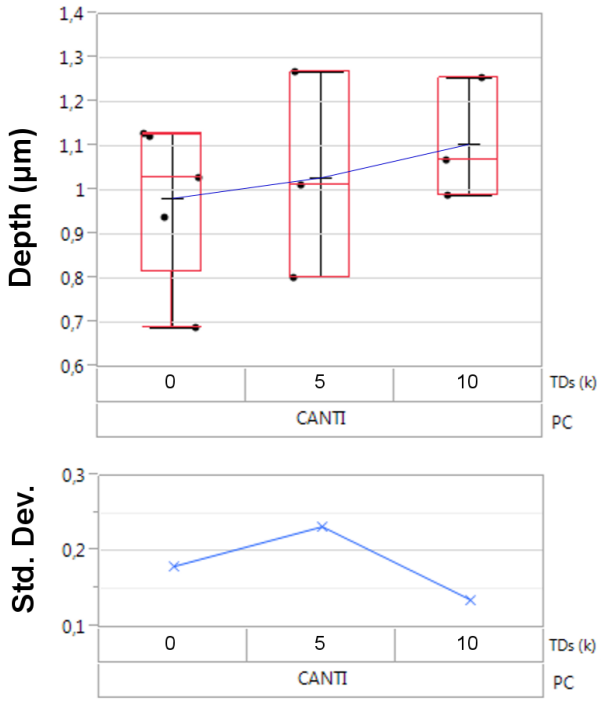


FIGURE 3.14: Probe Card Cantilever Marathon Test Analysis of the Probe Mark's Depth, showing the initial conditions and the status of the probe mark at 5k and 10k touchdowns.

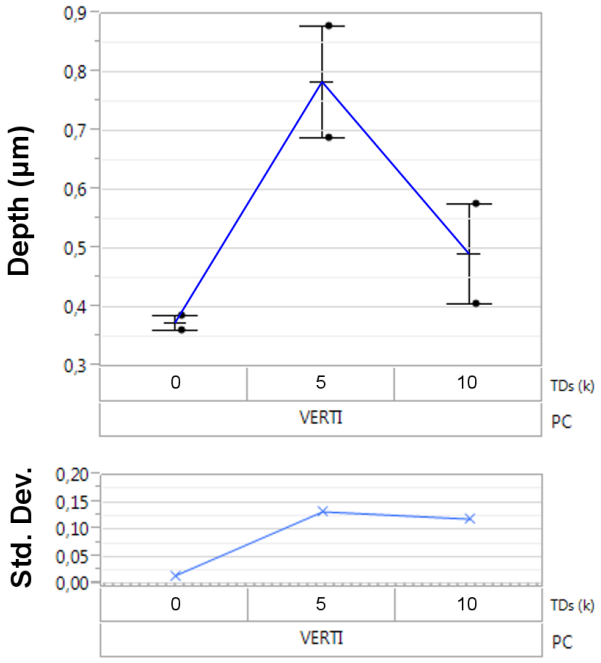


FIGURE 3.15: Probe Card Vertical Marathon Test Analysis of the Probe Mark's Depth, showing the initial conditions and the status of the probe mark at 5k and 10k touchdowns.

3.3.3 Electrical Testing

This section shows the set of electrical test evaluation, with the objective of understanding the capabilities and limits of the two proposed probe card design, while also including a comparison with respect to the reference low current probe card.

3.3.3.1 Over-current Test

With the objective of understanding the maximum safe current for VF testing of each probe card, several current levels were tested and the results are reported in Table 3.3, based on device failure analysis by delayering of the contact metal and SEM inspection on at the anode silicon surface.

TABLE 3.3: Over-current test, involving the initial setup low current probe card, cantilever and vertical ones.

Probe Card	**Current Level (A)**	**Current per Needle (A)**	**Device Damage**
Low Current	2,5	0,63	No
	5	1,25	No
	8	2,00	Yes
	12	3,00	Yes
	20	5,00	Yes
Cantilever	100	2,5	No
	115	2,88	No
	170	4,25	No
Vertical	100	3,03	No
	115	3,48	No
	170	5,15	Yes

For the low current probe card, a current level of $1,25\,A$ per needle can be considered as safe limit, since for all values above, a micro-fusion appears in correspondence of the probe mark on the surface of the silicon. An example of this phenomenon is reported in Fig. 3.16, where the passage of current generates a crater on the surface of the silicon, with a diameter of approximately $15\,\mu m$, the size of which depends on the current density and the quality of the contact with the needle at the anode metallization during VF test. Given the higher size of the needles for the high current probe cards, and the higher number of these latter, higher current levels per needle are achievable and both high-current designs support safe testing up to $115\,A$. But when overcoming the $5\,A$ per needle limit, the vertical probe card design shows signs of micro-fusion below the needles at the silicon surface. Oppositely, the cantilever probe card shows no damage even at a total current of $170\,A$.

In addition, a statistical analysis on a selected wafer measured with both probe cards highlights some differences between the two designs, and the result of this test is reported in Fig. 3.17. The variability chart shows a $30\,0mV$ statistical offset between the two probe cards, with the cantilever's median being higher than the vertical's. Moreover, the standard deviations are in the order of $75 \div 90\,mV$, a value which is considerably higher with respect to the same measurement at low current ($5\,A$). For this reason the next section will address further evaluation of the standard deviation values by taking

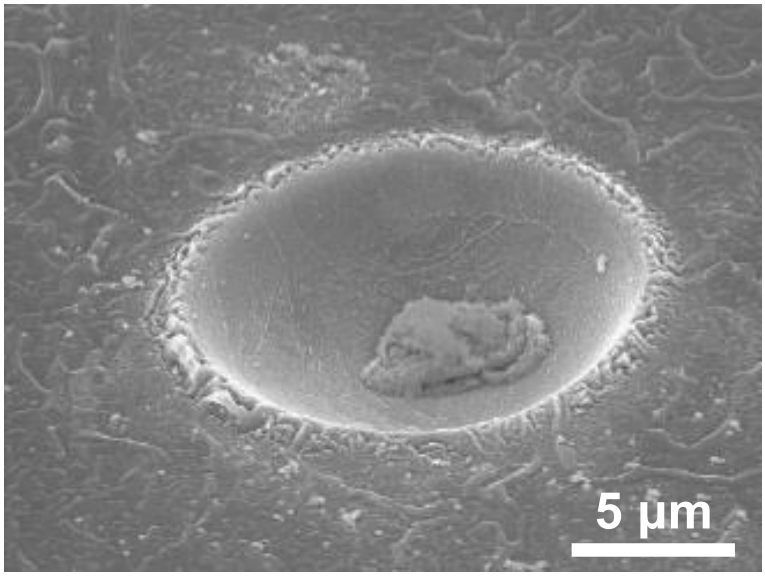


FIGURE 3.16: Example of micro fusion damage due to high current below a probe mark.

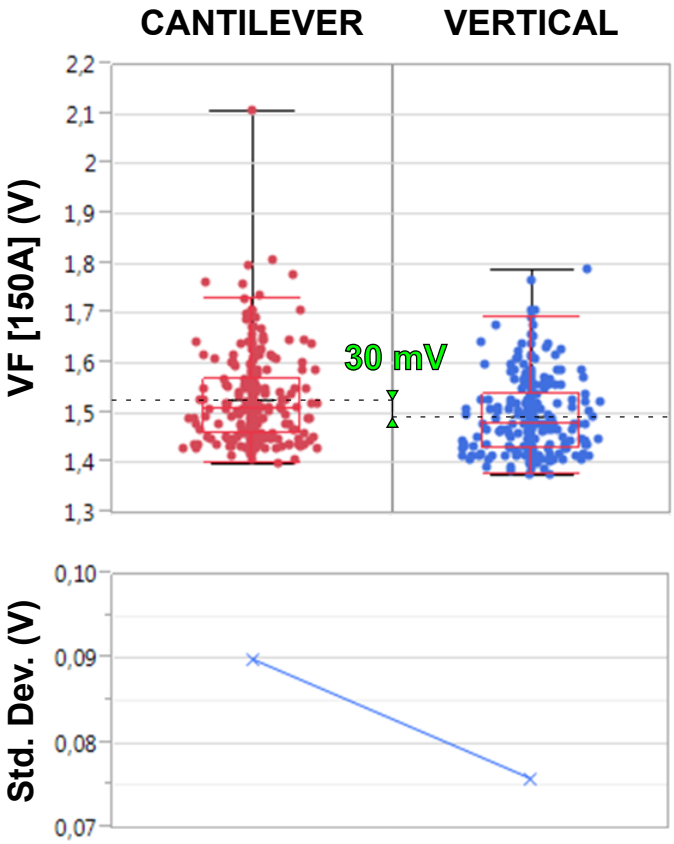


FIGURE 3.17: Variability chart of VF Testing at 150A: Cantilever vs Vertical. The difference between the median value of the two wafers is $\simeq 30\,mV$.

into account the assembly value as reference and comparing the baseline probe card data with respect to the high-current prototypes.

3.3.3.2 Assembly Data Analysis

In this section, sample devices are assembled in standard TO-247 in order to evaluate statistical differences between the VF testing at the wafer level and the assembly data. The chosen test vehicles are $600\,V$ power diodes samples with current rating of $250\,A$ with 400 assembled diodes per wafer.

Figure 3.18 and 3.20 show the measurement comparison performed respectively at $5\,A$ and $100\,A$ highlighting the difference in VF value and standard deviation, between the probe measurement and the assembly test with both the low current reference probe card and the high current cantilever design. The same comparison is done on the Vertical probe card and the results are summarized in Fig. 3.19 and 3.21.

At low current ($5\,A$), the median value of VF after the assembly process is always slightly lower than the probe level as to be expected, due to better contacting at the package level thanks to wire bonding, or possible offsets of the assembly test equipment with respect to the on-wafer VF testing equipment. In Fig. 3.18, the maximum value of the standard deviation ($16\,mV$) is reached by the low current probe card, while after the assembly this value shifts down significantly for the same reasons described previously in this paragraph, and holds for both the low current and cantilever probe cards. The same considerations can be done in the case of the Vertical probe card, whose analysis is reported in Fig. 3.19, and can be placed in direct comparison with the cantilever and low current probe card data. In this case, the lower VF standard deviation for wafer D and E is due to screening of the edge value dice at around $\simeq 1\,V$ and $\simeq 1,05\,V$ respectively due to the assembly test program screening, while at the probe level the standard deviation values are in line with those observed for both the cantilever and low current probe cards.

At high current ($100\,A$), the results highlight a significant lowering in the values of the standard deviation from probe to assembly, as highlighted by Fig. 3.20 and Fig.3.21. For the Cantilever probe card, the standard deviation for wafer A is lowered by $\simeq 50\,mV$ while for wafer C the downshift is exactly half the probe value being $\simeq 40\,mV$. Similarly, for the high current vertical probe card this shift is even more remarkable, where for wafer D the lowering is from $\simeq 70\,mV$ to $\simeq 10\,mV$, and for wafer E from $\simeq 70\,mV$ to $\simeq 40\,mV$. It is interesting to notice that for both probe cards, the probe value of the standard deviation seems to be almost fixed, independently from the nature of the wafer under test, for this reason an in-depth analysis of the assembly versus probe analysis is performed in the phase 2 of this methodology, with the main objective of understanding the cause behind the high-current VF standard deviation measured at the probe and lower this value to a level as close as possible to the low current one.

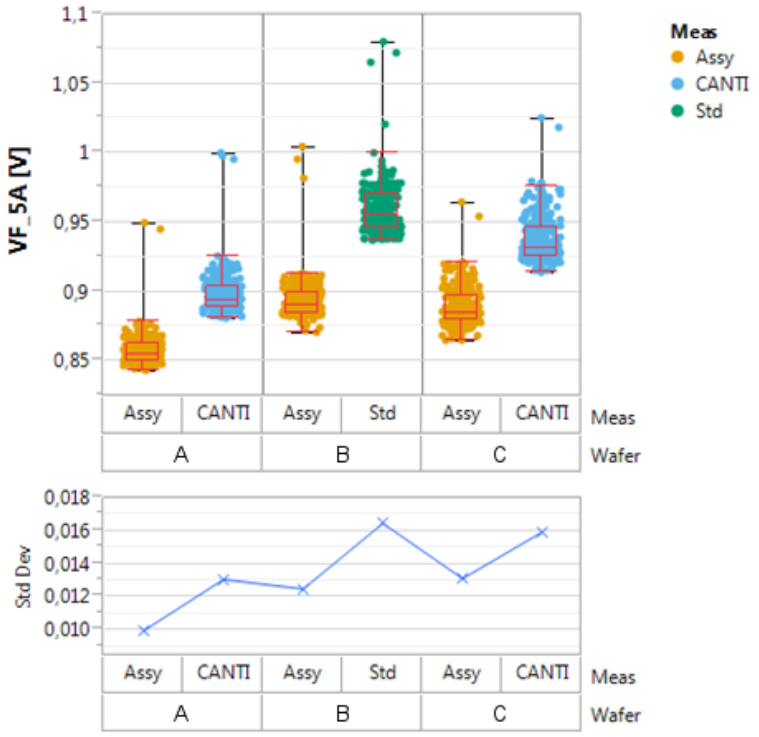


FIGURE 3.18: Cantilever versus low current probe card: assembly comparison at 5A.

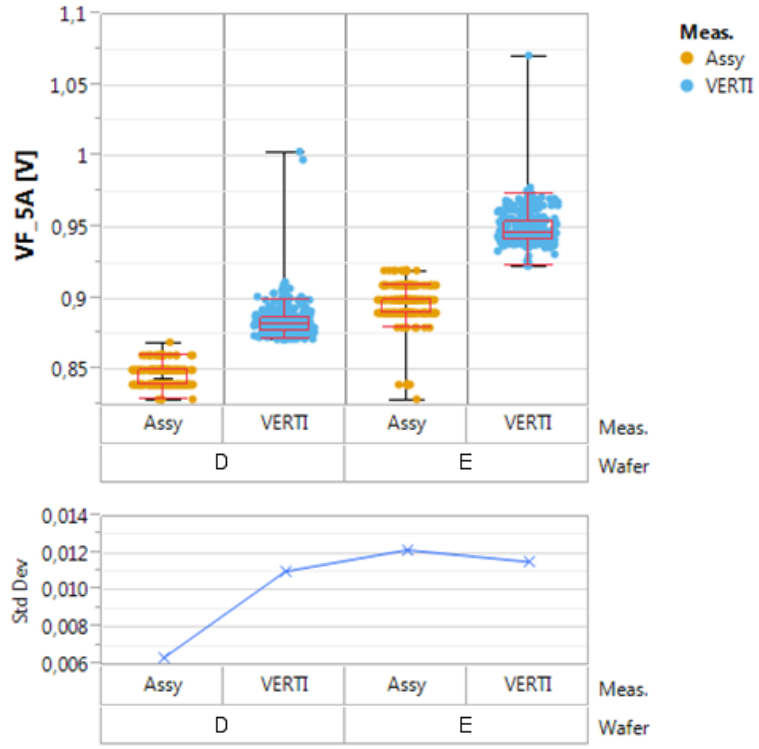


FIGURE 3.19: Vertical high current probe card assembly versus probe comparison at 5 A.

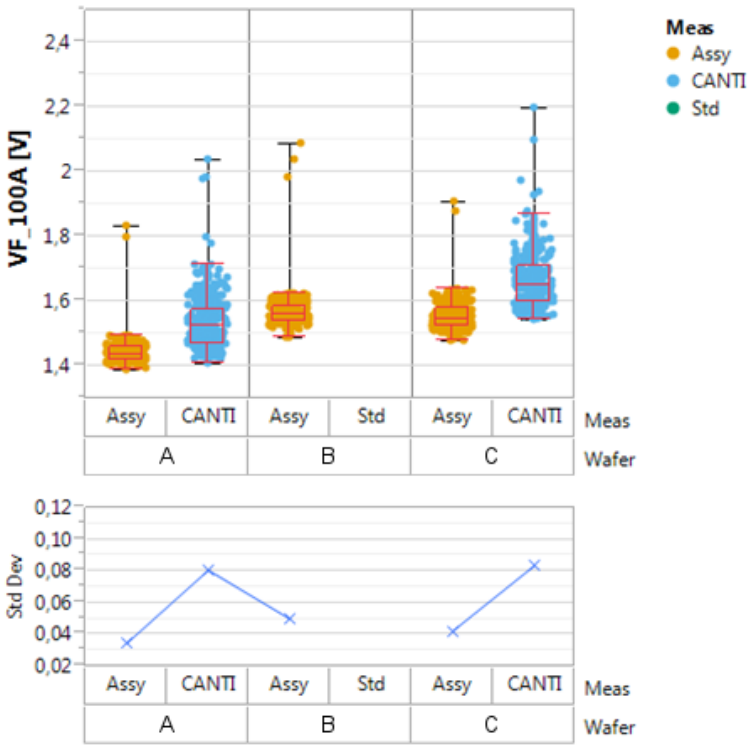


FIGURE 3.20: Cantilever versus low current probe card: assembly comparison at 100A.

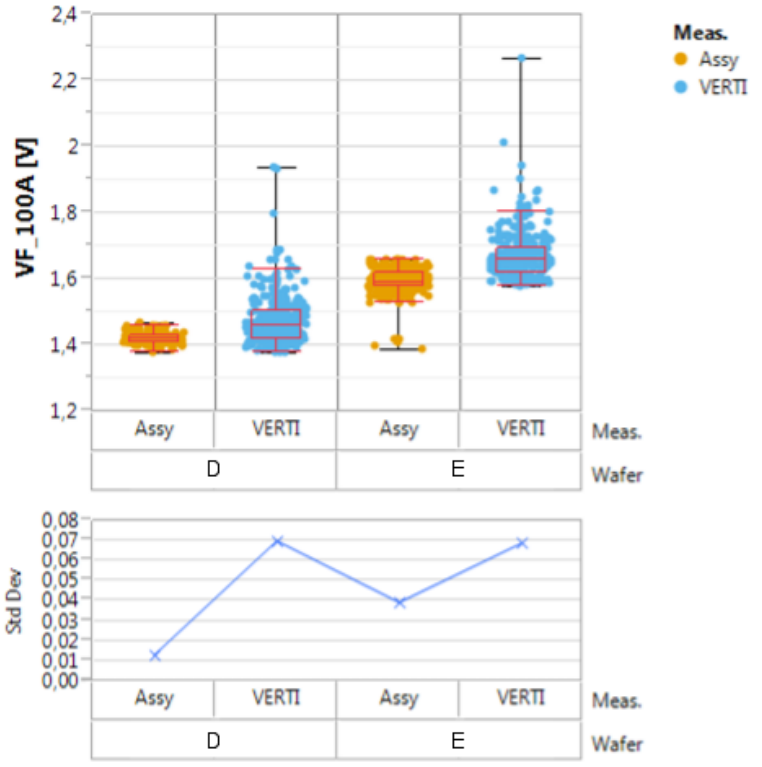


FIGURE 3.21: Vertical high current probe card assembly versus probe comparison at 100 A.

3.4 Methodology: Phase 2

The second part of this methodology focuses on the improvement of the VF standard deviation values at high current, which involved further analysis of the possible sources of VF variability, wafer map analysis, serialized testing of a set of device and eventually the design for the hardware improvement leading to the proposed solution and final test.

3.4.1 Possible Causes of standard deviation

In the first part of this analysis, several sources have been listed as a possible source of higher standard deviation as a part of the system, and their impact on the final VF measurement have been evaluated in order to identify the main source to be addressed by further testing and finally improve the precision of the test.

The first analyzed item is the power generator (Tester) (Fig. 3.2), which has been inspected and calibrated in order to bring the tool to its datasheet conditions, and showed performances in agreement with the expected ones, in terms of pulse shape, levels and ripple, as well as accuracy and precision. For this reason the analysis lead first to the evaluation of the wiring outside the tester, from the signal generator down to the prober assembly and eventually to the probe card (Fig. 3.2), the inspection of which revealed no issues in terms of signal interference, active or reactive power loss. The last analyzed time is the vacuum chuck contact below the wafer. This part of the hardware is a high conducting heavy metal plate, including a dedicated vacuum circuit allowing negative pressure to keep the wafer in place during the test. For the sample DUT wafer of this study, the back plane of the wafer contacting on the vacuum chuck is the common cathode of all chips during test, thus a non uniform contact or vacuum level could increase the series resistance yielding a higher VF value with respect to the real one of the selected chip.

For this reason, two test have been developed ion order to evaluate this hypothesis, a wafer rotation test and a serialized assembly test performed on a whole wafer row of chips, in order to confirm the discrepancy between the real value at the assembly and the VF measured on the wafer.

3.4.2 Wafer Rotation Test

A key measurement related to the issue exposed in the previous section, is the one involving 2 wafers measured twice, first in the standard position and then with a 180°C rotation. As it is possible to see in Fig. 3.22, the map of normalized VF values tested a 100 A, shows the presence of a set of patterns (A,B,C,D), appearing at the same location independently from the wafer under test, and the rotation of the latter.

This consideration is confirmed by statistical analysis in Fig. 3.23, showing no variation with respect to rotation, both in terms of median and standard deviation. As a consequence, a further test is selected to strengthen this observation, and will be described in the next section.

3.4.3 Serialized Assembly Test

As said in the previous section, in order to further confirm the presence of a high VF test pattern due to bad contact at the backside vacuum contact with the wafer (cathode contact), a serialized assembly test is performed on 31 devices from 2 wafers, as shown in 3.24 by correlating the map values 1:1 to those observed at the assembly test.

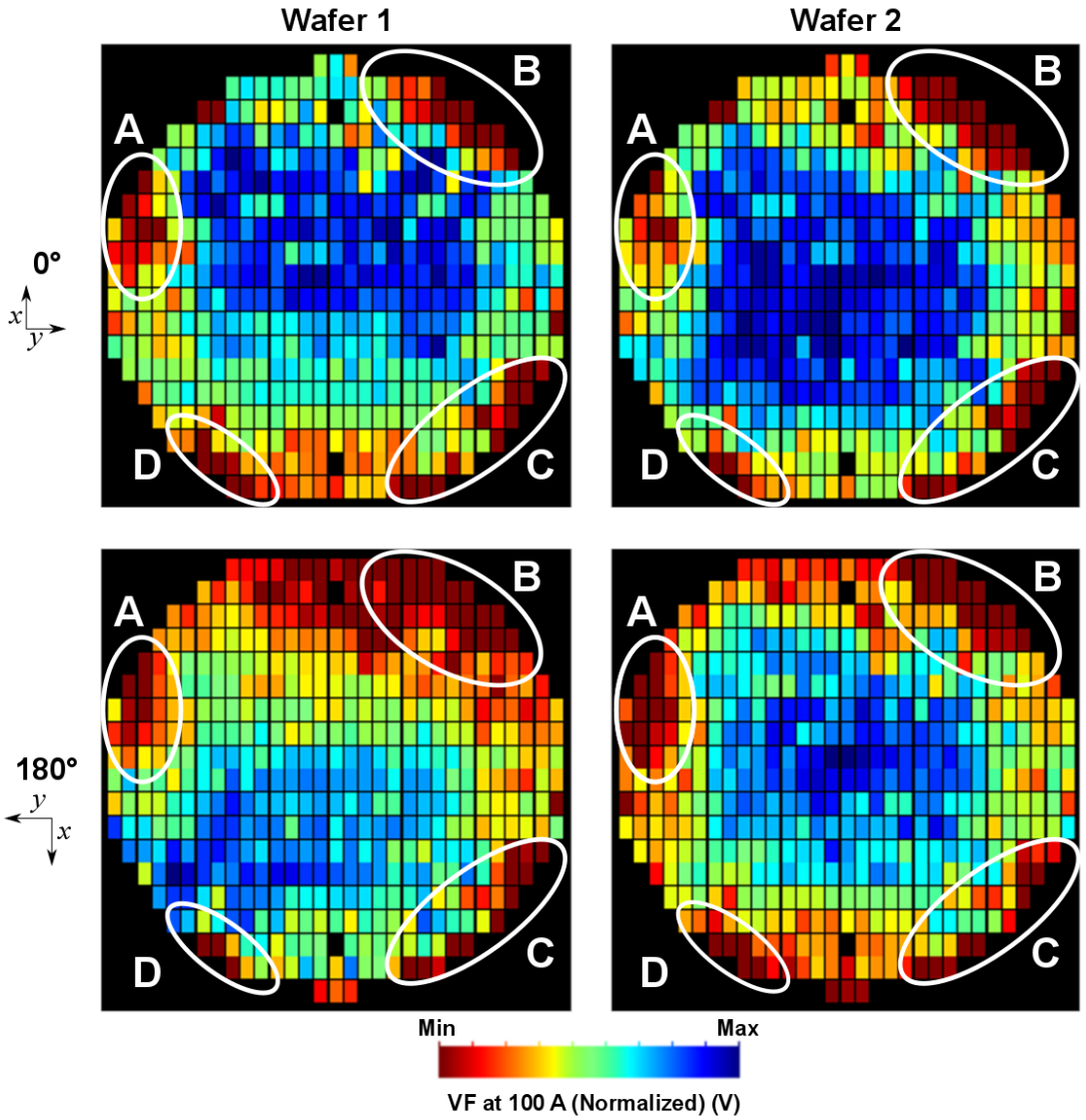


FIGURE 3.22: Wafer Rotation Test: VF Map at 100 A. The patterns A, B, C, and D repeat at the same positions independently from the rotation of the wafer.

The results of this test is reported in 3.25, showing that the probe values (blue squares) are not in line with the assembly values (red crosses), and how the difference between probe and assembly increases with the distance from the center of the wafer, confirming the results observed with the rotation test where the high VF pattern is observed (Fig. 3.22). This analysis is also complemented by the variability chart in 3.26, showing the same standard deviation reduction observed in 3.3.3.2. The results coming from this test, allow to move the focus of this analysis to the cathode contact with the vacuum chuck.

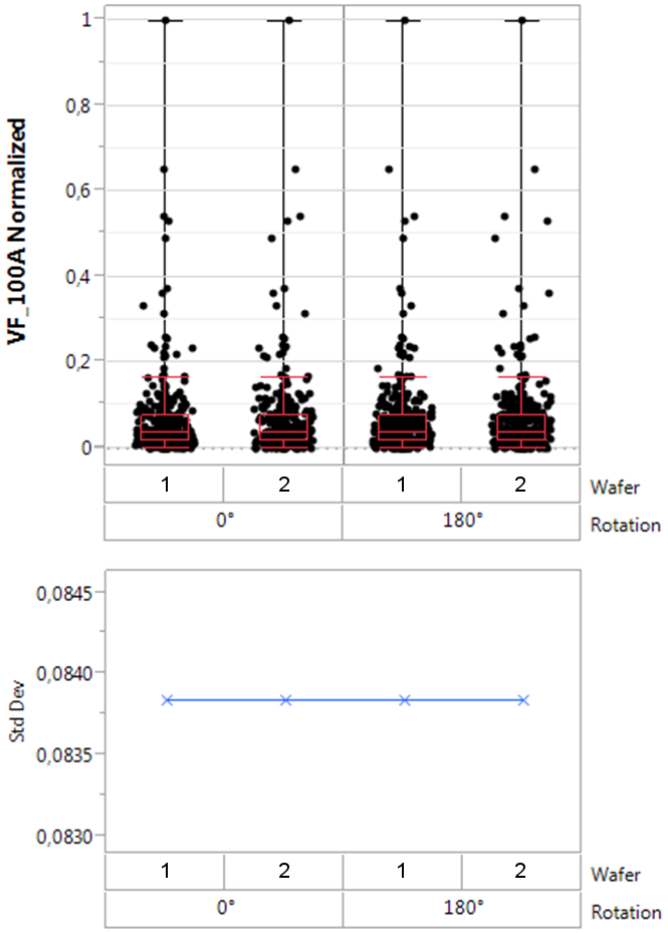


FIGURE 3.23: Wafer Rotation Test: VF Map at 100A.

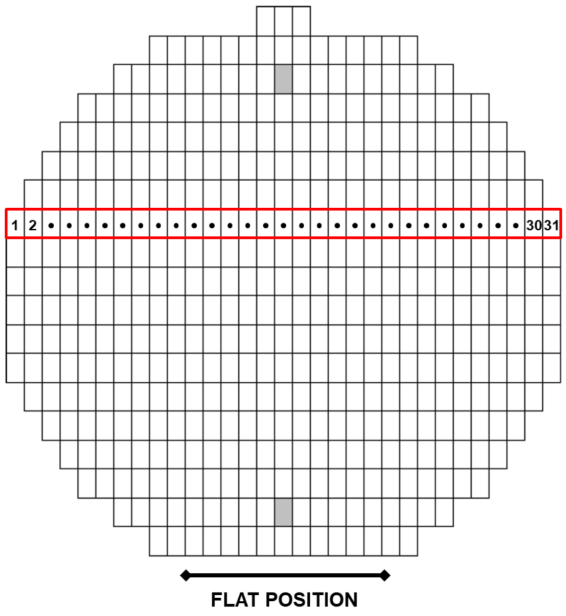


FIGURE 3.24: Wafer Schematic of the Serialized Assembly Test, highlighting the row of dice to be assembled for the 1:1 correlation of assembly high current VF values versus probe measurement.

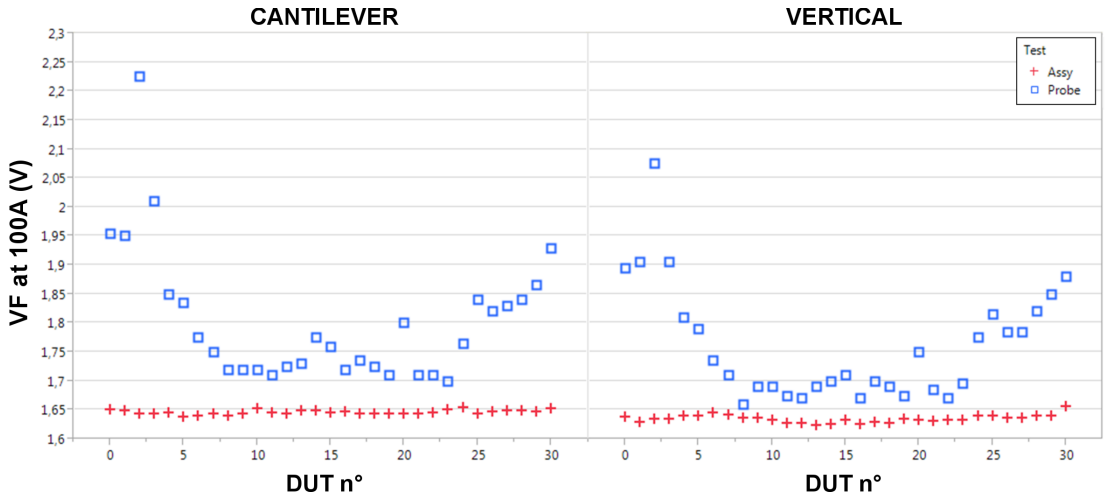


FIGURE 3.25: VF Serialized 1:1 Test Analysis, showing the difference between the values measured at the probe versus the assembly values of VF at high current. The difference increases with the distance from the center of the wafer.

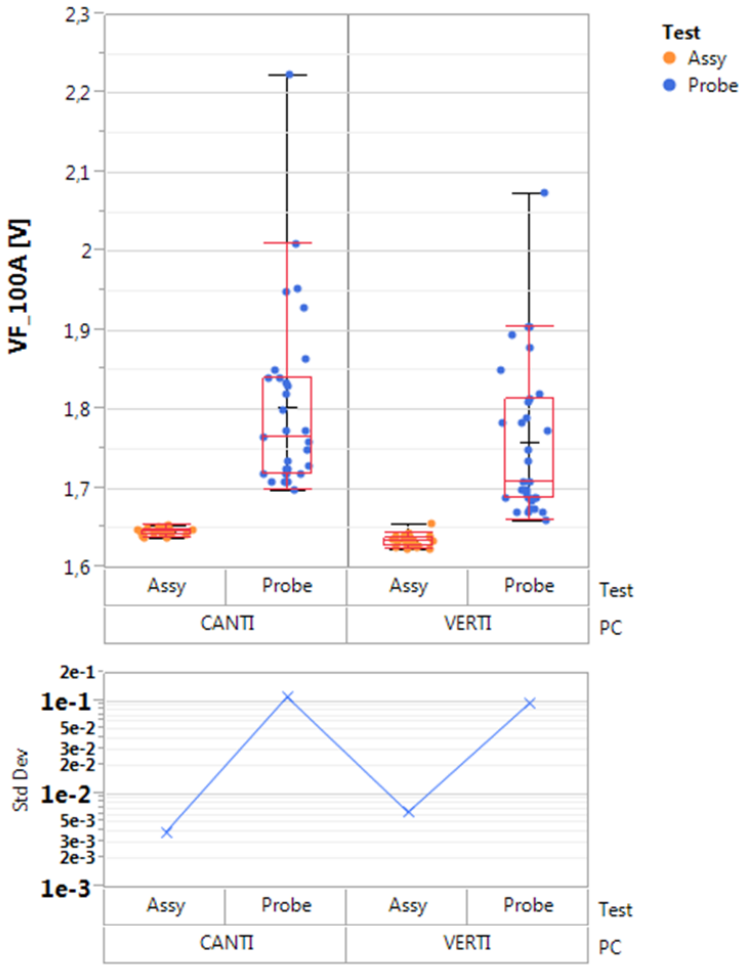


FIGURE 3.26: VF Serialized 1:1 Test Variability Chart

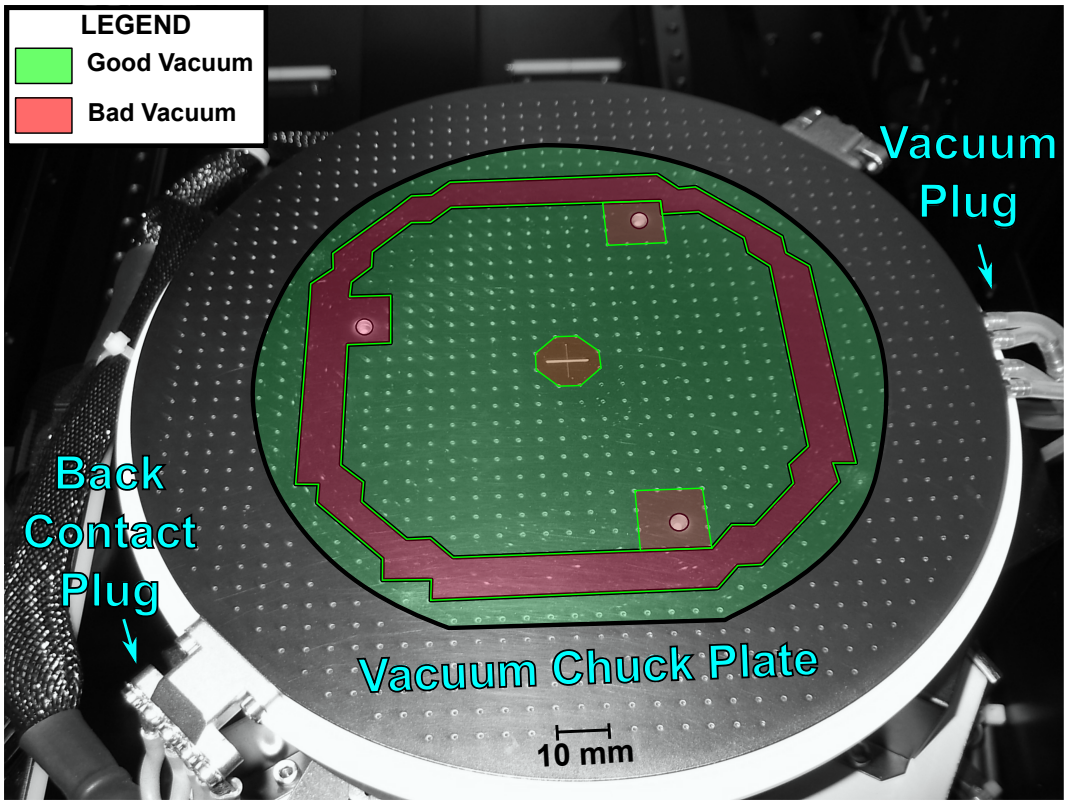


FIGURE 3.27: Initial Configuration of the Vacuum Chuck Plate, showing in red the bad vacuum region, and in green the good vacuum regions, with respect to the 6" wafer's edge.

3.4.4 Vacuum Chuck Analysis

In order to conclude the second phase of the methodology and obtain a significant improvement in high current VF standard deviation, the results from last sections identified the vacuum chuck as a good target of improvement.

3.4.4.1 Initial Conditions

The initial setup of the vacuum chuck plate is reported in 3.27, highlighting the main parts of the vacuum assembly and the regions of good vacuum (green), and bad vacuum (red). In the red regions the number of vacuum points is significantly lower than in the green region, and an entire ring where no without vacuum points is present in correspondence of a 4 inches edge wafer, as well as 3 bad vacuum region in correspondence of the wafer lifting pins for wafer movimentation. In addition, in this initial setup the minimum distance between vacuum point distance is 10 mm. Moreover, the 6 inches wafer edge is also outlined showing the similarities between the pattern in Fig. 3.22 and the red vacuum region, which is responsible for the high VF pattern not found at the assembly test. For these reasons a new vacuum chuck has been designed and implemented into the setup in order to achieve the wanted improvements in high-current VF standard deviation.

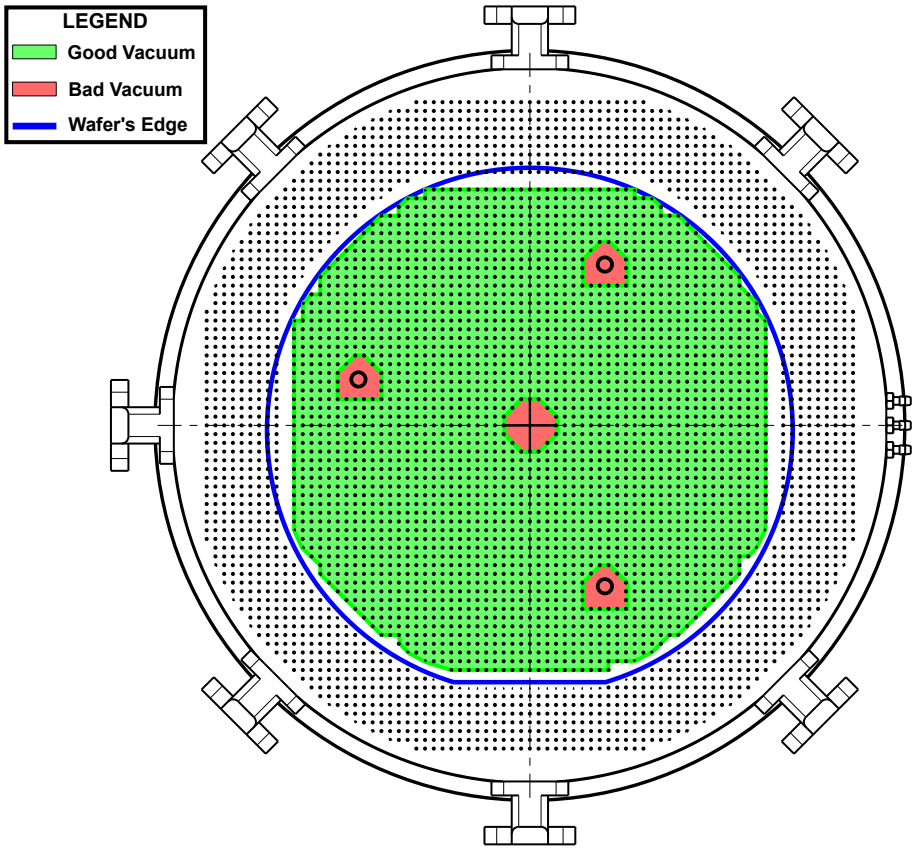


FIGURE 3.28: Schematic of newly designed vacuum chuck plate, showing in red the bad vacuum region, and in green the good vacuum regions, with respect to the 6" wafer's edge.

3.4.4.2 New Vacuum Chuck Design and Evaluation

Following the evidence described in the previous section 3.4.4.1 a new chuck has been designed in order to lower the standard deviation of VF at high current, and is reported in 3.28. In the new design the vacuum point density has been doubled, in particular the bad vacuum area due to the 4 inches vacuum chamber has been removed as well as any large contiguous region where no vacuum points were present, while the wafer lifting pins remain at the original location for compatibility reasons.

Following the same approach described in 3.4.2, a wafer rotation test has been performed in order to evaluate the improvements introduced by the new vacuum chuck design. The following trials have been performed only with one high current probe card (Cantilever), since no significant difference in standard deviation between the two high current designs were observed in the preliminary measurements. The results of the high current VF rotation test are mapped in Fig. 3.29, while the corresponding variability chart is reported in Fig. 3.30. The VF wafer map shows the absence of high VF pattern observed previously in Fig. 3.22 and the achievement of a lower standard deviation level is confirmed by the variability chart, showing a remarkable decrease of $\simeq 40\,mV$ which is approximately half the value measured with the initial vacuum chuck.

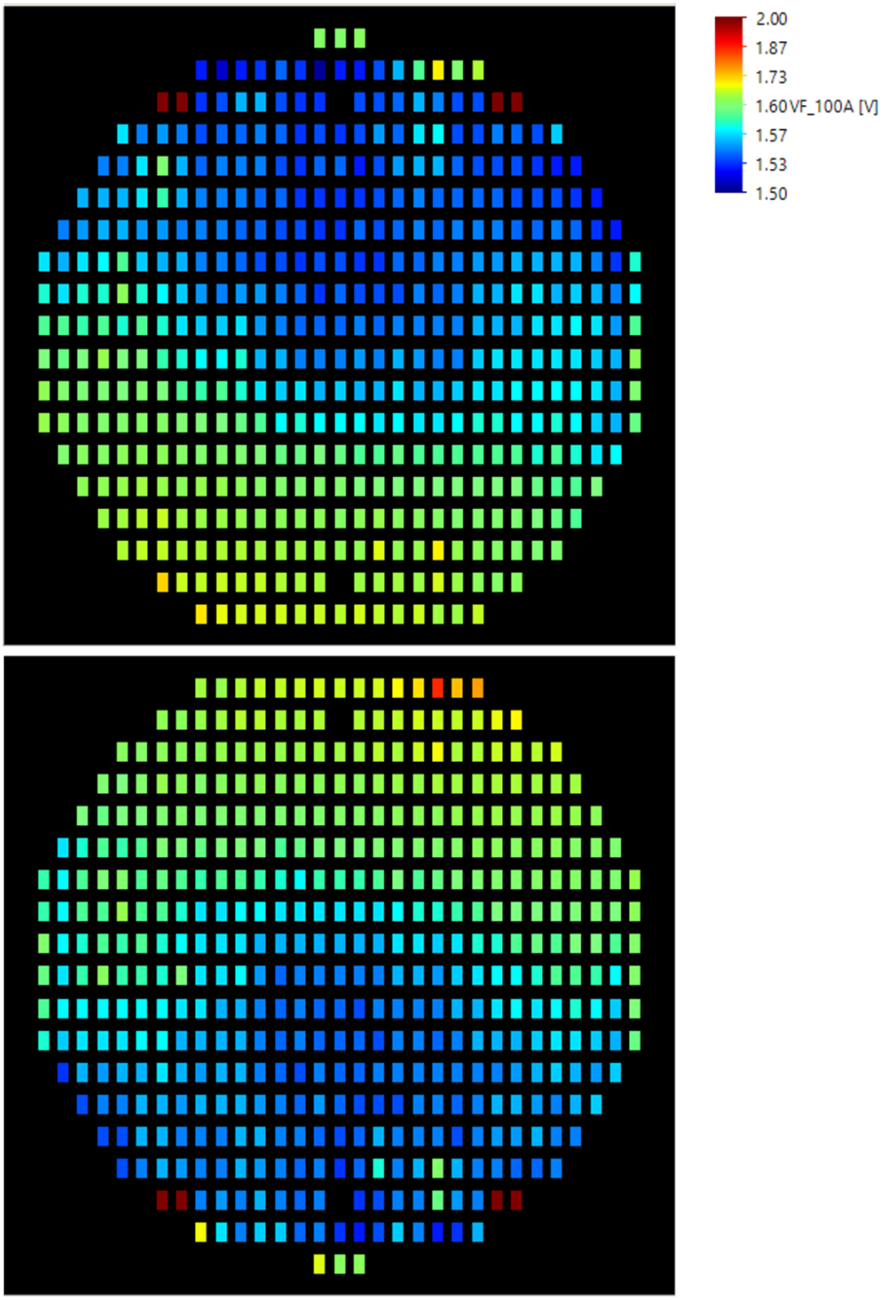


FIGURE 3.29: Wafer rotation test performed on the new vacuum chuck assembly for a selected wafer, measured before and after rotation (0° and 180°). The initial high current VF pattern is not present and negligible increases of VF are observed only in correspondence of the 3 lifting pins.

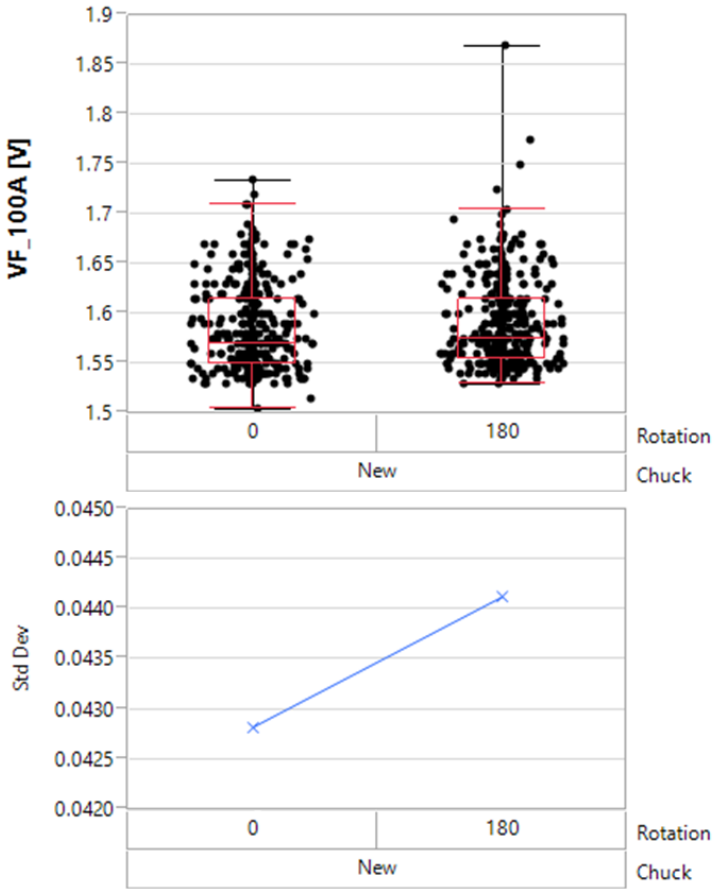


FIGURE 3.30: Wafer rotation test performed on the new vacuum chuck assembly. The variability chart shows a great improvement in standard deviation with respect to the initial setup.

3.5 Conclusions

The main objective of this chapter has been the design, implementation and evaluation of a wafer-level high current Forward Voltage Drop (VF) measurement setup on a pre-existing production apparatus. The initial test setup has been analyzed, and a manufacturer benchmark allowed to define the correct specifications for the new system. In the methodology, a set of two high current probe cards has been evaluated with a wide range of mechanical and electrical analyses, in order to understand the performance and limitations of the two solutions. In the second part, a further improvement of the test setup is performed by analyzing the possible sources of series resistance yielding high VF standard deviation. The pattern of high VF is correlated to the backside vacuum contact, which is re-designed and tested showing a great improvement of the high current VF standard deviation, and the removal of the observed edge pattern.

Part IV

Cosmic Ray Robustness Of Power Semiconductor Diodes

Chapter 4

Cosmic Ray Robustness

4.1 Introduction

This chapter is dedicated to the evaluation of the cosmic ray ruggedness of power semiconductor devices. The testing is performed in agreement with the JEDEC standard JEP151 "Test Procedure for the Measurement of Terrestrial Cosmic Ray Induced Destructive Effects in Power Semiconductor Devices"[4]. In the methodology section, the experimental work involves the development of a dedicated testing is described, followed by the description of the test campaign, and relative results, performed at the ISIS Neutron and Muon Source located at the Rutherford Appleton Laboratory in Didcot (UK). The experimental work has been carried out under the supervision of the Reliability and Radiation Effects on Advanced CMOS Technologies (RREACT) group from the University of Padova, Italy.

4.1.1 Nature of Cosmic Radiation

On Earth, cosmic radiation can have three main sources: galactic, extra-galactic and solar high energy particles, having a broad range of energies. When a particle first collides with the Earth's atmosphere it is called a primary cosmic ray, having a general composition of high energy protons (87%) alpha-particles (12%) and heavy nuclei (1%) and very small portion of positrons and antiprotons. After the collision, the primary ray generates a "particle shower" including several particles such as photons, muons, pions, electrons and positrons as shown in Fig.4.1 [114].

A great part of particles is coming from the sun, which is responsible for the majority of particles with energies below $10^{10}\,eV$. Above this value, probable sources can be supernova eruptions ($10^{16}\,eV$), from our galaxy up to $10^{18}\,eV$ Ultra High Energy Cosmic Radiation (UHECR). Beyond $5 \cdot 10^{19}\,eV$ Extreme Energy Cosmic Ray (EECR), the particles are coming probably from the core of distant active galaxies in the local supercluster. The higher the energy, the lower the occurrency, infact EECR are very rare, and are measured in the number of just 9 events per year in some observatories, while exceptional events like the so called Oh-my-god-particle in (1995) can be only detected a few times per decades [115].

Primary cosmic rays generally collide with atomic nuclei in the atmosphere and generally do not reach the Earth's surface, so a particle shower is a common event involving the production of a number of secondary particles as high as 10^{10}. The most interesting particles for the Single Event Burnout (SEB) phenomenon are neutrons and protons. In the case of neutrons a flux of $20\,cm^{-2}h^{-1}$ is typical of sea level [116], while this increases progressively and at common civil plane flight altitudes can reach even $7200\,cm^{-2}h^{-1}$ [117]. These values depend firstly by altitude and secondarily by the geographic coordinates of the occurrence. Given their lower interaction with matter with respect to protons, the neutron flux has a higher contribution in the lower atmosphere, but at flight

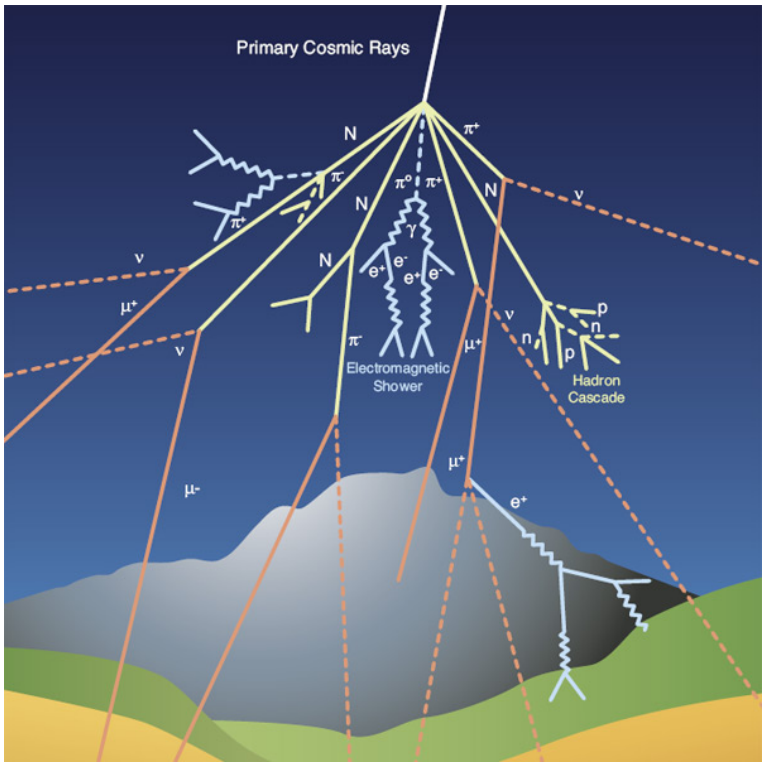


FIGURE 4.1: Schematic view of a primary cosmic radiation event generating a secondary particle shower, including photons, neutrons, protons, pions, neutrinos, electrons and muons. [114] © 2017.

altitudes (12.2km) protons can contribute to 50% of the total cosmic radiation flux, and above this altitude represent the majority of particle flux [118]. For these reasons, the incidence of cosmic ray failures is generally related mostly to neutrons at sea level, and due to the non-uniformity of the Earth's magnetic field, the flux intensity at the poles is 3 times higher [117].

4.1.2 Effects of Cosmic Radiation On Power Devices

The problem of cosmic ray ruggedness was first raised to the scientific audience in the first 1990s, when peculiar failures in the field were observed in blocking conditions for power semiconductor devices in electric traction and airspace applications. The same kind of devices for which failure was observed were tested in blocking conditions at high continuous voltage, confirming the manifestation of sudden failure without any detectable sign of failure before the occurrence in the emblematic "salt mine experiment" [119].

In this experiment reported in Fig.4.2, a set of 18 diodes wired in parallel and reverse biased at 4000 V is monitored during 4 phases for a total testing time of 9000 hours. In the first phase the 18 diodes are biased in a laboratory at ground floor, with only a tin roof shielding the setup, and 6 failures occurred in the first 700 hours. The whole setup was then moved in a salt mine at the depth of 140 m, and in these conditions no failure occurred for around 7000 hours. In the third part of the test the devices were brought back to the lab, and showed a similar failure rate as in the first phase of the test. Eventually the whole setup was moved into the cellar of a building, under 2,5 m of concrete above the setup, showing an appreciable reduction of the failure rate with

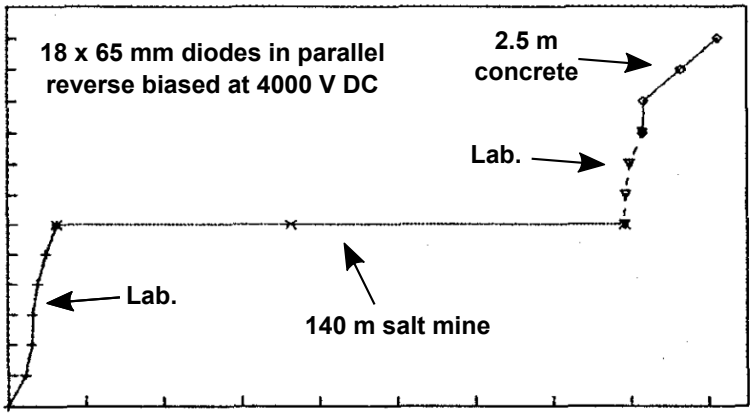


FIGURE 4.2: Cosmic ray salt mine experiment. A set of 18 4000 V power diodes is monitored for 9000h hours in 4 phases, in lab, under a 140m deep salt mine, again in the same lab and lastly under a 2.5 m concrete building, showing a correlation between exposure and the failure rate. Figure reproduced with permission from [119] © IEEE 1994.

respect to the lab conditions. This experiment outlined the presence of what today are called SEBs [120].

4.1.2.1 Single Event Effects in Power Devices

Power semiconductor devices such as Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and diodes can be sensitive to Single Event Effects (SEE) induced by ionizing radiation. SEE are caused by wandering ionizing particles, randomly hitting electronic devices in sensitive areas. SEE are stochastic effects which are generated by a single ionizing particle. At terrestrial levels, the natural sources of radiation responsible for SEE are atmospheric neutrons and alpha-emitting contaminants inside package and chip materials. There are two types of SEE that can affect a power MOSFET (a vertical device is shown in Fig. 4.3) hit by an ionizing particle:

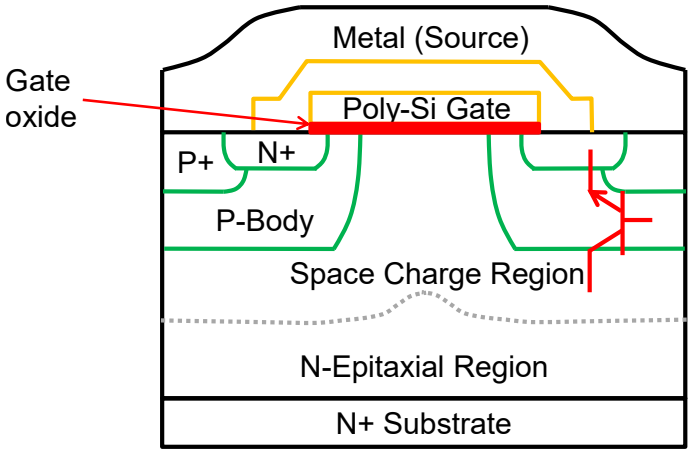


FIGURE 4.3: Sketch of a vertical power MOSFET.

1. Single Event Burnout (SEB), consisting in the activation of the parasitic bipolar transistor (e.g., in Fig. 4.3 source=emitter, p-body=base, n-epi=collector), especially in n-channel devices, which may cause permanent damage.

2. Single Event Gate Rupture (SEGR), consisting in the rupture of the transistor gate oxide (neck region), both in n-channel and p-channel devices.

Power diodes can experience SEB, and both SEB and Single Event Gate Rupture (SEGR) can be triggered by a single ionizing particle, depositing enough energy in the sensitive regions of the device, and leading to degradation in performance and/or system failure. In the following, the main features of SEB and SEGR phenomena will be summarized.

4.1.2.2 Single Event Burnout (SEB)

Figure 4.4 depicts a typical drain current versus drain voltage characteristic for a power MOSFET. As the drain voltage is increased avalanche breakdown takes place. Above the avalanche breakdown point, the drain current abruptly increases as a function of the drain voltage. The drain current flows through the body region, eventually causing the parasitic bipolar transistor to turn on. Afterwards, although the device current keeps increasing, the drain voltage starts to decrease. When the parasitic bipolar transistor is activated, the drain current flows through both the source and the p-body. At some point, the current-voltage condition that triggers second breakdown (i.e., sudden decrease in the device blocking voltage capability with an uncontrolled increase in current) is reached and catastrophic failure occurs. If a heavy ion traverses the power MOSFET and deposits enough charge in the drain depletion region, the parasitic bipolar transistor can be turned on in a tiny region. In case the applied drain voltage stress is high enough, the local current regeneratively increases and SEB occurs. As shown in Fig. 4.4, the I-V curve defines the operating region where a MOSFET is sensitive to SEB . The maximum operating voltage at which the MOSFET is insensitive to SEB is highlighted with a dotted line: if the device is operated at a drain voltage below the second breakdown, SEB is not a concern.

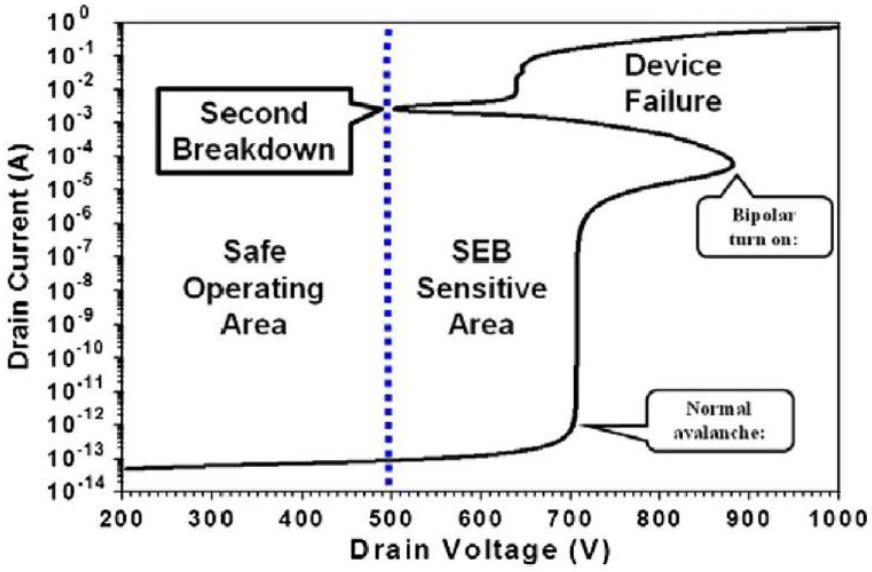


FIGURE 4.4: I-V characteristic of a power MOSFET. The SEB sensitive area is highlighted. [121]

The typical signature of SEB is an abrupt and large increase in the drain current, whereas the gate current is usually not impacted, as depicted in Fig. 4.5. Other characteristics typical of SEB are the following:

- SEB failure threshold voltage usually does not depend on the off-state gate bias
- SEB failure usually induces discoloration and/or die surface degradation
- SEB failure usually induces a resistive short between the drain and source (whereas the gate is not necessarily damaged after SEB)
- SEB is sensitive to circuit impedance (resistance and inductance) at the drain and source.

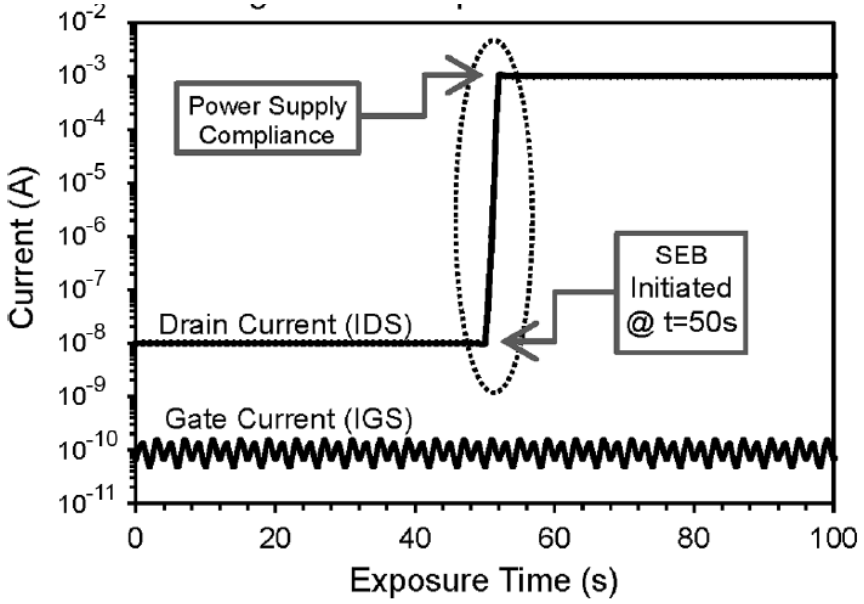


FIGURE 4.5: Evolution of the drain and gate current in a power MOSFET experiencing a SEB during heavy-ion irradiation.[121]

The occurrence of SEB strongly depends on the features of the impinging particles. In most of the reports about SEB , heavy ions with high ionizing power, i.e. with a Linear Energy Transfer (LET) larger than $25\,MeVcm^2/mg$, have been used, but in some cases even ions with LET values below $10\,MeVcm^2/mg$ have been shown to cause SEB phenomena [122]. Nevertheless, until some time ago, LET was believed to be the key factor for SEB . Fig. 4.6 illustrates the SEB cross section versus drain voltage for an unhardened 200 V N-channel power MOSFET, irradiated with four different heavy ions. As seen, the larger the ion LET, the lower the drain voltage at which the SEB is triggered. Inversely, the saturated cross section is independent of the particle species.

Recent data showed that an even stronger correlation exists with the atomic number of the impinging particle, with the heaviest ions having larger probability of inducing SEB (see Fig. 4.7) [123].

Also, an obvious dependence on the range of the particles used during the test has been reported: the shorter the range, the larger the failure threshold voltage for SEB [123]. Concerning the angular dependence of the impinging particle beam, usually SEB occurrence decreases with increasing ion angle, but it may increase as well, depending on the device geometry [121].

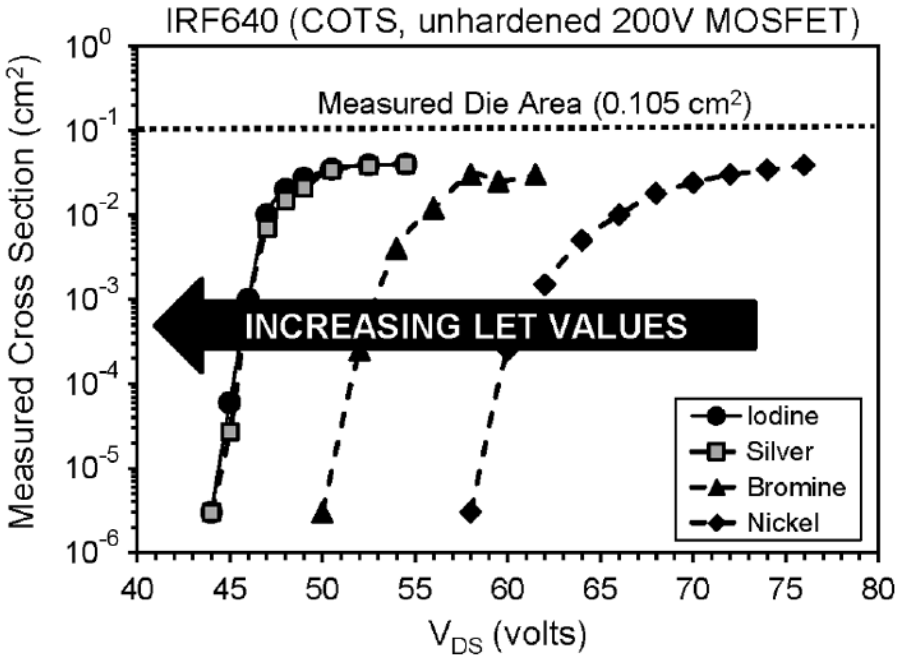


FIGURE 4.6: SEB cross section vs. applied drain voltage for an unhardened MOSFET exposed to different ions [121]

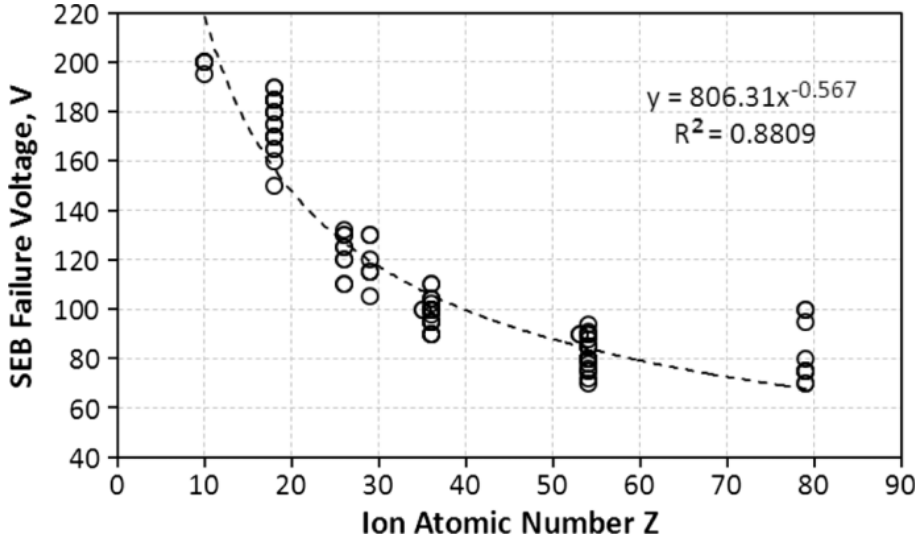


FIGURE 4.7: SEB failure voltage dependence on the atomic number Z of impinging ions. [123]

In addition to the particle features, there are also some device parameters that should be considered when evaluating SEB . One of these is the operating temperature. Generally, higher temperature increases the failure threshold voltage [124], although different devices may exhibit different behaviors. P-channel type devices are usually much less sensitive with respect to their N-channel counterparts [125]. Process and design hardening techniques to limit the susceptibility to SEB have been studied in several papers. One of these methods is the introduction of a buffer layer (i.e. a second epitaxial layer) [126]. Many of these SEB -hardening techniques tend to reduce the devices electrical performances, typically increasing the on-resistance, so there is generally a trade-off

between higher performances and lower SEB susceptibility.

4.1.2.3 Single Event Gate Rupture (SEGR)

SEGR takes place when an ionizing particle traverses the MOSFET gate oxide region, generating a plasma filament of electron-hole pairs between the gate oxide and the drain. This leads to an increase in the electric field between the gate oxide and the channel. In certain conditions (e.g., if the applied drain voltage is high enough, the gate voltage is zero or negative, ...) the gate oxide will experience a local rupture. An example of the evolution of the drain and gate currents when a SEGR is triggered during heavy-ion irradiation is depicted in Fig. 4.8. The typical signature is an abrupt increase in the gate current, accompanied by an increase in the drain current. Also, typically the die surface does not appear damaged after SEGR upon visual inspection (contrary to SEB).

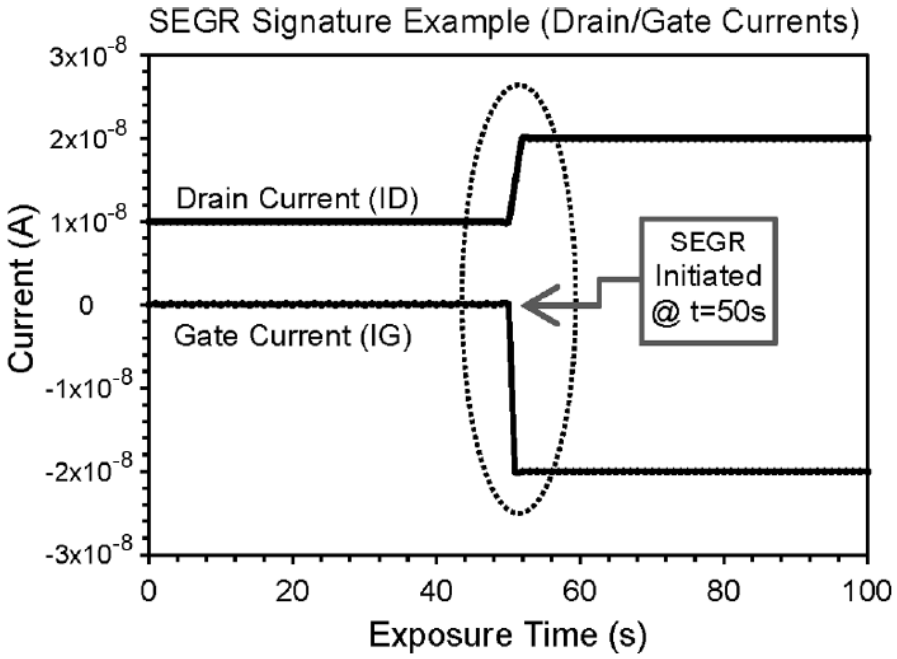


FIGURE 4.8: Evolution of drain and gate currents in a MOS experiencing SEGR during heavy-ion exposure [121].

Although the physics behind SEGR has not yet been completely elucidated, three components have been identified:

- The **capacitor** SEGR response (or dielectric SEGR response) corresponds to a temporary lowering of the breakdown voltage during the ion strike, down to a critical voltage Vcrit. This voltage has been shown to greatly depend on the ion atomic number [127], whereas the energy/range dependence is not relevant. Concerning angular effects, the worst-case occurs with perpendicular irradiations. Finally, the effect is more pronounced as the gate thickness decreases, as illustrated in Fig. 4.9. The dielectric SEGR response can be measured by applying 0 V to the drain and increasing the gate voltage in small steps, until SEGR is observed.
- The **epitaxial** layer SEGR response can be thought of as a heavy-ion induced field distortion, which results in coupling part of the drain voltage onto the gate

oxide. There are conflicting results in the literature about the ion energy/range dependence for the epitaxial layer SEGR response. Concerning angular effects, the worst-case occurs with tilted irradiations. This component is extremely sensitive to process and design parameters (e.g. width of the neck region), different from the capacitor SEGR response. Also, there is a negligible difference in the behavior of n-type and p-type channel MOSFETs.

- The **substrate** SEGR response is usually considered of minimal importance: as there is no depletion layer inside the substrate, the heavy-ion effect on the SEGR response is negligible.

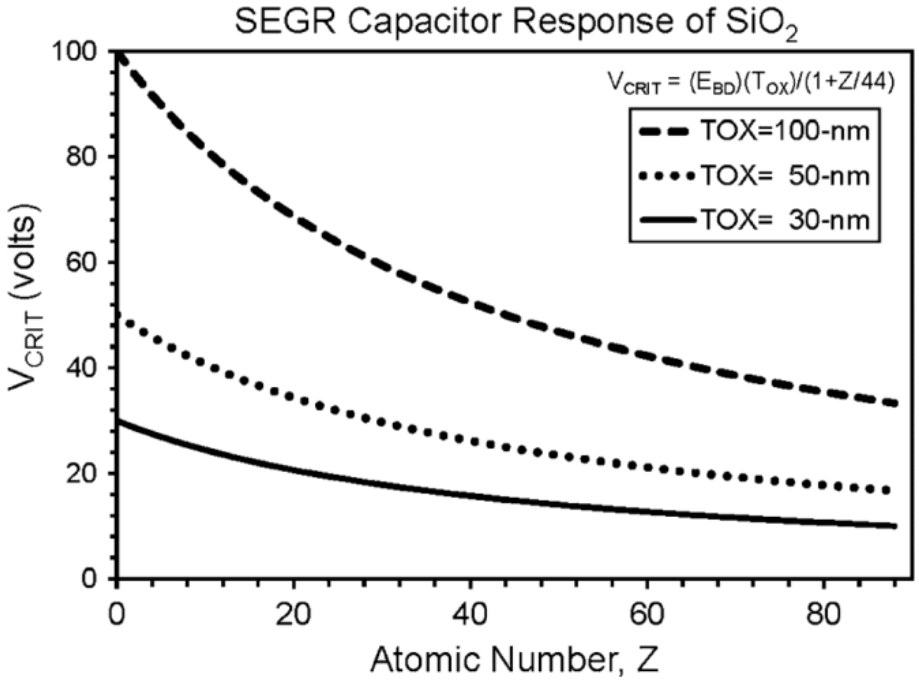


FIGURE 4.9: SEGR critical voltage versus ion atomic number, for different gate oxide thicknesses [121].

4.1.2.4 Neutron-induced single event effects in power devices

Differently from heavy ions, which are charged and can directly cause single event effects, neutrons are not charged and are the most abundant particles in the terrestrial natural radiation environment. They can only indirectly induce single event effects by generating charged secondary particles, through nuclear reactions and/or fragmentation. If the secondary particles (heavy ions) have enough mass and energy, a single event effect can occur. The data in the literature about neutron-induced single event effects in power devices are more sparse compared to heavy-ion data, but some phenomena, mainly SEB, were observed extensively also with neutrons. In general, for neutron-induced SEB a higher voltage stress is required with respect to ion-induced SEB. Neutron-induced SEGR is more rare but still possible [128]. The first evidence of SEB induced by high-energy neutrons dates back to 1996 [129]. Figure 4.10 shows the SEB cross section versus drain voltage for different power MOSFETs exposed to spallation neutrons at the Los Alamos National Laboratory WNR facility. Whereas the 200 V MOS exhibited failure only close to the full rated voltage, 400 V and 500 V ones experienced SEB at

drain voltages significantly below the full rated voltage. The observed drain current pulses were reported to be comparable to those previously observed during heavy-ion exposure. For all devices, the neutron-induced SEB threshold voltage is higher compared to the heavy-ion one. Also, as the MOSFET rated voltage increases, the neutron SEB threshold voltage was shown to get closer to the heavy-ion one.

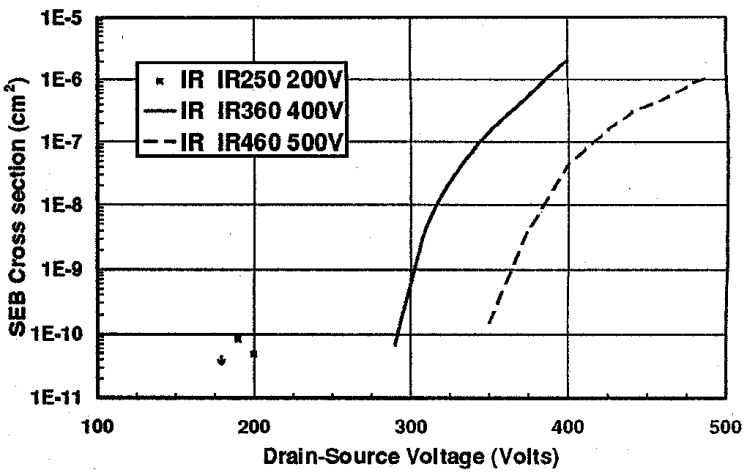


FIGURE 4.10: SEB cross section for different power MOSFETs exposed to spallation neutrons at WNR [129].

In most of the applications, MOSFETs are operated at a lower voltage with respect to their maximum breakdown voltage. For this reason, it is relevant to evaluate the failure rate as a function of the derated voltage. as illustrated in Fig. 4.11 [130]. Again, different power MOSFETs were subject to accelerated tests at the WNR spallation neutrons facility, and their SEB cross section is plotted versus the breakdown voltage percentage.

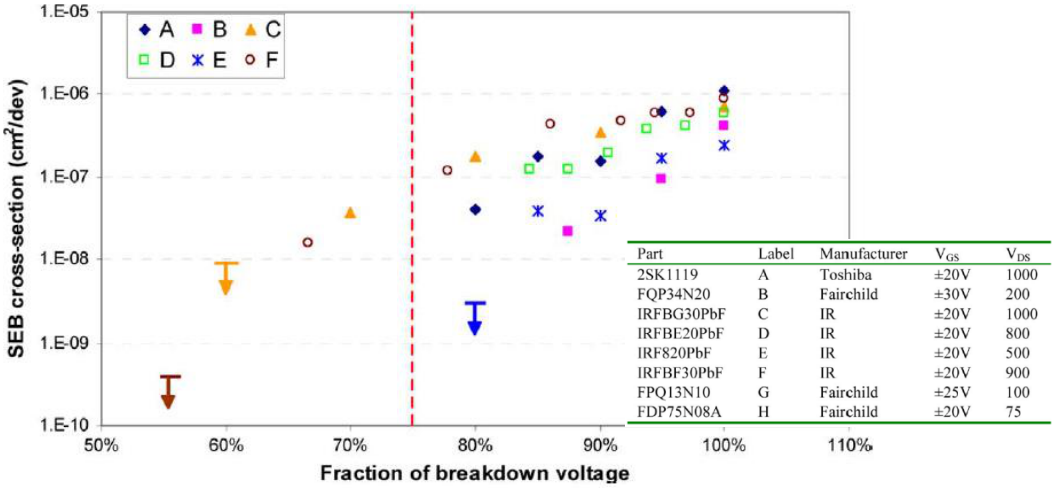
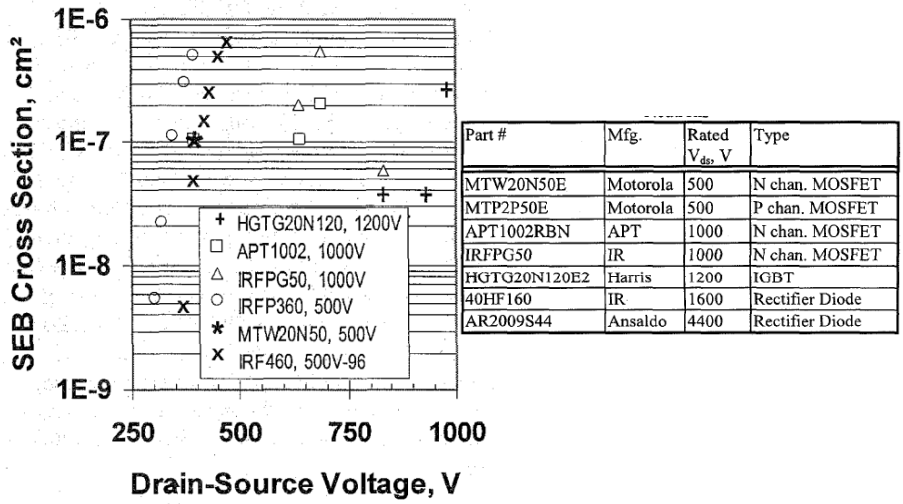


FIGURE 4.11: SEB cross section for different power MOSFETs exposed to spallation neutrons at WNR [130].

Fig. 4.11 highlights both the similarity in SEB cross-sections at maximum drain-source voltage, and the variability in the effect of derating for different high-voltage MOSFETs. As seen, for the lower voltage devices (B, E) the drop-off with respect to

breakdown voltage is more obvious than for the higher voltage devices (A, C, F). A derating factor of at least 75% has been recommended by Oberg et al. [129] and a even higher margin (50%) has been suggested for a more conservative approach [131]. The SEB cross sections for other power devices irradiated with neutrons at WNR, including high-power ones, are illustrated in Fig. 4.12.



Part #	Mfg.	Rated V_{ds}, V	Type
MTW20N50E	Motorola	500	N chan. MOSFET
MTP2P50E	Motorola	500	P chan. MOSFET
APT1002RBN	APT	1000	N chan. MOSFET
IRFPG50	IR	1000	N chan. MOSFET
HGTG20N120E2	Harris	1200	IGBT
40HF160	IR	1600	Rectifier Diode
AR2009S44	Ansaldo	4400	Rectifier Diode

FIGURE 4.12: SEB cross section for different power devices exposed to spallation neutrons at WNR [131].

If the SEB cross sections in Fig. 4.11 are translated to FIT rates in different atmospheric neutron environments, the plot in Fig. 4.13 is obtained. FITs larger than 100 were observed at sea level, depending on the device operating voltage.

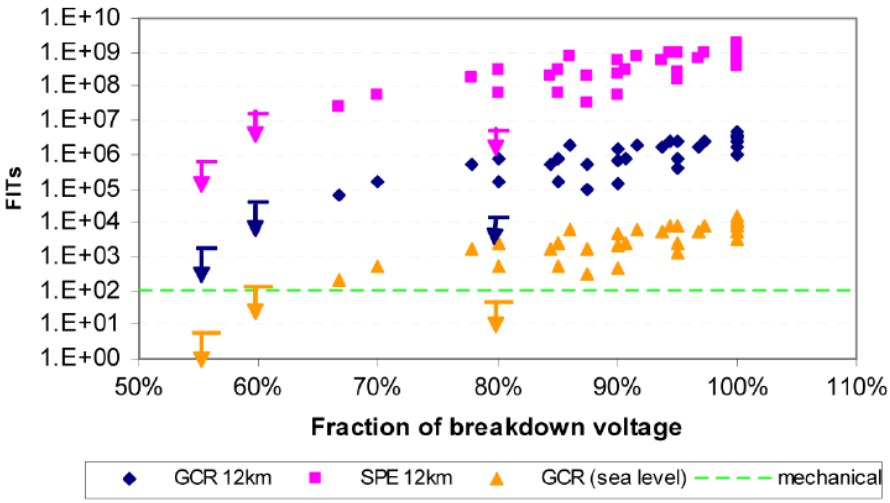


FIGURE 4.13: Failure rates in different atmospheric neutron environments, compared to a reference level of 100 FITs, typical of microelectronics mechanical fails [130].

Concerning SEB phenomena in power diodes, in the literature these events have been reported in high-voltage devices (> 1000 V). SEB at voltages as low as 67% of the maximum rating voltage were observed, hence 50% was recommended as a suitable safety margin [132].

4.2 Methodology

4.2.1 Recommended test setup to measure single event effects in power devices

Following the guidelines reported in JEDEC standard JEP151 [4], cosmic ray testing for SEE ruggedness is possible with either high energy protons or neutrons. In this case an accelerated neutron spectrum beam is selected [4, 133], and a recommended setup for SEE measurement in a power MOSFET Device Under Test (DUT) is shown in Fig. 4.14, including:

- Drain-to-source capacitor (stiffening capacitance, usually $> 250\mu F$) to minimize parasitic effects such as resistance and inductance of power cables (mandatory)
- Gate resistor–capacitor–resistor filter to protect the gate from external voltage transients (optional)
- Drain resistor to prevent permanent SEB -induced damage (optional)
- Parameter Analyzers/SMU (current limit replaces fuse)
- Transient current monitoring device (optional).

Generally, cables inductance should be minimized as it may reduce the SEB /SEGR DUT sensitivity. Also, resistance between source and ground should be avoided as it may induce device premature failure of the device, causing a voltage drop that may be reflected across the gate.

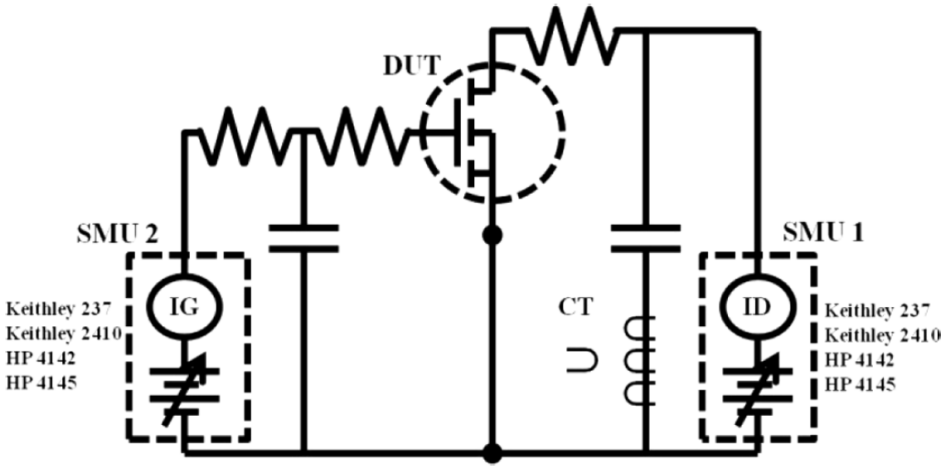


FIGURE 4.14: Example of the test setup to detect single event effects in power devices [121].

Table 4.1 shows an example of a neutron irradiation test plan, with 10 nominally identical power MOSFETs irradiated in parallel at ChipIr. With the numbers shown in Table 4.1, a fluence in the order of a few 10^8 n/cm^2 is reached in about 1 minute of exposure at the ChipIr beam, corresponding to an equivalent exposure time to the atmospheric neutrons spectrum at sea level (NYC) of about $2 \cdot 10^7$hours. The minimum observable failure rate in these conditions with a 90% confidence interval, assuming a Binomial distribution, is about 10 Failure in Time (FIT, i.e. the number of fails in 10^9 hours of operation). Of course, the actual run time (i.e. fluence) will depend on the DUT sensitivity to neutron-induced effects.

TABLE 4.1: Example of an irradiation test plan with 10 power MOSFETs exposed in parallel to accelerated neutron beam at ChipIr.

DUT n°	**Bias (V)**	**Flux** ($cm^{-2}s^{-1}$)	**Fluence** (cm^{-2})	**Exposure time (min)**	**Equivalent time at NYC (h)**
1	600	5.00+06	3.00E+08	1.00	2.31E+07
2	600	5.00+06	3.00E+08	1.00	2.31E+07
3	600	5.00+06	3.00E+08	1.00	2.31E+07
4	600	5.00+06	3.00E+08	1.00	2.31E+07
5	600	5.00+06	3.00E+08	1.00	2.31E+07
6	600	5.00+06	3.00E+08	1.00	2.31E+07
7	600	5.00+06	3.00E+08	1.00	2.31E+07
8	600	5.00+06	3.00E+08	1.00	2.31E+07
9	600	5.00+06	3.00E+08	1.00	2.31E+07
10	600	5.00+06	3.00E+08	1.00	2.31E+07

4.2.2 Irradiation facility and test setup

The accelerated neutron irradiation test campaign on power devices was performed at the ChipIr line, located at the Rutherford Appleton Laboratories (RAL, Didcot, UK). The ChipIr facility features a wide-energy neutron spectrum, which is very similar to the atmospheric one and a neutron flux accelerated by several orders of magnitude with respect to the sea-level flux (about 10^9). Further info regarding the irradiation facility are available at `https://www.isis.stfc.ac.uk/Pages/ChipIR.aspx`

Fig. 4.15 shows a picture of the ChipIr experimental chamber. The test board can be placed on movable tables that can be adjusted so that the neutron beam properly reaches the DUT. A patch panel (with USB, ethernet, RS232 connectors, SHV, etc.) below the table provides connections to the control room, where the users can safely monitor the experiment remotely. Instruments can be placed on the ground in the experimental room, outside the neutron beam. Critical and very expensive instruments can be placed in a shielded area and connected via the patch panel, as there are (few) neutrons in the experimental room, also outside of the area directly irradiated by the beam, that may damage the equipment. The size of the beam can be adjusted through the use of different collimators (e.g. 7x7 cm, 40x40 cm, ...). The neutron flux at ChipIr facility is in the order of $5 \cdot 10^6 cm^{-2}s^{-1}$. An on-line dosimetry system allows logging of the neutron fluence on the device under test once every 3 s during the irradiation run.

Due to activation issues (i.e. irradiated material becomes radioactive), the connectors that need to be touched (e.g. to change boards) should stay outside the beam area. Even though exposure times are limited, the amount of heavy metals in the beam should be reduced whenever possible. Finally, an interlock system is necessary for experiments with power devices, to ensure that when a person enters the experimental room the high voltage is removed.

4.2.3 Devices and irradiation test set-up

Two sample groups of power diodes, respectively 15 A PiN diode (type A) and a 30 A merged pin schottky (type B) and one group of 70 A n-channel power MOSFETs were tested with the accelerated neutron beam at the ChipIr line at the Rutherford Appleton Laboratories. The nominal supply voltage was 600 V for all tested devices.

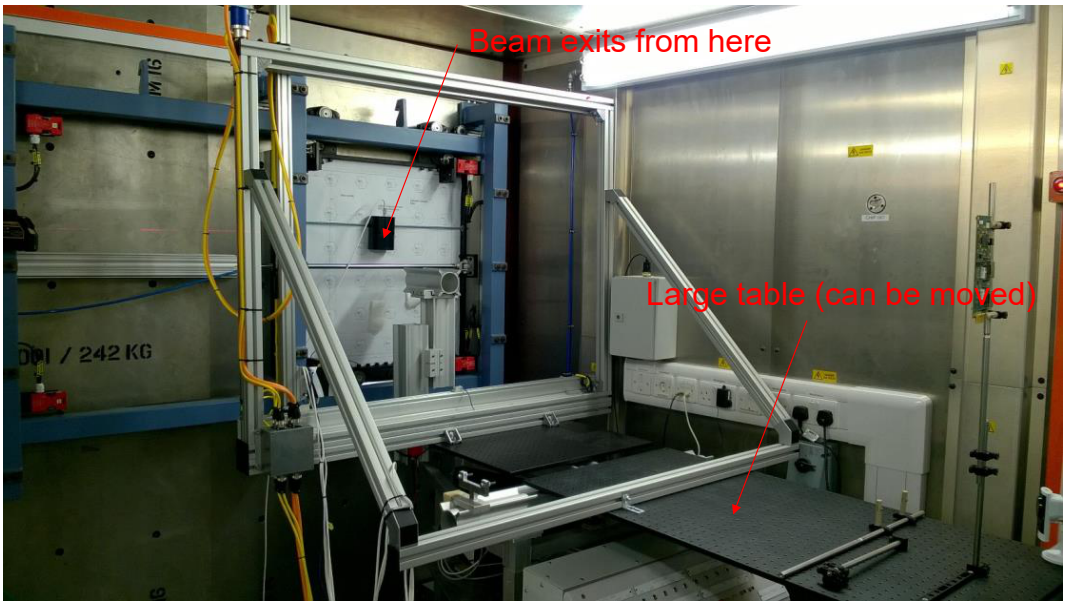


FIGURE 4.15: Picture of the experimental room for broad-energy spectrum neutron irradiation at ChipIr (RAL, UK).

Overall, 84 diodes (42 nominally identical samples for each of the two generations) and 18 MOSFETs were tested under neutron exposure. A sketch of the test set-up is depicted in Fig. 4.16. The board with the DUT was placed inside the experimental room and connected to the measurement unit (PXI) through a 40-pin flat cable. The patch panel in the experimental room was used to bring the high-voltage connections to the control room, where the power supply (EA-9750-04) was placed. The interlock system was attached to the power supply, with a key that allowed disabling the output voltage source before entering the experimental room. The power supply communicated with the control computer via Ethernet connection.

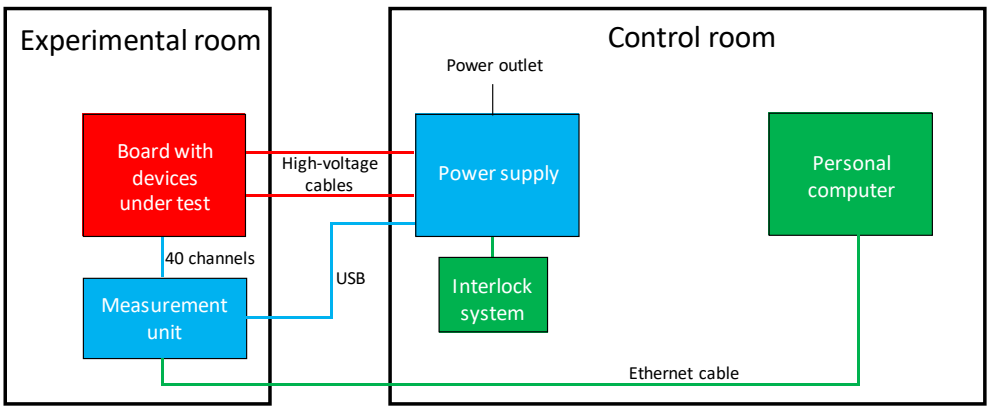


FIGURE 4.16: Sketch of the experimental set-up for accelerated neutron tests.

Three DUT boards were tested (in the following called Board #1, Board#2, and Board#3) with nominally identical devices. Each board included 14 type A diodes, 14 type B diodes, and 6 power MOSFETs. The diodes and MOSFETs were electrically connected as shown in the schematic in Fig. 4.17. The gate and source of each MOSFET were shorted together. Stiffening capacitors were placed between the source and drain of

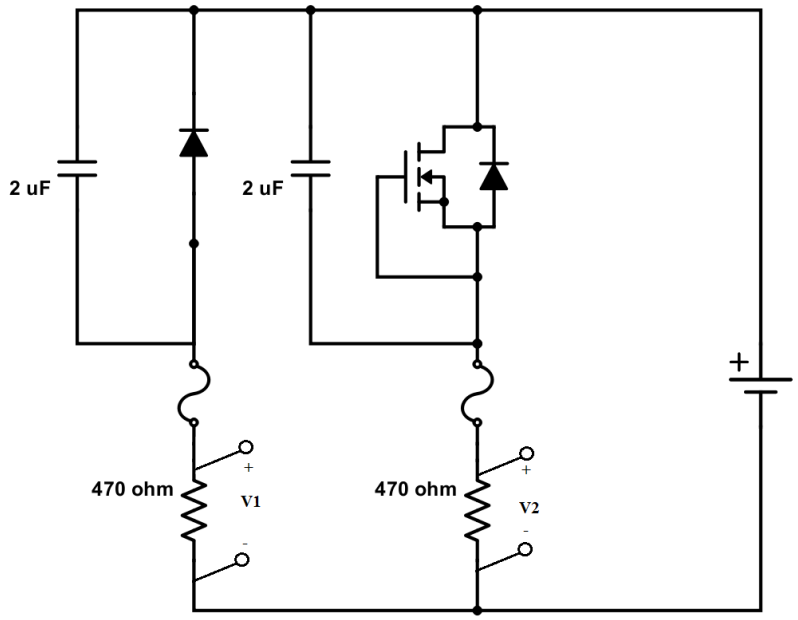


FIGURE 4.17: Schematic of the electrical connections for the devices under test (diodes and MOSFETs).

the MOSFET (or between the anode and cathode of the diodes). Shunt resistors were used to measure the current on each device (drain current or diode current). A fuse was placed in series with each DUT. A picture of the irradiation test set-up inside the experimental room is shown in Fig. 4.18. The DUT board exposed to neutron radiation is shown in Fig. 4.19.

4.2.4 Neutron irradiation runs

During each irradiation run, all the devices (diodes and MOSFETs) are biased at the same voltage level (in the range between 575 V and 675 V). The leakage current of each DUT is measured for each DUT, generally once every second (except for Run 1, where the current was measured once every 10 s), through a LabVIEW program controlling a PXI dedicated setup (the setup specifications are described in 2.3.1). A neutron-induced single event effect on a specific DUT was recorded when the corresponding current abruptly increased (and immediately afterwards dropped to zero due to the fuse). The time when the current dropped to zero (i.e. the time to failure of each DUT) was logged and related to the neutron fluence accumulated until that time. The presence of a fuse in parallel with each device under test allowed the measurement to continue until all the devices in the DUT board were non-functional. The details on all irradiation runs performed at ChipIr are described in Table 4.2. If some of the devices in the DUT board were still functional after a given run, another irradiation run on the same DUT board was carried out (sometimes at a different voltage), until all the devices in the board were not functional. The neutron fluences indicated in Table 4.2 are the total fluences accumulated in each run (devices failure times are not accounted for).

4.2.5 Neutron irradiation results

For each category of tested devices (diodes type A, diodes type B, and MOSFETs), the times to failure (hence the neutron fluences at the time of failure) were extracted at

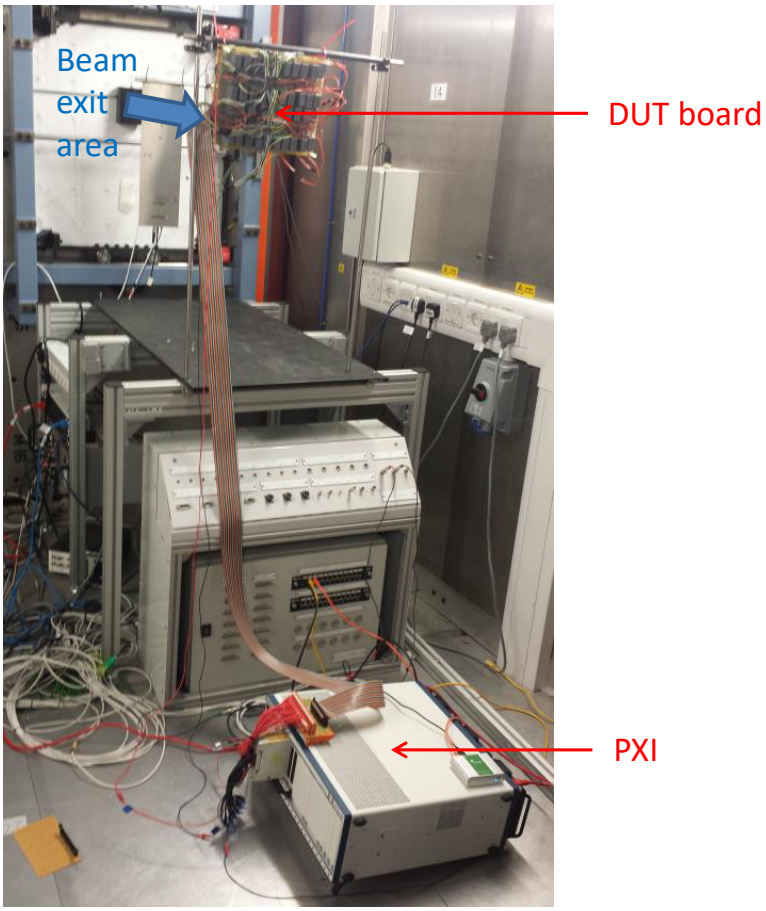


FIGURE 4.18: Picture of the accelerated neutron test set-up inside the ChipIr experimental room.

TABLE 4.2: Experimental runs performed during the neutron accelerated test campaign at ChipIr.

Test Run n°	**DUT Board ID**	**Voltage (V)**	**Neutron Fluence (n/cm-2)**	**Failed During Run**	**Functional After Run**
1	2	600	5.05E+08	MOSFETs, B diodes	A diodes
2	2	600	1.35E+10	-	A diodes
3	2	625	3.86E+09	A diodes	-
4	1	550	1.25E+10	MOSFETs, B diodes	A diodes
5	1	650	1.07E+09	A diodes	-
6	3	575	1.14E+09	MOSFETs, B diodes	A diodes
7	3	675	1.41E+08	A diodes	-

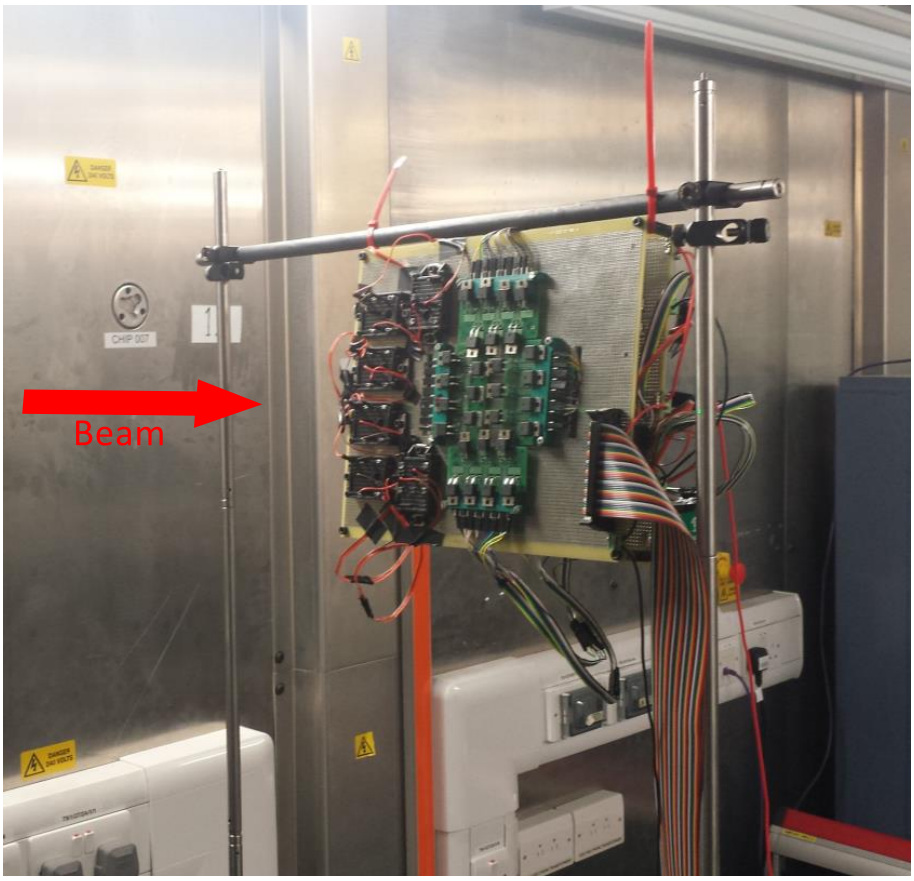


FIGURE 4.19: Picture of one of the three DUT boards exposed to the accelerated neutron beam at the ChipIr facility.

the different test voltages. It is worth to remark that the failure of one component has no impact on the functionality of the other components. After the testing campaign, electrical characterization confirmed that all failed devices exhibit a short circuit between the terminals, indicative of single event burnout. Table 4.3 shows the times to failure in accelerated conditions, observed during neutron irradiation for all the tested diodes and MOSFETs.

Nominal times to failure at NYC, the standard site for terrestrial neutron effects, have been calculated using the dosimetry data and are reported in Table 4.4 for all experimental runs and plotted in Fig. 4.20.

As shown in Fig. 4.20, there is a good repeatability of the measurements in nominally identical devices, as the failure times at each voltage are all consistent. From the nominal failure rates in Table 4.4, mean times to failure can be calculated for each tested device and for each operating voltage. If no failures were observed at a given voltage, an upper bound can be calculated for the failure rate with a given statistical confidence, based on the Binomial distribution. The mean times to failure for type A diodes, type B diodes, and MOSFETs are reported in Table 4.5 and 4.6, in units of hours and Failures In Time (FIT), i.e. number of failures in 10^9 hours at New York City (NYC). The failure rate upper bounds with a confidence of 99% in case of no recorded events are reported in Table 4.7.

Fig. 4.21 shows the experimental data for the three types of tested devices, with the failure rate (in FIT) plotted as a function of the operating voltage. Empty symbols represent upper bounds for the failure rate (when no neutron-induced events were

TABLE 4.3: Times to failure in accelerated conditions (expressed in seconds) for the diodes and MOSFETs exposed to neutron radiation.

Run n°	1	2	3	4	5	6	7
Board ID	2	2	2	1	1	3	3
Diodes A			443		89		48
			396		162		48
			709		149		47
			585		116		44
			488		115		48
			114		98		47
			154		63		47
			625		78		47
			444		58		49
			389		54		47
			379		57		48
			548		48		47
			163		59		47
Diodes B	98			1314		72	
	52			456		79	
	63			367		60	
	52			430		118	
	52			936		56	
	63			733		109	
	52			253		46	
	40			1591		71	
	40			786		71	
	63			2137		68	
	52			410		77	
	52			590		53	
	40			-		50	
	63			87		64	
MOSFET	29			33		42	
	29			33		42	
	29			33		36	
	29			30		35	
	29			30		35	
	29			30		43	
	29			37		42	
	29			37		42	
	29			37		42	
	29			37		42	
	17			44		42	
	17			45		42	

TABLE 4.4: Nominal times to failure (expressed in hours) for the diodes and MOSFETs exposed to neutron radiation in each run.

Run n°	1	2	3	4	5	6	7
Board ID	2	2	2	1	1	3	3
Diodes A			1,78E+08		3,50E+07		1,01E+07
			1,59E+08		6,57E+07		1,01E+07
			2,76E+08		5,96E+07		1,01E+07
			2,36E+08		4,64E+07		1,01E+07
			1,96E+08		4,64E+07		1,01E+07
			4,62E+07		3,92E+07		1,01E+07
			6,21E+07		2,53E+07		1,01E+07
			2,52E+08		3,12E+07		1,01E+07
			1,79E+08		2,34E+07		1,01E+07
			1,55E+08		2,22E+07		1,01E+07
			1,52E+08		2,34E+07		1,01E+07
			2,21E+08		1,95E+07		1,01E+07
			6,57E+07		2,34E+07		1,01E+07
Diodes B	3,58E+07			5,28E+08		3,14E+07	
	1,79E+07			1,88E+08		3,39E+07	
	2,26E+07			1,53E+08		2,65E+07	
	1,79E+07			1,77E+08		5,04E+07	
	1,79E+07			3,81E+08		2,39E+07	
	2,26E+07			2,98E+08		4,65E+07	
	1,79E+07			1,05E+08		2,01E+07	
	1,30E+07			6,44E+08		2,99E+07	
	1,30E+07			3,20E+08		2,99E+07	
	2,26E+07			8,67E+08		2,87E+07	
	1,79E+07			1,68E+08		3,28E+07	
	1,79E+07			2,42E+08		2,25E+07	
	1,30E+07					2,16E+07	
	2,26E+07			3,51E+07		2,75E+07	
MOSFET	7,67E+06			1,24E+07		1,86E+07	
	7,67E+06			1,24E+07		1,86E+07	
	7,67E+06			1,24E+07		1,60E+07	
	7,67E+06			1,12E+07		1,44E+07	
	7,67E+06			1,12E+07		1,44E+07	
	7,67E+06			1,12E+07		1,86E+07	
	7,67E+06			1,36E+07		1,86E+07	
	7,67E+06			1,36E+07		1,86E+07	
	7,67E+06			1,36E+07		1,86E+07	
	7,67E+06			1,36E+07		1,86E+07	
	3,35E+06			1,59E+07		1,86E+07	
	3,35E+06			1,71E+07		1,86E+07	

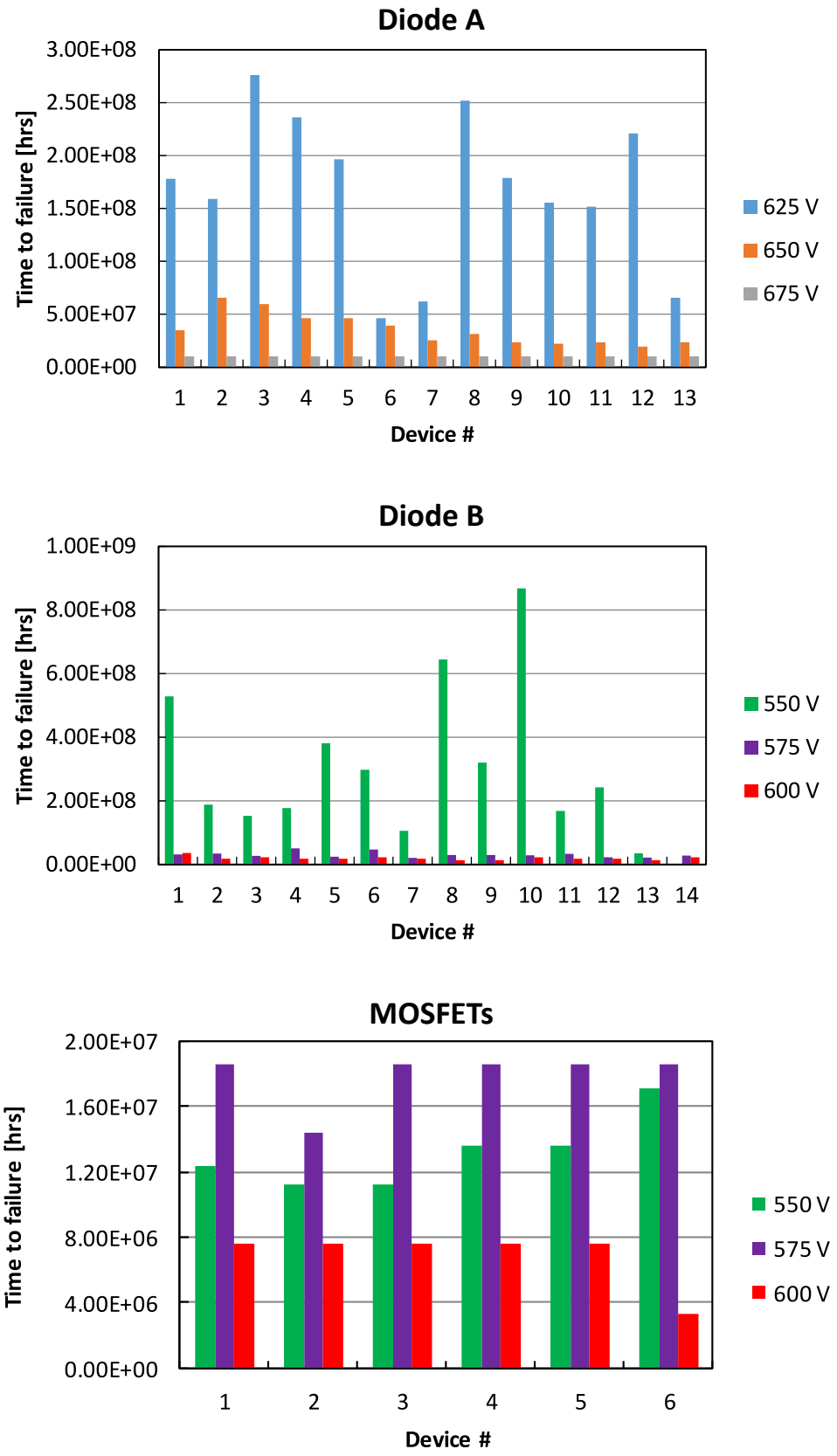


FIGURE 4.20: Time to failure for all tested type A diodes, type B diodes, and MOSFETs, at the different voltages.

TABLE 4.5: Mean time to failure at NYC (in hours) for the diodes and MOSFETs tested with neutrons.

Run n°	1	2	3	4	5	6	7
Voltage (V)	600	600	625	550	650	575	675
Diode A			1,68E+08		3,55E+07		1,01E+07
Diode B	1,94E+07			3,16E+08		3,04E+07	
MOSFET	6,95E+06			1,32E+07		1,79E+07	

TABLE 4.6: Mean time to failure at NYC (in FIT) for the diodes and MOSFETs tested with neutrons.

Run n°	1	2	3	4	5	6	7
Voltage (V)	600	600	625	550	650	575	675
Diode A			5,97		28,21	7,50	99,07
Diode B	51,42			3,17		32,87	
MOSFET	143,93			75,75		55,86	

TABLE 4.7: Upper bound (99% confidence) for mean time to failure at NYC (in FIT) for the diodes and MOSFETs tested with neutrons and not showing failures during the experimental run.

Run n°	1	2	3	4	5	6	7
Voltage (V)	600	600	625	550	650	575	675
Diode A		0,61		0,68			
Diode B							
MOSFET							

observed).

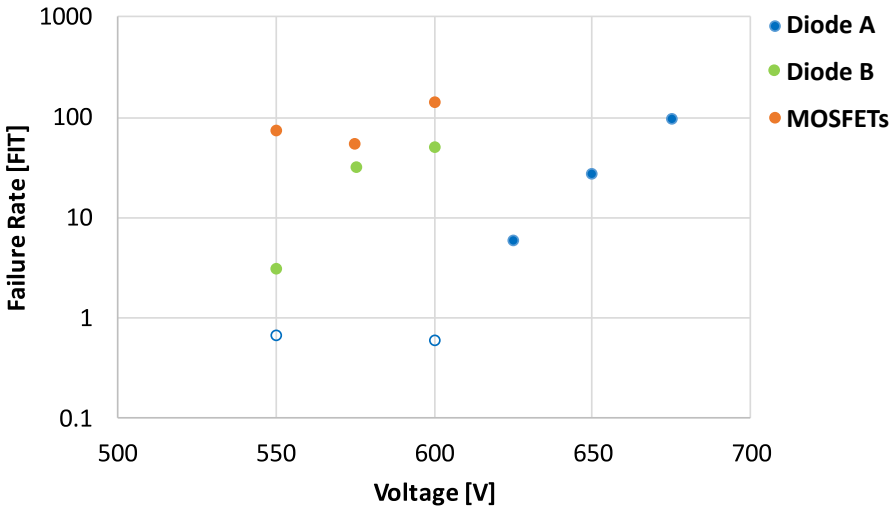


FIGURE 4.21: Failure rate (in FIT) versus operating voltage for MOSFETs, type A and type B diodes. Empty symbols represent upper bounds for the failure rate (if no events were observed).

As it has been seen, failures in type A diodes occur at a higher voltage with respect to type B diodes. Failure voltages for type A diodes are higher than 600 V (nominal voltage), whereas those for type B are lower than 600 V. The MOSFETs also fail at voltages smaller than 600V. Concerning the dependence of the failure rate on the operating voltage, for both generations of tested diodes the trend is similar to those observed in previous works [128, 129, 131, 134]. It has been reported that the best fit curve for SEB test data is an empirical curve that can be approximated to a simple power law for practical purposes [128]. For the MOSFETs, no clear trend of the failure rate with the operating voltage can be identified. Cross sections are in general agreement with previous reports, where power devices were reported to fail at voltages even well below the rated voltage [129]. The values of the failure rates in Fig. 4.21 are in line with those published in the literature after neutron irradiation [129–131].

4.3 Summary

In the first part of this chapter, a brief review of cosmic radiation effects on power devices is proposed, including the two main Single Event Effects (SEE) relative to power devices: Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR), with a particular focus on neutron-induced effects. In the methodology section a standard set-up following JEDEC guidelines ([4]) is outlined, in order to develop a dedicated test setup to monitor the failure of devices under accelerated stress at the ISIS neutron and muon source at the Rutherford Appleton Labroatory (UK). A description of the neutron irradiation facility is provided, as well as the description of test setup used for measuring the sensitivity of power devices to atmospheric neutrons. Then the results of an accelerated neutron test campaign on sample power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and diodes is reported, experimental data show a sensitivity which is in line with previously reported values for power devices under neutron exposure. In the case of MOSFETs the Failures In Time (FIT) value as a function of voltage shows an undefined trend in the investigation range, while trends on power diodes show results which are consistent with the existing scientific literature.

Part V

Conclusions

Chapter 5

Conclusions

The following doctoral thesis work has been carried out at the Polytechnic University of Turin, with an industrial scholarship offered by Vishay Intertechnology Inc. and carried out at Vishay Semiconductor Italiana S.P.A., a power semiconductor company located in Borgaro Torinese, Italy. The research work, has been focused on better understanding the effects of enhanced electrical and reliability testing conditions on state-of-the-art Power Semiconductor Devices (PSDs).

Part I gives a brief introduction on the major definitions in the field of reliability testing, focusing on the terms involved in the field of reliability which were of interest for this thesis, as well as an overview of current and possible future trends in the field.

In part II, the High Voltage Temperature Humidity Bias (HV-THB) highlights particular failure modes of power semiconductor diodes, due to the interaction of high voltage and humidity by using temperature as an acceleration factor. Given the importance of this test, the first part of the chapter proposes an overview of the existing test methodologies and approaches to HV-THB, as well as current developments in the field as an introduction to the methodology section, coming from the published review paper by the author in [2]. Secondly, in the methodology section, a dedicated system setup is successfully developed and described. The control software is customized in order perform a non-invasive analysis, by continuously monitoring the electrical evolution of the leakage current in the Devices Under Test (DUTs), while allowing automatic test stop in case of progressive degradation of the devices. Moreover, the functionalities of this system and its dedicated methodology, are then exploited to show results related to the testing of power diode modules, showing the capabilities of the test to enable significant reliability evaluation in the study of semiconductor passivation materials. This achievement is also complemented by failure analysis of the devices including Scanning Electron Microscopy (SEM) and Focused Ion Beam (FIB) characterization of the internal structures, giving remarkable insights and enabling further studies on the reliability of power semiconductor device passivations. The results coming from the studies in this chapter have been published, resulting in 2 papers from the author [1, 3].

Part III is dedicated to the the design, implementation and evaluation of a wafer-level high current Forward Voltage Drop (VF) measurement setup on a pre-existing power diode production apparatus. The initial test setup is analyzed, and a manufacturer benchmark allows to define the correct specifications for the new system. In the methodology, a set of two high current probe cards is successfully evaluated with a wide range of mechanical and electrical analyses, in order to understand the performance and limitations of the two solutions. In the second part of the methodology, a further improvement of the test setup is performed by further analyzing the possible sources of series resistance yielding high VF standard deviation. Furthermore, the high VF pattern at the edge of the wafers is then correlated to the backside vacuum contact, which is

re-designed and tested, showing a great improvement of the high current VF standard deviation, and confirming the removal of the observed high VF edge pattern.

In part IV, a brief review of cosmic radiation effects on power devices is proposed, including the two main Single Event Effects (SEE) relative to power devices: Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR), with a particular focus on neutron-induced effects. In the methodology section a standard set-up following JEDEC guidelines is described, in order to develop a dedicated test setup to monitor the failure of devices under accelerated stress at the ISIS neutron and muon source (Rutherford Appleton Labroatory, UK). A description of the neutron irradiation facility is provided, as well as the description of test setup used for measuring the sensitivity of power devices to atmospheric neutrons. The results of an accelerated neutron test campaign on sample power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and diodes are reported, and experimental data is analyzed, showing a cosmic ray sensitivity which is in line with previously reported values for both power diodes and MOSFETs under neutron exposure. In the case of MOSFETs the Failures In Time (FIT) value as a function of voltage shows an undefined trend in the investigation range, while trends on power diodes show results which are consistent with the existing scientific literature.

Bibliography

[1] D. Cimmino, R. Busca, S. Ferrero, F. Pirri, G. Richieri, and R. Carta, "High Voltage Temperature Humidity Bias Test (THB) customized system and methodologies for reliability assessment of power semiconductor devices", *Microelectronics Reliability*, vol. 100-101, p. 113 319, Sep. 2019, ISSN: 00262714. DOI: 10.1016/j.microrel.2019.06.011. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/S0026271419305268.

[2] D. Cimmino and S. Ferrero, "High-Voltage Temperature Humidity Bias Test (HV-THB): Overview of Current Test Methodologies and Reliability Performances", *Electronics*, vol. 9, no. 11, p. 1884, Nov. 2020, ISSN: 2079-9292. DOI: 10.3390/electronics9111884. [Online]. Available: https://www.mdpi.com/2079-9292/9/11/1884.

[3] R. Busca, D. Cimmino, S. Ferrero, L. Scaltrito, C. F. Pirri, G. Richieri, and R. Carta, "Multilayer film passivation for enhanced reliability of power semiconductor devices", *Journal of Vacuum Science & Technology B*, vol. 38, no. 2, p. 022 206, Mar. 2020, ISSN: 2166-2746. DOI: 10.1116/1.5121880. [Online]. Available: http://avs.scitation.org/doi/10.1116/1.5121880.

[4] JEDEC Solid State Technology Association, *Test Procedure for the Measurement of Terrestrial Cosmic Ray Induced Destructive Effects in Power Semiconductor Devices - JEP151*, 2015. [Online]. Available: https://www.jedec.org/standards-documents/docs/jep151.

[5] ZVEI Zentralverband Elektrotechnik-und Elektronikindustrie e.V., "Handbook for Robustness Validation of Automotive Electrical/Electronic Modules (2nd edition)", *ZVEI*, 2013. [Online]. Available: https://www.zvei.org/en/press-media/publications/handbook-for-robustness-validation-of-automotive-electricalelectronic-modules-2nd-edition.

[6] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, *Semiconductor Power Devices*. Cham: Springer International Publishing, 2018, ISBN: 978-3-319-70916-1. DOI: 10.1007/978-3-319-70917-8. [Online]. Available: http://link.springer.com/10.1007/978-3-319-70917-8.

[7] Wikipedia, *Reliability engineering - Wikipedia*. [Online]. Available: https://en.wikipedia.org/wiki/Reliability_engineering#cite_note-1.

[8] ECPE, "ECPE Position Paper - What Drives Power Electronics in the New Decade", *ECPE e.V./25.03.2020*, 2020. [Online]. Available: www.shorturl.at/gotJ1.

[9] A. Ghazanfari, C. Perreault, and K. Zaghib, "EV/HEV Industry Trends of Wide-bandgap Power Semiconductor Devices for Power Electronics Converters", in *2019 IEEE 28th International Symposium on Industrial Electronics (ISIE)*, vol. 2019-June, IEEE, Jun. 2019, pp. 1917–1923, ISBN: 978-1-7281-3666-0. DOI: 10.1109/ISIE.2019.8781528. [Online]. Available: https://ieeexplore.ieee.org/document/8781528/.

[10] PricewaterhouseCoopers, *Megatrends: 5 global shifts changing the way we live and do business.* 2017. [Online]. Available: https://www.pwc.co.uk/issues/megatrends.html.

[11] J. Falck, C. Felgemacher, A. Rojko, M. Liserre, and P. Zacharias, "Reliability of Power Electronic Systems: An Industry Perspective", *IEEE Industrial Electronics Magazine*, vol. 12, no. 2, pp. 24–35, 2018, ISSN: 1932-4529. DOI: 10.1109/MIE.2018.2825481. [Online]. Available: https://ieeexplore.ieee.org/document/8395338/.

[12] International Electrotechnical Commission, "IEC 60050-192:2015 International Electrotechnical Vocabulary (IEV) - Part 192: Dependability", in *IEC 60050-192:2015*, International Electrotechnical Commission, Ed., 1.0, International Electrotechnical Commission, 2015, p. 239. [Online]. Available: https://webstore.iec.ch/publication/21886.

[13] D. N. P. Murthy, M. Rausand, and T. Østerås, *Product Reliability*, 1st ed., ser. Springer Series in Reliability Engineering. London: Springer-Verlag London, 2008, pp. 55–89, ISBN: 978-1-84800-270-8. DOI: 10.1007/978-1-84800-271-5. [Online]. Available: http://link.springer.com/10.1007/978-1-84800-271-5.

[14] Wikipedia, *Failure rate - Wikipedia*. [Online]. Available: https://en.wikipedia.org/wiki/Failure_rate.

[15] D. J. Wilkins, *The Bathtub Curve and Product Failure Behavior*, 2002. [Online]. Available: https://www.weibull.com/hotwire/issue21/hottopics21.htm.

[16] K. C. Kapur and M. Pecht, *Reliability Engineering*. 2014, ISBN: 9781118841716. DOI: 10.1002/9781118841716.

[17] J. Lienig and H. Bruemmer, *Fundamentals of Electronic Systems Design*. Springer International Publishing, 2017, ISBN: 978-3-319-55839-4. DOI: 10.1007/978-3-319-55840-0. [Online]. Available: http://link.springer.com/10.1007/978-3-319-55840-0.

[18] Wikipedia, *Bathtub curve - Wikipedia*. [Online]. Available: https://en.wikipedia.org/wiki/Bathtub_curve.

[19] A. Feinberg, *Thermodynamic Degradation Science*. Chichester, UK: John Wiley & Sons, Ltd, Sep. 2016, ISBN: 9781119276258. DOI: 10.1002/9781119276258. [Online]. Available: http://doi.wiley.com/10.1002/9781119276258.

[20] U. Shipurkar, K. Ma, H. Polinder, F. Blaabjerg, and J. A. Ferreira, "A review of failure mechanisms in wind turbine generator systems", *2015 17th European Conference on Power Electronics and Applications, EPE-ECCE Europe 2015*, 2015. DOI: 10.1109/EPE.2015.7311669.

[21] Automotive Electronic Council, "Stress test qualification for automotive grade discrete semiconductors", *AEC-Q101-Rev-D1, Tech. Rep*, 2013.

[22] European Center for Power Electronics, "ECPE Guideline AQG 324 – Qualification of Power Modules for Use in Power Electronic Converter units in Motor Vehicles", in, 2nd ed., ECPE, 2019.

[23] T.-M. I. Bajenescu and M. I. Bazu, *Component reliability for electronic systems*. Artech House, 2010, p. 685.

[24] C. Pace, J. Hernandez-Ambato, L. Fragomeni, G. Consentino, A. D'Ignoti, S. Galiano, and A. Grimaldi, "A New Effective Methodology for Semiconductor Power Devices HTRB Testing", *IEEE Transactions on Industrial Electronics*, vol. 64, no. 6, pp. 4857–4865, Jun. 2017, ISSN: 0278-0046. DOI: 10.1109/TIE.2017.2669882. [Online]. Available: https://ieeexplore.ieee.org/document/7857053/.

[25] R. Rupp, R. Gerlach, A. Kabakow, R. Schorner, C. Hecht, R. Elpelt, and M. Draghici, "Avalanche behaviour and its temperature dependence of commercial SiC MPS diodes: Influence of design and voltage class", in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2014, ISBN: 9781479929177. DOI: 10.1109/ISPSD.2014.6855977.

[26] H. Yano, T. Kimoto, H. Matsunami, M. Bassler, and G. Pensl, "MOSFET performance of 4H-, 6H-, and 15R-SiC processed by dry and wet oxidation", *Materials Science Forum*, 2000, ISSN: 02555476. DOI: 10.4028/www.scientific.net/msf.338-342.1109.

[27] International Electrotechnical Commission, "IEC 60749-5 - Semiconductor devices - Mechanical and climatic test methods - Part 5: Steady-state temperature humidity bias life test", in, 2.0, International Electrotechnical Commission, 2017, p. 18. [Online]. Available: https://webstore.iec.ch/publication/27654.

[28] C. Zorn and N. Kaminski, "Temperature humidity bias (THB) testing on IGBT modules at high bias levels", in *CIPS 2014 - 8th International Conference on Integrated Power Electronics Systems, Proceedings*, 2014, ISBN: 9783800735785.

[29] N. Kaminski and C. Zorn, "Temperature-humidity-bias testing on insulated-gate bipolartransistor modules - failure modes and acceleration due to high voltage", *IET Power Electronics*, vol. 8, no. 12, pp. 2329–2335, Dec. 2015, ISSN: 1755-4535. DOI: 10.1049/iet-pel.2015.0031. [Online]. Available: https://digital-library.theiet.org/content/journals/10.1049/iet-pel.2015.0031.

[30] N. Kaminski, S. Rugen, and F. Hoffmann, "Gaining Confidence - A Review of Silicon Carbide's Reliability Status", in *2019 IEEE International Reliability Physics Symposium (IRPS)*, IEEE, Mar. 2019, pp. 1–7, ISBN: 978-1-5386-9504-3. DOI: 10.1109/IRPS.2019.8720578. [Online]. Available: https://ieeexplore.ieee.org/document/v.

[31] C. Buttay, D. Planson, B. Allard, D. Bergogne, P. Bevilacqua, C. Joubert, M. Lazar, C. Martin, H. Morel, D. Tournier, and C. Raynaud, "State of the art of high temperature power electronics", *Materials Science and Engineering: B*, vol. 176, no. 4, pp. 283–288, Mar. 2011, ISSN: 09215107. DOI: 10.1016/j.mseb.2010.10.003. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/S0921510710006136.

[32] International Electrotechnical Commission, "IEC 60749-25:2003 Semiconductor devices - Mechanical and climatic test methods - Part 25: Temperature cycling", in *IEC 60749-25:2003*, 1.0, International Electrotechnical Commission, 2003. [Online]. Available: https://webstore.iec.ch/publication/3363.

[33] J. J. Mikkelsen, "Failure Analysis on Direct Bonded Copper Substrates after Thermal Cycle in Different Mounting Conditions PC 15.5", in *Failure Analysis on Direct Bonded Copper Substrates after Thermal Cycle in Different Mounting Conditions PC 15.5*, PCIM, 2001, pp. 467–472.

[34] International Electrotechnical Commission, "IEC 60749-34:2010 Semiconductor devices - Mechanical and climatic test methods - Part 34: Power cycling", in *IEC 60749-34:2010*, International Electrotechnical Commission, Ed., 2.0, International Electrotechnical Commission, 2010, p. 21. [Online]. Available: https://webstore.iec.ch/publication/3381.

[35] U.-M. Choi, F. Blaabjerg, and S. Jorgensen, "Power Cycling Test Methods for Reliability Assessment of Power Device Modules in Respect to Temperature Stress", *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2531–2551, Mar. 2018, ISSN: 0885-8993. DOI: 10.1109/TPEL.2017.2690500. [Online]. Available: http://ieeexplore.ieee.org/document/7922584/.

[36] C. Wang, Y. He, C. Wang, L. Li, J. Li, and X. Wu, "Multi-chip parallel IGBT power module failure monitoring based on gate dynamic characteristics", in *Proceedings - 2020 5th Asia Conference on Power and Electrical Engineering, ACPEE 2020*, Institute of Electrical and Electronics Engineers Inc., Jun. 2020, pp. 1234–1238, ISBN: 9781728152813. DOI: 10.1109/ACPEE48638.2020.9136508.

[37] A. Hanif, S. Das, and F. Khan, "Active power cycling and condition monitoring of IGBT power modules using reflectometry", in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, vol. 2018-March, IEEE, Mar. 2018, pp. 2827–2833, ISBN: 9781538611807. DOI: 10.1109/APEC.2018.8341418. [Online]. Available: http://ieeexplore.ieee.org/document/8341418/.

[38] F. Gonzalez-Hernando, J. San-Sebastian, A. Garcia-Bediaga, M. Arias, F. Iannuzzo, and F. Blaabjerg, "Wear-Out Condition Monitoring of IGBT and mosfet Power Modules in Inverter Operation", *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 6184–6192, Nov. 2019, ISSN: 0093-9994. DOI: 10.1109/TIA.2019.2935985. [Online]. Available: https://ieeexplore.ieee.org/document/8805096/.

[39] C. Entzminger, W. Qiao, and L. Qu, "Case Temperature Monitoring-Based Online Condition Monitoring of SiC MOSFET Power Modules using a Radial Basis Function Network", in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, IEEE, Oct. 2020, pp. 5296–5301, ISBN: 978-1-7281-5826-6. DOI: 10.1109/ECCE44975.2020.9235653. [Online]. Available: https://ieeexplore.ieee.org/document/9235653/.

[40] X. Cheng, "Overview of Recent Progress of Semiconductor Power Devices based on Wide Bandgap Materials", *IOP Conference Series: Materials Science and Engineering*, vol. 439, no. 2, p. 022 033, Nov. 2018, ISSN: 1757-899X. DOI: 10.1088/1757-899X/439/2/022033. [Online]. Available: https://iopscience.iop.org/article/10.1088/1757-899X/439/2/022033.

[41] L. Spaziani and L. Lu, "Silicon, GaN and SiC: There's room for all: An application space overview of device considerations", in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, vol. 2018-May, IEEE, May 2018, pp. 8–11, ISBN: 978-1-5386-2927-7. DOI: 10.1109/ISPSD.2018.8393590. [Online]. Available: https://ieeexplore.ieee.org/document/8393590/.

[42] J. W. Milligan, S. Sheppard, W. Pribble, Y.-F. Wu, G. Muller, and J. W. Palmour, "SiC and GaN Wide Bandgap Device Technology Overview", in *2007 IEEE Radar Conference*, IEEE, Apr. 2007, pp. 960–964, ISBN: 1-4244-0283-2. DOI: 10.1109/RADAR.2007.374395. [Online]. Available: http://ieeexplore.ieee.org/document/4250443/.

[43] J. Hudgins, G. Simin, E. Santi, and M. Khan, "An assessment of wide bandgap semiconductors for power devices", *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 907–914, May 2003, ISSN: 0885-8993. DOI: 10.1109/TPEL.2003.810840. [Online]. Available: https://ieeexplore.ieee.org/document/1198071/.

[44] M. F. Fatahilah, K. Strempel, F. Yu, S. Vodapally, A. Waag, and H. S. Wasisto, "3D GaN nanoarchitecture for field-effect transistors", *Micro and Nano Engineering*, vol. 3, pp. 59–81, May 2019, ISSN: 25900072. DOI: 10.1016/j.mne.2019.04.001. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/S259000721930019X.

[45] L. Lorenz, "Power Semiconductor Devices-Development Trends and System Interactions", in *2007 Power Conversion Conference - Nagoya*, IEEE, Apr. 2007, pp. 348–354, ISBN: 1-4244-0843-1. DOI: 10.1109/PCCON.2007.372991. [Online]. Available: http://ieeexplore.ieee.org/document/4239181/.

[46] S. Wen, D. Huff, and Guo-Quan Lu, "Dimple-array interconnect technique for packaging power semiconductor devices and modules", in *Proceedings of the 13th International Symposium on Power Semiconductor Devices & ICs. IPSD '01 (IEEE Cat. No.01CH37216)*, Inst. Electr. Eng. Japan, 2001, pp. 69–74, ISBN: 4-88686-056-7. DOI: 10.1109/ISPSD.2001.934561. [Online]. Available: http://ieeexplore.ieee.org/document/934561/.

[47] R. Amro, J. Lutz, J. Rudzki, M. Thoben, and A. Lindemann, "Double-sided low-temperature joining technique for power cycling capability at high temperature", in *2005 European Conference on Power Electronics and Applications*, 2005, ISBN: 9075815085. DOI: 10.1109/epe.2005.219523.

[48] H. Zhang, J. Li, J. Dai, M. Corfield, X. Liu, Y. Liu, Z. Huang, and C. M. Johnson, "Improved Reliability of Planar Power Interconnect With Ceramic-Based Structure", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 175–187, Mar. 2018, ISSN: 2168-6777. DOI: 10.1109/JESTPE.2017.2758901. [Online]. Available: http://ieeexplore.ieee.org/document/8105796/.

[49] J. Schulz-Harder, K. Exel, A. Meyer, T. Licht, and M. Loddenkötter, "Micro channel water cooled power modules", in *Proc. PCIM Power Conversion Intelligent Motion Power Quality Conference. Nuremberg*, 2000.

[50] E. Schulze, C. Mertens, and A. Lindemann, "Pure Low Temperature Joining Technique power module for automotive production needs", in *2010 6th International Conference on Integrated Power Electronics Systems, CIPS 2010*, 2011, ISBN: 9781612848143. [Online]. Available: https://ieeexplore.ieee.org/document/5730659?arnumber=5730659.

[51] Z. Zhang, C. Chen, Y. Yang, H. Zhang, D. Kim, T. Sugahara, S. Nagao, and K. Suganuma, "Low-temperature and pressureless sinter joining of Cu with micron/submicron Ag particle paste in air", *Journal of Alloys and Compounds*, vol. 780, pp. 435–442, Apr. 2019, ISSN: 09258388. DOI: 10.1016/j.jallcom.

2018.11.251. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/S0925838818343834.

[52] J. A. P. Lopes, A. G. Madureira, M. Matos, R. J. Bessa, V. Monteiro, J. L. Afonso, S. F. Santos, J. P. S. Catalão, C. H. Antunes, and P. Magalhães, "The future of power systems: Challenges, trends, and upcoming paradigms", *WIREs Energy and Environment*, vol. 9, no. 3, May 2020, ISSN: 2041-8396. DOI: 10.1002/wene.368. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/wene.368.

[53] B. C. Papadopoulos, M. Rahimo, C. Corvasce, D. Schneider, R. Jabrany, N. Shin, K. Ruef, C. Widmer, G. Pâques, C. Papadopoulos, M. Rahimo, C. Corvasce, D. Schneider, R. Jabrany, N. Shin, K. Ruef, C. Widmer, G. Pâques, M. Amongero, C. Toker-Bieri, P. Strasser, R. Schnell, B. C. Papadopoulos, M. Rahimo, C. Corvasce, D. Schneider, R. Jabrany, N. Shin, K. Ruef, C. Widmer, and G. Pâques, "High Humidity Robustness of ABB ' s IGBTs and Diodes", *Bodo´s Power Systems*, no. May, p. 2, 2017. [Online]. Available: https://search.abb.com/library/Download.aspx?DocumentID=bp-05-2017&LanguageCode=en&DocumentPartId=&Action=Launch.

[54] C. Zorn, M. Piton, and N. Kaminski, "Impact of humidity on railway converters", *PCIM Europe 2017 - International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, no. May, pp. 16–18, 2017. DOI: 10.1109/SBMicro.2017.7990763.

[55] C. Papadopoulos, B. Boksteen, G. Paques, and C. Corvasce, "Humidity Robustness of IGBT Guard Ring Termination", in *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2019, pp. 1–8.

[56] C. Zorn and N. Kaminski, "Acceleration of temperature humidity bias (THB) testing on IGBT modules by high bias levels", in *2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, vol. 2015-June, IEEE, May 2015, pp. 385–388, ISBN: 978-1-4799-6259-4. DOI: 10.1109/ISPSD.2015.7123470. [Online]. Available: http://ieeexplore.ieee.org/document/7123470/.

[57] International Electrotechnical Commission, "IEC 60068-2-67:1995+AMD1:2019 - Environmental testing - Part 2-67: Tests - Test Cy: Damp heat, steady state, accelerated test primarily intended for components", in, 1.1, International Electrotechnical Commission, 2019, p. 40. [Online]. Available: https://webstore.iec.ch/publication/65410.

[58] D. Stroehle, "Influence of the Chip Temperature on the Moisture Induced Failure Rate of Plastic Encapsulated Devices", *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 6, no. 4, pp. 537–543, Dec. 1983, ISSN: 0148-6411. DOI: 10.1109/TCHMT.1983.1136209. [Online]. Available: http://ieeexplore.ieee.org/document/1136209/.

[59] M. Hanf, C. Zorn, N. Kaminski, M. Domeij, F. Allerstam, B. Buon, J. Franchi, and T. Neyer, "H3TRB test on 1.2 kv sic mosfets", *PCIM Europe Conference Proceedings*, no. 225809, pp. 1506–1511, 2018, ISSN: 21913358.

[60] J. Jormanainen, E. Mengotti, T. Batista, E. Bianda, D. Baumann, T. Friedli, A. Heineman, A. Vulli, and J. Ingman, "High humidity, high temperature and high voltage reverse bias-a relevant test for industrial applications", *PCIM Europe Conference Proceedings*, no. 225809, pp. 563–569, 2018, ISSN: 21913358.

[61] S. Kremp and O. Schilling, "Humidity robustness for high voltage power modules: Limiting mechanisms and improvement of lifetime", *Microelectronics Reliability*, vol. 88-90, no. June, pp. 447–452, 2018, ISSN: 00262714. DOI: 10.1016/j.microrel.2018.06.043. [Online]. Available: https://doi.org/10.1016/j.microrel.2018.06.043.

[62] H. T. Deng, J. L. Meng, D. B. Wang, and W. Zhang, "Breakdown voltage impact on lifetime of 1200V IGBT modules under H3TRB-HVDC testing", in *Proceedings of the International Symposium on the Physical and Failure Analysis of Integrated Circuits, IPFA*, IEEE, Jul. 2019, pp. 1–4, ISBN: 9781728135526. DOI: 10.1109/IPFA47161.2019.8984824. [Online]. Available: https://ieeexplore.ieee.org/document/8984824/.

[63] C. Papadopoulos, C. Corvasce, A. Kopta, D. Schneider, G. Pâques, and M. Rahimo, "The influence of humidity on the high voltage blocking reliability of power IGBT modules and means of protection", *Microelectronics Reliability*, vol. 88-90, no. June, pp. 470–475, 2018, ISSN: 00262714. DOI: 10.1016/j.microrel.2018.07.130. [Online]. Available: https://doi.org/10.1016/j.microrel.2018.07.130.

[64] D.-P. Sadik, J.-K. Lim, F. Giezendanner, P. Ranstad, and H.-P. Nee, "Humidity testing of SiC power MOSFETs — An update", in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, IEEE, Sep. 2017, P.1–P.8, ISBN: 978-90-75815-27-6. DOI: 10.23919/EPE17ECCEEurope.2017.8099061. [Online]. Available: http://ieeexplore.ieee.org/document/8099061/.

[65] G. DiGiacomo, "Metal Migration (Ag, Cu, Pb) in Encapsulated Modules and Time-to-Fail Model as a Function of the Environment and Package Properties", in *20th International Reliability Physics Symposium*, vol. 23, IEEE, Mar. 1982, pp. 27–33. DOI: 10.1109/IRPS.1982.363018. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/0026271483912088%20http://ieeexplore.ieee.org/document/4208420/.

[66] E. Bumiller and C. Hillman, "A review of models for time-to-failure due to metallic migration mechanisms", in *White paper issued by DfR Solutions*, 2009. [Online]. Available: https://www.dfrsolutions.com/hubfs/Resources/services/Review-of-Models-for-Time-to-Failure-Due-to-Metallic-Migration-Mechanisms.pdf.

[67] M. Paunovic and M. Schlesinger, *Fundamentals of Electrochemical Deposition*, 2nd. Hoboken, NJ, USA: John Wiley & Sons, Inc., Jul. 2005, ISBN: 9780470009406. DOI: 10.1002/0470009403. [Online]. Available: http://doi.wiley.com/10.1002/0470009403.

[68] IPC, "IPC-9201 Surface Insulation Resistance Handbook", in, Northbrook, IL: IPC, 1996. [Online]. Available: https://www.ipc.org/toc/ipc-9201.pdf.

[69] A. Hornung, "Diffusion of silver in borosilicate glass", in *Proceedings Electronic Components Conference*, 1968, p. 250.

[70] D. S. Peck, "Comprehensive model for humidity testing correlation", in *24th International Reliability Physics Symposium*, 1986, pp. 44–50.

[71] Ö. Hallberg and D. S. Peck, "Recent humidity accelerations, a base for testing standards", *Quality and Reliability Engineering International*, vol. 7, no. 3, pp. 169–180, May 1991, ISSN: 07488017. DOI: 10.1002/qre.4680070308. [Online]. Available: http://doi.wiley.com/10.1002/qre.4680070308.

[72] M. Pecht, A. Shukla, N. Kelkar, and J. Pecht, "Criteria for the assessment of reliability models", *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B*, vol. 20, no. 3, pp. 229–234, 1997, ISSN: 10709894. DOI: 10.1109/96.618221. [Online]. Available: http://ieeexplore.ieee.org/document/618221/.

[73] C. Shirley and C. Hong, "Optimal acceleration of cyclic THB tests for plastic-packaged devices", in *29th Annual Proceedings Reliability Physics 1991*, IEEE, 1991, pp. 12–21, ISBN: 0-87942-680-2. DOI: 10.1109/RELPHY.1991.145981. [Online]. Available: http://ieeexplore.ieee.org/document/145981/.

[74] J. H. Kim and S.-D. Park, "Acceleration of applied voltage on metallic ion migration of wires in NTC thermistor temperature sensors", *Engineering Failure Analysis*, vol. 28, pp. 252–263, Mar. 2013, ISSN: 13506307. DOI: 10.1016/j.engfailanal.2012.10.019. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/S1350630712002373.

[75] J. Osenbach and T. Evanosky, "Temperature-humidity-bias-behavior and acceleration model for InP planar PIN photodiodes", *Journal of Lightwave Technology*, vol. 14, no. 8, pp. 1865–1881, 1996, ISSN: 07338724. DOI: 10.1109/50.532025. [Online]. Available: http://ieeexplore.ieee.org/document/532025/.

[76] S. Yang and A. Christou, "Failure Model for Silver Electrochemical Migration", *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 1, pp. 188–196, Mar. 2007, ISSN: 1530-4388. DOI: 10.1109/TDMR.2007.891531. [Online]. Available: http://ieeexplore.ieee.org/document/4271511/.

[77] G. T. Kohman, H. W. Hermance, and G. H. Downes, "Silver Migration in Electrical Insulation", *Bell System Technical Journal*, 1955, ISSN: 15387305. DOI: 10.1002/j.1538-7305.1955.tb03793.x.

[78] S. C. Kolesar, "Principles of Corrosion", in *12th International Reliability Physics Symposium*, IEEE, Apr. 1974, pp. 155–167. DOI: 10.1109/IRPS.1974.362642. [Online]. Available: http://ieeexplore.ieee.org/document/4208020/.

[79] W. M. Paulson and R. P. Lorigan, "The Effect of Impurities on the Corrosion of Aluminum Metallization", in *14th International Reliability Physics Symposium*, IEEE, Apr. 1976, pp. 42–47. DOI: 10.1109/IRPS.1976.362720. [Online]. Available: http://ieeexplore.ieee.org/document/4208104/.

[80] M. Pecht, "A Model for Moisture Induced Corrosion Failures in Microelectronic Packages", *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, 1990, ISSN: 01486411. DOI: 10.1109/33.56172.

[81] R. B. Comizzoli, R. P. Frankenthal, P. C. Milner, and J. D. Sinclair, "Corrosion of electronic materials and devices", *Science*, vol. 234, no. 4774, pp. 340–345, 1986.

[82] G. S. Frankel, "Pitting Corrosion of Metals A Review of the Critical Factors", *Journal of the Electrochemical Society*, 1998. DOI: 10.1149/1.1838615.

[83] S. I. Pyun and S. M. Moon, "Corrosion mechanism of pure aluminium in aqueous alkaline solution", *Journal of Solid State Electrochemistry*, 2000, ISSN: 14328488. DOI: 10.1007/s100080050203.

[84] F. G. Will, K. H. Janora, J. G. McMullen, and A. J. Yerman, "Corrosion of Aluminum Metallization Through Flawed Polymer Passivation Layers; In-Situ Microscopy", in *25th International Reliability Physics Symposium*, IEEE, Apr. 1987, pp. 34–41. DOI: 10.1109/IRPS.1987.362152. [Online]. Available: http://ieeexplore.ieee.org/document/4208686/.

[85] M. Iannuzzi, "Reliability and Failure Mechanisms of Nonhermetic Aluminum SIC's: Literature Review and Bias Humidity Performance", *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 6, no. 2, pp. 181–190, Jun. 1983, ISSN: 0148-6411. DOI: 10.1109/TCHMT.1983.1136166. [Online]. Available: http://ieeexplore.ieee.org/document/1136166/.

[86] D. Peck and C. Zierdt, "The reliability of semiconductor devices in the bell system", *Proceedings of the IEEE*, vol. 62, no. 2, pp. 185–211, 1974, ISSN: 0018-9219. DOI: 10.1109/PROC.1974.9408. [Online]. Available: http://ieeexplore.ieee.org/document/1451338/.

[87] K. Li, L. Coulbeck, D. Li, M. Birkett, H. Luo, H. Li, Y. Wang, X. Dai, and G. Liu, "Reliability considerations of high power IGBT modules under high temperature/humidity/bias (HTHB) condition", in *PCIM Europe Conference Proceedings*, 2019, pp. 1052–1056, ISBN: 9783800749386.

[88] U. Grossner, A. Mihaila, and U. Vemulapati, "Passivation in High-Power Si Devices - An Overview", *ECS Transactions*, vol. 50, no. 3, pp. 267–277, Mar. 2013, ISSN: 1938-6737. DOI: 10.1149/05003.0267ecst. [Online]. Available: https://iopscience.iop.org/article/10.1149/05003.0267ecst.

[89] H. Matsushima, R. Yamada, and A. Shima, "Two Mechanisms of Charge Accumulation in Edge Termination of 4H-SiC Diodes Caused by High-Temperature Bias Stress and High-Temperature and High-Humidity Bias Stress", *IEEE Transactions on Electron Devices*, 2018, ISSN: 00189383. DOI: 10.1109/TED.2018.2845376.

[90] Q. Qian, Y. Liu, S. Irving, and T. Luk, "Analysis of the impact of polyimide coating on passivation reliability by simulation", *Proceedings - Electronic Components and Technology Conference*, pp. 264–268, 2007, ISSN: 05695503. DOI: 10.1109/ECTC.2007.373807.

[91] M. Rahimo, F. Richter, F. Fischer, U. Vemulapati, A. Kopta, C. Corvasce, S. Geissmann, M. Bellini, M. Bayer, and F. Bauer, "The impact on power semiconductor device operation due to local electric field alterations in the planar junction termination", *Microelectronics Reliability*, vol. 58, pp. 51–57, 2016, ISSN: 00262714. DOI: 10.1016/j.microrel.2015.12.021. [Online]. Available: http://dx.doi.org/10.1016/j.microrel.2015.12.021.

[92] N. Tanaka, K. Ota, S. Iura, Y. Kusakabe, K. Nakamura, E. Wiesner, and E. Thal, "Robust HVIGBT module design against high humidity", in *PCIM Europe2015, Nuremberg, Germany*, 2015, pp. 368–373.

[93] H. Matsushima, R. Yamada, and A. Shima, "Suppression of charge accumulation on termination area of 4H-SiC power devices", in *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, IEEE, May 2017, pp. 347–350, ISBN: 978-4-88686-094-1. DOI: 10.23919/ISPSD.2017.7988989. [Online]. Available: http://ieeexplore.ieee.org/document/7988989/.

[94] G. Drandova, A. Pacheco, C. Della-Morrow, E. Reese, and M. Poulton, "Moisture Compliance For GaN- And GaAs-Based Products", *EE World Online*, Nov. 2018. [Online]. Available: https://www.eeworldonline.com/moisture-compliance-for-gan-and-gaas-based-products/.

[95] T. McDonald, "Meeting Industry Requirements for GaN Device Reliability", Power Sources Manufaturers Association (PSMA), Anaheim, CA., Tech. Rep., 2019, p. 28. [Online]. Available: https://www.psma.com/sites/default/files/IS11.2%20Meeting%20Industry%20Requirements%20for%20GaN%20Device%20Reliability.pdf.

[96] M. Wolborski, "Characterization of dielectric layers for passivation of 4H-SiC devices", PhD thesis, KTH, 2006.

[97] G. L. Schnable, "Passivation Coatings on Silicon Devices", *Journal of The Electrochemical Society*, vol. 122, no. 8, p. 1092, 1975, ISSN: 00134651. DOI: 10.1149/1.2134402. [Online]. Available: https://iopscience.iop.org/article/10.1149/1.2134402.

[98] M. M. Atalla, E. Tannenbaum, and E. J. Scheibner, "Stabilization of Silicon Surfaces by Thermally Grown Oxides", *Bell System Technical Journal*, vol. 38, no. 3, pp. 749–783, May 1959, ISSN: 00058580. DOI: 10.1002/j.1538-7305.1959.tb03907.x. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6767459.

[99] B. E. Deal, "The Oxidation of Silicon in Dry Oxygen, Wet Oxygen, and Steam", *Journal of The Electrochemical Society*, vol. 110, no. 6, p. 527, 1963. DOI: 10.1149/1.2425807. [Online]. Available: https://doi.org/10.1149%2F1.2425807.

[100] ——, "Measurement and control of dielectric film properties during semiconductor device processing", in *Silicon Device Processing*, NBS Special Publication, 1970, pp. 36–50.

[101] A. S. Grove, *Physics and technology of semiconductor devices*. Wiley, 1967, ISBN: 978-0-471-32998-5.

[102] E. H. Nicollian, "Surface Passivation of Semiconductors", *Journal of Vacuum Science and Technology*, vol. 8, no. 5, S39–S49, Sep. 1971, ISSN: 0022-5355. DOI: 10.1116/1.1316388. [Online]. Available: http://avs.scitation.org/doi/10.1116/1.1316388.

[103] A. G. Revesz and K. H. Zaininger, "The Si-Si02 solid-solid interface system", *RCA Rev*, vol. 29, pp. 22–76, 1968.

[104] P. L. Castro and B. E. Deal, "Low-Temperature Reduction of Fast Surface States Associated with Thermally Oxidized Silicon", *Journal of The Electrochemical Society*, vol. 118, no. 2, p. 280, 1971. DOI: 10.1149/1.2408016. [Online]. Available: https://doi.org/10.1149%2F1.2408016.

[105] F. Montillo and P. Balk, "High-Temperature Annealing of Oxidized Silicon Surfaces", *Journal of The Electrochemical Society*, vol. 118, no. 9, p. 1463, 1971. DOI: 10.1149/1.2408355. [Online]. Available: https://doi.org/10.1149%2F1.2408355.

[106] B. Swaroop, "Ambient Effect On Ionic Charges in Dielectric Films", *IEEE Transactions on Parts, Hybrids, and Packaging*, vol. 9, no. 4, pp. 234–236, Dec. 1973, ISSN: 0361-1000. DOI: 10.1109/TPHP.1973.1136741. [Online]. Available: http://ieeexplore.ieee.org/document/1136741/.

[107] Y. T. Yeow, J. W. Clancy, and D. R. Lamb, "The influence of phosphosilicate glass deposition conditions on the surface state charge at the silicon-silicon dioxide interface!", *International Journal of Electronics*, vol. 34, no. 1, pp. 115–119, Jan. 1973, ISSN: 0020-7217. DOI: 10.1080/00207217308938418. [Online]. Available: http://www.tandfonline.com/doi/abs/10.1080/00207217308938418.

[108] J. W. Osenbach, "Water-Induced Corrosion of Materials Used for Semiconductor Passivation", *Journal of The Electrochemical Society*, vol. 140, no. 12, p. 3667, 1993, ISSN: 00134651. DOI: 10.1149/1.2221147. [Online]. Available: https://doi.org/10.1149%2F1.2221147%20https://iopscience.iop.org/article/10.1149/1.2221147.

[109] H. Matsushima, H. Okino, K. Mochizuki, and R. Yamada, "Analyzing charge distribution in the termination area of 4H-SiC diodes by measuring depletion-layer capacitance", *Japanese Journal of Applied Physics*, vol. 55, no. 4S, 04ER17, Apr. 2016, ISSN: 0021-4922. DOI: 10.7567/JJAP.55.04ER17. [Online]. Available: https://iopscience.iop.org/article/10.7567/JJAP.55.04ER17.

[110] ——, "The Impact of Interface Charge on the Breakdown Voltage of Terminated 4H-SiC Power Devices", *Materials Science Forum*, vol. 821-823, pp. 652–655, Jun. 2015, ISSN: 1662-9752. DOI: 10.4028/www.scientific.net/MSF.821-823.652. [Online]. Available: https://www.scientific.net/MSF.821-823.652.

[111] C. Zorn, F. Hoffmann, M. Hanf, N. Kaminski, F. Allerstam, A. Konstantinov, and T. Neyer, "H3TRB Test on 650 V SiC JBS Diodes", *Materials Science Forum*, vol. 924, pp. 581–584, Jun. 2018, ISSN: 1662-9752. DOI: 10.4028/www.scientific.net/MSF.924.581. [Online]. Available: https://www.scientific.net/MSF.924.581.

[112] H. Z. Wang, D. Y. Leung, M. K. Leung, and M. Ni, *A review on hydrogen production using aluminum and aluminum alloys*, May 2009. DOI: 10.1016/j.rser.2008.02.009.

[113] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. Cham: Springer International Publishing, 2019, ISBN: 978-3-319-93987-2. DOI: 10.1007/978-3-319-93988-9. [Online]. Available: http://link.springer.com/10.1007/978-3-319-93988-9%20https://link.springer.com/book/10.1007/978-3-319-93988-9.

[114] M. Lapka, "CMS Knowledge Transfer : Cosmic rays", *CMS Collection*, 2017. [Online]. Available: https://cds.cern.ch/record/2278189.

[115] Wikipedia, *Oh-My-God particle - Wikipedia*. [Online]. Available: https://en.wikipedia.org/wiki/Oh-My-God_particle.

[116] E. Normand, "Correlation of inflight neutron dosimeter and SEU measurements with atmospheric neutron model", in *IEEE Transactions on Nuclear Science*, 2001. DOI: 10.1109/23.983162.

[117] "IEC 62396-1:2016 - Process management for avionics - Atmospheric radiation effects - Part 1: Accommodation of atmospheric radiation effects via single event effects within avionics electronic equipment", in *IEC 62396-1:2016*, International Electrotechnical Commission, Ed., 2.0, International Electrotechnical Commission, 2016, p. 104. [Online]. Available: https://webstore.iec.ch/publication/24053.

[118] E. Dashdondog, S. Harada, Y. Shiba, and I. Omura, "Failure rate calculation method for high power devices in space applications at low earth orbit", *Microelectronics Reliability*, 2016, ISSN: 00262714. DOI: 10.1016/j.microrel.2016.07.114.

[119] H. Kabza, H.-J. Schulze, Y. Gerstenmaier, P. Voss, J. Schmid, F. Pfirsch, and K. Platzoder, "Cosmic radiation as a cause for power device failure and possible countermeasures", in *Proceedings of the 6th International Symposium on Power Semiconductor Devices and Ics*, Hartung-Gorre Verlag, 1994, pp. 9–12, ISBN: 3-89191-784-8. DOI: 10.1109/ISPSD.1994.583620. [Online]. Available: http://ieeexplore.ieee.org/document/583620/.

[120] A. Albadri, R. Schrimpf, D. Walker, and S. Mahajan, "Coupled electro-thermal Simulations of single event burnout in power diodes", *IEEE Transactions on Nuclear Science*, vol. 52, no. 6, pp. 2194–2199, Dec. 2005, ISSN: 0018-9499. DOI: 10.1109/TNS.2005.860691. [Online]. Available: http://ieeexplore.ieee.org/document/1589182/.

[121] J. L. Titus, "An updated perspective of single event gate rupture and single event burnout in power MOSFETs", *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1912–1928, 2013, ISSN: 00189499. DOI: 10.1109/TNS.2013.2252194.

[122] D. L. Oberg and J. L. Wert, "First nondestructive measurements of power mosfet single event burnout cross sections", *IEEE Transactions on Nuclear Science*, 1987, ISSN: 15581578. DOI: 10.1109/TNS.1987.4337546.

[123] S. Liu, J. M. Lauenstein, V. Ferlet-Cavrois, R. Marec, F. Hernandez, L. Scheick, F. Bezerra, M. Muschitiello, C. Poivey, N. Sukhaseum, L. Coquelet, H. Cao, D. Carrier, M. A. Brisebois, R. Mangeret, R. Ecoffet, K. Label, M. Zafrani, and P. Sherman, "Effects of ion species on SEB failure voltage of power DMOSFET", in *IEEE Transactions on Nuclear Science*, 2011. DOI: 10.1109/TNS.2011.2172958.

[124] A. E. Waskiewicz and J. W. Groninger, "Burnout thresholds and cross section of power MOS transistors with heavy ions", ROCKWELL INTERNATIONAL ANAHEIM CA, Tech. Rep., 1990.

[125] T. F. Wrobel and D. E. Beutler, "Solutions to Heavy Ion Induced Avalanche Burnout in Power Devices", *IEEE Transactions on Nuclear Science*, 1992, ISSN: 15581578. DOI: 10.1109/23.211346.

[126] S. Liu, J. L. Titus, and M. Boden, "Effect of buffer layer on single-event burnout of power DMOSFETs", in *IEEE Transactions on Nuclear Science*, 2007. DOI: 10.1109/TNS.2007.910869.

[127] J. L. Titus, C. F. Whealley, K. M. Van Tyne, F. Krieg, D. I. Burton, and A. B. Campbell, "Effect of ion energy upon dielectric breakdown of the capacitor response in vertical power mosfets", *IEEE Transactions on Nuclear Science*, 1998, ISSN: 00189499. DOI: 10.1109/23.736490.

[128] R. Sheehy, J. Dekter, and N. Machin, "Sea level failures of power MOSFETs displaying characteristics of cosmic radiation effects", in *PESC Record - IEEE Annual Power Electronics Specialists Conference*, 2002. DOI: 10.1109/psec.2002.1023062.

[129] D. L. Oberg, L. L. Wert, E. Normand, P. P. Majewski, and S. A. Wender, "First observations of power MOSFET burnout with high energy neutrons", *IEEE Transactions on Nuclear Science*, 1996, ISSN: 00189499. DOI: 10.1109/23.556885.

[130] A. Hands, P. Morris, K. Ryden, C. Dyer, P. Truscott, A. Chugg, and S. Parker, "Single event effects in power MOSFETs due to atmospheric and thermal neutrons", in *IEEE Transactions on Nuclear Science*, 2011. DOI: 10.1109/TNS.2011.2168540.

[131] E. Normand, J. L. Wert, D. L. Oberg, and P. P. Majewski, "Neutron-induced single event burnout in high voltage electronics", *IEEE Transactions on Nuclear Science*, 1997, ISSN: 00189499. DOI: 10.1109/23.659062.

[132] R. Edwards and J. Woodhouse, "Determination of high energy neutron voltage stress margins for high voltage IGBT and diode pairs from two manufacturers using energetic particle induced charge spectroscopy, EPICS", in *IEEE Radiation Effects Data Workshop*, 2006, ISBN: 1424406382. DOI: 10.1109/REDW.2006.295488.

[133] C. Frost, *ISIS ChipIr*. [Online]. Available: https://www.isis.stfc.ac.uk/Pages/ChipIR.aspx.

[134] J. L. Titus and C. F. Wheatley, "Experimentalstudies of single-event gate rupture and burnout in vertical power MOSFET's", *IEEE Transactions on Nuclear Science*, 1996, ISSN: 00189499. DOI: 10.1109/23.490899.

This thesis was typeset using LaTeX

Layout based on:
Masters/Doctoral Thesis LaTeX Template
Version 2.1 (2/9/15)
http://www.LaTeXTemplates.com

Original authors:
Steven Gunn and Sunil Patel