A Novel Stacked Cell Layout for High Frequency Power Applications

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Ferdinando Costanzo, *Member, IEEE*, Anna Piacibello, *Member, IEEE*, Marco Pirola, *Senior Member, IEEE*, Paolo Colantonio, *Senior Member, IEEE*, Vittorio Camarchia, *Senior Member, IEEE*, Rocco Giofrè, *Senior Member, IEEE*

***Abstract*—This letter presents an innovative stacked cell, where the common source device is split in two smaller devices leading to a more compact and symmetric structure, with almost negligible parasitics associated to the transistors connection. This novel configuration is rigorously compared, for the first time, with the two classical approaches commonly adopted to physically connect the two devices. The three different layouts are fabricated in Gallium Nitride technology for high frequency power applications, and experimentally compared by means of an extensive measurement campaign performed on several loads and in different bias conditions, ranging from class AB to C. The proposed novel configuration outperforms the other two in all conditions, thanks to the advantages of adopting two smaller devices with reduced parasitics, higher gain and higher power density. These features are common to different technologies, thus making the novel topology widely applicable for the design of high frequency stacked cells.**

***Index Terms*—Gallium Nitride, Stacked Cell, Ka-Band, High Efficiency.**

I. Introduction

In the design of Monolithic Microwave Integrated Circuit (MMIC) Power Amplifiers (PAs), it is usually necessary to combine several active devices to satisfy the output power requirement [1]. The most common combination strategy is in parallel, summing up the output currents onto the external load. At circuit level, this often requires the synthesis of matching networks with very large transformation ratio, characterized by high losses and narrowband behaviour, which compromises the PA performance [2]. This is especially true for watt-level PAs and low breakdown voltage technologies, such as Silicon and Gallium Arsenide [3], where stacking Field Effect Transistors (FETs) one on top of the other proved to be a viable solution to improve the PA performance [4].

Wide bandgap semiconductor technologies, such as Gallium Nitride (GaN), can work with higher drain supply voltage, thus higher optimum impedance, with the beneficial effects of lower transformation ratio, simpler matching networks with lower losses and wider bandwidth, thus more performing PAs. However, as the operating frequency increases and thus the gate length reduces, also GaN-based FETs need lower drain supply voltage. This is even more critical in space applications, where supply voltage derating has to be applied for reliability.

A standard stacked cell (SC) employs a common source (CS) device loaded by one, or more, quasi-common gate (CG). Theoretically, it increases drain supply voltage, output impedance and gain with respect to the current summing combination, at the expense of a more complex and sensitive design optimization phase, due to the higher integration level [4], [5]. Previous studies on SCs clearly pointed out that the parasitics associated to the CS-CG connection play a key role on the performance of the cell [6], [7]. Indeed, independently of the technology, the theoretical benefits of the stacking approach can be fully exploited only if these parasitics are minimized. The simulation of an innovative configuration, named Split, has been reported in [8]. To minimize CS-CG interconnection parasitics and to obtain a symmetric and compact layout, the idea was to split the CS in two identical smaller devices, keeping constant the overall gate periphery.

This contribution experimentally compares the Split configuration with the two already known layouts, in which a CS is loaded by a CG by using a wide transmission line or an ad-hoc fork structure. The SCs are extensively characterised on different loads and in several operating classes, from class AB to C, foreseeing also a possible application in a Doherty PA [8]. Experimental results shown that the Split SC achieves higher saturated power and efficiency in all conditions, confirming that splitting the CS stage allows to realize a compact structure that outperforms those commonly adopted. The experimental verification is here performed on three SCs fabricated on a GaN-Si process with 100 nm gate length, targeting K-band applications, but the advantages of the Split SC are independent of the adopted technology, since they stem from the adoption of smaller active devices, which are generally characterized by lower parasitics and higher gain and power density in any technology.

II. Implementation of the Stacked Cells

The basic voltage summing combination (stacking) employs a CS loaded by a CG. Theoretically, as graphically depicted in Fig. 1, it presents the remarkable advantage of requiring

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F. Costanzo, P. Colantonio, and R. Giofrè are with the E.E. Dept., University of Roma Tor Vergata, Roma, Italy e-mail: giofr@ing.uniroma2.it

A. Piacibello, M. Pirola, and V. Camarchia are with the Department of Electronics and Telecommunications, Politecnico di Torino, C.so Duca degli Abruzzi, 10129 Torino, Italy. e-mail: anna.piacibello@polito.it

A. Piacibello is also with the Microwave Engineering Center for Space Applications (MECSA), Rome, Italy.

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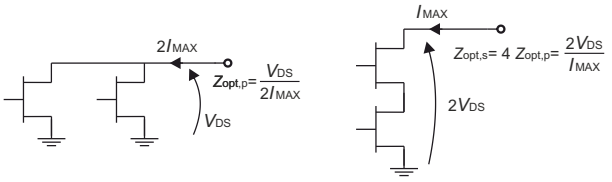


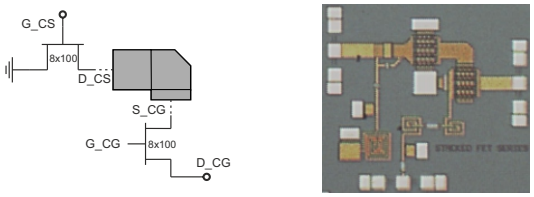
(a) Parallel combining (b) Stacking

Fig. 1. Current (a) and voltage (b) summing FET combination.

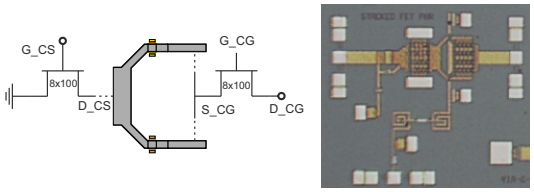
an optimum impedance that is four times higher than that of a current summing (parallel) combination having the same active periphery. Compared to the latter, a SC provides the same output power with doubled and halved voltage and current swings, respectively. Nevertheless, the design of a SC is not trivial and its power performance and stability, especially at high frequency, are heavily dependent on the CS-CG interconnection and the gate termination of the CG.

To investigate this aspect and thus to understand the link between SC layout and associated performance, we have conceived, realized and characterized three SCs having identical active periphery but different footprint. They have been designed for K-band applications ($f_0 = 18.8\,\text{GHz}$) and manufactured in a commercial 100 nm GaN-Si technology. The overall active periphery is 1.6 mm in all cases. Fig. 2(a) and Fig. 2(b) show the most commonly adopted configurations to implement a SC [6]. In Fig. 2(a) the drain of a CS device (8x100 μm periphery) is connected to the source of a CG (8x100 μm) by using a wide transmission line, hence the name Series SC. Instead in the Parallel configuration, reported in Fig. 2(b), the CS-CG connection is realized through an ad-hoc designed fork structure. However, both solutions are affected by some drawbacks that prevent the complete achievement of the theoretical advantages of a SC in a real MMIC implementation. In the Parallel topology, the fork introduces a significant resistive-inductive parasitic effect that hampers the realization of a broadband PA, especially at mm-wave. In the Series topology, this effect is partially mitigated by the low characteristic impedance of the wide transmission line. On the other hand, this introduces a significant asymmetry among the fingers of the CG, which has a negative impact on the achievable performance that becomes more severe as the frequency and number of fingers increase. Fig. 2(c) shows the scheme and layout of the innovative Split SC. In this configuration, the CS is split in two smaller devices with 4x100 μm periphery each, whereas the CG is kept unchanged. In this way the drain of each CS can be connected to the sources of the CG significantly reducing the associated parasitics, and resulting in a more compact and symmetric layout. Moreover, since smaller devices have higher gain and power density, the performance of the overall SC is improved.

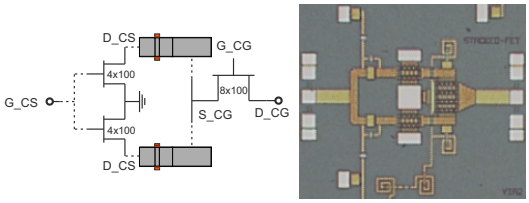
For the design of all topologies, the gate bias of the CS has been fixed to $V_{\text{G,CS}} = -1.5\,\text{V}$ (class AB, $I_{\text{D}} = 50\,\text{mA}$) and that of the CG to $V_{\text{G,CG}} = 9.5\,\text{V}$, considering an overall drain supply voltage of $V_{\text{DD}} = 22\,\text{V}$. The value of $V_{\text{G,CG}}$ is chosen in order to make the V_{GS} of the CS and CG devices identical, while achieving a symmetric division of V_{DD} between them along the whole dynamic range, and it is applied through a



(a) Series



(b) Parallel



(c) Split

Fig. 2. Schemes of the transistors' connections (left) and microscope photographies (right) of the manufactured SCs.

quarter-wavelength-like inductive network at center frequency. On the contrary, the dc bias voltage $V_{\text{G,CS}}$ of the CS and the overall drain one V_{DD} are applied by means of external bias tees through the input and output RF ports. In all the SCs, a series RC network is inserted at the gate of the CG to ensure the stability of the overall cell and to optimize its power performance. In particular, preliminary load-pull characterization campaigns have been performed on the individual CS devices to identify their optimum load at 18.8 GHz [9]. Consequently, for each SC, the CS-CG interconnection and the series RC network of the CG have been optimized simultaneously to ensure the correct loading condition to each stage, while maintaining stability. This resulted in an optimum load of the SCs ($Z_{\text{d,opt}}$) of (10+j10) Ω. Finally, in-band and low-frequency stability is enforced by means of series RC and shunt RL networks at the input of the CS stages. In the present test structures, no input and output matching networks are added, to leave additional degrees of freedom for the experimental characterization.

III. Experimental Results

The large signal characterization has been performed at center frequency on different load terminations, synthesized adopting a passive load-pull system. The source impedance is kept to 50 Ω throughout the characterization; incident input power and operating power gain are considered to ensure a fair comparison despite the possible input mismatch. Initially, the SCs have been measured on a 50 Ω load, yielding the performance reported in Fig. 3. It is clearly sub-optimum both in terms of output power and efficiency, since the adopted

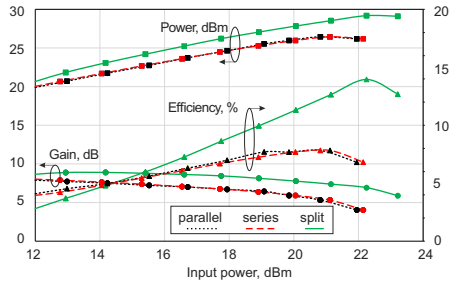


Fig. 3. Measured performance for a 50 mA class AB on 50 Ω at 18.8 GHz.

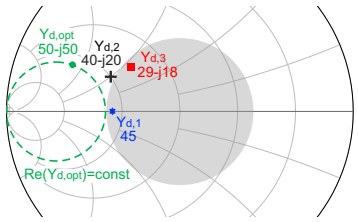
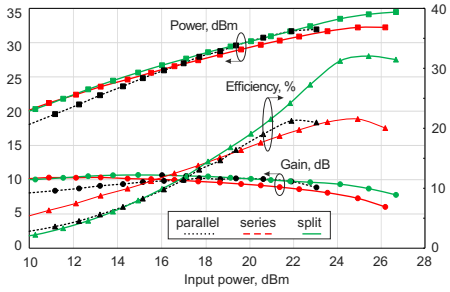


Fig. 4. Smith chart representation of the measured and optimum output terminations. Highlighted in green, the constant 50 mS conductance circle. The shaded circle represents the loads that can be synthesized with the adopted setup. Normalization impedance: 50 Ω, admittance values expressed in mS.

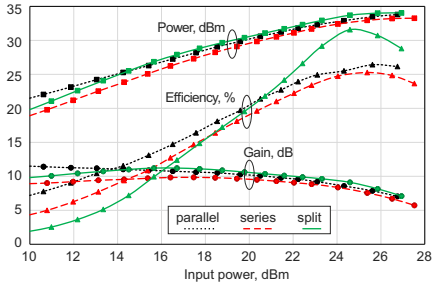
termination is far from the optimum one. However, it is already evident that the Split SC has better performance than the other two, which exhibit very similar behaviour.

The adopted setup can synthesize, in the targeted bandwidth, reflection coefficients with maximum magnitude of 0.4, therefore covering the region represented by the shaded circle in Fig. 4. For this reason, the desired optimum load determined during the design (corresponding to an admittance $Y_{\mathrm{d,opt}}$=(50-j50) mS) cannot be achieved at 18.8 GHz. Among the loads that can be synthesized, three have been selected: $Y_{\mathrm{d},1} = 45$ mS, which has a conductance as close as possible to the optimum one (highlighted in dashed green in Fig. 4) but offers no compensation of the reactive drain parasitics; $Y_{\mathrm{d},2} = (40 - j20)$ mS, which represents a trade-off between the real and imaginary parts of $Y_{\mathrm{d,opt}}$; and $Y_{\mathrm{d},3} = (29 - j18)$ mS, which is sub-optimum both in terms of real and imaginary parts. The realized SCs have been measured at 18.8 GHz in different bias points, ranging from class AB ($V_{\mathrm{G,CS}}$=-1.5 V, $I_{\mathrm{D}} = 50$ mA), to class B ($V_{\mathrm{G,CS}}$=-2 V) and finally class C ($V_{\mathrm{G,CS}}$=-3 V). The power sweeps of the SCs biased in class AB, on each of the three selected loads, are shown in Fig. 5. As already evidenced for the 50 Ω load case, the Split SC outperforms both the Parallel and Series SCs, in terms of output power and efficiency, while showing a similar power gain behaviour. The efficiency of the Split SC is from 6% (on $Y_{\mathrm{d},2}$ and $Y_{\mathrm{d},3}$) to 10% (on $Y_{\mathrm{d},1}$) higher than those of the other topologies. The measured performance exhibits the trend observed in simulation [8], with the Split outperforming the Parallel and Series configurations.

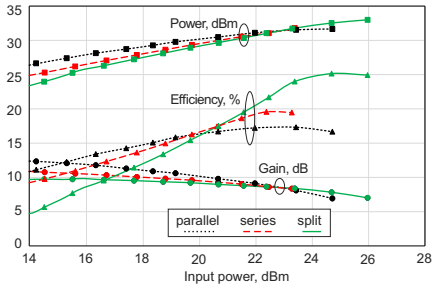
On the load providing the best trade-off ($Y_{\mathrm{d},2}$), the characterization has been performed also in the other operating classes. The resulting output power and efficiency at 3 dB gain compression are summarized in Table I. The trend evidenced



(a) on $Y_{\mathrm{d},1} = 45$ mS



(b) on $Y_{\mathrm{d},2} = (40 - j20)$ mS



(c) on $Y_{\mathrm{d},3} = (29 - j18)$ mS

Fig. 5. Measured performance of the SCs for a 50 mA class AB in different loading conditions at 18.8 GHz.

by the previous measurements is confirmed also in both class B and C bias conditions.

TABLE I
PERFORMANCE (OUTPUT POWER/EFFICIENCY AT 3 DB COMPRESSION) OF THE STACKED CELLS ON $Y_{\mathrm{d},2} = (40 - j20)$ MS AT 18.8 GHZ.

	class AB		**class B**		**class C**	
	Pout (dBm)	Eff (%)	Pout (dBm)	Eff (%)	Pout (dBm)	Eff (%)
Parallel	33.5	26.4	33.4	24.2	33.6	27.3
Series	33.2	24.8	33.3	24.4	33.3	27.1
Split	34.0	30.7	34.4	32.1	34.3	35.4

IV. CONCLUSION

This work reported the experimental verification of a novel approach to realize a high performance stacked cell for high frequency power applications. Adopting separate smaller devices, with higher gain and power density, in the common source stage enabled an easier interconnection to the common gate, with reduced parasitics, and resulted in a compact and symmetric layout. Higher performance was achieved with this strategy, which was demonstrated on a GaN-Si technology but is extendable to other MMIC technologies.

REFERENCES

[1] *Power Amplifier Design*. John Wiley Sons, Ltd, 2009, ch. 2, pp. 49–83. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/9780470746547.ch2

[2] *Power Combining*. John Wiley Sons, Ltd, 2009, ch. 10, pp. 369–434. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/9780470746547.ch10

[3] A. Piacibello, M. Pirola, V. Camarchia, C. Ramella, and R. Quaglia, "A Ku-band Compact MMIC PA based on Stacked GaAs pHEMT cells," in *2018 International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMIC)*, 2018, pp. 1–3.

[4] H. Dabag, B. Hanafi, F. Golcuk, A. Agah, J. F. Buckwalter, and P. M. Asbeck, "Analysis and Design of Stacked-FET Millimeter-Wave Power Amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1543–1556, 2013.

[5] G. van der Bent, P. de Hek, and F. E. van Vliet, "Design Procedure for Integrated Microwave GaAs Stacked-FET High-Power Amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 9, pp. 3716–3731, 2019.

[6] D. P. Nguyen and A. Pham, "An Ultra Compact Watt-Level Ka-Band Stacked-FET Power Amplifier," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 7, pp. 516–518, 2016.

[7] C. Ramella, A. Piacibello, V. Camarchia, and M. Pirola, "Electromagnetic Crosstalk Effects in a Millimeter-wave MMIC Stacked Cell," in *2020 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMiC)*, 2020, pp. 1–3.

[8] F. Costanzo, R. Giofrè, V. Camarchia, P. Colantonio, and E. Limiti, "A Ka-band Doherty Power Amplifier using an innovative Stacked-FET Cell," in *2019 15th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, 2019, pp. 165–168.

[9] R. Quaglia, A. Piacibello, F. Costanzo, R. Giofrè, M. Casbon, R. Leblanc, V. Valenta, and V. Camarchia, "Source/Load-Pull Characterisation of GaN on Si HEMTs with Data Analysis Targeting Doherty Design," in *2020 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, 2020, pp. 5–8.