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Zero Voltage Switching Condition in Class-E Inverter for Capacitive Wireless Power Transfer Applications / Corti, Fabio; Reatti, Alberto; Wu, Ya-Hui; Czarkowski, Dariusz; Musumeci, Salvatore. - In: ENERGIES. - ISSN 1996-1073. - ELETTRONICO. - 14:4(2021), pp. 1-21. [<https://doi.org/10.3390/en14040911>]

Availability:

This version is available at: 11583/2872896 since: 2021-03-02T14:49:37Z

Publisher:

MDPI

Published

DOI:<https://doi.org/10.3390/en14040911>

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Article

Zero Voltage Switching Condition in Class-E Inverter for Capacitive Wireless Power Transfer Applications

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Abstract: This paper presents a complete design methodology of a Class-E inverter for capacitive wireless power transfer (CWPT) applications, focusing on the capacitance coupling influence. The CWPT has been investigated in this paper, because most of the literature refers to inductive power transfer (IWPT). However, CWPT in perspective can result in lower cost and higher reliability than IWPT, because it does not need coils and related shields. The Class-E inverter has been selected, because it is a single switch inverter with a grounded MOSFET source terminal, and this leads to low costs and a simple control strategy. The presented design procedure ensures both zero voltage switching (ZVS) and zero derivative switching (ZDS) conditions at an optimum coupling coefficient, thus enabling a high transmission and conversion efficiency. The novelties of the proposed method are that the output power is boosted higher than in previous papers available in the literature, the inverter is operated at a high conversion efficiency, and the equivalent impedance of the capacitive wireless power transfer circuit to operate in resonance is exploited. The power and the efficiency have been increased by operating the inverter at 100 kHz so that turn-off losses, as well as losses in inductor and capacitors, are reduced. The closed-form expressions for all the Class-E inverter voltage and currents waveforms are derived, and this allows for the understanding of the effects of the coupling coefficient variations on ZVS and ZDS conditions. The analytical estimations are validated through several LTSpice simulations and experimental results. The converter circuit, used for the proposed analysis, has been designed and simulated, and a laboratory prototype has been experimentally tested. The experimental prototype can transfer 83.5 W at optimal capacitive coupling with operating at 100 kHz featuring 92.5% of the efficiency, confirming that theoretical and simulation results are in good agreement with the experimental tests.

Keywords: capacitive wireless power transfer; Class-E inverter; resonant converter; zero voltage switching

Citation: Corti, F.; Reatti, A.; Wu, Y.-H.; Czarkowski, D.; Musumeci, S. Zero Voltage Switching Condition in Class-E Inverter for Capacitive Wireless Power Transfer Applications. *Energies* **2021**, *14*, 911. <https://doi.org/10.3390/en14040911>

Academic Editor:

Pedro Roncero-Sanchez

Received: 28 December 2020

Accepted: 4 February 2021

Published: 9 February 2021

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1. Introduction

Over the last few years, wireless power transfer (WPT) has increasingly attracted industry and academia attention, and it is utilized in an increasing number of applications. One of the WPT systems main applications is that of battery charging in biomedical implants [1], electric vehicle wireless charging [2–4], mobile phone and electronic consumers [5,6], moving robots [7], and wireless sensors [8,9]. This is due to advantages introduced by this technology; some of them are as follows: WPT allows the product to be completely sealed, making it waterproof; it facilitates the charging process avoiding the use of bulky power cables; and finally, it allows the product life to be increased. By eliminating the physical limitations of connectors, like mating cycles and corrosion of contacts, wireless power transfer results in more robust products [10].

The capacitive wireless power transfer (CWPT) is a recent alternative to the more investigated inductive wireless power transfer (IWPT) [11–13]. A schematic block representation of a CWPT system is shown in Figure 1. The architecture is similar to an IWPT

system [14,15], but coupling among the primary and secondary sides is based on the electric field, rather than the magnetic field. A primary inverter impresses a high-frequency alternative voltage to the transmission circuit. An electric field-based power transfer between metallic plates without a direct electrical connection is achieved. In a wireless charging application, requiring the load to be supplied by a DC voltage, the power received from the secondary plates is rectified to supply a load. Compared to an IWPT system, a CWPT system has several advantages, such as:

- Lower cost: CWPT does not need expensive magnetic cores and Litz wires to reduce the parasitic resistance due to skin and proximity effects [15,16]. The power is transferred through low-cost metallic plates. Because of this characteristic, a CWPT also results in smaller volumes and weights than IWPT.
- Higher stability in metallic surrounding environment: metallic materials block an inductor magnetic flux transmitted between two coils. Additionally, eddy currents induced by a changing magnetic field generate heat and increase the power losses and safety concerns.
- Capability to transfer power through metal barriers thanks to the coupling capacitive effect.
- Less leakage flux leading to less electromagnetic interference (EMI): an IWPT system uses a magnetic field whose flux tends to propagate in any direction; in contrast, a CWPT system uses an electrical field that traps energy between metal plates [17,18].

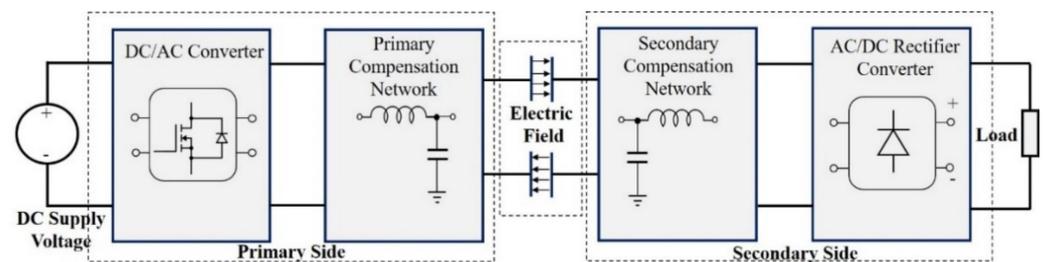


Figure 1. Block diagram of a general capacitive wireless power transfer system.

To capitalize on these advantages over IWPT, several research projects have recently started to study and improve CWPT [10].

In a CWPT system, the metal plates are electrically coupled through the air, leading to a coupling capacitance of a few picofarads. To reduce the equivalent capacitive reactance of the system, the converter must be operated at a high switching frequency, and this results in high switching losses in hard switching converters. Wide bandgap (WBG) devices represent a suitable solution to transfer a high power at a high switching frequency, but they also result in a significant cost increase and EMI problems [18].

A suitable solution to overcome these problems is constituted by the utilization of soft-switching converters, e.g., resonant converters, where LC networks are utilized to reduce switching power losses due to voltage and current crossing during the switch turn-on and turn-off. The zero voltage switching (ZVS) condition is usually referred to a voltage equal to zero across the switching devices [19] and its turn-on, and this reduces to zero the turn-on losses. In a power MOSFET, turn-on loss is due to the dissipation of the energy stored in the MOSFET output parasitic capacitance, and this energy is reduced to zero when the voltage across the capacitance is zero.

The Class E converter is appropriate for a high-frequency operation, because it can achieve ZVS, and under optimum operation, the voltage derivative is also zero. This last condition is known as the zero derivative switching (ZDS) condition, and it plays a key role to reduce EMI interference [20]. The total harmonic distortion (THD) of the output voltage is very small. For this reason, this converter is one of the best solutions for the realization of inverters with a rated power of up to a few hundred Watts. Additionally, being made up from one single MOSFET, it allows the reduction of the converter cost and dimension

and increases its reliability. Moreover, this circuit results in an easy gate drive requirement, because it is composed of a grounded single switch. In this converter, the switch ZVS turns on and high efficiencies are possible if the component values of the resonant circuit are properly chosen [21–23].

For this reason, several studies have been made to use the Class-E topology for capacitive WPT. In [24], a capacitive Class-E inverter for rotating applications has been presented. The experimental setup operates at 6.78 MHz, and it can transfer 20 W with 80% efficiency. A capacitive Class-E² DC-DC converter able to transfer 1.7 W over a distance of 5 mm with 75% efficiency operating at 1 MHz is presented in [25]. In [26], a Class-E power amplifier for capacitively coupled for biomedical implants is presented. The system can transfer 5 W with 96.34% efficiency operating at 13.56 MHz. Being designed for biomedical applications, the rated output power is limited to ensure safe operations. In [27], a Class-E capacitive power transfer with a full-wave rectifier able to transfer 3 W with 85% efficiency operating at 6.78 MHz is presented. In [28], the ZVS operation of a capacitive Class-E inverter is extended by adding or removing capacitances to operate in resonance. The experimental setup operates at 2 MHz and can transfer 360 mW. In [29], an LC capacitive Class-E inverter able to transfer 10 W operating at 1 MHz with 93.4% conversion efficiency is presented. Finally, in [30], a capacitive Class-E inverter able to transfer 9.45 W operating at 1 MHz with 98.44% efficiency is presented.

A Class-E inverter circuit is sensitive to the parameters due to the CWPT operations, e.g., at a given input voltage, the power flow strongly depends on the capacitive coupling, that is, to the distance of the plates. Some researchers have been led out to maintain the ZVS operation by a proper control methodology such as in [28], where suitable capacitors have been added to achieve ZVS despite the variations of the capacitive coupling or load conditions. To preserve ZVS operation without a control methodology approach in the case of the distance variation between the two plates of CWPT, an impedance matching circuit in the Class-E converter is needed; in [31], the variation of capacitive coupling is analyzed versus the distance of the plates, this paper investigation is derived at a constant resistive load. ZVS also depends on the load when the distance among the capacitive plates is constant [25].

This paper investigates the influence of the capacitor coupling at a constant load to determine the conditions that allow the soft-switching operations to be maintained. The analysis is based on the analytical model developed in [32,33]; several simulations have been carried out to evaluate the effects of capacitive coupling on the ZVS operative conditions. A laboratory prototype has been built and tested to validate the analysis and simulation results. The experimental Class-E inverter with single silicon super junction MOSFET features a 100 kHz switching frequency, a $V_{in} = 21$ V input voltage, and an output power rate up to $P_o = 83.5$ W with maximum efficiency of 92.5%. Furthermore, the analysis of the capacitive coupling impact in CWPT on the ZVS operation allows optimizing the converter design giving some correct guidelines for an effective project of a CWPT system with a Class-E converter.

The paper in brief is organized as follows. In Section 2, the analysis of the coupling capacitance in CWPT applications is introduced to clarify the issues focused in the paper. In Section 3 the Class-E converter is analyzed, and an optimum design procedure is carried out. In Section 4, the variation of the coupling capacitance and its impact on ZVS operation are investigated. In Section 5, simulations and experimental results are presented to show the ZVS and ZDS versus different coupling capacitance conditions at a constant load.

Finally, the processed data are discussed and linked to derive appropriate design constraints for the Class E converter in CWPT applications.

2. LC Compensated Capacitive Wireless Power Transfer System

The four-plate parallel structure, shown in Figure 2a, represents the most common solution to create air-coupled capacitors [9]. As shown in [34] and Figure 2a, plates P_1 and P_3 represent the primary side plates, while P_2 and P_4 are the secondary side plates. In

general, the coupling between the plates P_i and P_j is modeled by a capacitance C_{ij} . The couplings C_{12} and C_{34} are known as main capacitances, while C_{14} , C_{23} , C_{24} , and C_{13} are called cross-coupling capacitances. Adopting the parallel structures shown in Figure 2a and assuming that the plates P_1 and P_2 are distant enough from P_3 and P_4 the cross-coupling capacitances can be neglected, making the analysis of the circuit easier. The analysis proposed in this paper is valid for any four-plate architecture system; therefore, even the cross-coupling capacitances are taken into account. By applying the Kirchhoff voltage law (KVL) and the Kirchhoff current law (KCL) to Figure 2a, it is possible to reconfigure the six-capacitance matrix into the equivalent π -topology circuit shown in Figure 2b, where

$$C_M = \frac{C_{24}C_{13} - C_{14}C_{23}}{C_{13} + C_{14} + C_{23} + C_{24}} \tag{1}$$

$$C_A = C_{12} + \frac{(C_{13} + C_{14})(C_{23} + C_{24})}{C_{13} + C_{14} + C_{23} + C_{24}} - C_M \tag{2}$$

$$C_B = C_{34} + \frac{(C_{13} + C_{23})(C_{14} + C_{24})}{C_{13} + C_{14} + C_{23} + C_{24}} - C_M \tag{3}$$

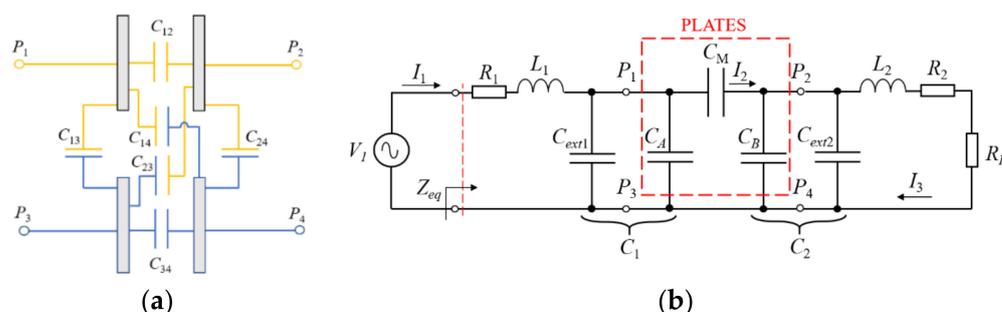


Figure 2. Parallel four plates structure. (a) Coupling capacitances. (b) Equivalent electric circuit of CWPT.

The plates being coupled through the air, the values of these capacitances usually are of few pF; thus, a high operating frequency must be used. To transfer the desired power to the load at any frequency, two external capacitances C_1 and C_2 are connected in parallel with C_A and C_B and must be designed to resonate with inductances L_1 and L_2 at an angular frequency ω_0 . The insertion of these two external capacitances produces two equivalent capacitances $C_1 = C_{ext1} + C_A$ and $C_2 = C_{ext2} + C_B$, as shown in Figure 2b. To reduce the reactive power due to the low coupling between metal plates and increase the active output power, two external inductances L_1 and L_2 must be designed; to resonate with the capacitances C_1 and C_2 , their values are derived as follows

$$L_1 = \frac{1}{\omega_0^2 C_1} \tag{4}$$

$$L_2 = \frac{1}{1 - k_c} \frac{1}{\omega_0^2 C_2} \tag{5}$$

where k_c is the coupling factor, and it is expressed as

$$k_c = \frac{C_M}{\sqrt{C_1 C_2}} \tag{6}$$

Being $C_1 \gg C_M$ and $C_2 \gg C_M$, the coupling coefficient $k_c \cong 0$.

2.1. Equivalent Impedance

The knowledge of the equivalent impedance of the CWPT is crucial to achieve ZVS. Usually, the external capacitances are higher than the cross-capacitance, thus $C_1 = C_{ext1} + C_A \cong C_{ext1}$ and $C_2 = C_{ext2} + C_B \cong C_{ext2}$. The geometry of the plates is symmetrical resulting in $R_1 = R_2 = R$, $L_1 = L_2 = L$ and $C_1 = C_2 = C$; the equivalent impedance is

$$Z_{eq} = \frac{1 + \omega^2 [\alpha(R\beta - \omega^2 L^2) - 2LC] + j\omega [(R + \beta)(C + \alpha\omega^2 L)]}{\alpha\beta\omega^2 + j\omega(C - \alpha\omega^2 L)} \quad (7)$$

where $\alpha = C_M^2 - C_1 C_2$ and $\beta = R + R_L$. The impedance $Z_{eq} = R_{eq} + j X_{eq}$ real and imaginary parts are

$$R_{eq} = \frac{\alpha\beta \{1 + \omega^2 [\alpha(R\beta - \omega^2 L^2) - 2LC]\} + [(R + \beta)(C + \omega^2 L\alpha)^2]}{\omega^2 \alpha^2 \beta^2 + (C + \omega^2 L\alpha)^2} \quad (8)$$

$$X_{eq} = \frac{(C + \omega^2 L\alpha) \{ \alpha\omega^2 (R + \beta) - 1 - \omega^2 [\alpha(R\beta - \omega^2 L^2) - 2LC] \}}{\omega [\omega^2 \alpha^2 \beta^2 + (C + \omega^2 L\alpha)^2]} \quad (9)$$

The sign of the reactive part X_{eq} changes depending on the value of the coupling capacitance C_M . The value of C_M resulting in $X_{eq} = 0 \Omega$ is

$$C_0 = \sqrt{C^2 + \frac{1 - 2\omega^2 LC}{\omega^2 (\beta^2 + \omega^2 L^2)}} \quad (10)$$

If $C_M < C_0$, the reactance $X_{eq} > 0 \Omega$ and the equivalent impedance is resistive-inductive with

$$L_{eq} = \frac{X_{eq}}{\omega_O} = \frac{(C + \alpha\omega^2 L) \{ \alpha\omega^2 (R + \beta) - 1 - \omega^2 [\alpha(R\beta - \omega^2 L^2) - 2LC] \}}{\omega^2 [\alpha^2 \beta^2 \omega^2 + (C + \alpha\omega^2 L)^2]} \quad (11)$$

On the other hand, $C_M > C_0$ results in $X_{eq} < 0 \Omega$ and the equivalent impedance is resistive-capacitive with

$$C_{eq} = -\frac{1}{\omega_O X_{eq}} = -\frac{(C + \alpha\omega^2 L)^2 + \alpha^2 \beta^2 \omega^2}{(C + \alpha\omega^2 L) \{ \alpha\omega^2 (R + \beta) - 1 - \omega^2 [\alpha(R\beta - \omega^2 L^2) - 2LC] \}} \quad (12)$$

The blue trace in Figure 3a represents the ratio between the equivalent resistance R_{eq} and the load resistance R_L , while the red trace represents the reactance X_{eq} for different values of capacitive coupling C_M . In Figure 3b, the ratio is between the equivalent resistance R_{eq} and the load resistance R_L , while the red trace represents the reactance X_{eq} for different values of load resistance R_L . In Figure 3c, the variation of R_{eq}/R under both coupling and load resistance variation is shown, while in Figure 3d, the 3D plot of the reactive part X_{eq} for different coupling and load resistance is shown.

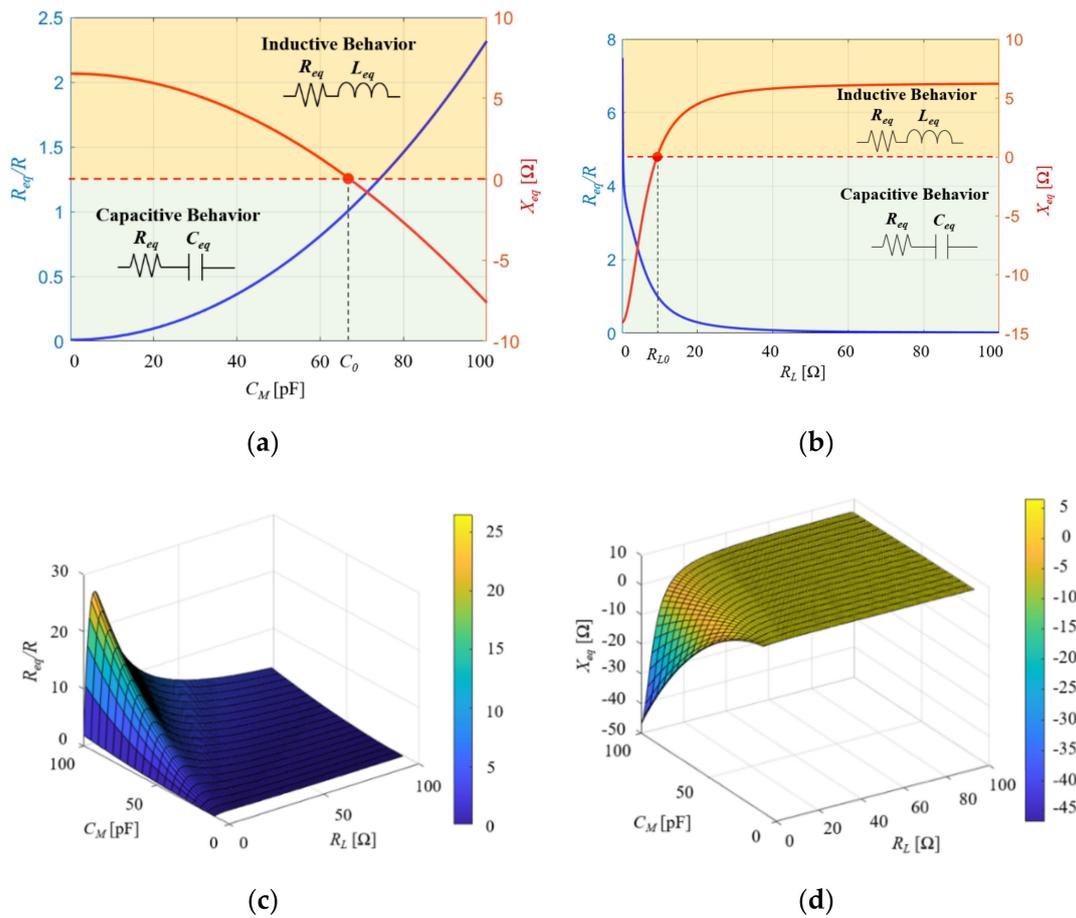


Figure 3. Equivalent impedance under capacitive coupling and load resistance variations. (a) Real and imaginary equivalent impedance part at fixed load resistance $R_L = 10 \Omega$ and different coupling capacitance C_M . (b) Real and imaginary equivalent impedance part at fixed load resistance $C_M = 32 \text{ pF}$. (c) The real part of the equivalent impedance. (d) The imaginary part of the equivalent impedance.

2.2. Efficiency and Output Power

The efficiency is calculated as

$$\eta = \frac{P_o}{P_o + P_{in}} = \frac{R_L}{R_L + R_2 + R_1 \left| \frac{I_1}{I_3} \right|^2} \quad (13)$$

where the ratio between the input and output currents is expressed by applying the KVL and KCL to the circuit of Figure 2b as

$$\frac{I_1}{I_3} = \frac{C_M \beta (R_{eq} - R) + \omega L X_{eq} + j [\omega L (R_{eq} - R) - \beta X_{eq}]}{C (R_{eq} - R)^2 + X_{eq}^2} \quad (14)$$

Assuming that the CWPT operates at the resonance, (14) simplifies as

$$\left| \frac{I_1}{I_3} \right|^2 = \frac{C_M^2}{C^2} \frac{\beta^2 + \omega^2 L^2}{(R_{eq} - R)^2 + X_{eq}^2} \quad (15)$$

Thus, the transmission efficiency is

$$\eta = \frac{R_L}{\beta C^2 [(R_{eq} - R)^2 + X_{eq}^2] + R_1 C_M^2 (\beta^2 + \omega^2 L^2)} \quad (16)$$

and the output current is expressed as

$$I_3 = -\frac{C_M}{C_M R_L + j\omega\beta R(C^2 - C_M^2)} \tag{17}$$

leading to an output power given by

$$P_o = -\frac{V_i^2 C_M^2 R_L}{(R_L C_M)^2 + [\omega\beta R(C^2 - C_M^2)]^2} \tag{18}$$

3. CWPT Class-E Inverter Circuit Analysis

In this section, the integration of the CWPT system with the Class-E inverter is presented.

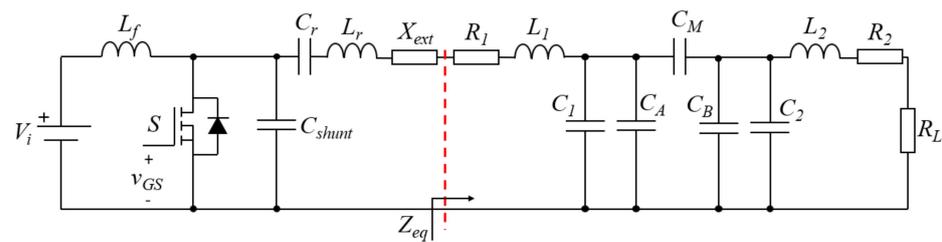
3.1. Assumptions

The analysis is derived according to the following assumptions.

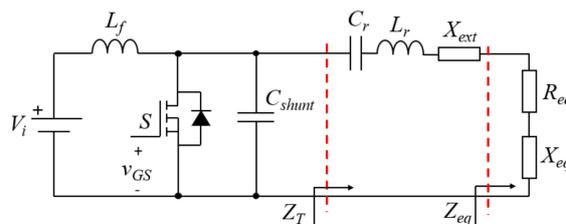
- The duty cycle D of the MOSFET is 0.5;
- The MOSFET turns ON and OFF instantly;
- The MOSFET ON-resistance is zero;
- The MOSFET output capacitance is linear and frequency invariant;
- The loaded quality factor Q_L of the resonant network is high enough such that the currents through the transformer windings are sinusoidal (e.g., $Q_L > 7$);
- The choke inductance is large enough to neglect the input current ac component. The dc resistance of the choke inductor is ignored. The self-capacitance of the choke inductor is absorbed into the shunt capacitance of the MOSFET.

3.2. Circuit Descriptions

Figure 4a shows the Class-E DC–AC inverter for capacitive wireless power applications. Here, V_i is the DC supply voltage source, L_f is the choke inductor, S is the switch implemented by using a power MOSFET, and C_{shunt} is the voltage-shaping shunt capacitor across the switch. The power MOSFET output capacitance and the self-capacitance of the choke are included in the overall capacitance C_{shunt} connected in parallel with the switch.



(a)



(b)

Figure 4. Circuit of capacitive wireless power transfer Class-E inverter. (a) Circuit topology. (b) Circuit topology with equivalent impedance.

In some applications, it is preferable to work at not excessively high frequencies, especially when the transferred power is high. Therefore, to integrate the CWPT into the Class-E inverter topology, it is necessary to add the capacitances C_1 and C_2 and the inductances L_1 and L_2 , as shown in Figure 4a. The circuit can be represented in the basic topology of Figure 4b introducing the equivalent impedance of CWPT Z_{eq} . Then, the components C_r and L_r , representing the resonant tank, can be properly tuned to achieve inductive load for soft-switching operation. The typical voltage and current waveforms of the circuit operating at ZVS/ZDS conditions are shown in Figure 5.

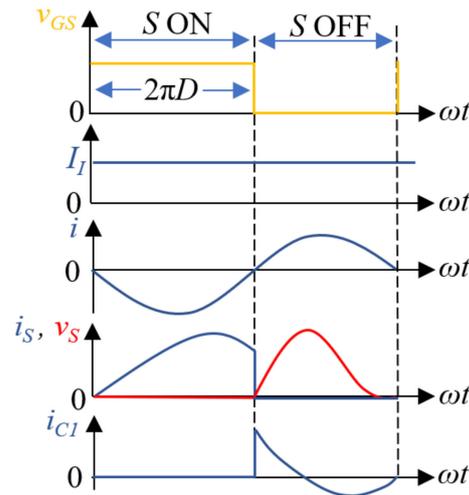


Figure 5. Waveforms in Class-E zero-voltage-switching inverter for optimum operation.

3.3. Optimum Design Procedure

Figure 4b shows the DC–AC Inverter where the CWPT system is replaced by its equivalent impedance $Z_{eq} = R_{eq} + j X_{eq}$. As discussed in the previous section, depending on the value of C_M , the equivalent reactance results to be either inductive or capacitive, as shown in Figure 3b. Let us assume that the system is working at the switching frequency $f = \omega / (2\pi)$.

Depending on the application, an optimal value of coupling C_M^{opt} must be defined.

To reduce the current circulation, the reactive part of the equivalent impedance X_{eq} must be canceled by adding an external reactance X_{ext} in series, leading to

$$X_{ext} = -X_{eq}. \tag{19}$$

In this way, when the system operates at $C_M = C_M^{opt}$, the equivalent impedance of the CWPT system is purely resistive $Z_{eq} = R_{eq}$. The external inductance, which must be series connected to the LC resonant tank when $X_{eq} < 0 \Omega$ to satisfy (19), is

$$L_{ext} = -\frac{1}{\omega X_{eq}} = \frac{1}{\omega^2 C_{eq}} \tag{20}$$

When $X_{eq} > 0 \Omega$, the external capacitance series-connected with the LC resonant tank to satisfy (19) is given by

$$C_{ext} = \frac{1}{\omega X_{eq}} = \frac{1}{\omega^2 L_{eq}} \tag{21}$$

Assuming that the load resistance R_L , the operating frequency $f_0 = \omega_0 / (2\pi)$, and the output power P_o values are known as design specifications, the expressions for the components needed to reach the ZVS and ZDS condition at $C_M = C_M^{opt}$ are given by [35]

$$V_i = \sqrt{\frac{\pi^2 + 4}{8} P_o R_{eq}} \tag{22}$$

$$C_{shunt} = \frac{8}{\pi(\pi^2 + 4)} \frac{1}{\omega C_1 R_{eq}} \quad (23)$$

$$L_r = \frac{Q_L R_{eq}}{\omega} \quad (24)$$

$$C_r = \frac{1}{\omega R_{eq} \left(Q_L - \frac{\pi(\pi^2 - 4)}{16} \right)} \quad (25)$$

Regarding the choke inductor, it can be calculated as [36]

$$L_f = \frac{14\pi R_{eq}}{\omega} \quad (26)$$

If the position of plates is not in the optimal position, the coupling is different from the nominal value C_M^{opt} , and therefore (19) is not satisfied. An in-depth analysis of the Class-E inverter under misalignment between plates is derived in Section 4.

3.4. Design Example

In this case of study, the considered power inverter has a nominal output power $P_O = 100$ W, the load resistance is $R_L = 10 \Omega$, the operating frequency is $f_0 = 100$ kHz, and the quality factor is selected to be $Q_L = 10$. The parasitic resistances are assumed to be $R_1 = R_2 = 0.1 \Omega$.

The coupling capacitance is $C_M = 64$ pF. It is assumed that C_A and C_B are much lower than the external capacitances C_1 and C_2 . These capacitances are fixed as $C_1 = C_2 = 3$ nF. From (6), the coupling factor is $k_c = 0.023$. Thus, the primary and secondary inductances are

$$L_1 = L_2 = \frac{1}{1 - k_c} \frac{1}{\omega_0^2 C} = 844 \mu\text{H} \quad (27)$$

From (8)–(20), the equivalent impedance is $Z_{eq} = R_{eq} + j X_{eq} = 3.2 - j0.0411$, $X_{eq} < 0$, according to (11)–(21), so

$$C_{eq} = \frac{1}{\omega X_{eq}} = 38.7 \mu\text{F} \quad (28)$$

$$L_{ext} = \frac{1}{\omega^2 C_{eq}} = 65.4 \text{ nH} \quad (29)$$

Finally, by using (22)–(26), the shunt capacitance, the resonant inductance, the resonant capacitor, and the choke inductance are calculated as $C_{shunt} = 91$ nF, $L_r = 51 \mu\text{H}$, $C_r = 56$ nF, and $L_f = 200 \mu\text{H}$, respectively.

The proposed design procedure is represented as a flowchart in Figure 6. Starting from the four plates capacitive wireless power transfer structure, the equivalent π electric circuit can be extrapolated. Defining the system characteristics, such as the operating frequency, the output power, and the load resistance, the equivalent impedance Z_{eq} can be calculated. To cancel the reactive part X_{eq} , a capacitor C_{ext} can be added if $X_{eq} > 0$.

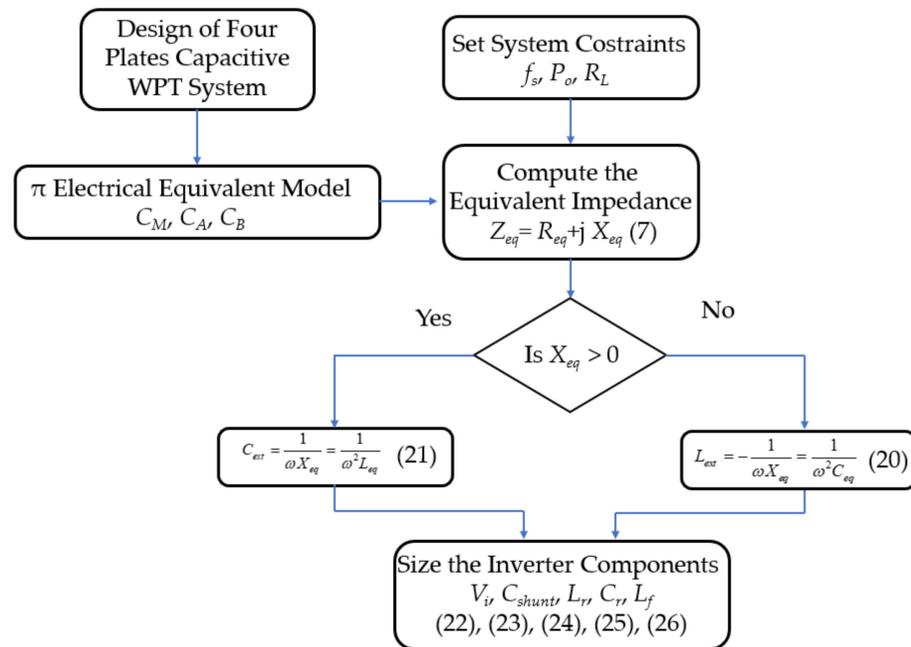


Figure 6. Design procedure flowchart representation.

4. Class-E Inverter Behavior at Any Coupling Coefficient

4.1. Analytical Model

In this section, the analytical expressions of current and voltage waveforms across the components are derived. According to Figure 4, an equivalent impedance $Z_T = R_T + jX_T$ can be defined; its phase is

$$\psi = \arctan\left(\frac{R_T}{X_T}\right) \tag{30}$$

The current through the series-resonant circuit is sinusoidal and given by

$$i = I_m \sin(\omega t + \varphi) \tag{31}$$

where I_m is the amplitude, and φ is the initial phase. The vector relationship between the angle ψ and φ is shown in Figure 7. If $X_T > 0 \Omega$, the voltage across the equivalent inductance V_{LT} leads by 90° the voltage across the equivalent resistance V_{RT} , as shown in Figure 7a; while if $X_T < 0 \Omega$, voltage V_{RT} leads by 90° voltage V_{CT} , as shown in Figure 7b.

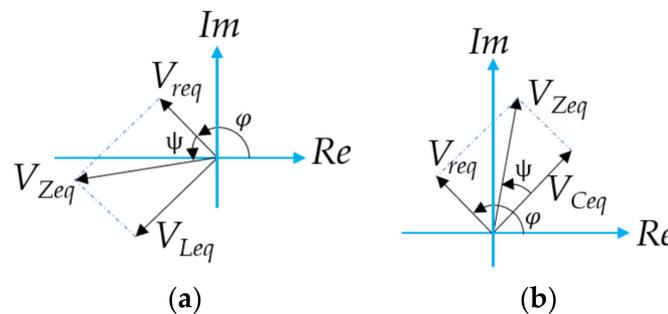


Figure 7. Vector representation of the relationship between φ and ψ angles. (a) Resistive-inductive equivalent impedance. (b) Resistive-capacitive equivalent impedance.

If the impedance is resistive–inductive, the first harmonic of the voltage v_{shunt}^1 applied to Z_T can be split into the voltage across the equivalent resistance R_T and that across the equivalent reactance X_T .

$$v_{shunt}^1(\omega t) = v_{Rt}(t) + v_{Lt}(t) = V_{Rt} \sin(\omega t + \varphi) + V_{Lt} \cos(\omega t + \varphi) \tag{32}$$

Using (31), the relationship between the angles ψ and φ , at a fixed duty cycle is derived as

$$\tan(\psi) = \frac{\pi^2 + 2 \cos(\psi) \cos(2\pi D + \psi) + \cos(2(\pi D + \psi)) - 1}{4 \sin(\pi D + \psi) \cos(\pi D + \psi)} \tag{33}$$

This relationship is also shown in Figure 8, for three different values of the duty cycle.

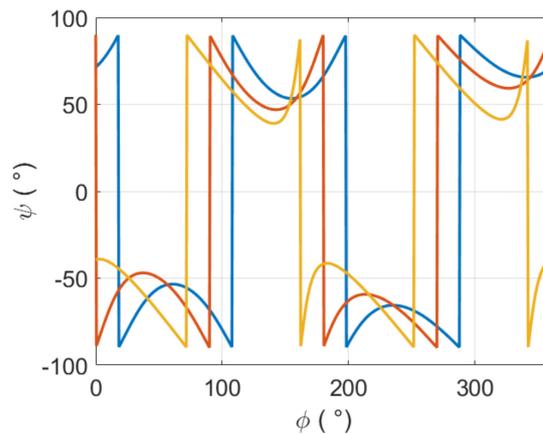


Figure 8. Relationship between φ and ψ angles.

The drain to source voltage across the MOSFET is

$$v_s(\omega t) = \frac{1}{C_1} \int_{2\pi D}^{\omega t} i_{C1} d\omega t = \begin{cases} 0 & 0 < \omega t < 2\pi D \\ \frac{1}{\omega C_1} \{I_I(\omega t - 2\pi D) + I_m[\cos(\omega t + \varphi) - \cos(2\pi D + \varphi)]\} & 2\pi D < \omega t < 2\pi \end{cases} \tag{34}$$

If the choke inductance L_f is big enough to assume the input current I_I to be constant, the input voltage V_I can be calculated as the average value of the v_s

$$V_i = \frac{1}{2\pi} \int_{2\pi D}^{2\pi} v_s d(\omega t) = \frac{1}{2\pi} \int_{2\pi D}^{2\pi} \frac{1}{\omega C_1} \{I_I(\omega t - 2\pi D) + I_m[\cos(\omega t + \varphi) - \cos(2\pi D + \varphi)]\} d(\omega t) = \frac{1}{2\pi \omega C_1} \left\{ 2\pi I_i(1 - D)^2 + I_m \{ \sin(\varphi)[1 - \cos(2\pi D)] - \sin(2\pi D) \cos(\varphi) - 2\pi(1 - D) \cos(2\pi D + \varphi) \} \right\} \tag{35}$$

Under the assumptions used for this analysis, the power losses for the circuit can be neglected. This means that $P_o = V_o I_o$ and $P_i = V_i I_i$. Thus, the amplitude of the current through the resonant tank can be expressed as

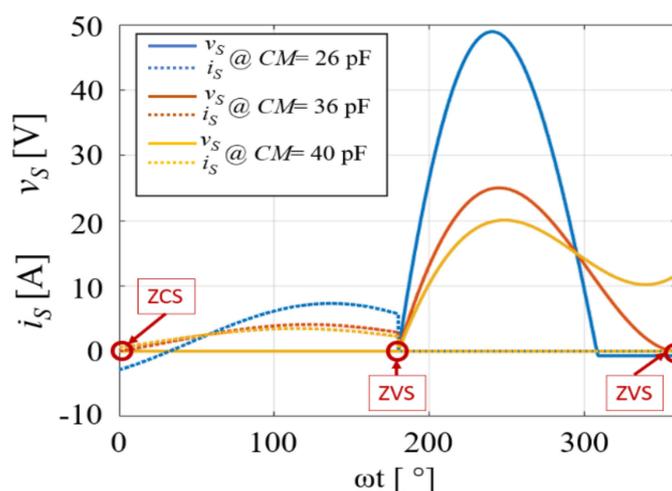
$$I_m = \frac{2\pi \omega V_i - 2\pi^2 I_i(1 - D)^2}{\sin(\varphi)[1 - \cos(2\pi D)] - \sin(2\pi D) \cos(\varphi) - 2\pi(1 - D) \cos(2\pi D + \varphi)} \tag{36}$$

4.2. Voltage and Current Waveforms

The equations shown in the previous section allow the study of the system behavior under capacitive coupling changes. Using (34) and (36), the voltage and the current through the MOSFET for three different values of coupling capacitance C_M were calculated. The waveforms computed using the previous equations using the nominal values summarized in Table 1 are shown in Figure 9.

Table 1. Component values for the designed system.

Parameter	Calculated
C_M^{opt}	32 pF
V_i	23.6 V
L_f	200 μ H
C_{shunt}	91 nF
L_r	51 nH
C_r	56 nF
L_1	844 μ H
C_1	3 nF
L_2	844 μ H
C_2	3 nF
R_L	10 Ω

**Figure 9.** Voltage and current waveforms through the MOSFET for three different values of coupling capacitance C_M .

The dotted lines in Figure 9 represent the current through the MOSFET i_s , while the continuous line is the drain to source voltage v_s . Note that the ZVS/ZDS condition is achieved only for the optimum value of coupling capacitance $C_M^{opt} = 32$ pF. When the plates are strayed leading to a lower coupling capacitance $C_M < C_M^{opt}$, the ZVS condition is still achieved, as shown for $C_M = 25$ pF. When $C_M = C_M^{opt}$, at $\omega t = 0$ both ZCS and ZVS are reached, being both the current and the voltage across the MOSFET zero, while, when $\omega t = 180^\circ$, only ZVS is achieved, being the current different from zero. When the plates come closer with respect to the optimum position $C_M > C_M^{opt}$, the ZCS condition is not achieved at $\omega t = 0$, while it is almost achieved $C_M < C_M^{opt}$.

5. Simulation and Experimental Results

To validate the analysis results obtained using the analytical equations, the circuit was implemented in LTSpice and validated experimentally.

5.1. Simulations

The results obtained by using the analytical model described in the previous section are here validated through simulations. The circuit is implemented in LTSpice as shown in Figure 10 with the values component values shown in Table 1. To evaluate the effects of misalignment, three different values of coupling capacitance C_M were studied. Figure 11a shows the current and voltage waveforms resulting at $C_M = 25$ pF. The power delivered to the load is reduced to $P_o = 89$ W, and also the efficiency reduces to $\eta = 0.91$. In Figure 11b, the case with $C_M = C_M^{opt} = 32$ pF is considered, both ZVS and ZDS are achieved, the

output power is $P_o = 92$ W, and the system efficiency is $\eta = 0.95$. Finally, the circuit with $C_M = 45$ pF is simulated, ZVS condition is not achieved, and the transmitted power increases to $P_o = 95$ W, but the converter efficiency further decreases to $\eta = 0.89$, as shown in Figure 11c. Note that at $C_M = 25$, pF ZVS is still achieved, but the voltage stress across the MOSFET significantly increases if compared with the other couplings.

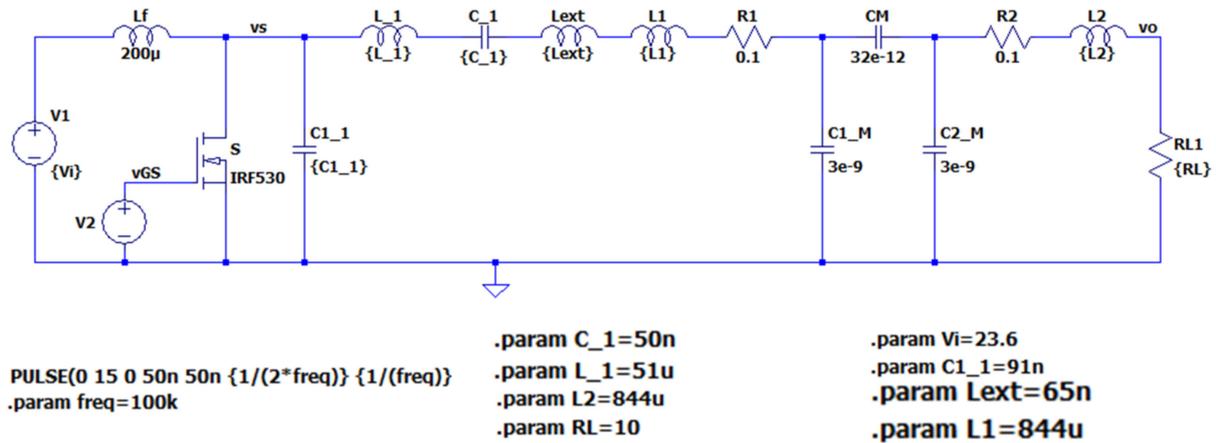
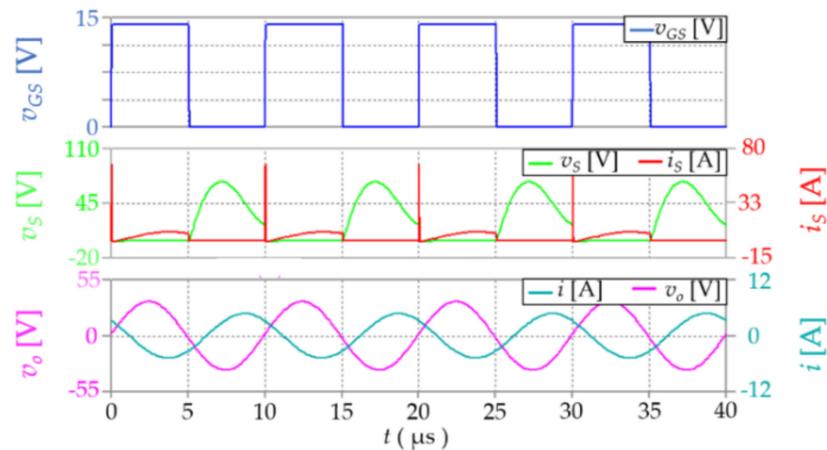
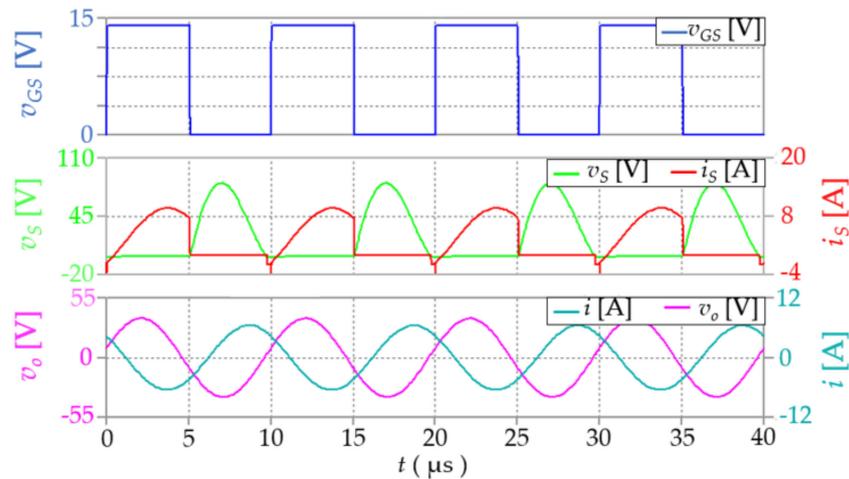


Figure 10. LTSpice circuit schematic.

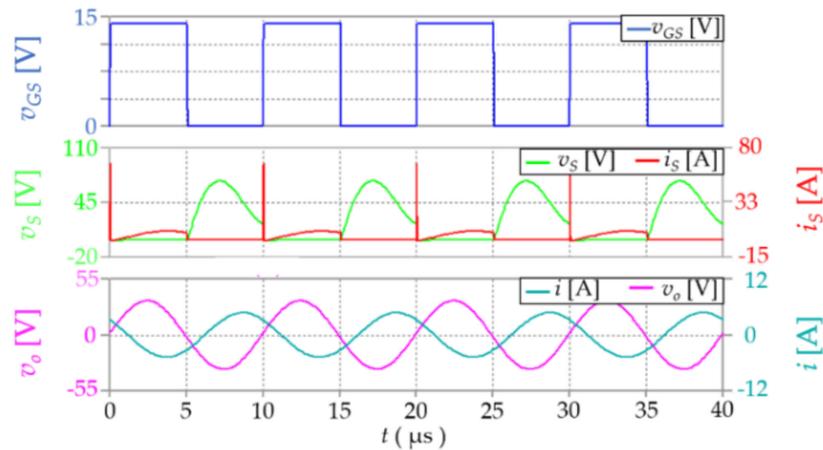


(a)

Figure 11. Cont.



(b)



(c)

Figure 11. Simulated waveforms at several coupling capacitance C_M values. (a) 25 pF. (b) 32 pF. (c) 45 pF.

5.2. Experimental Results

To validate the simulations, a power converter experimental circuit has been realized. A picture of the experimental setup is shown in Figure 12a. An enlargement of the PCB board is shown in Figure 12b, while the equivalent electric circuit is shown in Figure 12c. The four plates are steel made. The measured values and the component parasitic resistances are given in Table 2. The inductance was made by using AWG40 Litz wire to reduce the parasitic resistance at $f_s = 100$ kHz. A Silicon Super Junction MOSFET-R6020JNJ is used [37]. The main MOSFET parameters are reported in Table 3.

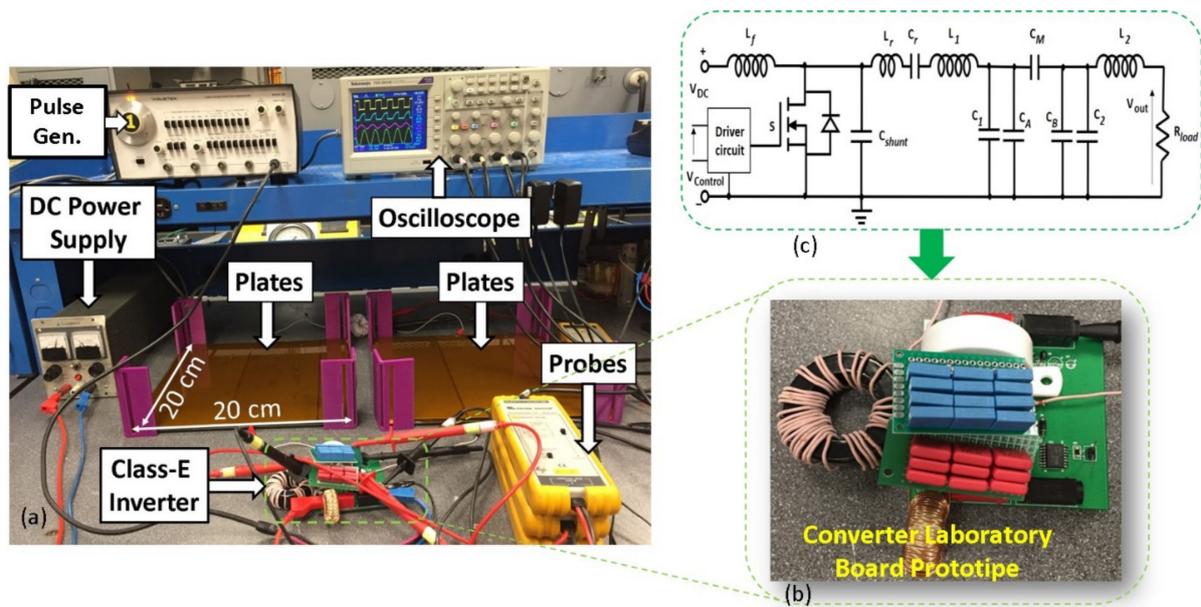


Figure 12. Experimental setup. (a) Board and instrumentations. (b) Experimental board. (c) Electrical schematic.

Table 2. Experimentally measured values of components and their parasitics.

Parameter	Measured
C_{opt}^M	32 pF
V_i	23.6 V
f_s	100 kHz
L_f	214.3 μ H/ $ESR_{L_f} = 26$ m Ω
C_{shunt}	90.2 nF/ $ESR_{C_{shunt}} = 35$ m Ω
L_r	50.3 nH/ $ESR_{L_r} = 35$ m Ω
C_r	57.3 nF/ $ESR_{C_r} = 7$ m Ω
L_1	839.6 μ H/ $ESR_{L_1} = 13$ m Ω
C_1	3.2 nF/ $ESR_{C_1} = 4$ m Ω
L_2	842.3 μ H/ $ESR_{L_2} = 13$ m Ω
R_L	9.96 Ω

Table 3. Main super junction MOSFET parameters.

Parameter	Value	Conditions
$V_{BR,DSS}$	600 V	$V_{GS} = 0$ V, $I_D = 1$ mA
$R_{DS,ON}$	0.234 Ω	$V_{GS} = 15$ V, $I_D = 10$ A, $T_J = 25$ $^{\circ}$ C
I_D	20 A	$T_a = 25$ $^{\circ}$ C
C_{iss}	1500 pF	$V_{GS} = 0$ V, $V_{DS} = 100$ V, $f = 1$ MHz
C_{oss}	90 pF	—
C_{rss}	1.9 pF	—

The experimental tests were performed under three different values of C_M . Figure 13a shows the waveforms at $C_M = 25$ pF. The amplitude of the LC resonant current is $I = 8.9$ A, the output voltage is $V_o = 39.8$ V, and the output power $P_o = 80$ W with a transmission efficiency $\eta = 82.4\%$. In Figure 13b, the measured waveforms at $C_M = C_M^{opt} = 32$ pF are shown. The waveforms of the current flowing into the LC resonant tank i and that of the voltage across the load resistance v_o are perfectly sinusoidal with amplitudes of $I = 8.3$ A and $V_o = 28.9$ V, respectively.

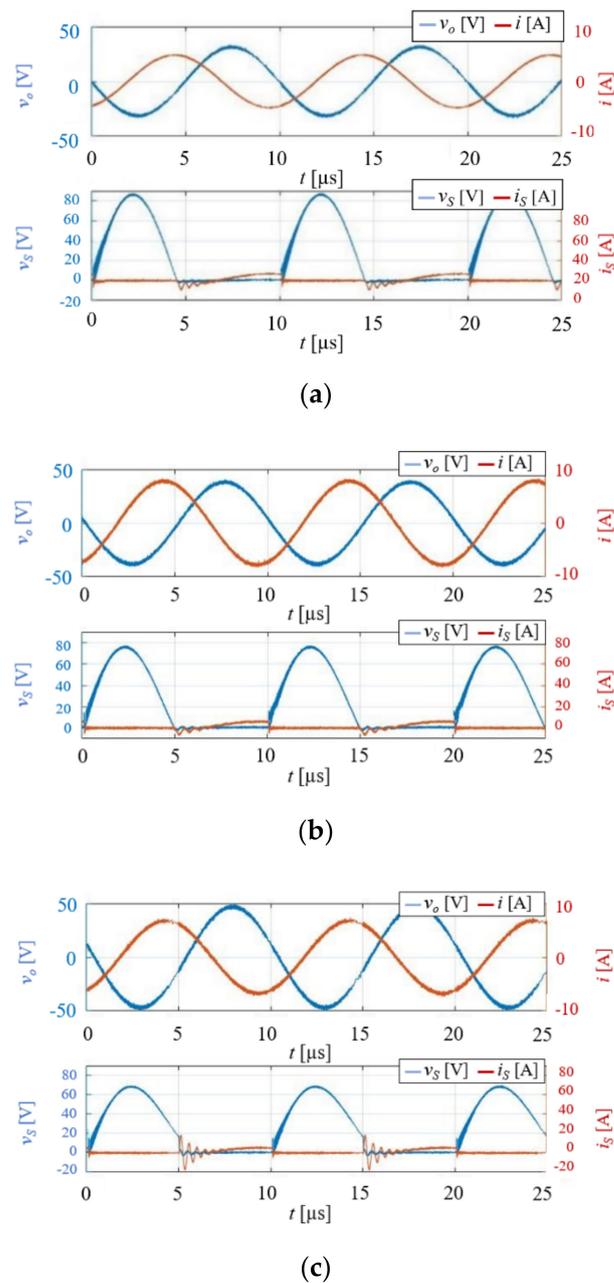


Figure 13. Experimental waveforms versus C_M variations. (a) 25 pF. (b) 32 pF. (c) 45 pF.

The measured transmission efficiency is $\eta = 92.5\%$. Finally, in Figure 13c, the waveforms at $C_M = 45$ pF are shown. The current flowing through the resonant tank stays approximately constant to $I = 8.3$ A, but the voltage across the load is $V_o = 47.8$ V, the transmitted power $P_o = 90.6$ W, and a transmission efficiency $\eta = 88.5\%$. Concerning the achievement of the ZVS condition, it can be seen that for $C_M = 25$ pF, the ZVS condition is still achieved, but the voltage stress across the MOSFET is increased reaching a maximum voltage $V_{DS}^{max} \cong 90$ V.

Operating with $C_M = C_M^{opt} = 32$ pF, both the ZVS/ZDS conditions are achieved, while when the coupling increases as for $C_M = 45$ pF, the ZVS condition is not achieved anymore, leading to ringing and switching power losses.

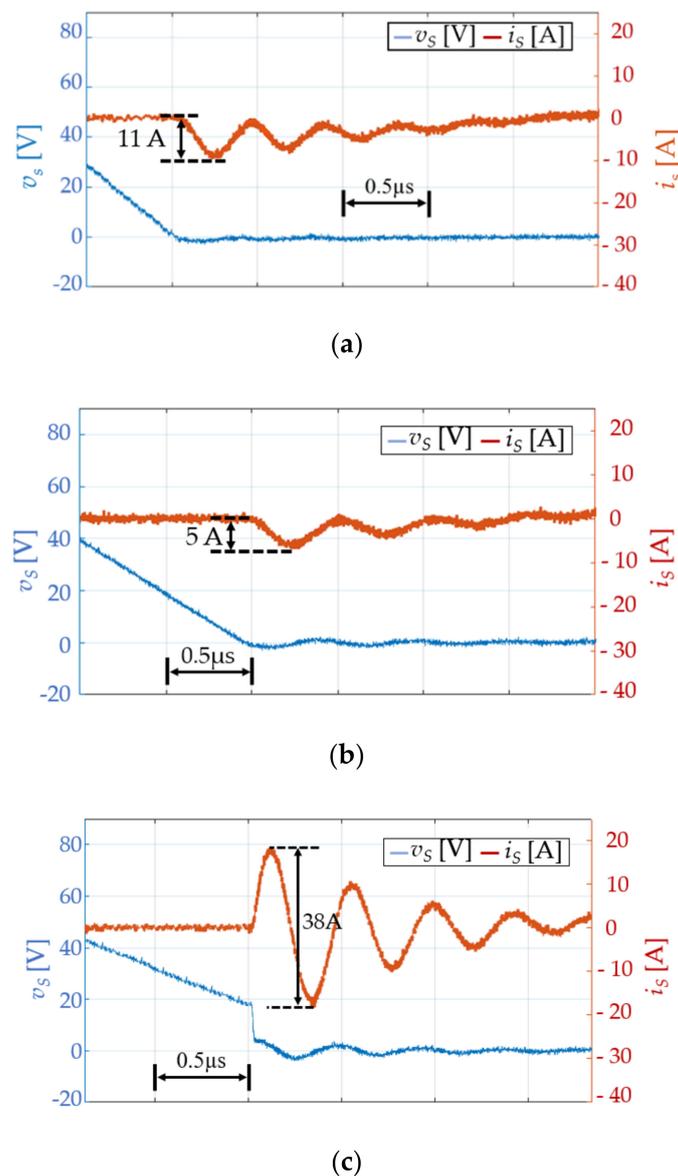
The converter also results in a very low output voltage total harmonic distortion (THD) as shown in Table 4, where the DC component and the THD of the output voltage for the three different capacitive couplings are summarized.

Table 4. Output voltage harmonic content.

Capacitive Coupling	DC	THD
25 pF	493 μ V	0.35%
32 pF	238 μ V	0.64%
45 pF	238 μ V	0.42%

Although the conversion efficiency is highly sensitive to coupling variation, the THD of the output voltage is also very low when the converter operates outside the optimum coupling.

An enlargement of the turn-on switching voltage and current waveforms for the three coupling cases is shown in Figure 14. The blue trace represents the voltage across the MOSFET v_S , while the red trace represents the current i_S . It can be seen that for both the cases, $C_M = 25$ pF and $C_M = 32$ pF ZVS is achieved, while for $C_M = 45$ pF, the ZVS condition is not achieved, and a higher current oscillation occurs after the turn-on, thus leading to higher switching losses.

**Figure 14.** Drain-to-source voltage and current versus C_M variation. (a) 25 pF. (b) 32 pF. (c) 45 pF.

The experimental results confirm both the analysis and simulation results. Mutual capacitance C_M is one of the key parameters to investigate to achieve the ZVS and ZDS operations. The same transient behavior obtained from analytical equations and simulations is highlighted. When plates are moved from the optimal position, ZVS is still reached, but the power is transferred to the load, and the efficiency decreases. On the other hand, when the plates are placed at a closer distance than that of the optimal position, the transferred power increases, but the ZVS is not achieved, leading to a lower transmission efficiency. The abovementioned behavior of the converter versus coupling capacitance C_M is illustrated in Figure 15, where the experimentally measured output power and conversion efficiency are shown. The maximum DC–AC conversion efficiency occurs at the optimum coupling capacitance C_M^{opt} . This is due to the achievement of the ZVD/ZDS condition, which drastically reduces the MOSFET switching losses, while the conduction losses are mainly related to the switch current root mean square (RMS) $i_{s,rms}$ (Figure 9) and the $R_{DS,ON}$ of the chosen device [38,39]. Figure 15 also shows that the transferred power increases if the plate coupling increases.

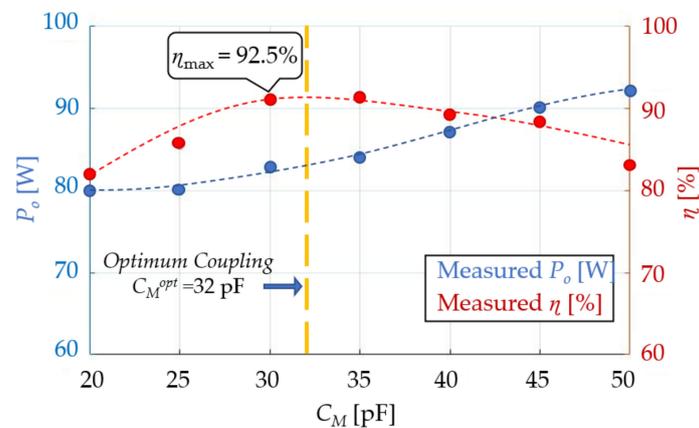


Figure 15. Experimental measurement of DC–AC conversion efficiency and output power at various C_M values, where the blue line is the output power P_O and the red line is the efficiency η .

In Table 5, the comparison in terms of output power, efficiency, operating frequency, and capacitive coupling between Class-E circuits available in the literature is shown.

Table 5. Comparison between literature systems.

Parameter	Output Power	Frequency	Efficiency	Capacitive Coupling
[24]	20 W	6.78 MHz	80%	5.8 pF
[25]	1.7 W	1 MHz	75%	112 pF
[26]	5 W	13.56 MHz	95%	176 pF
[27]	3 W	6.78 MHz	85%	940 pF
[28]	360 mW	2 MHz	-	250 pF
[29]	10 W	1 MHz	93.4%	350 pF
[30]	9.45 W	1 MHz	98.4%	2.20 nF
Proposed	83.5 W	100 kHz	92.3%	32 pF

As shown, the proposed solution allows the increase of the transferred power operating at reduced switching frequency despite the low capacitive coupling.

6. Conclusions

This paper presents a complete analysis and the design procedure of the CWPT system based on a Class-E inverter. The analysis is focused on the coupling capacitance and its effects on the design constraints. It has been shown that the inverter satisfies both ZVS

and ZDS conditions at a selected optimum coupling capacitance C_M^{opt} and satisfies ZVS conditions for $0 < C_M < C_M^{opt}$, yielding a high conversion efficiency. The expressions for the inverter current and voltages have been determined as functions of the coupling capacitance C_M , so that the converter behavior also under misalignment between plates is predicted. Simulations and experimental results have been provided to validate the theoretical derivations.

Using the results of this paper, CWPT Class-E inverters can be designed for applications with fixed or variable coupling coefficient at any fixed load impedance. Additionally, thanks to the LC compensation, the operation at a lower frequency is allowed. This feature is obtained through a simpler control strategy with reduced switching losses and high quality of output waveforms (low THD). Therefore, compared with the similar experimental setup available in the literature, the proposed system is characterized by a higher output power transfer and a lower switching frequency.

Lower switching frequency operation allows controlling the system using controllers with low computational capabilities, which can be a useful feature for low-cost applications.

Furthermore, it operates at a lower frequency, leading to core losses reduction. On the other hand, this solution is useful for those applications where the optimization of the dimension and weight of the inverter is not of primary importance.

Practical applications of the considered CWPT circuit are in a wide variety of areas, including wireless power charging, induction heating, wireless-charged biomedical transplants, DC–DC power conversion, and DC–AC power inversion.

As future development, the performance of the DC–AC inverter using different four plates structures will be evaluated. A comparison between different structure solutions in terms of horizontal and vertical misalignment will be studied. Additionally, an extensive analysis of the power losses in the circuit will be evaluated, placing attention on the MOSFET losses and the losses due to parasitic components.

Author Contributions: Conceptualization: Y.-H.W., F.C., A.R., S.M., and D.C.; validation: Y.-H.W., and F.C.; writing–original draft preparation: F.C.; writing–review and editing: F.C., A.R., and S.M.; visualization: Y.-H.W., F.C., A.R., S.M., and D.C.; supervision: A.R., S.M., and D.C.; project administration: Y.-H.W., F.C., A.R., S.M., and D.C. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the Ministry of Science and Technology of Taiwan, R.O.C. with grant number MOST-108-2221-E-606-015.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Informed consent was obtained from all subjects involved in the study.

Data Availability Statement: Conceptualization, Y.W., F.C., A.R., S.M., and D.C.; validation, Y.W., F.C.; writing–original draft preparation, F.C.; writing–review and editing, F.C., A.R., and S.M.; visualization, Y.W., F.C., A.R., S.M. and D.C.; supervision, A.R., S.M. and D.C.; project administration, Y.W., F.C., A.R., S.M., and D.C. All authors have read and agreed to the published version of the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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