Capacitance-to-Digital Converter for Operation Under Uncertain Harvested Voltage down to 0.3V with No Trimming, Reference and Voltage Regulation

5.2 Capacitance-to-Digital Converter for Operation Under Uncertain Harvested Voltage down to 0.3V with No Trimming, Reference and Voltage Regulation

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In low-cost battery-less systems, capacitive sensing via capacitance-to-digital conversion (CDC) needs to operate with minimal or no support from additional circuitry such as voltage regulation, voltage/current references or digital post-processing as shown in Fig. 5.2.1 (e.g., for linearization). At the same time, direct harvesting demands operation down to very low voltages and power, to consistently fit the power available from the environment even when scarce (e.g., down to ~nW/mm^2 in light harvesters under realistic conditions). To enable continuous monitoring at power lower than the μW-range of state-of-the-art ~12-bit CDCs [1-3], 7-to-8-bit architectures with power down to sub-nW have been demonstrated for sensor nodes [4], although their supply voltage requirement (≥0.6V) is not suitable for direct harvesting, similar to [5]. CDCs for continuous monitoring at lower resolution (~7 bit) with sub-nW operation at 0.6V have been also demonstrated [6], although their power is burdened by the additional contribution of digital post-processing (~nWs) and others. A fully digital CDC has been introduced in [7] in the form of capacitance-to-voltage conversion via capacitor linear discharge due to a ring oscillator and final voltage-to-digital conversion, which requires two supply voltages of 0.45V and 1V. Operation at minimal power also comes with measurement times in the sub-second or second scale [6,8] in addition to the reduced resolution, which are still in the range required by continuous monitoring in several applications [6,8] (e.g., temperature, humidity, proximity, fluid level monitoring).

In this work, a capacitance-to-digital converter for low-cost systems that can be powered directly by a harvester is presented. The digital architecture based on swappable oscillators removes the need for any system infrastructure in terms of voltage regulation, references and digital post-processing, and enables operation down to 0.3V. nW-power operation is obtained by introducing swapped-voltage biasing in dual-mode logic gates [9]. The CDC is equipped with a load-agnostic self-calibration that reduces system cost by removing the need for accurate test load or clock, avoiding any additional testing time, while being executable any time (i.e., at boot and run time) without disconnecting the available load. Operation under a 1mm^2 solar cell at indoor lighting level is demonstrated.

The proposed CDC (Fig. 5.2.1) is based on two nominally identical (see calibration below) relaxation oscillators OSC1 and OSC2 with swappable loads C_x and C_{REF}, which are respectively the unknown capacitance to be measured and the reference capacitance. Direct (swapped) connection in Fig. 5.2.2 loads OSC1 with C_x (C_{REF}) and OSC2 with C_{REF} (C_x), and their oscillations are respectively counted by a down- and an up-counter. Under direct connection, the down-counter defines the measurement time window $t_{MEASURE}$ of M periods of $T_X \propto C_X$, which is statically adjustable via the pre-loaded start count and ends when down-count reaches 00…0. During this window, the number n of rising edges of OSC2 with period $T_{REF} \propto C_{REF}$ is counted by the up-counter so that $C_x=(T_X/T_{REF})\cdot C_{REF} \approx (n/M)\cdot C_{REF}$, within an error of C_{REF}/M due to the time quantization of $n\cdot T_{REF}$ within the exact window $M\cdot T_X$ (error of up to 1 cycle, Fig. 5.2.3). For a given C_x, higher M leads to a higher n and hence improves the resolution (ultimately limited by oscillator jitter) at the expense of longer $t_{MEASURE}$ over the range of C_x. Under swapped connection, both loads, periods and counts are swapped, and C_X hence results to $(T_{REF}/T_X)\cdot C_{REF} \approx (M/n)\cdot C_{REF}$. To minimize the necessary down-counter counts M for a given resolution (i.e., n), the direct (swapped) connection is always preferred for $C_X > C_{REF}$ ($C_{REF} \leq C_X$) since this makes $n>M$ in any case, as allowed by the swappable oscillators. From the resulting measurement flowchart in Fig. 5.2.2, a measurement is first performed with direct connection assuming $C_X > C_{REF}$ and checking if this is true (i.e., $n>M$), otherwise the measurement is repeated after swapping. For the targeted nW-power applications, both the control logic and the oscillators are implemented in dual-mode logic [9] to 1) reduce supply sensitivity over standard CMOS, and 2) reduce leakage by ~4× by swapping the original header/footer biasing, while avoiding its very slow operation at minimum-power operation (Fig. 5.2.2).

The CDC is inherently insensitive to global process, voltage and temperature (PVT) variations, as they equally affect the capacitance-to-period conversion gain T_x/C_x and T_{REF}/C_{REF} of OSC1 and OSC2, thus keeping T_x/T_{REF} unaltered. The oscillator mismatch is compensated with the on-chip load-agnostic self-calibration in Fig. 5.2.3. Under a given and unknown C_X, the up-counter count $n_1=T_{REF,1}/T_{X,1}$ is first evaluated under direct connection, and then again in double-swapped connection (i.e., with swapped load and swapped counters via multiplexers) to evaluate $n_2=T_{REF,2}/T_{X,2}$. In case of mismatch, n_1 becomes smaller (larger) than n_2 if OSC1 turns out to be faster (slower) than OSC2. In this case, a calibration capacitance C_{CAL} is added in parallel to the load capacitance of OSC1 (OSC2) to bring its frequency closer to the other oscillator, and hence reduces the mismatch error. The measurements of n_1 and n_2 are then repeated, and the compensation capacitance is tuned depending on the result of the comparison by a successive approximation register (SAR) logic on 4 bits with 10fF resolution. The calibration can be occasionally repeated to reduce the minor impact (Fig. 5.2.4) of temperature variations.

The 0.18μm CDC test chip (Fig. 5.2.7) occupies 0.2mm^2 area and operates at 0.3V-to-1.8V power supply, where the minimum allowed voltage is enabled by the inherently robust operation of dual-mode logic below 0.3V [9]. At V_{DD}=0.3V and M=32 (good compromise between $t_{MEASURE}$ and accuracy, see above), the capacitance range handled by the CDC is 0 to 30pF and its nominal resolution is C_{LSB}=125fF. The testing results are based on a minimum capacitance of 2pF due to the parasitics in parallel to C_x. The characterization in Fig. 5.2.4 reveals a noise-limited resolution $C_{NOISE,rms}$ of 45.7fF (0.36LSB), as estimated on 100 measurements. The maximum (RMS) INL after self-calibration is 125fF (49fF), corresponding to 1LSB (0.39LSB) at nominal C_{LSB}=125fF. This is a 1.4× improvement over the CDC before self-calibration, whose maximum (RMS) INL is 177fF (64fF), corresponding to 1.4LSB (0.51LSB). Considering both noise and nonlinearity, the absolute capacity resolution is therefore equivalent to 67fF after self-calibration (78.5fF before self-calibration), yielding an SNDR of 44dB corresponding to an ENOB of 7.0 bits. From post-calibration measurements on five dice, the maximum (RMS) INL value ranges from 0.51 LSB to 0.66 LSB (0.25 to 0.39 LSB), ENOB ranges from 6.94 bits to 7.24 bits, and SNDR ranges from 43.54dB to 45.16dB. In Fig. 5.2.4, temperature variations in the -25°C to 75°C range and supply voltage variations from 0.3V to 1.8V induce an error that is always below 1LSB, and is further reduced by nearly 0.5LSB after self-calibration. When sweeping V_{DD} from 0.3V to 0.5V, the maximum (RMS) post-calibration INL is in the 0.51 to 0.62 LSB range (0.39 to 0.45 LSB), the ENOB is in the 6.8 to 7 LSB range, and SNDR ranges from 40.4 LSB to 43.5 LSB.

From Fig. 5.2.5, the power under different supply voltages expectedly increases at larger voltages with a much more graceful (i.e., flatter) trend compared to a commercial solar cell, thus assuring sustained operation across any environmental conditions. At indoor light conditions (Fig. 5.2.5), the harvested voltage varies from 0.3V to 0.6V and the power moderately increases from 1.37 to 6nW. The measurement time and energy per conversion are expectedly proportional to C_X and the counter preset (Fig. 5.2.5). At M=32 and at the maximum capacitance of 30pF, power is 1.37nW and the worst-case measurement time is 1.04s, leading to an energy per conversion of 1.42nJ.

A comparison of this work with state-of-the-art converters is shown in Fig. 5.2.6. Compared to prior art, the proposed CDC is uniquely able to consistently provide 7-bit conversion over the wide voltage range from 0.3V to 1.8V, whose lower end is 2-to-5.3× lower than prior art [1-8]. Such capability avoids the conventional need for a voltage regulator, and enables its usage in directly harvested systems for low-cost applications. Exhibiting the third lowest power, the proposed CDC uniquely achieves true nW-range power through the avoidance of any additional reference (as compared to [1,3,5]) and digital post-processing for output correction (as compared to [6]). Low testing cost is enabled by the suppression of testing-time calibration, compared to [1,3-6]. Sustained operation with a 1mm^2 solar cell is achieved under any practical lighting condition.

Acknowledgements:

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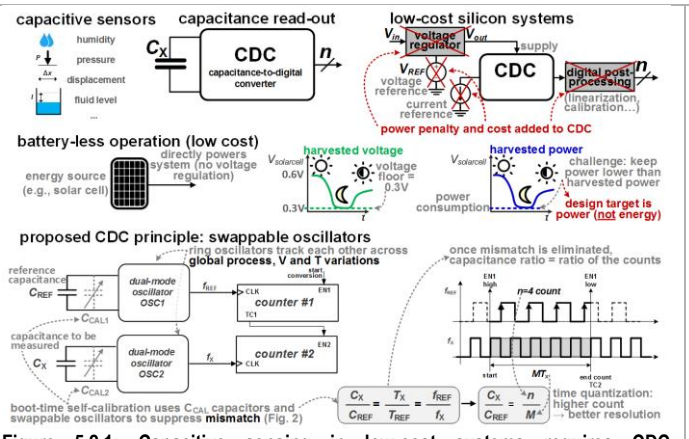

Figure 5.2.1: Capacitive sensing in low-cost systems requires CDC architectures that do not require additional support circuitry (top-right). Battery-less operation with direct harvesting reduces cost and demands operation at very low voltages and power (center), as enabled by the proposed CDC (bottom).

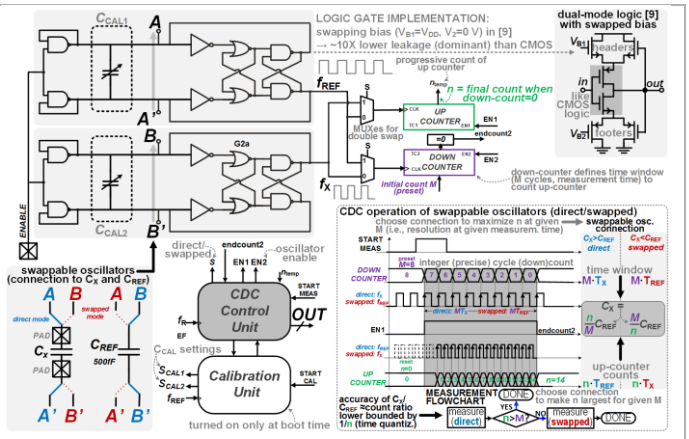

Figure 5.2.2: Detailed schematic of the CDC with swappable oscillators (top-left), dual-mode logic gate with swapped biasing (top-right), and proposed CDC operation in direct and swapped mode (bottom-right).

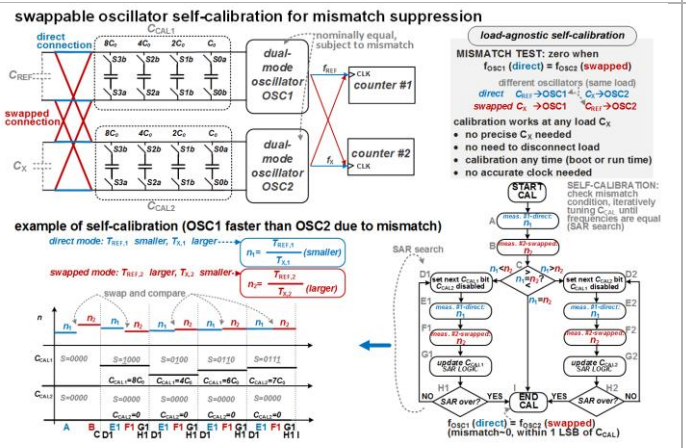

Figure 5.2.3: Self-calibration suppresses mismatch between the oscillators, matching their mutual count at direct and swapped connection of load C_X and reference capacitor C_{REF} (top-left). The mismatch frequency test guides SAR-like tuning (right) of calibration capacitors C_{CAL1} and C_{CAL2} (top-left), as exemplified on bottom-left.

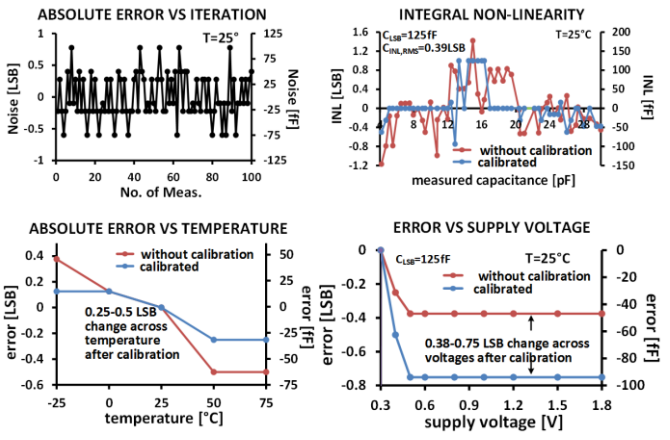

Figure 5.2.4: Measured noise vs. measurement iteration (top-left), integral non-linearity before/after self-calibration (top-right), absolute error vs. temperature (bottom-left), and absolute error vs. supply voltage before/after calibration (bottom-right).

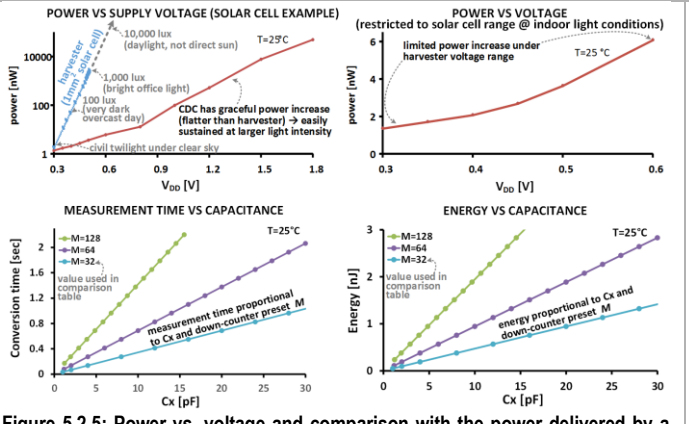

Figure 5.2.5: Power vs. voltage and comparison with the power delivered by a 1mm² solar cell (top-left), and zoomed-in plot under indoor light conditions (top-right). Measurement time vs. capacitance (bottom-left) and energy per conversion vs. capacitance (bottom-right).

	This work	[1] JSSC19	[2] JSSC17	[3] ISSCC19	[4] JSSC19	[5] JSSC20	[6] VLSI20	[7] ISSCC15	[8] VLSI17
process [nm]	180	180	40	40	65	130	65	40	160
architecture	self-calibrating ring oscillators	ΔΣ + SAR	SAR+VCO	SAR+TDΔΣ	SAR	PM	SAR	iterative discharge	SAR+ΔΣM
area [mm²]	0.2 [a]	0.76	0.033	0.06	0.08	0.14 per channel	0.00644	0.0017	0.33 [b]
supply voltage [V]	0.3-1.8[g]	1.1	1.1/0.6[h]	1.1/0.6[h]	0.6	0.8	0.6 / 1	V_{HIGH}=1 / V_{LOW}=0.45	1.6 - 2
ENOB [bit]	7.0	11.8	12.1	12.34	7.76	11.7	7.7	7.9	18.7
cap range [pF]	0 - 30 [c]	0 -18.12	0-5	0-5	2.97-7.67	0-20	0.458-5.886	0.7-10.000	0 - 3.8
abs. resolution [fF]	67	1.24	1.1	0.29	6.19	2.345	6.98	12.3	0.0025
max meas. time [ms]	1,040	0.85	0.001	0.0125	0.02	0.482	0.01 – 1,000	0.019	100
power [d] [uW]	0.00137	3.11 [e] [f]	75 [f]	6.64 [e] [f]	0.0001 [f]	8.2 [f]	0.000044 [g]	1.84 [f]	3.24
energy/conv. [nJ]	1.42	2.64	0.075	0.083	0.0048	0.235	0.00094	0.035	324
SNDR [dB]	44.0	74.3	64.2	75.8	48.6	70.3	48.42	49.7	114.6
energy FoM [d] [pJ/c-s]	11.1	0.66	0.055	0.016	0.022	0.079	0.0043	0.14	0.74
calibration @ testing time needed	NO (self-calibration)	YES	NO	YES	3-point calibration	2-point calibration	2-point calibration	NO (self-calibration)	NO
current reference needed	NO	YES	NO	YES	NO	YES	NO	NO	NO
voltage regulation needed	NO	YES	YES (2 supplies)	YES	YES	YES	YES (2 supplies)	YES (2 supplies)	YES
linearity correction needed	NO	NO	NO	NO	NO	NO	YES	NO	NO

[a] Area assuming that an on-chip microcontroller can execute the self-calibration procedure (otherwise custom self-calibration block would add 0.3mm²)
[b] Whole readout, including voltage and temperature readout
[c] Tested from 2.5pF onwards, due to testing setup parasitics
[d] In the considered battery-less applications, power (not energy FoM) is the relevant metric for efficiency, since the harvester limits the instantaneous power
[e] Power does not include current reference
[f] Power does not include voltage regulation
[g] Power does not include linearity correction in the order of nWs (in 65nm LP process with HVT transistors, a single 8-bit adder/comparator has a leakage power of ~1nW)
[h] Analog/Digital supply
[i] Results in the table refer to nominal 0.3V supply.

Figure 5.2.6: Comparison table and summary of the state of the art.

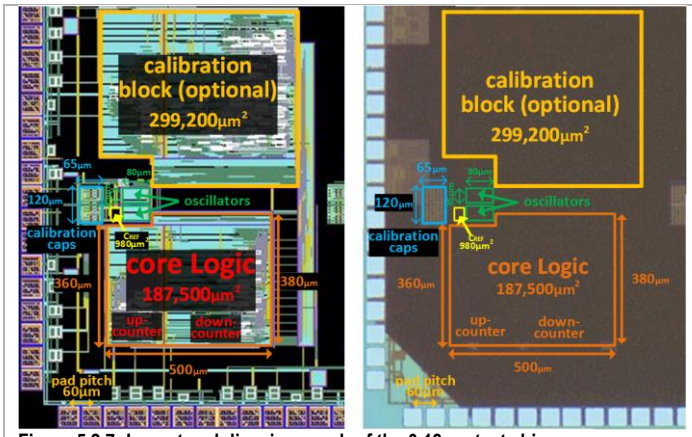

Figure 5.2.7: Layout and die micrograph of the 0.18µm test chip.