FPGA-Based Relaxation D/A Converters With Parasitics-Induced Error Suppression and Digital Self-Calibration

FPGA-Based Relaxation D/A Converters with Parasitics-Induced Error Suppression and Digital Self-Calibration

Roberto Rubino, *Graduate Student Member, IEEE,* Paolo Crovetti, *Senior Member, IEEE,* and Francesco Musolino, *Member, IEEE*

***Abstract*—In this paper, the implementation on a Field Programmable Gate Array (FPGA) of Relaxation Digital to Analog Converters (ReDACs), which take advantage of the impulse response of a first-order *RC* network to generate and combine binary weighted voltages, is addressed. For this purpose, the dominant ReDAC nonlinearity limitation related to the parasitics of the *RC* network is analyzed and a simple and robust technique for its effective suppression is proposed. Moreover, a ReDAC foreground digital calibration strategy suitable to FPGA implementation is introduced to tune the clock frequency of the converter, as requested for ReDAC operation. The novel error suppression technique and calibration strategy are finally implemented on a 13-bit, $514\,\mathrm{S/s}$ prototype (ReDAC1) and on a 11-bit, $10.5\,\mathrm{kS/s}$ prototype (ReDAC2), which are experimentally characterized under static and dynamic conditions. Measured results on ReDAC1 (ReDAC2) reveal $1.68\,\mathrm{LSB}$ $(1.53\,\mathrm{LSB})$ maximum INL, $1.54\,\mathrm{LSB}$ $(1.0\,\mathrm{LSB})$ maximum DNL, $76.4\,\mathrm{dB}$ $(67.9\,\mathrm{dB})$ THD, $79.7\,\mathrm{dB}$ $(71.4\,\mathrm{dB})$ SFDR and $71.3\,\mathrm{dB}$ $(63.3\,\mathrm{dB})$ SNDR, corresponding to 11.6 (10.2) effective bits (ENOB).**

***Index Terms*—D/A Converter (DAC), Relaxation D/A Converter (ReDAC), Field Programmable Gate Array (FPGA)**

I. Introduction

RECONFIGURABLE hardware platforms allowing fast deployment of integrated circuits (ICs) and systems are more and more often regarded as strategic assets to reduce time-to-market, design effort and development costs of ICs, so that to keep the pace of the increasing complexity of present day electronic systems and applications [1].

While digital Field-Programmable Gate Arrays (FPGAs) are extremely versatile and enable cost-effective prototyping and small/medium-scale production of most digital circuits of practical interest, reconfigurable analog platforms proposed in recent literature [2]–[4] are less attractive since they either target only specific analog blocks (e.g. filters or amplifiers) and/or do not achieve comparable performance with full-custom analog design in most of the cases.

In this framework, the digital-based implementation of analog and mixed-signal (AMS) interfaces, which has been explored in recent years to address the challenges of ultra-low voltage, energy- and area-efficient operation in nanoscale CMOS [5]–[10], paves the way to a new, flexible approach to fast AMS circuits prototyping, by enabling the seamless deployment of AMS and digital functions in a conventional FPGA and their possible mapping with consistent performance on application specific integrated circuits (ASICs), which can automatically be synthesized at minimum effort in a standard cell digital flow from the same hardware description language (HDL) source code developed for the FPGA prototype.

Under this perspective, FPGA-based Digital-to-Time Converters (DTCs) [11], Time-to-Digital Converters (TDCs) [12], Digital-to-Analog Converters (DACs) [13]–[17] and Analog-to-Digital Converters (ADCs) [18] have extensively been explored in the last years. Focusing on DACs, in particular, the limitations of FPGA converters based on digital-pulse width modulation (DPWM) [13], [14] and single-bit sigma-delta ($\Sigma\Delta$) modulation [15], [16], [19], have been recently addressed by Dyadic Digital Pulse Modulation (DDPM) [17] and by Relaxation DACs (ReDACs) [20]–[22].

In this scenario, ReDACs, which take advantage of the exponential impulse response of a first-order RC network to perform energy efficient, mismatch insensitive D/A conversion at medium-low sample rate (from kS/s up to MS/s) and medium (10-12bit) resolution, have been introduced first and demonstrated on an FPGA in [20]. The proof-of-concept FPGA-based ReDAC presented in [20], however, requires impractical manual calibration and its effective resolution (7 ENOB) and sample rate (400S/s) are severely limited by the parasitics of the RC network. Even if a ReDAC foreground self-calibration strategy suitable to on-chip implementation has been proposed in [22], this approach is not suitable to a conventional FPGA since it requires voltage controlled oscillator (VCO) cells and pass-gates.

In this paper, the major ReDAC linearity limitation related to the RC network parasitics is addressed, and a simple approach to fully suppress its dominant error contribution is proposed. Moreover, a novel fully digital foreground self-calibration strategy, suitable to FPGA implementation, is also introduced. The new error suppression technique and calibration strategy are finally implemented in two FPGA-based ReDACs operating at 514S/s (10.5kS/s) with 13 bit (11 bit) resolution, which are experimentally characterized for validation.

The paper has the following structure: in Section II, the relaxation D/A conversion technique and the ReDAC self-calibration concepts are revised. The main factors limiting the post-calibration accuracy of a practical ReDAC are then discussed in Section III, highlighting the critical role of RC network parasitics. In the same section, the high-order parasitic

Manuscript received April 19, 2005; revised August 26, 2015.

R.Rubino, P.S.Crovetti and F.Musolino are with the Department of Electronics and Telecommunications (DET), Politecnico di Torino, 10129 Torino, Italy. e-mail: {roberto_rubino,paolo.crovetti,francesco.musolino}@polito.it

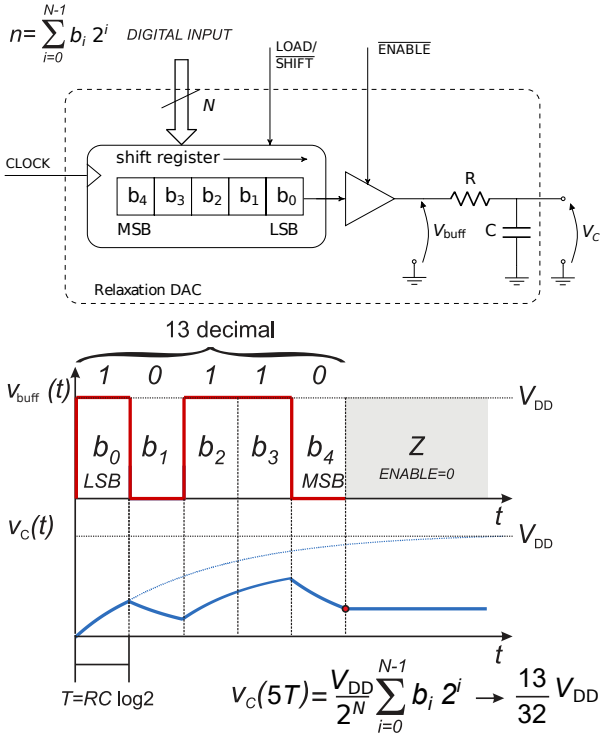

Fig. 1. Architecture of an $N = 5$ bits Relaxation DAC (ReDAC) and main waveforms.

effects of the RC network are analyzed in detail and a robust approach to suppress their dominant ReDAC error contribution is proposed. In Section IV, a new ReDAC self-calibration strategy, which is suitable to FPGA implementation and includes the error suppression approach presented in Section III, is then discussed. In Section V, two FPGA-based ReDAC prototypes featuring the solutions proposed in Sections III and IV are presented and their measured performance is reported in Section VI, where they are compared with previous ReDAC implementations and other FPGA-based DACs in the literature. Finally, some conclusions are drawn in Section VII.

II. Relaxation Digital-To-Analog Conversion Principle

A ReDAC [20], whose block diagram is shown in Fig.1, exploits the impulse response of a first-order *RC* network to convert an *N*-bit digital word n, expressed in terms of its binary representation $(b_{N-1}, \dots b_0)$ as

$$n = \sum_{i=0}^{N-1} b_i 2^i \tag{1}$$

into a proportional analog voltage.

For this purpose, the *RC* network is driven for $t \in [0, NT]$ by a three-state buffer with a voltage

$$v_{\text{buff}}(t) = V_{\text{DD}} \sum_{i=0}^{N-1} b_i \Pi\left(\frac{t}{T} - i - \frac{1}{2}\right) \tag{2}$$

where the unit pulse function $\Pi(x)$ is defined as

$$\Pi(x) = \begin{cases} 1 & |x| < \frac{1}{2} \\ \frac{1}{2} & |x| = \frac{1}{2} \\ 0 & |x| > \frac{1}{2}, \end{cases}$$

i.e. by a binary stream consisting of N rectangular pulses of width T and amplitude $V_{\text{DD}} b_i$ dependent on the logical value of the i^{th} bit in the digital word to be converted, and is left in high impedance for $t > NT$. Such a stream can easily be obtained by digital means, e.g. by a shift register initialized with the digital input word n at the beginning of the conversion, which is right-shifted at each clock cycle T, as shown in Fig.1.

Under the above hypotheses, the capacitor voltage $v_{\text{C}}(t)$ in the i^{th} clock cycle $[iT, (i+1)T]$ can be expressed in terms of the initial capacitor voltage $v_{C,i} = v_C(iT)$, of the steady-state voltage $v_{C,i}(\infty) = V_{\text{DD}} b_i$, equal either to V_{DD} or 0V depending on the corresponding bit b_i, and of the time constant $\tau = RC$ as:

$$v_{\text{C}}(t) = v_{C,i}(\infty)\left[1 - e^{-\frac{t-iT}{\tau}}\right] + v_{C,i} e^{-\frac{t-iT}{\tau}}. \tag{3}$$

Assuming[1] $v_C(0) = v_{C,0} = 0$ and iterating (3) for each clock cycle $i = 0 \dots N-1$, after N cycles:

$$v_{\text{C}}(NT) = V_{\text{DD}}\left(1 - e^{-\frac{T}{\tau}}\right) \sum_{i=0}^{N-1} b_i e^{-\frac{(N-1-i)T}{\tau}}. \tag{4}$$

As a consequence, if the clock period T is chosen so that

$$e^{-\frac{T}{\tau}} = \frac{1}{2} \quad \Rightarrow \quad T = \tau \log 2 = T^* \tag{5}$$

the capacitor voltage at the end of the N-th clock cycle is

$$v_{\text{C}}(NT^*) = \frac{V_{\text{DD}}}{2^N} \sum_{i=0}^{N-1} b_i 2^i = \frac{n}{2^N} V_{\text{DD}} = V_{\text{DAC}}(n) \tag{6}$$

and is proportional to the value of n expressed by (1), as expected in a DAC.

Under the hypotheses considered thus far, the ReDAC operation relies just on the ratio T/τ so that it is sufficient to tune the clock frequency to enforce the single condition (5) to enable robust, matching-insensitive D/A conversion over process, voltage and temperature variations, making this solution very attractive for implementation in nanoscale technologies. Moreover, the analysis of the effects of the deviations in the clock period T from T^* in (5), reveals that (5) can ideally be enforced by single-point foreground calibration strategy [20], as shortly revised in what follows.

A. Timing Error and ReDAC Calibration

If condition (5) is not exactly met and the clock period deviates from T^* by a fixed quantity $\Delta T = T - T^*$, the ReDAC is affected by a nonlinearity error (in LSB):

$$\varepsilon(n) = V_{\text{DAC}}(n)|_{T^*+\Delta T} \frac{2^N}{V_{\text{DD}}} - n \tag{7}$$

[1]Even if the assumption $v_C(0) = v_{C,0} = 0$ is considered in the derivation for the sake of illustration, it has been shown [20] that an initial capacitor voltage $v_C(0) = v_{C,0} \neq 0$ results in a negligible variation of the ReDAC output voltage of less than 0.5 LSBs. As a consequence, it is not necessary to discharge the capacitor before starting a conversion.

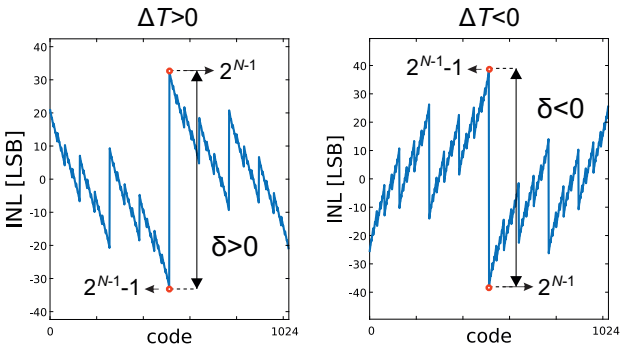

Fig. 2. Impact of the clock error ΔT on the ReDAC nonlinearity.

which, for small ΔT, can be expressed by series expansion of (7) around $T = T^*$ as

$$\begin{aligned}\varepsilon(n) &= 2\left(1-\frac{1}{2}e^{-\frac{\Delta T}{\tau}}\right)\sum_{i=0}^{N-1} b_i 2^i e^{-\frac{(N-1-i)\Delta T}{\tau}} - n \\ &\simeq \left(1+\frac{\Delta T}{\tau}\right)\sum_{i=0}^{N-1} b_i 2^i \left[1-(N-1-i)\frac{\Delta T}{\tau}\right] \\ &= \frac{\Delta T}{T^*}\cdot\log 2\cdot\left[n(2-N)+\sum_{i=0}^{N-1} 2^i i b_i\right]. \end{aligned} \quad (8)$$

The integral nonlinearity (INL) error due to ΔT, as exemplified in Fig.2, is maximum in magnitude at half swing, i.e. for codes $n = 2^{N-1}-1$ and $n = 2^{N-1}$, where it evaluates to

$$\varepsilon(2^{N-1}-1) = \left(-2^{N-1}+N\right)\log 2\cdot\frac{\Delta T}{T^*} \quad (9)$$

and

$$\varepsilon(2^{N-1}) = 2^{N-1}\log 2\cdot\frac{\Delta T}{T^*}, \quad (10)$$

respectively, resulting in a maximum differential nonlinearity (DNL) error

$$\delta = \mathrm{DNL}_{\max} = (2^N - N)\log 2\cdot\frac{\Delta T}{T^*} \simeq 2^N \log 2\cdot\frac{\Delta T}{T^*} \quad (11)$$

which is monotonically increasing with ΔT.

As pointed out in [20], the monotonic increase of δ with ΔT highlighted in (11) and in Fig.2 can be exploited for calibration purposes, by sensing the difference in DAC output voltages

$$\Delta V_{\mathrm{DAC}} = V_{\mathrm{DAC}}(2^{N-1}) - V_{\mathrm{DAC}}(2^{N-1}-1) \quad (12)$$

expressed as

$$\Delta V_{\mathrm{DAC}} = 1\mathrm{LSB}\cdot\left(1+2^N\log 2\cdot\frac{\Delta T}{T^*}\right) = (1+\delta)\mathrm{LSB} \quad (13)$$

and tune the clock period, reducing it if $\Delta V_{\mathrm{DAC}} > 0$ and increasing it if $\Delta V_{\mathrm{DAC}} < 0$ according to the procedure illustrated in Fig.3 until condition

$$\Delta V_{\mathrm{DAC}} = 0 \quad (14)$$

is enforced[2].

[2]Based on (8) it can be observed that for any couple of successive input codes 2^{N-I-1}, $2^{N-I-1}-1$ with $0 \le I < N-1$

$$\begin{aligned}\Delta V_{DAC,I} &= V_{DAC}(2^{N-I-1}) - V_{DAC}(2^{N-I-1}-1) \\ &= 1\mathrm{LSB}\cdot\left(1+2^{N-I}\log 2\cdot\frac{\Delta T}{T^*}\right)\end{aligned}$$

which has the same form of (13). As a consequence, the ReDAC can be calibrated in principle by enforcing $\Delta V_{\mathrm{DAC},I} = 0$ for any I. Anyway, at higher I the residual error can be controlled with less accuracy since the sensitivity of $\Delta V_{\mathrm{DAC},I}$ to ΔT decreases with I. The choice $I = 0$ considered in (13) and hereafter in the paper is therefore the most convenient.

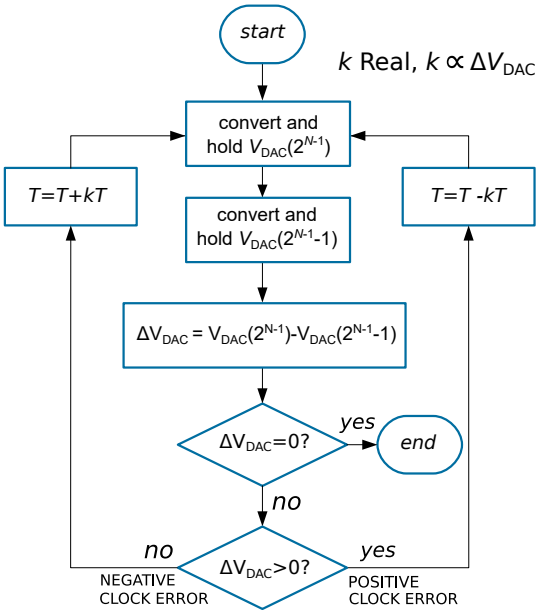

Fig. 3. ReDAC calibration principle [20].

Based on (13), such a condition is equivalent to

$$\Delta V_{\mathrm{DAC}} = 0 \rightarrow \delta = -1\mathrm{LSB} \quad (15)$$

with an error of 1LSB on N bits.

If condition (14) is imposed at $N+E$ bit resolution instead of at the nominal N bit resolution, the post-calibration ReDAC nonlinearity resulting from (15) can be made arbitrarily small (reduced by a factor 2^{-E}) so that condition (14) implies $\delta = 0$ and hence $T = T^*$. As a consequence, such a simple, single-point calibration strategy ideally enforces linear operation over the whole ReDAC input range $n \in [0, 2^N - 1]$.

In practice, the residual nonlinearity of IC and FPGA ReDACs after calibration can be degraded by several non-ideal effects, which will be analyzed in what follows to highlight the main ReDAC linearity limiting factor and to devise a simple strategy to effectively mitigate it. Moreover, the FPGA implementation of the ReDAC calibration strategy in Fig.3, which has not been proposed so far in the literature, will be presented in Section V. The new nonlinearity mitigation technique and the new self-calibration strategy will be then adopted in a new FPGA-based ReDAC.

III. ReDAC Nonlinearity Analysis and Mitigation

As outlined in [20], [21], non-idealities in practical ReDAC implementations, i.e. finite transition times t_{tr} of the digital buffer, finite resolution in the calibration process, random clock jitter δT, power supply noise, nonlinear loading effect in the output buffer, clock feedthrough, leakage in the output capacitor and in the three-state buffer during the hold phase, and the parasitics of the RC network, result in deviations from

the assumptions considered in Section II and give rise to noise and/or linearity errors in the ReDAC output voltage, even if condition (5) is nominally enforced by calibration.

While most ReDAC non-idealities can easily be made negligible at resolutions exceeding 10-12 bits by careful design without sacrificing performance and energy efficiency, the critical role played by the RC network parasitics, which turn out to be the main accuracy limiting factor, is highlighted in what follows with reference to the ReDAC design flow. Then, the effects of parasitics are analyzed in details and a simple approach for effective compensation is proposed.

A. ReDAC Accuracy and Design Tradeoffs

In ReDAC design, the clock period T should be large enough so that the transition times $t_{\rm tr}$ of the digital buffer are negligible compared to T at the target resolution, i.e.

$$\frac{t_{\rm tr}}{T} < \frac{1}{2^{N+1}} \quad \rightarrow \quad T > 2^{N+1} t_{\rm tr}. \tag{16}$$

This requirement limits the conversion time to

$$T_{\rm conv} > (N+\beta)T = (N+\beta)2^{N+1} t_{\rm tr} \tag{17}$$

where a $T_{\rm hold} = \beta T$ hold phase is assumed for each conversion. At $N = 10$ bit resolution, condition (17) is compatible with a ReDAC sample rate in the MS/s range for IC implementations ($t_{\rm tr}$ in the 10ps range) and in the tens of kS/s range for discrete component implementations ($t_{\rm tr}$ in the ns range).

The duration of the hold phase is limited by the capacitor voltage droop error, mainly related to the leakage of the three-state buffer in high impedance and to the capacitor self-discharge current. To keep the droop error at the end of the hold phase below 0.5 LSB, in particular, it should be

$$T_{\rm hold} < \frac{CV_{\rm DD}}{2^{N+1} I_{\rm leak,max}}$$

where $I_{\rm leak,max}$ is the maximum overall leakage current. In the following, $T_{\rm hold} = \beta T$ with $\beta = 2$ is chosen for the ReDACs considered in the experiments, which results in negligible droop in the hold phase at the target resolution, component values and test conditions.

A further limitation to the minimum clock cycle T is related to the resolution $\Delta T_{\rm res}$ at which (5) can be enforced [20]. If T is obtained by counting an integer number of periods of a higher frequency clock $T_{\rm clk}$, in particular, $\Delta T_{\rm res} = T_{\rm clk}$ and, based on (10), $T_{\rm clk}/T$ needs to be less than $1/(2^N \log 2)$, which demands $T > 2^N \log 2 \cdot T_{\rm clk}$. Such a limitation, however, can be overcome by high resolution frequency division techniques available in most FPGAs [23], or by fine-tuning the control voltage of a voltage controlled oscillator (VCO) in the calibration phase, as in [22].

Moreover, based on (8) and on the analysis in [20], random jitter in the ReDAC period T gives rise to random fluctuations in the output voltage with a code-dependent root mean square (r.m.s.) value $\sigma_{V_{\rm DAC}}(n)$, which is maximum for $n = 2^{N-1}$, where it can be expressed in terms of the r.m.s. jitter σ_T on T as

$$\sigma_{V_{\rm DAC}}(2^{N-1}) = \frac{\sigma_T}{T} \cdot \log 2 \cdot \frac{V_{\rm DD}}{2}.$$

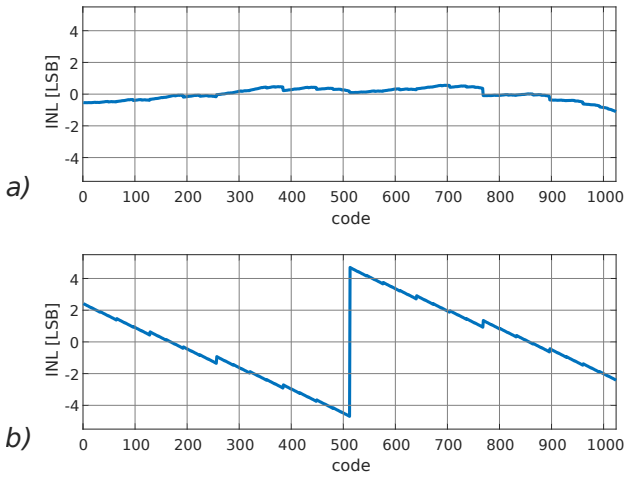

Fig. 4. Simulated INL of a calibrated 10bit, 2MS/s ReDAC in 40nm, with $R = 144\,\text{k}\Omega$ and $C = 444\,\text{fF}$ for: a) an ideal RC network driven by a transistor-level model of the ReDAC, b) a realistic RC network model with parasitics, driven by an ideal voltage source. The larger INL in b) compared to a) reveals the dominance of the error contribution due to parasitics.

For σ_T in the ps-range, which can easily be achieved by a crystal oscillator in the tens of megahertz range, the effect of clock jitter is compatible with ReDACs operating in the MS/s range with an effective resolution exceeding 13 bits. An even higher jitter-limited ReDAC resolution is achieved in FPGA-based ReDACs in which a larger $T = M \cdot T_{\rm clk}$ is obtained by counting M cycles of a higher frequency clock $T_{\rm clk}$ and[3]

$$\frac{\sigma_T}{T} = \frac{\sigma_{T_{\rm clk}}}{T_{\rm clk}} \frac{1}{\sqrt{M}}.$$

The effect of jitter can be more critical when T is not derived from a crystal oscillator, even if effective jitter-limited ReDAC resolutions exceeding 10 bits are rather easy to be achieved at several kS/s [20].

Having fixed T, since there is no matching requirement in a ReDAC, the capacitance C can be designed close to the thermal noise limit (i.e. in the sub-pF range at 10 bit resolution), as discussed in [21] for high energy efficiency and small area and the resistance R can be final designed as

$$R = \frac{\tau}{C} = \frac{T}{C \log 2}. \tag{18}$$

to get a time constant τ meeting condition (5) at a ReDAC clock cycle T.

Based on (18), for a 10 bit ReDAC R should be in the $100\,\text{k}\Omega$ range for IC implementations and in the $1\,\text{M}\Omega$ for discrete component implementations. Even if these values are compatible with IC and discrete component technologies and make the nonlinear loading effect on the output buffer negligible for buffers with an output resistance in the $10 - 100\,\Omega$ range, being R relatively large, the distributed parasitic capacitance $C_{\rm par}$ of the resistor can easily be comparable with C and gives rise to significant deviations from the ideal first-order RC behavior assumed in Section II, resulting in the dominant contribution to the ReDAC nonlinearity.

[3] A random gaussian clock jitter is assumed.

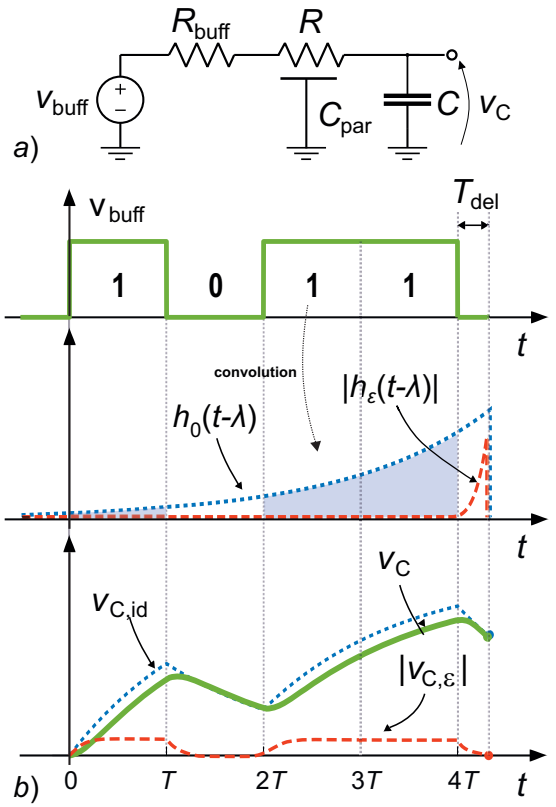

Fig. 5. a) RC distributed model driven by the Thevenin equivalent of the threestate buffer. b) Convolution of the digital word 1101 with the first order and the second order impulse response

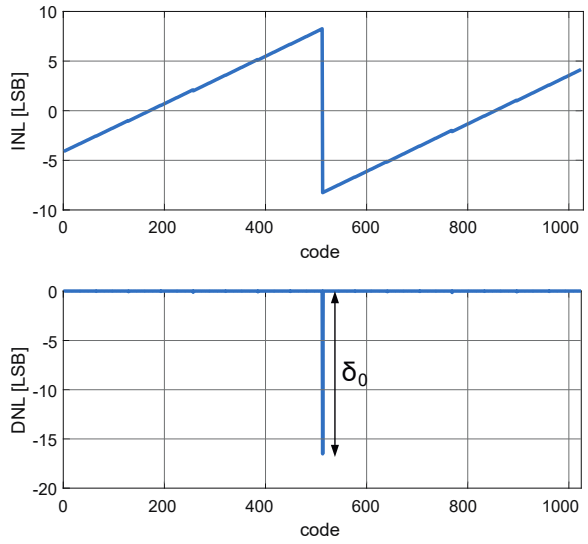

Fig. 6. INL and DNL errors due to higher-order parasitics of the RC network for a ReDAC implementation in 40nm with a Hi-res poly resistor ($R = 144\,\mathrm{k\Omega}$) total parasitic capacitance towards the substrate ($C_{\mathrm{par}} = 36\,\mathrm{fF}$) and a MiM capacitor $C = 444\,\mathrm{fF}$, for which the ReDAC operation condition (5) is exactly met for the dominant time constant τ_0, i.e. $T = \tau_0 \log 2$.

The dominance of ReDAC errors related to the RC parasitics can clearly be observed in Fig.4, where the residual INL after clock period calibration of a 10bit, 2MS/s ReDAC in 40nm, simulated at transistor level with and ideal RC network (which is affected by all non-idealities except those due to the RC network parasitics), reported in Fig.4a, is more than 5X smaller compared to the INL after clock period calibration of the same ReDAC, in which the parasitics of the RC network are properly taken into account and the buffer is modelled by an ideal square-wave voltage source (which is affected only by the errors related to the RC network parasitics), and is reported in Fig.4b for comparison.

The problem can be mitigated by reducing R under constant $\tau = RC$, thus increasing C much above the minimum dictated by thermal noise. This solution, however, is not satisfactory, since the higher robustness to parasitics is traded off with increased power, area and nonlinear loading effect in the digital buffer, which in turns limits the ReDAC accuracy. It can be therefore concluded that the parasitic distributed capacitance of the resistor is a key limiting factor in the ReDAC design. In view of that, the effects of parasitics will be analyzed and their mitigation will be addressed in what follows.

B. RC Network Parasitics

The effects of the distributed parasitic capacitance C_{par} of the resistor R can be described analyzing the ReDAC *RC* network as an RC transmission line driven by a voltage source with internal resistance[4] R_{buff}, and loaded by the capacitor C, as depicted in Fig.5a. With reference to such a circuit, the linear transfer function $H(s) = V_{\mathrm{c}}(s)/V_{\mathrm{buff}}(s)$ is no longer first-order, as assumed in Section II, and it can be expressed as [24]:

$$H(s) = \frac{1}{(1 + sCR_{\mathrm{buff}})\cosh\gamma + \left(\frac{R_{\mathrm{buff}}}{Z_0} + sCZ_0\right)\sinh\gamma} \tag{19}$$

where $\gamma = \sqrt{RC_{\mathrm{par}}s}$ and $Z_0 = \sqrt{\frac{R}{sC}}$, and can be conveniently approximated as a Q^{th} order low-pass transfer function:

$$H(s) = \prod_{k=0}^{Q} \frac{1}{s\tau_k + 1} = \sum_{k=0}^{Q} \frac{a_k}{s\tau_k + 1} \tag{20}$$

where

$$a_k = \prod_{h \neq k} \frac{1}{1 - \frac{\tau_k}{\tau_h}} \tag{21}$$

are the residues of the poles of $H(s)$.

By expanding in series the denominator of (19), the dominant time constant τ_0 in (20) can be expressed as [24]:

$$\tau_0 = (R + R_{\mathrm{buff}})\left(C + \frac{C_{\mathrm{par}}}{2}\right) + \frac{1}{2}C_{\mathrm{par}}R_{\mathrm{buff}} \tag{22}$$

and basically corresponds to the time constant τ of the ideal RC circuit, in which one half of the total parasitic capacitance C_{par} of the resistor is added to C and the output resistance

[4]being the output resistance of the buffer nonlinear, R_{buff} should be regarded as its best linear approximation, which can be roughly estimated from the standard electrical parameters of a digital buffer as $R_{\mathrm{buff}} \simeq \frac{V_{\mathrm{DD}} - V_{\mathrm{OH,min}}}{I_{\mathrm{OH,max}}} \simeq \frac{V_{\mathrm{OL,max}}}{I_{\mathrm{OL,max}}}$

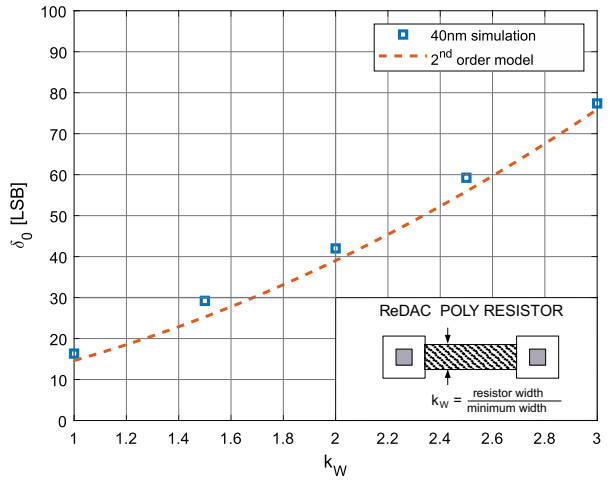

Fig. 7. Maximum DNL error δ_0 as a function of resistor width normalized w.r.t. minimum technology width.

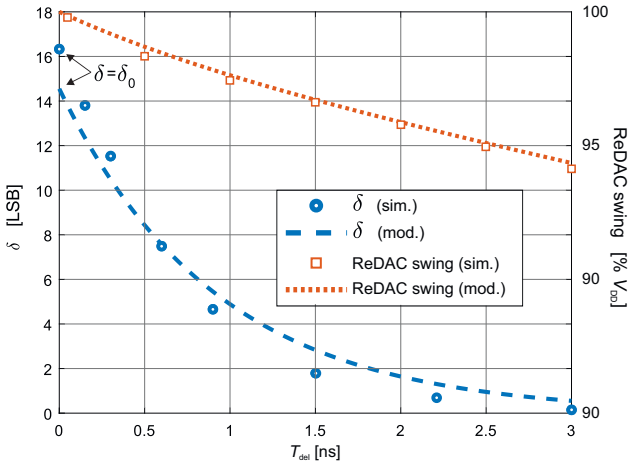

Fig. 8. Maximum DNL δ as a function of $T_{\rm del}$, and the correspondent DAC swing attenuation.

of the buffer $R_{\rm buff}$ is added to R, and the first non-dominant time constant can be expressed as

$$\tau_1 = \frac{1}{6}(3R_{\rm buff} + R)\, C_{\rm par} \simeq \frac{1}{6}\frac{C_{\rm par}}{C}\tau_0 \qquad (23)$$

where the last approximation holds assuming $R_{\rm buff} \ll R$ and $C_{\rm par} \ll C$ both in (22) and in (23).

Based on (20), the impulse response of the capacitor voltage, normalized with respect to the residue of the dominant pole, can be written as

$$\begin{aligned} h(t) &= \mathrm{e}^{-\frac{t}{\tau_0}} + \sum_{k=1}^{Q} \frac{a_k}{a_0}\mathrm{e}^{-\frac{t}{\tau_k}} \\ &= h_0(t) + h_\varepsilon(t) \end{aligned} \qquad (24)$$

where h_0 can be regarded as the impulse response of an ideal first-order RC network, as in Section II, with $\tau = \tau_0$, whereas $h_\varepsilon(t)$ is the error term due to the distributed parasitic capacitance of the resistor.

Based on (24), in particular, the ReDAC capacitor voltage can be expressed as the convolution product of the buffer output stream (2) during the conversion and the impulse response h as:

$$v_{\rm C}(t) = (v_{\rm buff} * h)(t) = \underbrace{(v_{\rm buff} * h_0)(t)}_{v_{\rm C,id}(t)} + \underbrace{(v_{\rm buff} * h_\varepsilon)(t)}_{v_{\rm C,\varepsilon}(t)} \qquad (25)$$

where the first term $v_{\rm C,id}(t)$, analogous to (3), is the capacitor voltage of a ReDAC with an ideal first-order RC network with $\tau = \tau_0$ and $v_{\rm C,\varepsilon}(t)$ is the error due to the parasitic high-order terms, as illustrated in Fig.5b (red dashed curve), and results in a ReDAC conversion error (in LSBs)

$$\varepsilon_{\rm par}(n) = v_{\rm C,\varepsilon}(NT)\frac{2^N}{V_{\rm DD}}. \qquad (26)$$

With reference to a 10-bit ReDAC, based on an RC network with $R = 144\,\mathrm{k\Omega}$, $C = 444\,\mathrm{fF}$, $C_{\rm R} = 36\,\mathrm{fF}$, $R_{\rm buff} = 4.2\mathrm{k\Omega}$ (design values considered in [21]), limiting the expansion to $Q = 2$:

$$\tau_0 = 68.5\,\mathrm{ns}, \quad \tau_1 = 0.94\,\mathrm{ns}, \quad \frac{a_1}{a_0} = 0.014 \qquad (27)$$

and the mid-range worst-case ReDAC DNL error δ_0 due to the RC network parasitics only, assuming that the ReDAC clock period is fixed to $\tau_0 \log 2$, thus meeting condition (5) for the dominant time constant τ_0, can be expressed as:

$$\begin{aligned} \delta_0 &= \varepsilon_{\rm par}(2^{N-1}) - \varepsilon_{\rm par}(2^{N-1} - 1) \\ &\simeq -2^N \frac{a_1}{a_0} - 1 \simeq -15\,\mathrm{LSB} \end{aligned} \qquad (28)$$

and is close to the worst-case DNL of $-16.33\,\mathrm{LSB}$ predicted by simulations of the full ReDAC at transistor level shown in Fig.6, thus confirming the dominant effect of the RC network parasitics to the ReDAC nonlinearity. This is also confirmed by the results presented in Fig. 7, where δ predicted by (28) is also compared with transistor-level simulations under the same total R and C, for different normalized width $k_{\rm W} = W/W_{\rm min}$ of the polysilicon resistor, which results in different per unit length parasitic capacitance.

C. Nonlinearity compensation strategy

The insight into the ReDAC nonlinearity error due to the parasitic high-order response of the RC network, which has been gained in the previous Subsection, is now exploited to reduce this dominant ReDAC error contribution.

Based on (25), if the ReDAC buffer output in Fig.1 is not put in high impedance immediately at $t = NT$, but it is driven low for $t > NT$, the nominal ReDAC output voltage for $t > NT$ can be expressed as

$$\begin{aligned} &(v_{\rm buff} * h_0)(NT + t) = \\ &\quad = \int_{-\infty}^{\infty} v_{\rm buff}(\lambda) e^{-\frac{NT+t-\lambda}{\tau_0}} d\lambda \\ &\quad = e^{-\frac{t}{\tau_0}} \int_{-\infty}^{\infty} v_{\rm buff}(\lambda) e^{-\frac{NT-\lambda}{\tau_0}} d\lambda \\ &\quad = v_{\rm C,id} \cdot e^{-\frac{t}{\tau_0}} \end{aligned} \qquad (29)$$

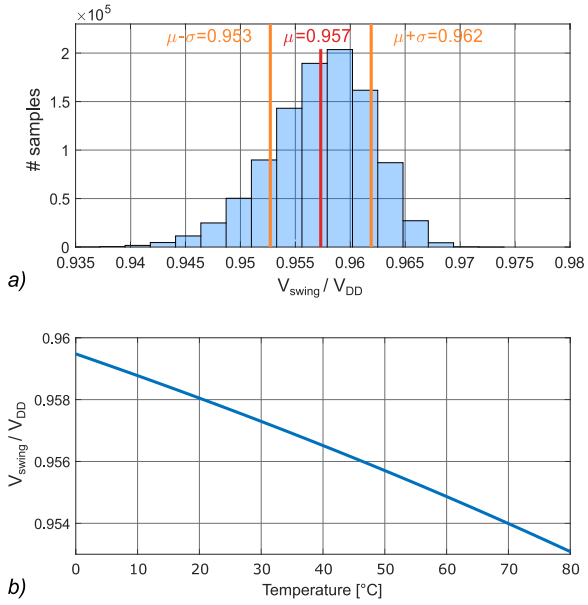

Fig. 9. a) Statistical distribution of the attenuation under variations of R and C obtained by Monte Carlo simulations (10^6 runs) and b) swing attenuation variation related to temperature variations from 0°C to 80°C.

whereas the error term on the ReDAC capacitor voltage

$$\begin{aligned} v_{\mathrm{C},\varepsilon}(NT+t) &= (v_{\mathrm{buff}} * h_\varepsilon)(NT+t) \\ &= \int_{-\infty}^{\infty} v_{\mathrm{buff}}(\lambda) \sum_{k=1}^{Q} \frac{a_k}{a_0} e^{-\frac{NT+t-\lambda}{\tau_k}} \mathrm{d}\lambda \\ &= \sum_{k=1}^{Q} e^{-\frac{t}{\tau_k}} \underbrace{\frac{a_k}{a_0} \int_{-\infty}^{\infty} v_{\mathrm{buff}}(\lambda) e^{\frac{-NT+\lambda}{\tau_k}} \mathrm{d}\lambda}_{v_{C,\varepsilon,k}} \\ &= \sum_{k=1}^{Q} v_{\mathrm{C},\varepsilon,k} \cdot \mathrm{e}^{-\frac{t}{\tau_k}} \end{aligned} \tag{30}$$

can be expressed as the sum of the error components $v_{C,\varepsilon,k}$ associated to the non-dominant time constants τ_k of the RC network, which decay exponentially in time as $\mathrm{e}^{-\frac{t}{\tau_k}}$.

Based on (29) and (30), since the first non-dominant time constant τ_1 given by (23) is orders of magnitude smaller than τ_0 in practice, if the ReDAC output buffer is driven low at $t = NT$ and is put in high impedance at time $t = NT + T_{\mathrm{del}}$, with a delay T_{del} so that

$$3\tau_1 \simeq T_{\mathrm{del}} \ll \tau_0, \tag{31}$$

it follows that

$$\begin{aligned} v_C(NT+T_{\mathrm{del}}) &= v_{\mathrm{C,id}} \cdot e^{-\frac{T_{\mathrm{del}}}{\tau_0}} + \sum_{k=1}^{Q} v_{\mathrm{C},\varepsilon,k} \cdot e^{-\frac{T_{\mathrm{del}}}{\tau_k}} \\ &\simeq v_{\mathrm{C,id}} \cdot e^{-\frac{T_{\mathrm{del}}}{\tau_0}} \end{aligned} \tag{32}$$

in which the ideal ReDAC component $v_{\mathrm{C,id}}$ is attenuated by a negligible factor

$$e^{-\frac{T_{\mathrm{del}}}{\tau_0}} \simeq e^{-\frac{3\tau_1}{\tau_0}} \simeq 1,$$

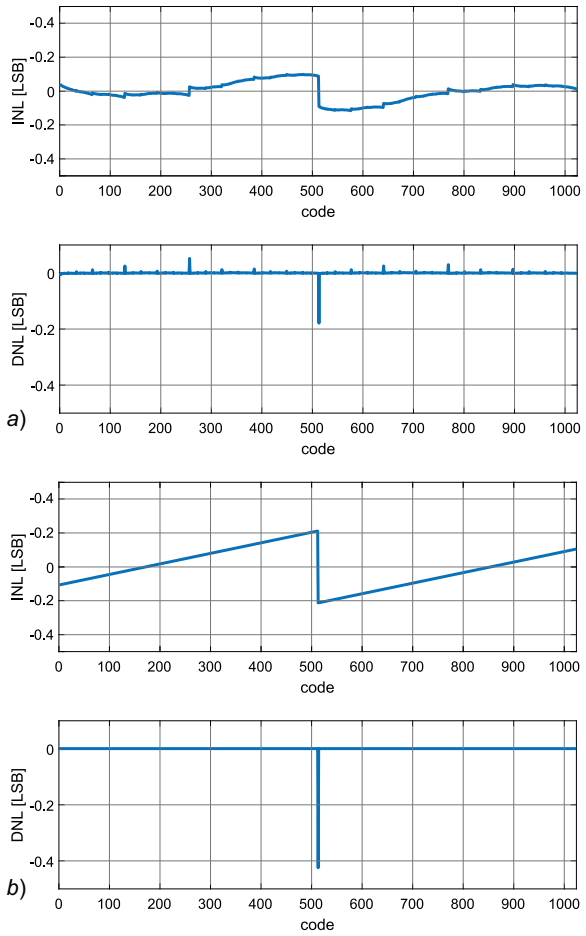

Fig. 10. ReDAC INL and DNL characteristics under $T_{\mathrm{del}} = 3.13\,\mathrm{ns}$, corresponding to the minimum T_{del} which is sufficient to reduce the error contribution due to the high-order parasitics below 0.5 LSB: a) evaluated based on time-domain transistor-level simulations in 40nm CMOS and b) evaluated based on the model in (32).

whereas the error components are strongly attenuated by at least $\mathrm{e}^{-3} \simeq 0.05$, becoming negligible in practice. The effectiveness of the proposed approach in suppressing the ReDAC error related to parasitics can be observed in Fig.8, where the maximum ReDAC DNL error δ simulated at transistor level including the parasitics of the RC network is plotted versus T_{del}, revealing exponential decay in fair agreement with (32) at negligible signal attenuation.

With reference to the numerical values in (27), with $T_{\mathrm{del}} = 3\tau_1 = 2.82\,\mathrm{ns}$, the ideal ReDAC component is attenuated by only 0.959, whereas the error component is reduced to 0.05 of its original value, i.e. to $7.3 \cdot 10^{-4}$ of the ReDAC full swing or 0.7 LSB at 10 bit resolution. It is also worth observing that, as far as $\tau_0 \gg \tau_1$, T_{del} does not need to be precisely controlled: in the above example, for instance, a 10% larger T_{del} results in a 0.04 reduction (compared to 0.05) in the dominant error component and in a 0.956 attenuation (compared to 0.959) of the nominal signal component, which does not affect the ReDAC linearity and corresponds to a gain error of only 0.03dB and to a maximum absolute error at full swing of 4LSBs. The approach is therefore robust to technology-related variations in the values of parasitics and

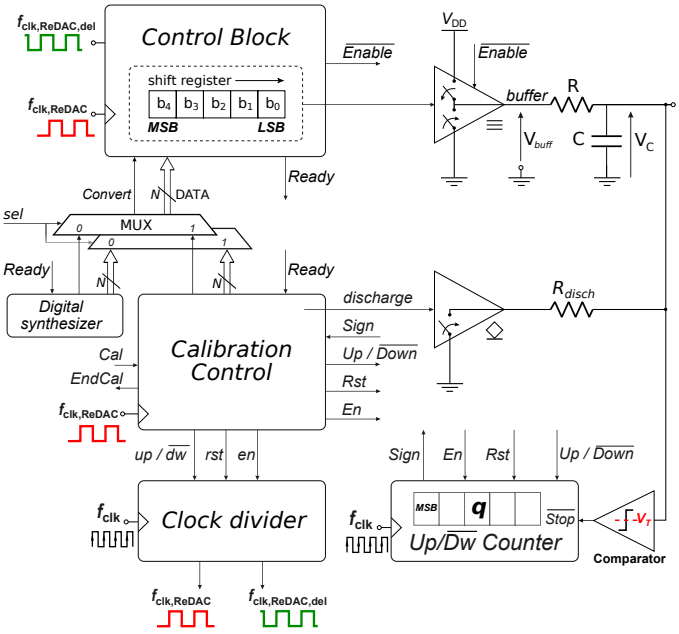

Fig. 11. Block diagram of the ReDAC with calibration circuit

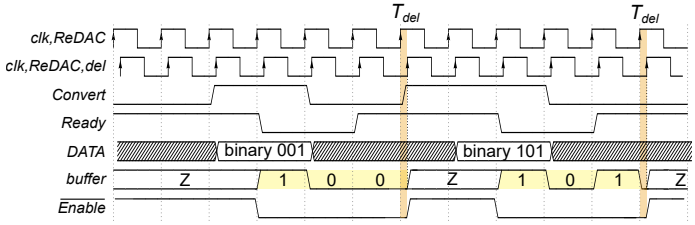

Fig. 12. Timing diagram of the ReDAC Control block operation, example for $N = 3$bit

fairly insensitive to fabrication tolerances and temperature variations in R and C, as observed in Fig.9, where the statistical distribution of the nominal signal attenuation under process variations (Fig.9a) and over temperature (Fig.9b) is reported for the above ReDAC design example, based on the process parameters of a minimum-width Hi-res poly resistor and of a MiM capacitor.

The proposed error suppression strategy can easily be implemented both in IC and FPGA-based ReDACs, just forcing the output of the buffer in Fig.1 low at the end of the MSB conversion and then driving it in the high impedance mode after a sub-clock cycle delay $T_{\rm del}$, both in the normal operation and in the calibration phase.

Based on (32), the ReDAC error due to the parasitics can be imposed to be less than one half LSB by enforcing

$$\delta_0 \cdot \mathrm{e}^{-\frac{T_{\rm del}}{\tau_1}} \leq \frac{1}{2}\mathrm{e}^{-\frac{T_{\rm del}}{\tau_0}}$$

i.e. for

$$T_{\rm del} > \frac{\tau_0\tau_1}{\tau_0 - \tau_1}\log(2\delta_0) \qquad (33)$$

which corresponds to $T_{\rm del} > T_{\rm del,min} = 3.13\,\mathrm{ns}$ for the ReDAC design discussed so far. The ReDAC INL characteristics obtained for $T_{\rm del} = T_{\rm del,min}$ evaluated by transistor-level simulations and by the model in (32) are reported in Fig.10 and reveal the effectiveness of the proposed approach.

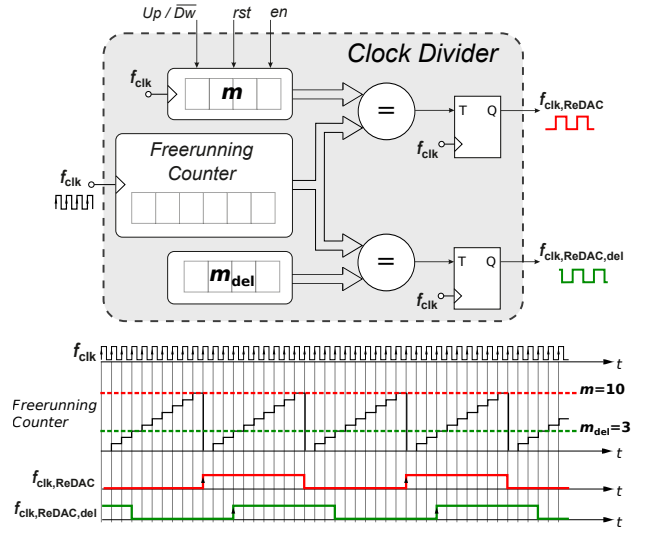

Fig. 13. Generation of ReDAC clock period $T = 2m/f_{\rm clk}$ and the $T_{\rm del} = m_{\rm del}/f_{\rm clk}$ delayed period

IV. FPGA-BASED REDAC SELF-CALIBRATION

While an IC implementation of the ReDAC self-calibration strategy in Section IIA has been proposed in [22], that approach does not include the parasitic-induced error suppression technique discussed in Section III and is not suitable to direct synthesis on FPGA, since it is based on voltage-controlled oscillators (VCOs) not available in standard FPGAs. A new calibration architecture, which is suitable to be implemented in an FPGA-based ReDAC, and which includes the novel error suppression strategy described above is therefore introduced in this Section.

A. Self-Calibration Module Architecture

The architecture of the proposed ReDAC with self-calibration module is shown in Fig.11. Here, the ReDAC Control Block starts the conversion of the digital input (DATA), generated by an external digital synthesizer (during normal operation) or by the Calibration Control block (during calibration), at the first active edge of $f_{\rm clk,ReDAC}$ after the *Convert* signal is asserted, as illustrated in Fig.12. Both the ReDAC and the Calibration Control blocks are operated at a clock frequency $f_{\rm clk,ReDAC}$ obtained from the system clock $f_{\rm clk}$ of the FPGA by a divide-by-$2m$ frequency divider, implemented by a free-running counter[5], that toggles the ReDAC clock when the count reaches the terminal count m, as shown in Fig.13.

[5]It is assumed that the ratio $f_{\rm clk}/f_{\rm clk,ReDAC}$ is high enough so that the ReDAC clock frequency can be tuned with a resolution comparable to the target ReDAC resolution, as discussed in [20]. Even if a finer time resolution could be achieved by fractional-N PLLs normally available in FPGAs, a binary counter, which limits the time resolution in T to $T_{\rm clk} = 1/f_{\rm clk}$, is considered in this paper for a platform-independent implementation and for the sake of simplicity.

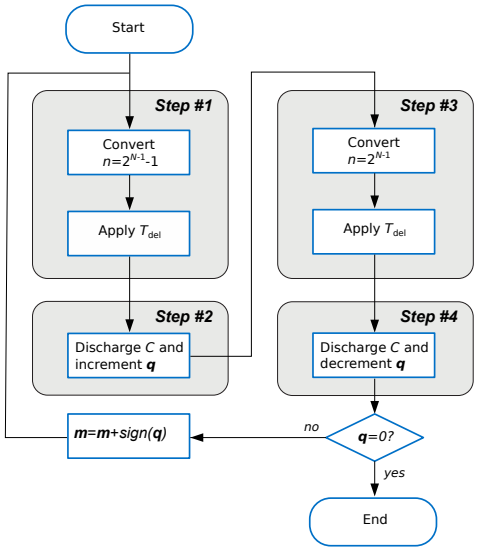

Fig. 14. FPGA calibration flowchart.

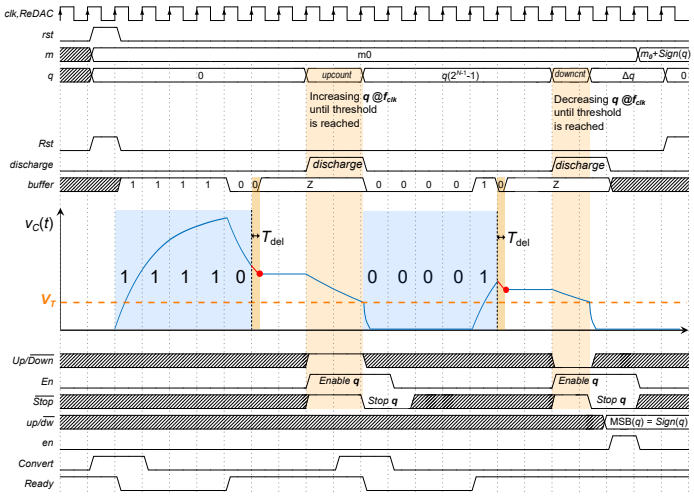

Fig. 15. FPGA-based ReDAC self-calibration timing diagram, for an $N = 5$bit converter.

The frequency division factor m is initialized to $m = m_0 = \lceil f_{\rm clk} T^*/2 \rfloor$ so that to meet the ReDAC requirement (5) for the nominal values of $f_{\rm clk}$, R, C, and then is fine-tuned by the proposed self-calibration procedure to precisely enforce (5) in the presence of tolerances and drifts in passive components and in the output buffer, as described in what follows.

The same free-running counter is exploited to generate a delayed clock (clk,ReDAC,del) at $f_{\rm clk,ReDAC}$, as required in the error suppression strategy presented in Section III. For this purpose, the delayed clock is toggled when the counter crosses a second threshold $m_{\rm del}$, i.e. $T_{\rm del} = m_{\rm del} T_{\rm clk}$, after the main ReDAC clock is toggled.

The self-calibration module also includes a capacitor discharging network, consisting of a resistor $R_{\rm disch}$ driven by an open-drain digital buffer, a voltage comparator and an up/down counter operated at $f_{\rm clk}$, which are employed as a non-linear single-slope ADC, driven by the calibration control unit (finite state machine), to compare two ReDAC voltages, as requested in the calibration strategy in Section II and discussed in what follows with reference to the flow chart in Fig.14.

B. Self-Calibration Procedure

At the first step of the self-calibration procedure, the ReDAC operates at frequency $f_{\rm clk,ReDAC} = f_{\rm clk}/2m_0$ and converts the digital input $2^{N-1} - 1$. After the conversion of the MSB, the buffer is driven low on the rising edge of the ReDAC clock and then is put in high impedance on the rising edge of the delayed clock, i.e. after $T_{\rm del}$ (red dot in Fig.15) to implement the error suppression strategy discussed in Section III.

At the next active edge of $f_{\rm clk}$ (second step), the up/down counter is enabled in up count mode and the discharging network is activated, thus connecting $R_{\rm disch}$ in parallel to the ReDAC output capacitor. As a consequence, the capacitor, initially charged at $V_{\rm DAC}(2^{N-1} - 1)$, is discharged with a time constant $\tau_{\rm disch} = R_{\rm disch} C$, until its voltage reaches the comparator threshold $V_{\rm T} < V_{\rm DAC}(2^{N-1})$, which terminates the discharge and disables the counter. The content q of the counter at the end of the second calibration step is therefore

$$q(2^{N-1} - 1) = \lfloor T_{\rm disch}(2^{N-1} - 1) f_{\rm clk} \rfloor$$

and is proportional to the quantized discharge time

$$T_{\rm disch}(2^{N-1} - 1) = \tau_{\rm disch} \cdot \log \left[\frac{V_{\rm DAC}(2^{N-1} - 1)}{V_{\rm T}} \right], \quad (34)$$

which is in turn a nonlinear, monotonic function of $V_{\rm DAC}(2^{N-1} - 1)$.

In the third calibration step, the same operations performed in the first step for the input code $2^{N-1}-1$, are repeated for the input code 2^{N-1} and in the fourth step, the discharge network is activated as done in the second step, but with the up/down counter enabled in down count mode, till the capacitor voltage crosses $V_{\rm T}$, i.e. after

$$T_{\rm disch}(2^{N-1}) = \tau_{\rm disch} \cdot \log \left[\frac{V_{\rm DAC}(2^{N-1})}{V_{\rm T}} \right]. \quad (35)$$

Neglecting time quantization, the content of the up/down counter at the end of the fourth calibration step is therefore proportional to the signed difference of the discharge times in the second and fourth calibration step, i.e.

$$\begin{aligned} \Delta q &= q(2^{N-1} - 1) - q(2^{N-1}) \\ &= f_{\rm clk} \lfloor T_{\rm disch}(2^{N-1} - 1) - T_{\rm disch}(2^{N-1}) \rfloor \\ &\simeq -f_{\rm clk} \tau_{\rm disch} \cdot \log \left[\frac{V_{\rm DAC}(2^{N-1})}{V_{\rm DAC}(2^{N-1} - 1)} \right], \end{aligned} \quad (36)$$

and it is zero if and only if

$$\Delta V_{\rm DAC} = V_{\rm DAC}(2^{N-1}) - V_{\rm DAC}(2^{N-1} - 1) = 0, \quad (37)$$

whereas it is positive (negative) if $\Delta V_{\rm DAC} < 0$ ($\Delta V_{\rm DAC} > 0$).

Being $\Delta V_{\rm DAC}$ related to the ReDAC clock error ΔT by (13), as discussed in Section II, $\Delta q = 0$ implies that the condition (5) on the ReDAC clock period is properly met (within 1LSB ReDAC error) and the calibration procedure can be terminated. Otherwise, the frequency division factor m of the divider which generates the ReDAC clock is updated

according to Δq (i.e., it is decreased (increased) if $\Delta q > 0$ ($\Delta q < 0$)) so that to enforce (5). The calibration steps 1-4 are then repeated until $\Delta q = 0$.

With the notations used in (17), the duration of each calibration step, which includes two conversions and two discharge periods, can be expressed as

$$T_{\rm cs} \simeq 2 \cdot [(N+\beta)T^* + T_{\rm disch}(2^{N-1})]. \qquad (38)$$

At each calibration cycle the value of m is updated of ± 1, so that the number of steps $\#cs$ required to complete the calibration process is equal to the difference $\#cs = |m_0 - m^*|$ between the initial guess m_0 of the frequency division factor and the value m^* achieving (5). Once the ReDAC is calibrated, a few steps of the same calibration procedure can be periodically repeated to compensate possible deviations from (5) due to temperature variations in R and C provided that temperature variations are slow enough and re-calibration time slots can be scheduled. Post-calibration ReDAC errors due to temperature variations in R and C can be also limited either by using discrete components with an intrinsically low thermal drift (a thermal drift in R and C in the $10\text{ppm}/^\circ\text{C}$ range is sufficient, based on (26), to keep the worst-case INL variations below 2LSB at 12-bit ReDAC resolution over the whole $0^\circ\text{C} - 70^\circ\text{C}$ temperature range) or by using a primary frequency reference $f_{\rm clk}$ tracking the ReDAC RC temperature variations (e.g. a relaxation oscillator in which the frequency is set by a resistor and a capacitor of the same type).

C. Self-Calibration Module Design

The capacitor discharge network in the self-calibration module can be designed considering that the difference in the discharge times in (34) and (35)

$$\begin{aligned} \Delta T_{\rm disch} &= T_{\rm disch}(2^{N-1}) - T_{\rm disch}(2^{N-1}-1) \\ &= \tau_{\rm disch} \log \frac{V_{\rm DAC}(2^{N-1})}{V_{\rm DAC}(2^{N-1}-1)} \simeq \tau_{\rm disch} 2^{-N+1} \end{aligned}$$

needs to be larger than the time resolution $T_{\rm clk}$ of the time-to-digital conversion in calibration steps #2 and #4 which, for a given $T_{\rm clk}$, requires

$$\tau_{\rm disch} = R_{\rm disch} C > T_{\rm clk} 2^{N-1}. \qquad (39)$$

The comparator threshold $V_{\rm T}$ does not need to be set to a precise value, provided that it does not vary during calibration and that both $V_{\rm DAC}(2^{N-1}-1)$ and $V_{\rm DAC}(2^{N-1})$ are above $V_{\rm T}$ even in the presence of large initial error in the ReDAC period ΔT. Once the discharge time and $V_{\rm T}$ are fixed, the bit width of the counter q can finally be designed to accommodate a value greater than the number of clock periods in the discharge period

$$q > f_{\rm clk} T_{\rm disch}(2^{N-1}) \simeq f_{\rm clk} T_{\rm disch}(2^{N-1}-1).$$

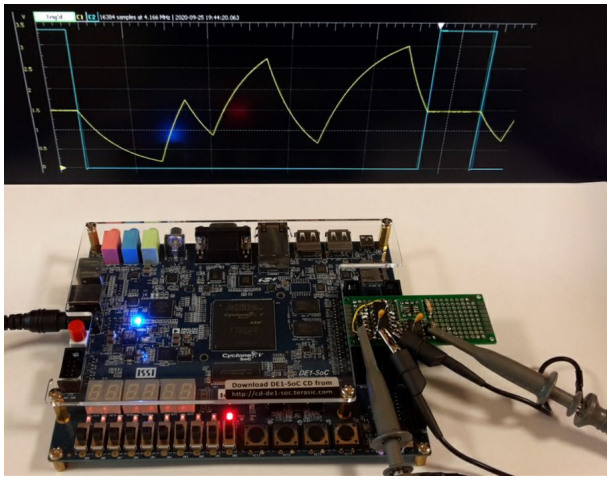

Fig. 16. Photo of the ReDAC FPGA prototype, showing the piecewise exponential capacitor voltage of a generic ReDAC conversion. The blue waveform is the three-state enabling signal $\overline{Enable}$ of Fig. 11.

V. ReDAC Design and FPGA Implementation

Two FPGA-based ReDAC prototypes, ReDAC1 and ReDAC2, intended to operate at 13 bit resolution and 514S/s and at 11 bit resolution and 10.5kS/s, respectively, both featuring the error suppression technique discussed in Section IV and the self-calibration procedure described in Section V, have been implemented on an Altera DE1-SoC FPGA board, mounting a Cyclone V (5CSEMA5F31C6) FPGA chip, operating at 3.3V power supply and 50 MHz clock frequency generated on the FPGA test board by a crystal oscillator, which enables to tune the ReDAC clock frequency with a 12bit resolution.

Following the ReDAC design procedure outlined in Sect.IIIa, $C = 1\text{nF}$ and $R = 180\text{k}\Omega$ have been chosen for the ReDAC1 prototype, while $C = 2.2\text{nF}$ and $R = 4.7\text{k}\Omega$ have been chosen for ReDAC2 prototype. In the calibration network of both prototypes, a discharge resistor $R_{\rm disch} = 820\text{k}\Omega$ which meets the condition (39) with a large margin for both the ReDACs, has been employed and a comparator threshold voltage $V_{\rm T} = V_{\rm DD}/4$ has been obtained by a resistive voltage divider. The RC networks and the discharge resistors are implemented by surface mounted devices (SMD) soldered on two prototyping boards (PBs) to be connected to the general purpose I/Os (GPIO) of the FPGA test board. The ReDAC three-state output buffer, and the comparator employed in the calibration procedure have also been implemented in the PBs to keep their distance to the RC network to a minimum and to reduce the parasitics on the ReDAC output node[6], considering that the length of the tracks connecting the FPGA pins to the GPIO connectors in the DE1-SoC board is in the 10cm-range.

In a custom FPGA board, a GPIO buffer and a low voltage differential signaling (LVDS) input of the FPGA can directly be used to implement the buffer and the comparator, with no need of external components. On the same PB, an operational

[6]Even adopting the proposed parasitic error suppression strategy, it is recommended to minimize the parasitics so that the higher-order time constants are negligible with respect to the dominant one, as required in (31) to keep $T_{\rm del}$ and the nominal signal attenuation as small as possible.

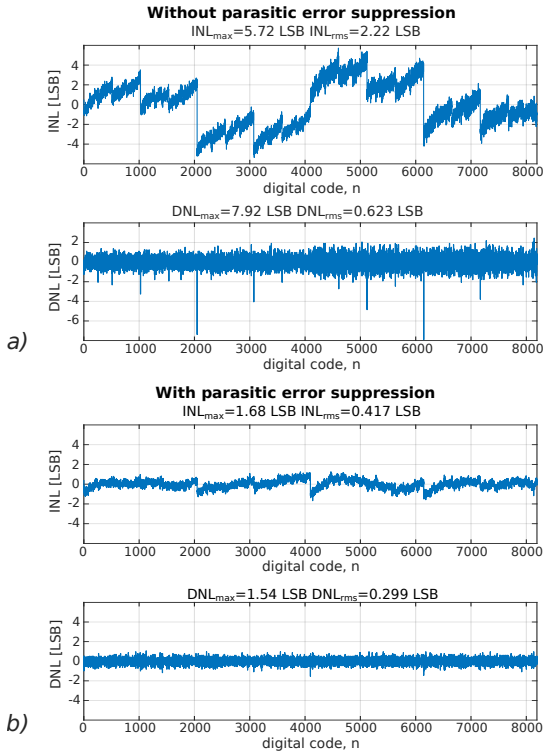

Fig. 17. ReDAC1 measured INL and DNL without (a) and with (b) the proposed parasitic error suppression strategy.

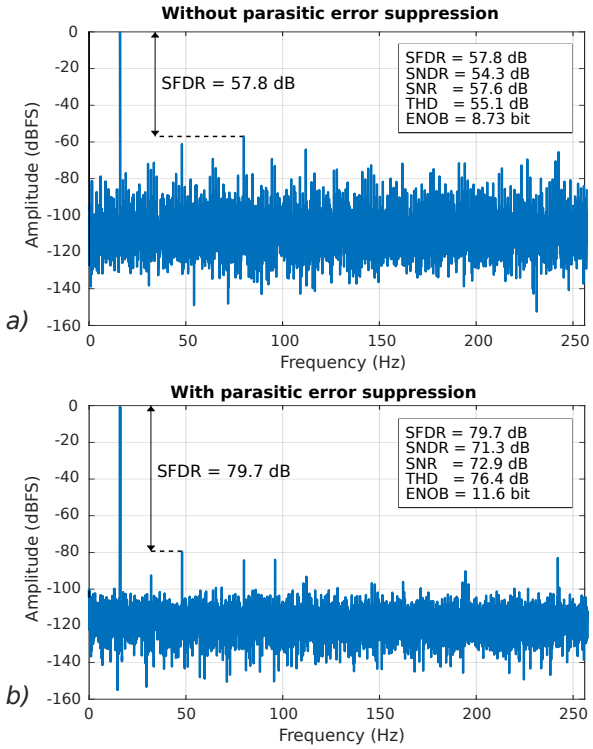

Fig. 18. ReDAC1 output spectrum under sinewave input at 16 Hz, 90% input swing without (a) and with (b) the proposed parasitic error suppression strategy.

amplifier connected in the voltage follower configuration is used as an active probe to decouple ReDAC output node from the testing harness. A photograph of the FPGA ReDAC prototype and of the experimental test setup employed for its characterization is reported in Fig.16.

The main ReDAC module and the calibration module have been automatically synthesized starting from a behavioral VHDL description and require 6 and 105 FPGA logic elements, respectively. The error suppression technique discussed in Section III has been implemented, by generating a delayed clock as described in Section III and a delay time $T_{\rm del} = 2.4\mu$s ($T_{\rm del} = 0.6\mu$s) has been found to be sufficient to fully suppress the nonlinearity due to the parasitics in the proposed ReDAC1 (ReDAC2) FPGA implementation. A programmable digital synthesizer has also been implemented on the same FPGA to generate the test patterns required to test the ReDAC performance under static and dynamic conditions.

VI. Experimental Results and Comparison

Both the FPGA-based ReDAC prototypes ReDAC1 and ReDAC have been automatically calibrated for operation at optimal clock frequency by the procedure discussed in Section IVb and have been experimentally characterized under static and dynamic conditions.

A. Experimental Results

The measured INL and DNL of ReDAC1 obtained with and without the parasitic error suppression strategy proposed in Section II (i.e. for $T_{\rm del} = 2.4\,\mu$s and $T_{\rm del} = 0$, respectively) are reported in Fig.17, which reveals that the maximum (rms) INL of $5.72\,$LSB $(2.22\,$LSB$)$ and the maximum (rms) DNL of $7.92\,$LSB $(0.623\,$LSB$)$ achieved by ReDAC1 without the parasitic error suppression are effectively reduced to a maximum (rms) INL of $1.68\,$LSB $(0.417\,$LSB$)$ and a maximum (rms) DNL of $1.54\,$LSB $(0.299\,$LSB$)$ by the adoption of the proposed error suppression.

Moreover, based on the dynamic characterization measurements reported in Fig.18 performed under sinewave input at 90% swing and 16Hz frequency, without the error suppression strategy, the ReDAC achieves an SFDR of $57.8\,$dB, a THD of $55.1\,$dB, a SNR of $57.6\,$dB and a SNDR of $54.3\,$dB, yielding to 8.73 effective bits (ENOB) whereas the introduction of the parasitic error suppression makes it possible to achieve, under the same test conditions, a SFDR of $79.7\,$dB, a THD of $76.4\,$dB, a SNR of $72.9\,$dB and a SNDR of $71.3\,$dB, corresponding to 11.6 ENOB, with an improvement of 2.87 effective bits.

In Fig.19 the dynamic characterization over input sine wave frequency (at constant sine wave input amplitude of 90% full swing) and over input sine wave amplitude (at constant sine wave frequency of $0.3\,$Hz) are reported and reveal consistent operation with low distortion up to the Nyquist frequency and over the whole input swing.

In Fig.20 and in 21 the static characterization of ReDAC2 featuring the proposed error suppression strategy and its output spectrum are reported, revealing proper operation at $10.5\,$kS/s and $11\,$bit resolution with maximum (rms) INL of $1.53\,$LSB $(0.415\,$LSB$)$ and the maximum (rms) DNL

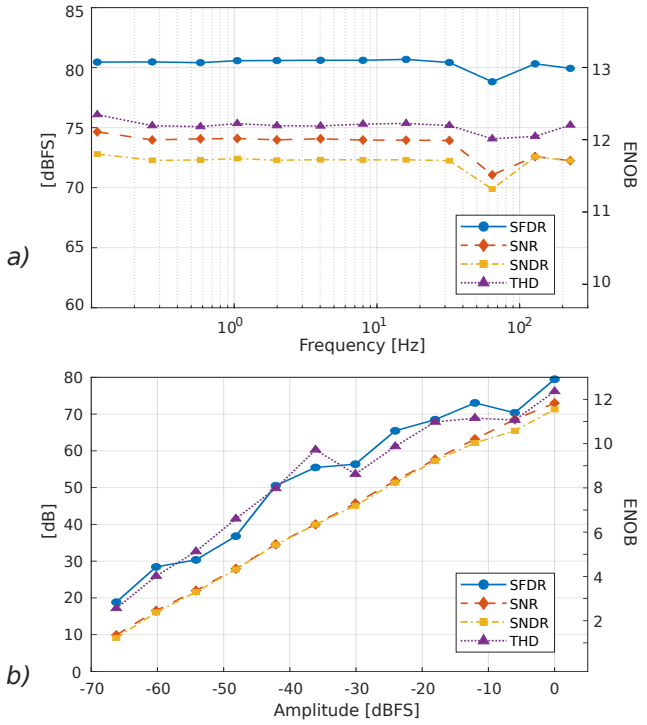

Fig. 19. ReDAC1 dynamic characterization (with proposed parasitic error suppression): a) over input sine wave frequency at constant 90% full swing amplitude, b) over input sinewave amplitude at constant sine wave frequency of 0.3Hz.

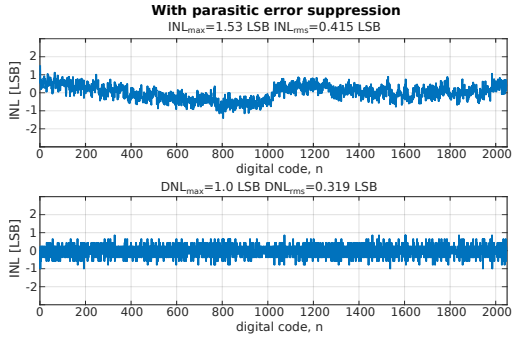

Fig. 20. ReDAC2 measured INL and DNL with the proposed parasitic error suppression strategy.

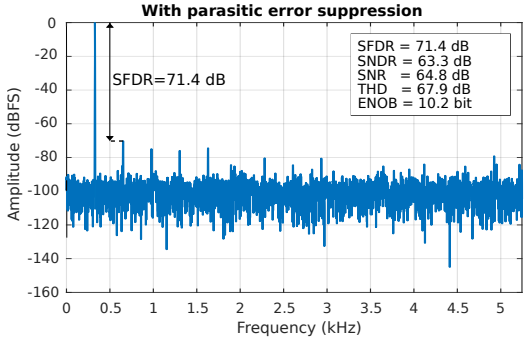

Fig. 21. ReDAC2 output spectrum (with proposed parasitic error suppression) under sinewave input at 330 Hz, 90% input swing with the proposed parasitic error suppression strategy.

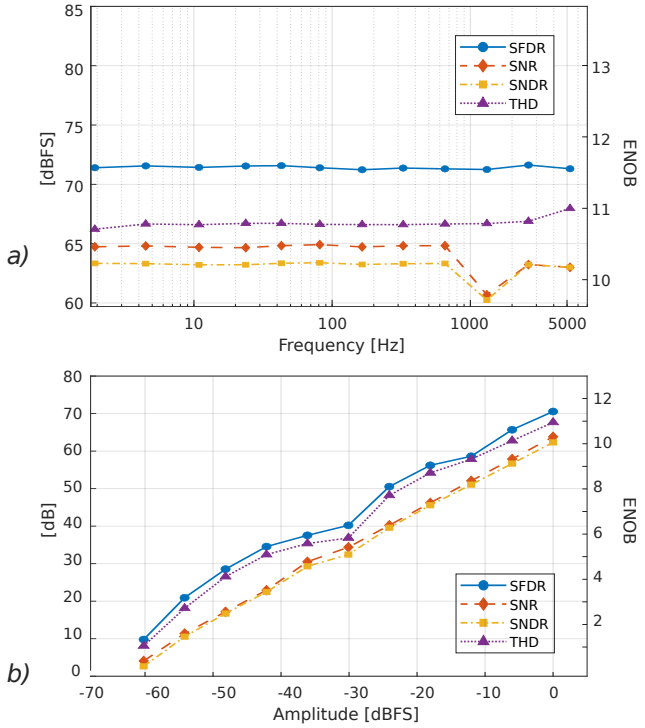

Fig. 22. ReDAC2 dynamic characterization (with proposed parasitic error suppression): a) over input sine wave frequency at constant 90% full swing amplitude, b) over input sinewave amplitude at constant sine wave frequency of 1.5Hz.

of 1.0 LSB (0.319 LSB), and a SFDR of 71.4 dB, a THD of 67.9 dB, a SNR of 64.8 dB and a SNDR of 63.3 dB, corresponding to 10.2 effective bits (ENOB) under 330 Hz, 90% swing sine wave input. The dynamic characterization over input sine wave frequency (at constant sine wave input amplitude corresponding to 90% of the swing) and over input sine wave amplitude (at constant sine wave frequency of 1.5Hz) are reported in Fig.22 and reveal consistent ReDAC2 operation up to the Nyquist frequency and over the whole input swing.

B. Comparison

The performance of the proposed FPGA-based ReDACs are compared in Tab.I with previous ReDAC implementations (both FPGA-based and integrated) and other FPGA-based DACs.

Compared to previous ReDAC implementations, thanks to the proposed parasitic error suppression technique, the proposed FPGA-based ReDACs show the best reported effective resolution. The ReDAC1 prototype, in particular, shows 4.47 effective bits more at 1.7X higher sample rate compared to the proof-of-concept FPGA-based ReDAC implementation [20], and 1.7-2.2 effective bits more than the post-layout simulated performance of the ReDACs implementations in 40nm presented in [21], [22], whose sample rate is however 778X-3,112X higher.

Compared to other FPGA-based bitstream DACs, the proposed ReDACs require just 6 logic elements, 8.8X less than a DDPM DAC and 2,237X less than a $\Sigma\Delta$ DAC, in which

TABLE I
DAC PERFORMANCE COMPARISON

	Units	[13]	[16]	[19]	[17]	[7]	[20]	[21]	[21]	**This Work**	
Type		PWM	$\Sigma\Delta$	$\Sigma\Delta$	DDPM	DDPM	ReDAC	ReDAC	ReDAC	ReDAC1	ReDAC2
Valid.		Meas.	Meas.	Sim.[a]	Meas.	Meas.	Meas.	Sim.	Sim.	Meas.	
Techn.	nm	FPGA	FPGA	FPGA	FPGA	40	FPGA	40	40	FPGA	
R	kΩ	N/A[b]	N/A	0.1	180	300	100	288	128	180	4.7
C	pF	N/A[b]	N/A	80,000	1,000	5	2,200	1	0.45	1,000	2,200
Area	μm^2	N/A	N/A	N/A	N/A	270	N/A	910	677	N/A	
Logic Elements		N/A	87	13,426	53	N/A	N/A	N/A	N/A	6	6
Logic Elements (cal.)		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	105	105
Resolution	bit	N/A	16	24	16	12	10	10	10	13	11
Sample Rate	kS/S	172	20	44.1	1.525	110	0.3	400	2,000	0.514	10.5
OSR		Nyq.	50	128	Nyq.	Nyq.	Nyq.	Nyq.	Nyq.	Nyq.	
$\mathrm{INL}_{\max}$	LSB	N/A	N/A	N/A	13	3	2.4	0.33	0.72	1.68	1.53
$\mathrm{INL}_{\mathrm{rms}}$	LSB	N/A	N/A	N/A	N/A	1	0.9	0.10	0.34	0.417	0.415
$\mathrm{DNL}_{\max}$	LSB	N/A	N/A	N/A	1	1	3.3	0.2	1.27	1.54	1.0
$\mathrm{DNL}_{\mathrm{rms}}$	LSB	N/A	N/A	N/A	N/A	0.47	0.62	0.01	0.07	0.299	0.319
SNDR (Low Freq.)	dB	50	57.3	N/A	N/A	71.6	43.27	61.0	58.3	71.3	63.3
SNDR (Nyq.)	dB	< 10	N/A	N/A	N/A	35	N/A	N/A	N/A	72.3	63.01
SFDR	dB	37	78	N/A	N/A	85	51.36	76.8	62.4	79.7	71.4
THD	dB	N/A	63.7	N/A	N/A	85	47.52	66.7	62.2	76.4	67.9
SNR	dB	57	58.5	141	N/A	75	44.66	66.7	62.2	72.9	64.8
ENOB	bit	8	9.2	23.4	12.1[c]	11.6[c]	7.13	9.9	9.4	11.6	10.2
Calibration		No	No	N/A	Manual[c]	Manual[c]	Manual	Manual	Auto	Auto	

[a]Measurements performed on the digitally acquired bitstream, not comparable with a true analog characterization.
[b]Second-order Sallen Key filter used,
[c]Double-slope error calibration considered for comparison, higher effective resolution in [17] requires more complex 8-segment calibration.

the calibration network (also needed for the DDPM DACs) is not included for fair comparison, and are therefore very attractive in very low cost applications. Moreover, the effective resolution of the proposed ReDACs is significantly better than the DPWM DAC in [13] (+3.6/+2.2 effective bits for ReDAC1/ReDAC2), which operates at (334X/16.4X higher sample rate compared to ReDAC1/ReDAC2) and is comparable with DDPM DACs with two-segment, double slope error calibration [7], [17], which however require 2^N pulses per conversion, while the proposed ReDAC requires just $N+2$ pulses, suggesting a significant energy advantage for the proposed ReDAC (even if it cannot be quantified in the proposed FPGA implementation since the ReDAC power cannot be directly measured).

Even if the performance in terms of SNR and effective resolution of the high-order $\Sigma\Delta$ DAC [19] implemented on FPGA seems to be significantly better, such a circuit cannot be fairly compared since the results presented in [19] are obtained by the FFT of the output bitstream and a full analog characterization is not reported. Compared to a 16-bit second-order $\Sigma\Delta$ FPGA DAC implemented on a similar FPGA [16] and properly characterized by an analog spectrum analyzer, the ReDAC1/ReDAC2 prototypes still achieve a 2.4/1.0 effective bits higher resolution at comparable hardware complexity.

VII. CONCLUSION

The main factors limiting the accuracy of a Relaxation DAC have been analyzed and a simple technique, suitable to effectively suppress the dominant error contribution resulting from high-order parasitics of the RC network, has been proposed. Moreover, a new ReDAC self-calibration strategy, suitable to be implemented on FPGA has been presented.

The effectiveness of the proposed parasitic error suppression technique and of the ReDAC clock frequency self-calibration have been verified on a 13-bit, 514S/s prototype (ReDAC1) and on a 11-bit, 10.5kS/s prototype (ReDAC2), which have been implemented on FPGA using just 6 (111) logic elements excluding (including) the self-calibration network, and have been experimentally characterized.

Based on experimental results, the ReDAC1 prototype achieves a maximum INL of $1.68\,\mathrm{LSB}$, a maximum DNL of $1.54\,\mathrm{LSB}$ and an SNDR exceeding $71\,\mathrm{dB}$, corresponding to 11.6 effective bits (ENOB), whereas the ReDAC2 prototype achieves a maximum INL of $1.53\,\mathrm{LSB}$, a maximum DNL of $1.0\,\mathrm{LSB}$ and an SNDR exceeding 63dB corresponding to $10.2\,\mathrm{ENOB}$. The experimental results, which outperform previous ReDAC implementations, fully demonstrate the effectiveness of the new parasitic error suppression technique and digital self-calibration and reveal the potential of ReDACs as an ultra-low cost solution for the fast prototyping and implementation of analog interfaces in digital reconfigurable platforms.

ACKNOWLEDGMENT

The Altera DE1-SoC FPGA board used for the prototype has been provided by Intel corp. under the Intel FPGA Academic Program.

REFERENCES

[1] "Circuit realization at faster timescales (craft) project, defense advanced research projects agency (darpa)," https://www.darpa.mil/program/circuit-realization-at-faster-timescales, accessed: 2010-09-30.

[2] J. C. Kemerling, R. Greenwell, and B. Bharath, "Analog- and mixed-signal fabrics," *Proceedings of the IEEE*, vol. 103, no. 7, pp. 1087–1101, 2015.

[3] N. Suda, J. Suh, N. Hakim, Y. Cao, and B. Bakkaloglu, "A 65 nm programmable analog device array (panda) for analog circuit emulation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 2, pp. 181–190, 2016.

[4] J. Suh, N. Suda, C. Xu, N. Hakim, Y. Cao, and B. Bakkaloglu, "Programmable analog device array (panda): A methodology for transistor-level analog emulation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 6, pp. 1369–1380, 2013.

[5] P. Toledo, G. R. Rubino, F. Musolino, and P. Crovetti, "Re-thinking analog integrated circuits in digital terms: A new design concept for the iot era," *IEEE Transactions on Circuits and Systems II: Express Briefs*, pp. 1–1, 2021.

[6] O. Aiello, P. Crovetti, and M. Alioto, "Fully synthesizable, rail-to-rail dynamic voltage comparator for operation down to 0.3 v," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018, pp. 1–5.

[7] ——, "Standard cell-based ultra-compact dacs in 40-nm cmos," *IEEE Access*, vol. 7, pp. 126 479–126 488, 2019.

[8] ——, "Fully synthesizable low-area analogue-to-digital converters with minimal design effort based on the dyadic digital pulse modulation," *IEEE Access*, vol. 8, pp. 70 890–70 899, 2020.

[9] P. S. Crovetti, "A digital-based virtual voltage reference," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 5, pp. 1315–1324, 2015.

[10] P. S. Crovetti, "Spectral characteristics of DDPM streams and their application to all-digital amplitude modulation," *Electronics Letters*, vol. n/a, no. n/a. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/ell2.12050

[11] P. Chen, P. Chen, J. Lai, and Y. Chen, "FPGA vernier digital-to-time converter with 1.58 ps resolution and 59.3 minutes operation range," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 6, pp. 1134–1142, 2010.

[12] P. Chen, J. Lan, R. Wang, N. My Qui, J. C. J. S. Marquez, S. Kajihara, and Y. Miyake, "High-precision PLL delay matrix with overclocking and double data rate for accurate FPGA time-to-digital converters," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 4, pp. 904–913, 2020.

[13] B. Lonla Moffo and J. Mbihi, "A novel digital duty-cycle modulation scheme for FPGA-based digital-to-analog conversion," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 6, pp. 543–547, 2015.

[14] R. F. Foley, R. C. Kavanagh, W. P. Marnane, and M. G. Egan, "An area-efficient digital pulsewidth modulation architecture suitable for FPGA implementation," in *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005.*, vol. 3, 2005, pp. 1412–1418 Vol. 3.

[15] X. Li and A. Lee, "An fpga implemented 24-bit audio DAC with 1-bit sigma-delta modulator," in *2010 IEEE Asia Pacific Conference on Circuits and Systems*, 2010, pp. 768–771.

[16] *Integrated DAC for Altera Cyclone-IV Devices*, Missing Link Electronics, 2011, technical Brief 20110426. [Online]. Available: https://www.missinglinkelectronics.com/devzone/files/papers/MLE-TB20110426.pdf

[17] P. S. Crovetti, "All-digital high resolution D/A conversion by dyadic digital pulse modulation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 3, pp. 573–584, 2017.

[18] H. Homulle, S. Visser, and E. Charbon, "A cryogenic 1 GSa/s, soft-core fpga adc for quantum computing applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 11, pp. 1854–1865, 2016.

[19] Z. Kulka and P. Woszczek, "Implementation of digital sigma-delta modulators for high-resolution audio digital-to-analog converters based on field programmable gate array," *Archives of Acoustics*, vol. 33, no. 1, pp. 93–101, 2018.

[20] P. S. Crovetti, R. Rubino, and F. Musolino, "Relaxation digital-to-analogue converter," *Electronics Letters*, vol. 55, no. 12, pp. 685–688, Jun. 2019. [Online]. Available: http://dx.doi.org/10.1049/el.2019.0784

[21] R. Rubino, P. S. Crovetti, and O. Aiello, "Design of relaxation digital-to-analog converters for internet of things applications in 40nm cmos," in *2019 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2019, pp. 13–16.

[22] P. S. Crovetti, R. Rubino, and F. Musolino, "Relaxation digital-to-analog converter with foreground digital self-calibration," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS2020)*, 2020, p. In press.

[23] *Implementing Fractional PLL Reconfiguration with Altera PLL and Altera PLL Reconfig IP Cores*, Altera, 2019, aN-661 Technical Brief.

[24] A. B. Kahng and S. Muddu, "Two-pole analysis of interconnection trees," in *Proceedings of 1995 IEEE Multi-Chip Module Conference (MCMC-95)*, 1995, pp. 105–110.