Design Space Optimization of a Three-Phase LCL Filter for Electric Vehicle Ultra-Fast Battery Charging

*energies*

MDPI

*Article*

# Design Space Optimization of a Three-Phase LCL Filter for Electric Vehicle Ultra-Fast Battery Charging †

**Davide Cittanti *, Fabio Mandrile, Matteo Gregorio and Radu Bojoi**

Energy Department "Galileo Ferraris", Politecnico di Torino, 10129 Torino, Italy; fabio.mandrile@polito.it (F.M.); matteo.gregorio@polito.it (M.G.); radu.bojoi@polito.it (R.B.)

* Correspondence: davide.cittanti@polito.it

† This paper is an extended version of our paper published in 55th International Universities Power Engineering Conference (UPEC), Torino, Italy, 1–4 September 2020.

**Abstract:** State-of-the-art ultra-fast battery chargers for electric vehicles simultaneously require high efficiency and high power density, leading to a challenging power converter design. In particular, the grid-side filter, which ensures sinusoidal current absorption with low pulse-width modulation (PWM) harmonic content, can be a major contributor to the overall converter size and losses. Therefore, this paper proposes a complete analysis, design and optimization procedure of a three-phase *LCL* filter for a modular DC fast charger. First, an overview of the basic LCL filter modeling is provided and the most significant system transfer functions are identified. Then, the optimal ratio between grid-side and converter-side inductance is discussed, aiming for the maximum filtering performance. A novel design methodology, based on a graphical representation of the filter design space, is thus proposed. Specifically, several constraints on the *LCL* filtering elements are enforced, such that all feasible design parameter combinations are identified. Therefore, since in low-voltage high-power applications the inductive components typically dominate the overall filter volume, loss and cost, the viable *LCL* filter design that minimizes the total required inductance is selected. The proposed design procedure is applied to a 30 kW, 20 kHz 3-level unidirectional rectifier, employed in a modular DC fast charger. The performance of the selected optimal design, featuring equal grid-side and converter-side 175 µH inductors and 15 µF capacitors, is verified experimentally on an active front-end prototype, both in terms of harmonic attenuation capability and current control dynamics. A current total harmonic distortion (THD) of 1.2% is achieved at full load and all generated current harmonics comply with the applicable harmonic standard. Moreover, separate tests are performed with different values of grid inner impedance, verifying the converter control stability in various operating conditions and supporting the general validity of the proposed design methodology.

**Keywords:** LCL filters; grid-connected converters; active front-end (AFE); power factor corrector (PFC); battery charging; ultra-fast charging (UFC); electric vehicles (EVs)



**Citation:** Cittanti, D.; Mandrile, F.; Gregorio, M.; Bojoi, R. Design Space Optimization of a Three-Phase LCL Filter for Electric Vehicle Ultra-Fast Battery Charging. *Energies* **2021**, *14*, 1303. https://doi.org/10.3390/en14051303

Academic Editor: Hugo Morais

Received: 4 February 2021
Accepted: 22 February 2021
Published: 27 February 2021



## 1. Introduction

Even though the performance of Li-ion batteries is constantly increasing, their weight and cost still pose a major barrier to a widespread vehicle electrification [1]. Nevertheless, the limited range of electric vehicles (EVs) can be addressed with a distributed DC ultra-fast charging infrastructure, which would allow charging times comparable with the refueling of an internal combustion engine (ICE) vehicle, thus providing a solution to the infamous EV range anxiety for most of the population. The present and future challenges for implementing such an infrastructure are mainly related to available power electronics technology, competing industry standards and the impact on the grid of widespread high power charging stations [2–4]. In spite of the challenges, the electric mobility market is expanding exponentially and thousands of DC fast-charging stations are currently being installed around the world [5,6], making this topic of particular interest for both industry and academia.

State of the art DC ultra-fast chargers (UFCs) are typically connected to the low-voltage grid, thus leveraging the industrial power electronics expertise and availability [3,7–9]. The charger generally consists of two power converter stages [3], which are schematically represented in Figure 1. The first stage, referred to as active front-end (AFE), is a grid-connected three-phase AC/DC converter with unity power factor correction (PFC) capabilities. This stage must absorb the total charging power from the grid, meanwhile ensuring sinusoidal input current shaping with low distortion and harmonic content [10]. The second stage is an isolated DC/DC converter, which controls the charging process (i.e., the battery-side current) and provides galvanic isolation from the grid [11].

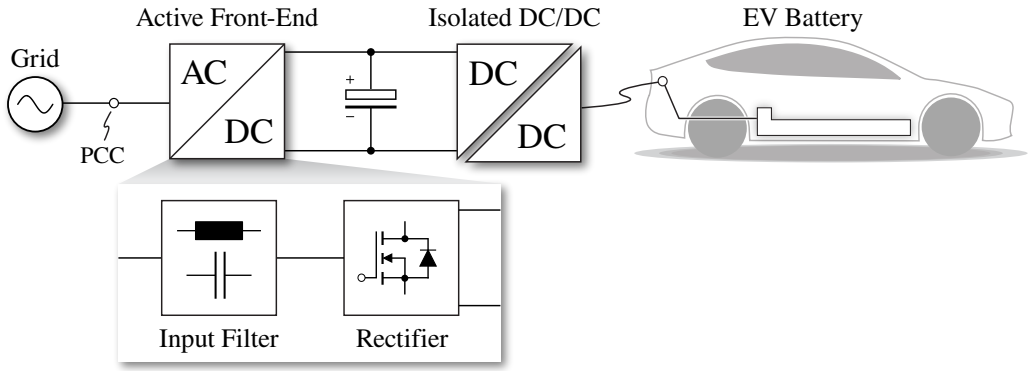


**Figure 1.** Schematic overview of an electric vehicle (EV) ultra-fast battery charger, with highlight of the active front-end (AFE) structure.

The main requirements of a UFC include (1) high efficiency, (2) high power density, (3) sinusoidal input current absorption, (4) wide input/output voltage range and (5) low battery-side current ripple, which may affect the battery aging process [12]. While requirements (4) and (5) are mainly addressed by the DC/DC stage, (1), (2) and (3) also affect the AC/DC converter, which is the focus of this work.

The most simple and widely adopted topology for active rectification is the 2-level inverter, which benefits from inherent bidirectional capabilities. However, due to its 2-level output voltage waveform and the high voltage rating of the employed semiconductor devices, this converter is affected by a severe performance trade-off between achievable efficiency and power density. In fact, a smaller overall size can only be achieved by increasing the operating switching frequency, thus leading to higher switching losses and lower conversion efficiency [13,14]. An effective approach to simultaneously improve both performance indices of the AC/DC converter is to adopt multi-level topologies, which offer better overall performance in exchange for higher complexity and component count.

Since UFCs only require that the power flows from the grid to the vehicle, 3-level unidirectional rectifiers represent an attractive alternative to their 2-level counterpart, as they achieve an excellent trade-off between efficiency, power density and overall complexity [13–16]. In particular, the multi-level structure of these rectifiers allows them to simultaneously increase the switching frequency (i.e., adopting devices with lower voltage rating) and the number of output voltage levels, notably reducing the stress on the filtering components and thus enabling an improved trade-off between efficiency and power density. Moreover, due to their unidirectional nature, 3-level rectifiers ensure minimum converter complexity, as the number of active devices is lower than or equal to 2-level inverters and no switching dead-times are required (i.e., each converter leg features a single 4-quadrant switch).

The main tasks of a 3-level AFE for battery charging are (1) to ensure sinusoidal input current with low distortion and harmonics, (2) to regulate the DC-link voltage according to the DC/DC stage optimal operating conditions [11], (3) to minimize the third-harmonic voltage oscillations of the DC-link mid-point, typical of 3-level converters [17,18], and (4) to fully control the steady-state mid-point voltage deviation [19]. While all of these tasks require a converter control with sufficient dynamical performance [10] and an appropriate

modulation strategy [20], (1) also requires a proper design of the grid-side filter, which may strongly affect the overall converter performance and is thus the subject of this work.

The AFE input filter, schematically represented in Figure 1, must ensure that the converter complies with grid current harmonic restrictions at the point of common coupling (PCC), such as IEEE 519 [21]. The role of the filter is to attenuate the high-frequency harmonics generated by the pulse-width modulation (PWM) operation of the converter, such that they do not flow into the grid and affect other devices connected to the PCC.

The most simple filter topology is the purely inductive *L* filter, which corresponds to the direct utilization of the AFE boost inductors for filtering purposes. However, despite its simplicity, this filter provides very low harmonic attenuation for a given total inductance (i.e., 20 dB/dec roll-off), thus resulting in excessive volume, weight and power loss [22]. Substantially better performance are achieved with an *LCL* filter, due to its superior attenuation capability (i.e., up to 60 dB/dec roll-off) and thus reduced filter size and losses [22]. A lower total inductance leads to lower filter cost and enables higher converter dynamical performance, if the filter and the control loop are properly designed. However, the high order of the filter affects the complexity of the design procedure, since multiple degrees of freedom are available and several constraints of different nature must be enforced. Furthermore, the filter resonance may amplify unwanted harmonics and may negatively affect the closed-loop current control gain and phase margins, even leading to instability [23,24]. Therefore, the resonance peak must be mitigated either by passive or active damping methods [25,26], which add further complexity to the filter design and/or to the converter control [27].

It is worth noting that in modern high-frequency power converters, the *LCL* filter generally represents the first element of a multi-stage differential-mode EMI filter [28], as it provides the required attenuation for the current harmonics with highest energy content, i.e., situated in the lower part of the 0.15–30 MHz CISPR range [29]. Nevertheless, high-frequency EMI filtering is a complex and broad topic and does not represent the scope of this work, therefore it is not discussed further in this paper.

Due to the complexity and the importance of the input filter in grid-connected converters, several design procedures have been proposed in literature [22,30–37]. Most of these approaches are based on iterative step-by-step solutions [22,30,32–35], which require the verification of either the filter parameter constraints, the attenuation results or the converter control stability within the design procedure itself, leading to a not straightforward solution. In the following paragraphs each reference is analyzed individually, to better highlight the contributions of the present work.

Among the above mentioned design approaches, [22] aims at minimizing the total energy stored by the *LCL* filter. However, the energy minimization criteria ensures neither the total volume nor the total loss minimization, since the energy storage density of inductors and capacitors can differ by multiple orders of magnitude [38] and inductor losses tend to dominate over capacitor ones, especially in high power applications.

The design methodologies adopted in [30,32] determine the converter-side inductance from a maximum current ripple target, select the filter capacitance to achieve a fixed reactive power generation and determine the grid-side inductance from the harmonic attenuation requirement. These procedures particularly fail to identify the role of the ratio between the grid-side and the converter-side inductance values in the filter size and loss minimization, thus leading to sub-optimal filter designs.

This issue is addressed in [33], where the advantages of having equal grid-side and converter-side inductance values are leveraged to minimize the filter size, however the filter resonance frequency is fixed from active-damping considerations, severely limiting the filter design space and thus leading to sub-optimal results.

The most promising optimization approach is proposed in [34,35], which also leverages equal grid-side and converter-side inductance values, meanwhile taking into account several design constraints on the filter parameters. This procedure achieves optimal design results with minimum total inductance and capacitance, however no constraint on the minimum converter-side inductance value is applied, which can lead to excessive

inductor current ripple and losses, translating in low overall efficiency. Moreover, a partial graphical approach is attempted to identify the required total inductance as function of the switching-to-resonance frequency ratio. However, not all filter constraints are here displayed, thus inhibiting the full view of the actual filter design space.

Besides considering the filter size, the design procedures proposed in [31,36,37] also take into account the filter losses, either generated by passive damping resistors or by the filtering components (i.e., inductors, capacitors). In particular, in [31] a conventional filter design procedure is followed, however the inductance and capacitance values that minimize the overall filter losses, meanwhile complying with the attenuation requirements, are selected. Nevertheless, this design methodology is based on a fixed resonance frequency (i.e., selected from control bandwidth considerations), resulting in sub-optimal design results. In [36,37], instead, a Pareto-optimization approach is undertaken, sweeping the filter component values and searching for an optimal design trade-off between filter size and losses. Nevertheless, no direct design procedure is provided, as the design results are found by means of a parametric sweep.

Even though the literature on *LCL* filters and their applications is extensive and well established, according to the authors' best knowledge, no direct (i.e., non-iterative) optimization procedure aiming at minimizing the filter size and losses, meanwhile taking into account all relevant constraints, has yet been presented. In particular, all found design methodologies either miss some parameter constraints, achieve sub-optimal design results or do not provide a step-by-step repeatable approach. Moreover, no procedure provides a clear overview of the filter degrees of freedom and their boundaries, which may prove extremely useful to both experienced designers and engineers unfamiliar with the topic. As a further note, none of the mentioned *LCL* filter design procedures has been applied to 3-level unidirectional rectifiers.

Therefore, this work proposes a novel non-iterative design procedure for *LCL* filters, based on a complete graphical representation of the filter design space. This simple and straightforward approach, first proposed in [39] (i.e., applied to differential-mode EMI filters for switch-mode AC power sources), allows for a better understanding of the degrees of freedom available to the designer and the constraints that must be enforced, thus simplifying the identification of the optimal design results. In particular, this work is an extension of [40], where the design procedure has only been briefly described. The major contribution of this paper is to present exclusive experimental results, aimed at validating the proposed design methodology with a purposely built *LCL* filter for a 30 kW 3-level unidirectional AFE unit for EV ultra-fast charging.

This paper is structured as follows. In Section 2 the equivalent circuit model of the system under consideration is reported and the most significant *LCL* filter transfer functions are discussed. In Section 3 the filter degrees of freedom and parameter constraints are identified and the proposed graphical design methodology is described. This procedure is then applied to the input filter of a 30 kW, 20 kHz 3-level AFE for EV ultra-fast charging, identifying the feasible *LCL* filter design with lowest total inductance. In Section 4 the performance evaluation of the designed filter is performed both in simulation environment and experimentally, verifying the PCC current distortion and the closed-loop control stability on a converter prototype. Finally, Section 5 summarizes and concludes this paper.

## 2. Filter Model

The system under consideration consists of a three-phase active rectifier, an *LCL* filter and the grid. The equivalent circuit of the complete system is reported in Figure 2. The grid is modeled by three sinusoidal voltage sources $u_{\mathrm{abc}}$, each in series with an inductive impedance $L_{\mathrm{g}}$, representing the sum of the line inductance and the leakage inductance of the distribution transformer. The active rectifier is modeled by two three-phase sets of voltage sources, representing the grid-frequency (i.e., low-frequency) voltage components $v_{\mathrm{abc,LF}}$ and the switching-frequency (i.e., high-frequency) voltage components $v_{\mathrm{abc,HF}}$, respectively. Additionally, the *LCL* filter may include a set of damping resistors in series with the filtering capacitors, depending whether passive damping needs to be provided.

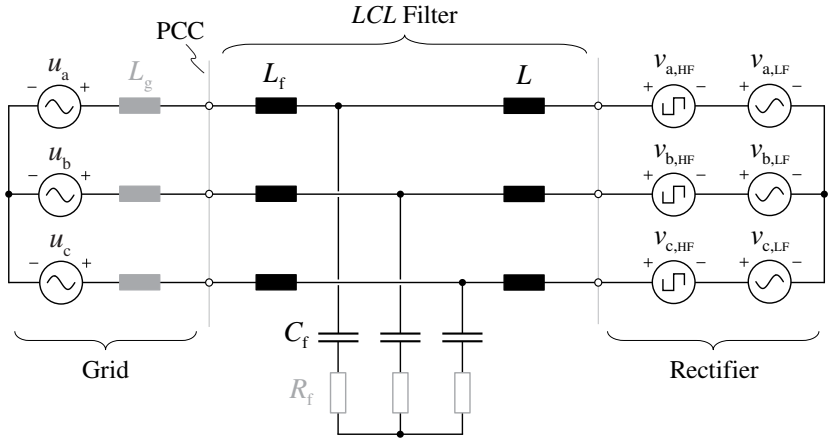


**Figure 2.** Equivalent circuit of the considered three-phase system, consisting of the active rectifier, the *LCL* filter and the grid. $L$ is the converter-side inductance, $C_f$ is the filter capacitance and $L_f$ is the grid-side filter inductance. Additionally, $L_g$ represents the grid internal inductance and $R_f$ is the filter damping resistance. Since these components are not always present or quantitatively meaningful to the analysis, they are shown in grey.

Due to its symmetrical three-phase properties, the considered model can be represented with the single-phase equivalent circuit illustrated in Figure 3. It must be noted that the low-frequency voltage sources of Figure 2 appear as short circuits, both from a high-frequency harmonic perspective (i.e., filter attenuation) and from a small-signal stand point (i.e., closed-loop control stability).

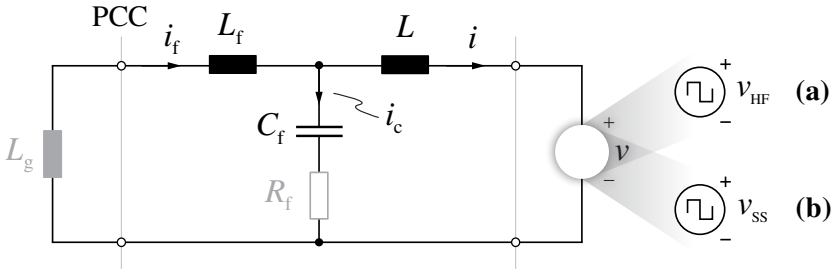


**Figure 3.** Single-phase equivalent circuit of the considered system, where the converter is represented by the voltage source $v$. The circuit is valid both from (**a**) a high-frequency harmonic perspective ($v = v_{HF}$) and from (**b**) a small-signal (i.e., control) stand point ($v = v_{SS}$).

The most relevant system transfer functions for the filter design can be directly derived from an impedance analysis of the derived equivalent circuit. Referring to the naming conventions of Figure 3,

$$Y(s) = \frac{i(s)}{v(s)} = \frac{1}{sL}\,\frac{s^2 + 2\,\xi_f\,\omega_f\,s + \omega_f^2}{s^2 + 2\,\xi_0\,\omega_0\,s + \omega_0^2}, \tag{1}$$

$$Y_c(s) = \frac{i_c(s)}{v(s)} = \frac{1}{L}\,\frac{s}{s^2 + 2\,\xi_0\,\omega_0\,s + \omega_0^2}, \tag{2}$$

$$Y_f(s) = \frac{i_f(s)}{v(s)} = \frac{1}{s\,(L + L_f + L_g)}\,\frac{2\,\xi_0\,\omega_0\,s + \omega_0^2}{s^2 + 2\,\xi_0\,\omega_0\,s + \omega_0^2}, \tag{3}$$

are obtained, where

$$\begin{cases} \xi_f = \dfrac{\omega_f\,R_f\,C_f}{2} \\ \omega_f^2 = \dfrac{1}{C_f\,(L_f + L_g)} \end{cases}, \tag{4}$$

$$\begin{cases} \xi_0 = \dfrac{\omega_0 R_f C_f}{2} \\ \omega_0^2 = \dfrac{L + L_f + L_g}{C_f L (L_f + L_g)} \end{cases} . \tag{5}$$

The admittance $Y(s)$ links the voltage applied by the converter to the generated (and controlled) converter-side current. This transfer function plays a key role in the closed-loop current control, affecting its performance and the system stability. The admittance $Y_c(s)$ allows to determine the current flowing into the capacitor branch, thus enabling the estimation of the power losses in the damping resistors (if any) and the voltage ripple on the filter capacitors. Finally, $Y_f(s)$ is the actual filter admittance, relating the high-frequency voltage components generated by the converter (i.e., $v_{abc,HF}$) with the current harmonics injected into the grid at the PCC. This transfer function determines the frequency-dependent filter attenuation and is thus essential for the $LCL$ filter design. A qualitative representation of the magnitude Bode plots of $Y(s)$, $Y_c(s)$ and $Y_f(s)$ is provided in Figure 4, where the effect of different damping resistance values is illustrated.

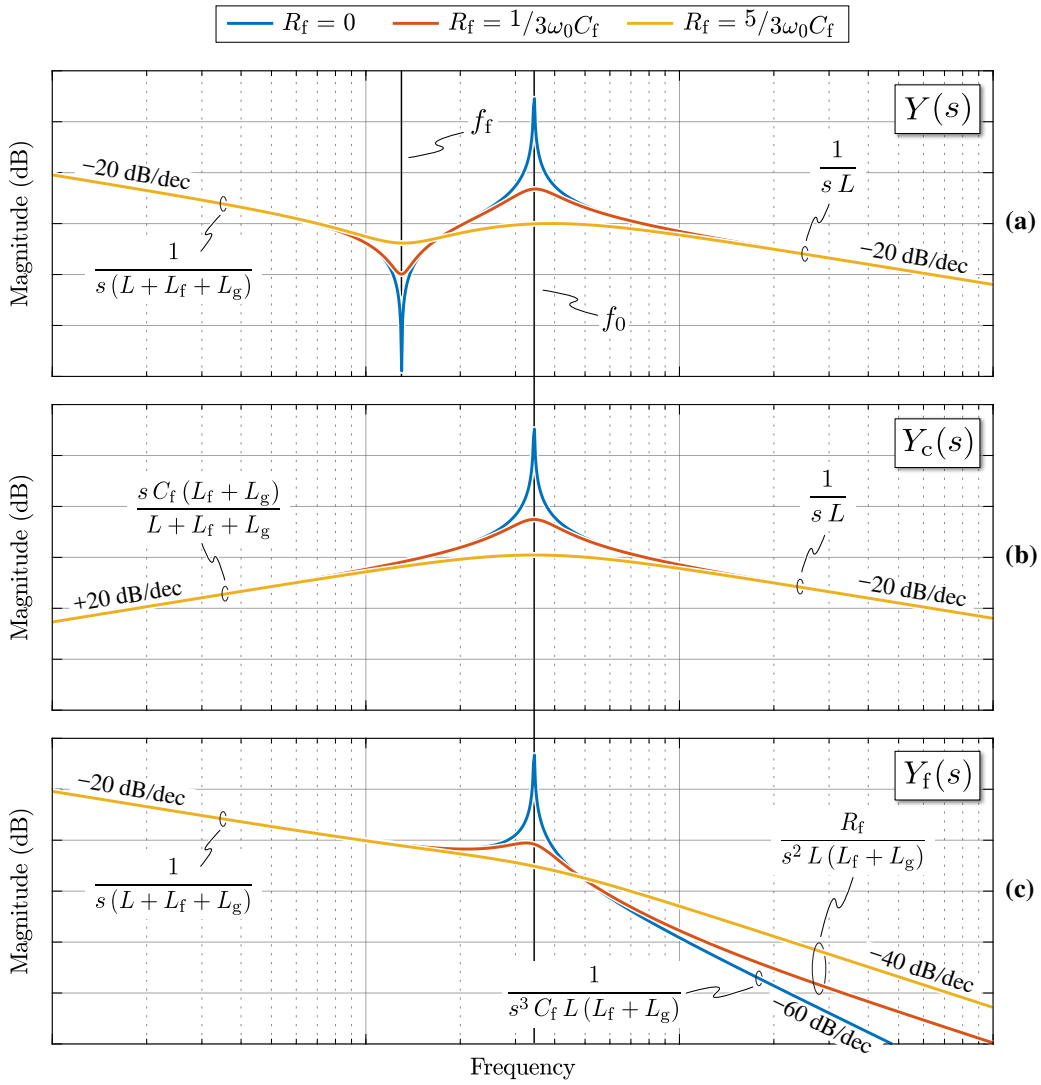


**Figure 4.** Qualitative representation in the logarithmic scale of the magnitude of $Y(s)$ (**a**), $Y_c(s)$ (**b**) and $Y_f(s)$ (**c**), for different values of damping resistance $R_f$. The resonance frequencies $f_f = \omega_f/2\pi$ and $f_0 = \omega_0/2\pi$ are indicated, while the asymptotic trends of the transfer functions are noted on the curves.

One parameter that deeply affects the *LCL* filter performance is the ratio between the grid-side and the converter-side inductance values $k_L = (L_f + L_g)/L$, as reported in [33]. In particular, this ratio can be optimized so that the filter attenuation for a given total amount of inductance $L_{tot} = L + L_f + L_g$ is maximized. The asymptotic expression of the filter admittance, which corresponds to the inverse of the filter attenuation $A$, is derived as

$$Y_f(s) \overset{s\to\infty}{=} \frac{1}{A(s)} = \begin{cases} \dfrac{1}{s^3\, C_f\, L_{tot}^2} \dfrac{(1+k_L)^2}{k_L} & \text{undamped } (R_f = 0) \\ \dfrac{R_f}{s^2\, L_{tot}^2} \dfrac{(1+k_L)^2}{k_L} & \text{damped } (R_f \neq 0) \end{cases} . \tag{6}$$

It can be observed that the minimum filter admittance (i.e., the maximum filter attenuation) is obtained for $k_L = 1$ (i.e., $L = L_f + L_g$), as illustrated in Figure 5.

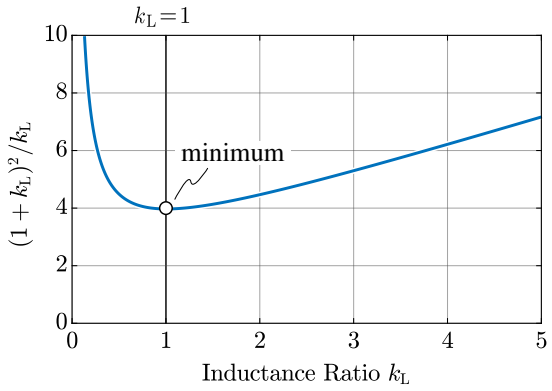


**Figure 5.** Asymptotic filter admittance trend $\propto (1+k_L)^2/k_L$ as function of the inductance ratio $k_L$.

According to (6), for a given attenuation requirement, $k_L = 1$ minimizes the product between the filter capacitance $C_f$ and the total filter inductance $L_{tot}$, thus resulting in minimum required capacitance for a given total inductance and vice-versa [33,35]. $k_L = 1$ is a necessary condition for the overall *LCL* filter size minimization, however it is not sufficient: the global minimum must be identified among all possible $(L_{tot}, C_f)$ combinations. Interestingly, two different Pareto optimizations in [37] yield *LCL* filter designs with equal converter-side and grid-side inductors, indirectly demonstrating the benefits of $k_L = 1$.

In general, the size of both inductive and capacitive components can be assumed to scale proportionally to their stored energy, respectively $\propto LI^2$ and $\propto CV^2$ [38]. Moreover, the energy storage density of inductors ($e_L$) and capacitors ($e_C$) typically differs by multiple orders of magnitude, being $e_L \ll e_C$ [38]. Therefore, it can be easily understood that in low-voltage ($V \downarrow\downarrow$) high-power ($I \uparrow\uparrow$) systems, as in the present case, the size of filter inductors largely dominates over the size of filter capacitors.

Moreover, in a first assumption, also filter cost and losses are primarily related to inductive components. This is quantitatively demonstrated in [41] and in [42], where a cost breakdown and a loss breakdown of grid-connected inverter systems are respectively reported.

As a consequence, a direct Pareto optimization is not strictly needed for determining the optimal component values, since a procedure aiming at the minimization of the total filter inductance should be pursued. Nevertheless, since too low inductance values can lead to excessive converter-side current ripple, i.e., generating undesired additional losses in the semiconductor devices and the inductive components themselves, a lower limit to the converter-side inductance value must be set.

Further benefits of minimizing the total filter inductance are minimum voltage drop under load, which allows to minimize the DC-link voltage and thus the semiconductor switching losses, and better dynamic performance, if the control loop is properly designed.

Moreover, $k_L = 1$ (i.e., $L = L_f$ disregarding $L_g$) allows to adopt equal converter-side and grid-side inductor designs, thus providing substantial effort and cost benefits.

It is worth mentioning that the value of $k_L$ affects the filter sensitivity to the parameter variations, which may in turn affect the converter control stability. One of the most relevant indicators of the *LCL* filter performance, both from a control and an attenuation perspectives, is the filter resonance frequency $f_0$. The per unit sensitivities of $f_0$ with respect to the per unit filter parameter variations can be obtained from (5), as in [33]:

$$\frac{df_0/f_0}{dL/L} = -\frac{1}{2}\frac{k_L}{1+k_L}, \tag{7}$$

$$\frac{df_0/f_0}{dC_f/C_f} = -\frac{1}{2}, \tag{8}$$

$$\frac{df_0/f_0}{d(L_f+L_g)/(L_f+L_g)} = -\frac{1}{2}\frac{1}{1+k_L}. \tag{9}$$

These expressions are graphically represented in Figure 6, as functions of $k_L$. While the resonance frequency sensitivity towards the variations of $L$ and $C_f$ (i.e., due to manufacturing tolerances) are of little importance, the sensitivity towards $(L_f + L_g)$ is much more relevant, since the grid inductance $L_g$ may vary depending on the converter installation location and may change with time. This is because $L_g$ reflects the equivalent grid inner impedance at the PCC, which is affected by the distribution grid operating conditions. It is observed from (9) that $k_L$ values higher than unity increase the control robustness against grid impedance variations, as also reported in [33]. Nevertheless, $k_L = 1$ results in a fairly good compromise, as diminishing benefits are obtained by further increasing $k_L$ (see Figure 6).

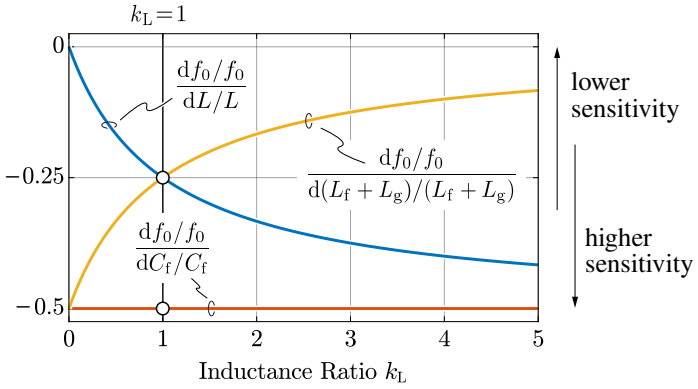


**Figure 6.** Per unit sensitivities of the *LCL* filter resonance frequency $f_0$ with respect to the per unit filter parameter variations, as functions of the inductance ratio $k_L$.

The adoption of an *LCL* filter has a substantial effect on the converter closed-loop control, as the filter resonance strongly affects the system stability. In some cases, depending on the control tuning and the *LCL* filter component values [23], the control stability may be lost. To avoid this, the most suitable approaches are to reduce the controller bandwidth (if/when allowed) or to adopt active or passive damping solutions [24].

Active damping operates by introducing additional feedback mechanisms inside the control loop, to improve its performance and achieve robust stability [43–46]. On the contrary, passive damping is achieved in a simpler way, by inserting resistors in series with the filter capacitors to directly damp the resonance peak [26], as previously shown in Figure 4, or adopting alternative filter structures with higher complexity [47–51]. Even though passively damped *LCL* filters are characterized by power losses in the resistors and lower overall asymptotic attenuation (i.e., 40 dB/dec), passive damping is typically preferred, due to its simple implementation, straightforward design and no need for additional measurements and computational overhead (i.e., required instead for active damping).

It is worth noting that the required damping cannot be determined without knowing the current control loop transfer function [26]. Nevertheless, when this is the case, a resistance value similar to the impedance of the filter capacitor at the resonance frequency is normally selected, such as $R_f = 1/(3\omega_0 C_f)$ [32].

As previously mentioned, the grid inductance $L_g$ is generally not known during the filter design process. In fact, the converter installation location is usually undefined and it may witness large inductance variations during the day and/or along the year. In general, the converter control stability can be compromised by a weak grid with high inductive impedance and low short-circuit ratios (SCRs), as the filter resonance frequency $f_0$ decreases and may interfere with the controller bandwidth [52]. For this reason, a suitable margin must be considered during the filter design and the converter control tuning stages.

## 3. Design Procedure

In this section, the proposed *LCL* filter design space optimization procedure is described and applied to the specific requirements of an AFE unit for EV ultra-fast battery charging. Therefore, the specifications and performance targets given by the application are first reported. Then, the constraints affecting the *LCL* filter parameters are analytically derived and formally expressed, so that the filter design space is identified. Finally, the *LCL* parameter combination minimizing the total filter inductance is selected among the feasible results, ensuring an optimal filter size/loss trade off (i.e., minimum losses for a fixed volume and vice versa).

### *3.1. Specifications and Performance Targets*

This work considers a modular UFC (consisting of N modules) connected to the European low-voltage grid (i.e., 50 Hz, 400 V line-to-line), schematically illustrated in Figure 7. Each of the N AFE modules consists of a 3-level unidirectional T-type rectifier and an *LCL* filter, both rated at 30 kW nominal active power. Notably, each module must ensure proper filtering at the PCC by itself, since the number of paralleled modules in one installation is generally not defined. The specifications and nominal operating conditions of a single converter unit are summarized in Table 1.

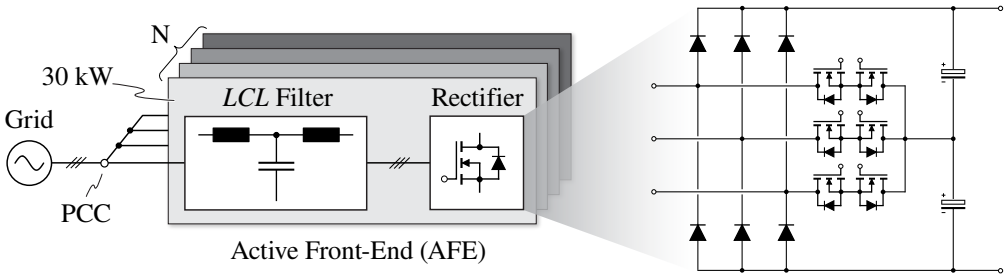


**Figure 7.** Schematic overview of the considered modular electric vehicle (EV) ultra-fast battery charger with highlight of the active front-end (AFE) T-type converter topology. Each of the N modules is rated at 30 kW nominal active power.

**Table 1.** Active front-end (AFE) specifications and nominal operating conditions.

| Parameter | Description | Value |
|---|---|---|
| $f$ | grid frequency | 50 Hz |
| $P$ | nominal active power | 30 kW |
| $Q$ | no-load reactive power | $\leq$ 3 kvar |
| $V$ | peak phase voltage | 325 V |
| $I$ | peak phase current | 61.5 A |
| $\cos\varphi$ | power factor | $\geq$0.995 |
| $V_{dc}$ | DC-link voltage | 650–800 V |
| $f_{sw}$ | switching frequency | 20 kHz |

The fundamental role of the *LCL* filter is to achieve the AFE compliance with the harmonic emission standards at the PCC, prescribed by IEEE 519 [21,53]. These standards restrict the maximum amplitude of the current harmonics injected into the grid, varying with the grid voltage level and short-circuit ratio (SCR). In fact, these limits were originally developed to maintain the voltage harmonics at the PCC within a defined percentage of the nominal voltage, considering a purely inductive distribution system [29] (i.e., lower SCR values translate in higher voltage distortion for equal injected current harmonics).

The relevant IEEE 519 harmonic limits for the present application are reported in Table 2 as a percentage of the nominal current. These limits are more stringent for even-order harmonics, which are set to 25% of the odd ones. Since the installation of the converter is not predetermined, as already mentioned, the worst-case SCR ratio (i.e., <20) is considered herein. Moreover, since $f_{sw} = 20\,\text{kHz}$, all the switching harmonics generated by the converter are higher than the 35th (i.e., 1750 Hz), therefore 0.3% and 0.075% limits apply to odd and even harmonics respectively. Even though IEEE 519 also defines a maximum current total harmonic distortion (THD), the stringent harmonic limits at high frequency allow to directly satisfy the maximum THD constraint by a large margin, given that the low-frequency harmonics are effectively minimized by the converter control.

**Table 2.** IEEE 519 current harmonic limits for distribution systems with a 0.12–69 kV nominal operating voltage [21]. The reported values refer to the maximum injected odd-harmonic current distortion in percent of $I$. Even-order harmonics are limited to 25% of the odd-harmonic limits.

| $I_{sc}/I$ (SCR) | $h < 11$ | $11 \leq h < 17$ | $17 \leq h < 23$ | $23 \leq h < 35$ | $35 \leq h$ |
|---|---|---|---|---|---|
| <20 | 4.0 | 2.0 | 1.5 | 0.6 | 0.3 |
| 20 ... 50 | 7.0 | 3.5 | 2.5 | 1.0 | 0.5 |
| 50 ... 100 | 10.0 | 4.5 | 4.0 | 1.5 | 0.7 |
| 100 ... 1000 | 12.0 | 5.5 | 5.0 | 2.0 | 1.0 |
| >1000 | 15.0 | 7.0 | 6.0 | 2.5 | 1.4 |

$I_{sc}$: short-circuit current, $I$: rated current, $h$: harmonic number.

### *3.2. Parameters and Constraints*

Due to its high-order structure, an *LCL* filter has multiple design degrees of freedom, i.e., the filter component values $L$, $L_f$, $C_f$ and $R_f$. Since the grid inner inductance $L_g$ is generally not known, the proposed design procedure considers $L_g = 0$, such that the attenuation performance of the *LCL* filter are satisfied in every condition.

One design degree of freedom is removed by fixing the ratio between the grid-side inductance and the converter-side inductance at $k_L = 1$ (i.e., $L = L_f$), according to the considerations reported in Section 2. As previously mentioned, this ratio allows to maximize the attenuation performance of the filter for a given amount of total inductance $L_{tot}$, thus representing a necessary condition for the filter size and loss minimization.

Another degree of freedom is eliminated either by considering an active damping control strategy (i.e., $R_f = 0$) or by selecting the passive damping resistance value as a function of the filter capacitor impedance at the resonance frequency, i.e., $R_f = 1/(3\omega_0 C_f)$ as in [32]. To ease the controller implementation, the passive damping solution is adopted herein.

Therefore, only two design degrees of freedom remain, namely the choice of $C_f$ and of one between $L$ and $L_f$. Being $k_L = 1$, the parameter $L_{tot} = L + L_f = 2\,L$ best represents the second degree of freedom.

A three-phase high-power *LCL* filter for EV ultra-fast battery charging must comply with several design constraints of different nature, namely:

1. The filter resonance frequency $f_0$ must be higher than 10 times the grid frequency ($f_{0,min} = 10\,f$), to avoid resonance interactions in the lower part of the harmonic spectrum and allow for a sufficient current control bandwidth (i.e., $f_{bw} < f_0$).
2. The filter resonance frequency $f_0$ must be lower than half of the switching frequency ($f_{0,max} = f_{sw}/2$), to avoid unwanted amplification of switching harmonics. Even if

damped, the resonance peak tends to amplify the nearby harmonics (see Figure 4c), which may thus exceed the IEEE 519 limits.

3. The current ripple in the converter-side inductor $L$ must be kept below a specified amount to avoid excessive losses in the semiconductor devices (i.e., conduction and switching losses) and in the inductors themselves (i.e., winding and core losses). Moreover, in the present unidirectional case, this current ripple must be limited to narrow the discontinuous conduction mode operation around the waveform zero-crossings, which causes low-frequency harmonic distortion [54]. This limit is set to 20% of the peak nominal current ($\Delta I_{\mathrm{pp,max}} = 0.2\,I$).
4. The maximum voltage drop in nominal load conditions must be lower than a specified value depending on the high-line grid voltage ($U_{\mathrm{max}} = 1.1\,U_{\mathrm{nom}}$), the maximum modulation index of the active rectifier ($M_{\mathrm{max}} = 2/\sqrt{3} \approx 1.15$, with $M = 2\,V/V_{\mathrm{dc}}$) and the minimum DC-link voltage $V_{\mathrm{dc,min}}$, resulting in $\Delta V_{\mathrm{max}} = \sqrt{V_{\mathrm{dc,min}}^2/3 - U_{\mathrm{max}}^2}$.
5. The maximum no-load reactive power generation is set to 10% of the nominal power ($Q_{\mathrm{max}} = 0.1\,P$). The reactive current circulation generates losses in the system components (i.e., the $LCL$ filter and the distribution equipment), therefore it must be limited accordingly.
6. The minimum power factor at a specified minimum load condition ($P_{\mathrm{min}} = P/2$) is set to $\cos\varphi_{\mathrm{min}} = 0.995$, taking into account that the unidirectional rectifier cannot generate or absorb reactive power without affecting the low-frequency input current distortion. $P_{\mathrm{min}} = P/2$ is selected taking into account that the adopted modular structure (see Figure 7) allows to turn-off selected converter modules with decreasing load, thus ensuring high power factor over the complete charging range.
7. The minimum filter attenuation $A^*(f_{\mathrm{d}})$ must ensure that the injected current harmonics comply with the IEEE 519 limits (see Table 2). An additional margin of 50% (i.e., $\approx 3.5\,\mathrm{dB}$), taking into account component tolerances and unmodeled factors, is assumed herein.

Since the $LCL$ filter design space is characterized by two degrees of freedom, all constraints are expressed as functions of $C_{\mathrm{f}}$ and $L_{\mathrm{tot}}$ in Table 3.

**Table 3.** $LCL$ filter design constraints in terms of $C_{\mathrm{f}}$ and $L_{\mathrm{tot}}$, considering $L_{\mathrm{g}} = 0$, $L = L_{\mathrm{f}}$ (i.e., $k_{\mathrm{L}} = 1$) and $R_{\mathrm{f}} = 1/(3\omega_0 C_{\mathrm{f}})$.

| Description | Constraint | Analytical Expression |
|---|---|---|
| ① minimum resonance frequency | $f_0 \geq f_{0,\mathrm{min}}$ | $C_{\mathrm{f}} \leq \dfrac{1}{\pi^2 f_{0,\mathrm{min}}^2 L_{\mathrm{tot}}}$ |
| ② maximum resonance frequency | $f_0 \leq f_{0,\mathrm{max}}$ | $C_{\mathrm{f}} \geq \dfrac{1}{\pi^2 f_{0,\mathrm{max}}^2 L_{\mathrm{tot}}}$ |
| ③ maximum inductor current ripple | $\Delta I_{\mathrm{pp}} \leq \Delta I_{\mathrm{pp,max}}$ | $L_{\mathrm{tot}} \geq 2\dfrac{\Delta\Psi_{\mathrm{pp}}}{\Delta I_{\mathrm{pp,max}}}$ |
| ④ maximum load voltage drop | $\Delta V \leq \Delta V_{\mathrm{max}}$ | $L_{\mathrm{tot}} \leq \dfrac{\sqrt{V_{\mathrm{dc,min}}^2/3 - U_{\mathrm{max}}^2}}{2\pi f I}$ |
| ⑤ maximum no-load reactive power | $Q \leq Q_{\mathrm{max}}$ @ $P = 0$ | $C_{\mathrm{f}} \leq \dfrac{Q_{\mathrm{max}}}{3\pi f U^2}$ |
| ⑥ minimum power factor | $\cos\varphi \geq \cos\varphi_{\mathrm{min}}$ @ $P = P_{\mathrm{min}}$ | $C_{\mathrm{f}} \leq L_{\mathrm{tot}}\dfrac{I_{\mathrm{min}}^2}{U^2} + \dfrac{P_{\mathrm{min}}}{3\pi f U^2}\dfrac{\sqrt{1-\cos^2\varphi_{\mathrm{min}}}}{\cos\varphi_{\mathrm{min}}}$ |
| ⑦ minimum IEEE 519 attenuation | $I_{\mathrm{h}} \leq I_{\mathrm{IEEE,519}}(f_{\mathrm{h}})\ \forall\ \mathrm{h}$ | $\begin{cases} C_{\mathrm{f}} \geq \dfrac{A^*(f_{\mathrm{d}})}{2\pi^3 f_{\mathrm{d}}^3 L_{\mathrm{tot}}^2} & \text{undamped } (R_{\mathrm{f}} = 0) \\ C_{\mathrm{f}} \geq \dfrac{A^{*2}(f_{\mathrm{d}})}{36\pi^4 f_{\mathrm{d}}^4 L_{\mathrm{tot}}^3} & \text{damped } (R_{\mathrm{f}} \neq 0) \end{cases}$ |

The identification of constraints ③ and ⑦ requires either analytical or numerical estimations of the converter voltage waveforms in the time/frequency domains. A numerical approach is pursued herein, implementing a simple and straightforward simulation in MATLAB environment as in [20]. The peak-to-peak converter-side inductor flux ripple $\Delta\Psi_{pp}$ (required by ③) and the full harmonic spectrum of the converter output voltage (required by ⑦) are obtained in post-processing by means of discrete Fourier transforms (DFTs).

A specific 3-level modulation strategy is considered in this work, namely the zero mid-point current modulation (ZMPCPWM) [20]. This strategy practically eliminates the 150 Hz DC-link mid-point voltage ripple typically present in 3-level converters [17,18], thus ensuring minimum DC-link capacitance requirement. Moreover, this feature is particularly needed in EV fast charging, as separate DC/DC units are usually connected to the upper and lower side of the AFE DC-link [55]. In fact, these converter units are subject to the mid-point voltage ripple and they may not be able to reject it [11], allowing for the voltage oscillation to get through and reach the battery-side.

The converter-side inductor flux ripple $\Delta\psi$ is obtained by integration of the high-frequency component of the phase voltage $v_{HF}$ (see Figures 2 and 3), assuming that it is completely applied across $L$ (i.e., no voltage ripple at the filter capacitor terminals):

$$\Delta\psi_x(t) = \int_0^t v_{HF,x}\,dt \qquad x = a, b, c. \tag{10}$$

The peak-to-peak flux ripple $\Delta\Psi_{pp}$ is calculated for different values of DC-link voltage within the operating range reported in Table 1. The results are shown in Figure 8 and a maximum value $\Delta\Psi_{pp} = 2.16$ mVs (required by constraint ③) is found for $V_{dc} = 800$ V.

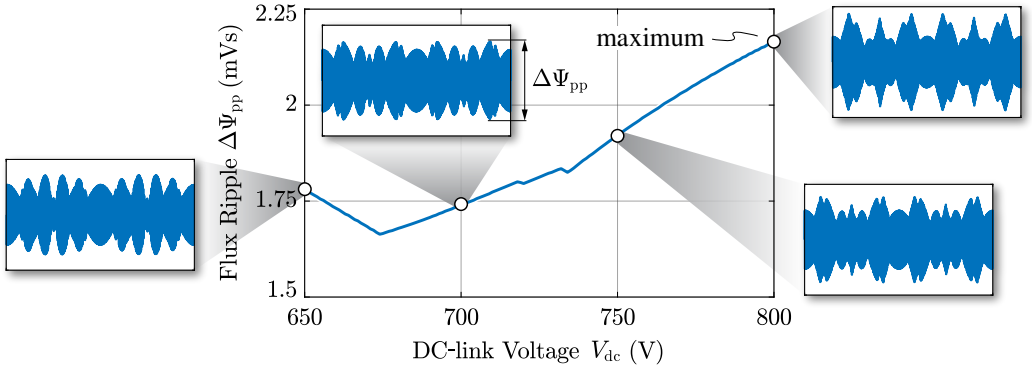


**Figure 8.** Peak-to-peak grid-side inductor flux ripple $\Delta\Psi_{pp}$ considering zero mid-point current modulation and variable DC-link voltage $V_{dc}$. A highlight of the time-domain waveforms is provided.

To calculate the minimum attenuation $A^*$ needed to comply with IEEE 519 (i.e., constraint ⑦), the asymptotic filter transfer function expression (6) can be exploited, as the $LCL$ resonance frequency $f_0$ is sufficiently lower than the switching frequency:

$$A(f_h) = \frac{1}{|Y_{f,s\to\infty}(j2\pi f_h)|} = \frac{\pi^2 f_h^2 L_{tot}^2}{R_f} \qquad f_h \gg f_0. \tag{11}$$

In the present passively damped case, the filter attenuation increases with a 40 dB/dec rate. $A(f_h)$ represents the input-to-output filter impedance at the h-th harmonic, linking the voltage harmonics $V_h$ generated by the converter to the current harmonics $I_h$ injected at the PCC. Therefore, the required harmonic attenuation to satisfy the IEEE 519 limits, including a safety margin, can be described in logarithmic scale (dB) as

$$A^*_{dB}(f_h) = V_{h,dB}(f_h) - I_{h,limit,dB}(f_h) + \text{margin}_{dB}. \tag{12}$$

The harmonic frequency $f_h$ which requires the largest filtering effort to comply with the harmonic limits is referred to as the design frequency $f_d$:

$$f_d = f_h \iff \max\left[A^*(f_h) - 40\log_{10}(f_h)\right]. \tag{13}$$

This frequency value identifies the worst-case filter design condition, corresponding to the maximum filter component values.

Same as for the flux ripple case, the maximum required attenuation is found for maximum DC-link voltage. The harmonic spectrum of the converter output voltage at $V_{dc} = 800\,\text{V}$ is illustrated in Figure 9, showing an even-order design frequency $f_d = 19.6\,\text{kHz}$ and a required attenuation $A^*(f_d) \approx 570\,\Omega \approx 55\,\text{dB}\,\Omega$ including the 50% design margin.

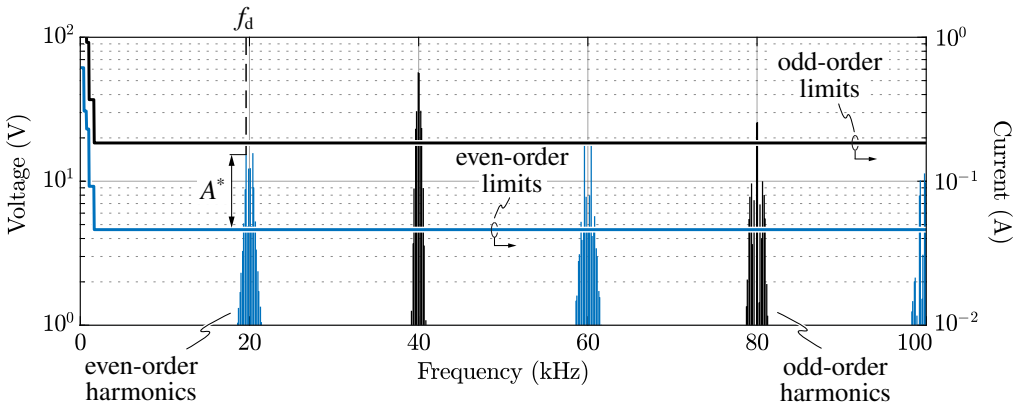


**Figure 9.** Converter output voltage harmonic spectrum at $V_{dc} = 800\,\text{V}$ and current harmonic limits according to IEEE 519. Odd and even-order harmonics are colored in black and blue respectively. The filter design frequency $f_d$ and the required attenuation $A^*$ (without the margin) are indicated.

It is worth noting that, even though the averaged voltage waveform that is synthesized at the converter output is characterized by half-wave symmetry, the instantaneous PWM waveform is not, thus leading to the generation of both odd and even-order switching harmonics [56]. In particular, the generated harmonic orders can only be odd combinations of the carrier frequency (index $m$) and the fundamental frequency (index $n$):

$$f_h = m\,f_{sw} \pm n\,f \qquad m,n \in \mathbb{N} \text{ and } (m \pm n) = 2k+1,\ k \in \mathbb{Z} \tag{14}$$

Therefore, if $m$ is odd, all sideband harmonics with $n$ even disappear and vice-versa. In particular, being $f_{sw} = 20\,\text{kHz}$ an even multiple of $f = 50\,\text{Hz}$, the $h$-th harmonic will be an odd or even-order multiple of $f$ only depending on the index $n$. For instance, the first switching harmonic distribution (i.e., corresponding to $m = 1$) only consists of even-order $h$ harmonics, being $n$ even (i.e., $n = 2, 4, \ldots$). On the contrary, the second switching harmonic distribution (i.e., corresponding to $m = 2$) is only made up by odd-order $h$ harmonics, being $n$ odd (i.e., $n = 1, 3, \ldots$). This alternating behavior is better illustrated in Figure 9, where odd and even-order harmonics are differently colored.

### *3.3. Filter Design Space*

The proposed design methodology is based on translating the constraints ①–⑦ into boundaries in the filter design space ($C_f$, $L_{tot}$), so that the feasible design region can be identified. This representation allows to have a clear view of the available freedom for the filter optimization. Even though multiple different optimization criteria have been proposed in literature (see Section 2), in this work the feasible design with lowest total inductance $L_{tot}$ is considered as the best candidate, since in low-voltage high-power applications inductive components dominate the overall filter size, cost and losses.

The results of the proposed design procedure are illustrated in Figure 10, where the design constraints are graphically represented and bound the available design space. The feasible $LCL$ filter design with minimum total inductance is here found at the intersection between boundaries ③ (i.e., maximum converter-side inductor current ripple) and

⑦ (i.e., minimum required attenuation). The parameters $L$, $C_f$, $L_f$ and $R_f$ of the selected optimal design are reported in Figure 10.

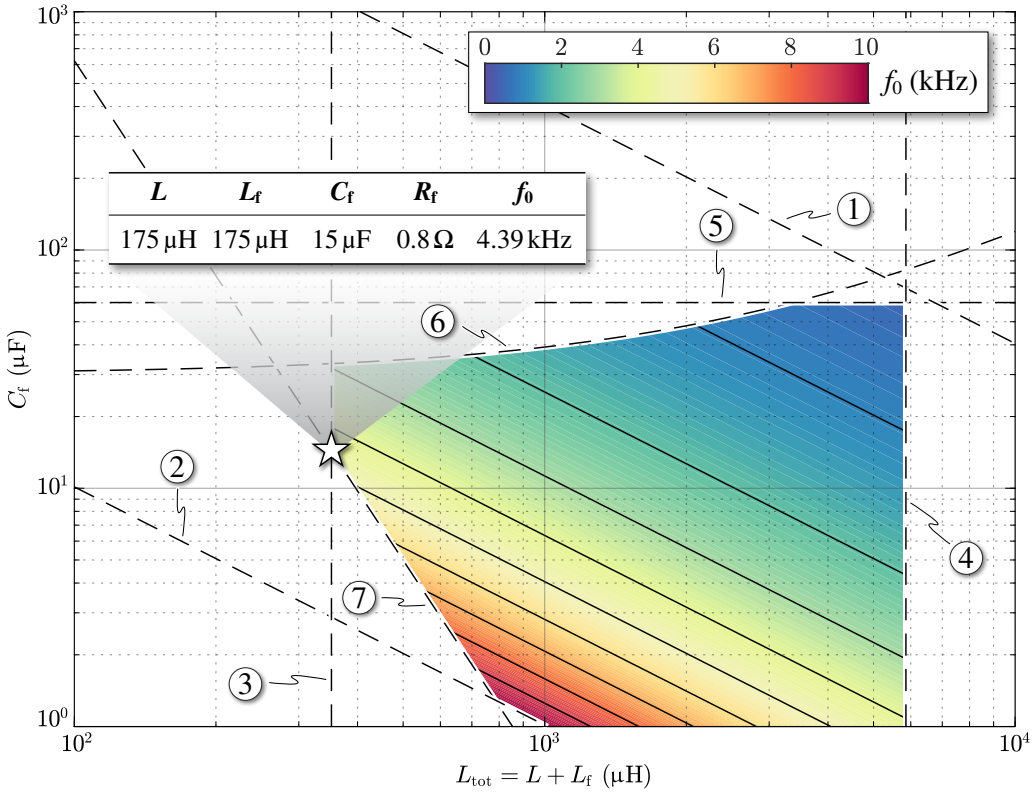


**Figure 10.** *LCL* filter design space in the $(C_f, L_{tot})$ logarithmic plane. Constraints ①– ⑦ bound the feasible design region. The design with minimum total inductance is selected and the parameter values of the *LCL* filter are reported in the highlighted table.

To evaluate the impact of resistor losses on the converter efficiency, they can be calculated by assuming that the high-frequency current ripple $\Delta i_{RMS}$ completely flows into the capacitor branch (i.e., $\Delta i_{RMS} = \Delta \psi_{RMS}/L$) as

$$P_{loss} = 3\,R_f \left[ \Delta i_{RMS}^2 + \frac{U_{RMS}^2}{[1/(j\,2\pi f C_f) + R_f]^2} \right], \tag{15}$$

which are illustrated in Figure 11. In the optimal design point the total damping losses amount to ≈ 13 W, thus yielding a negligible efficiency drop of 0.04%.

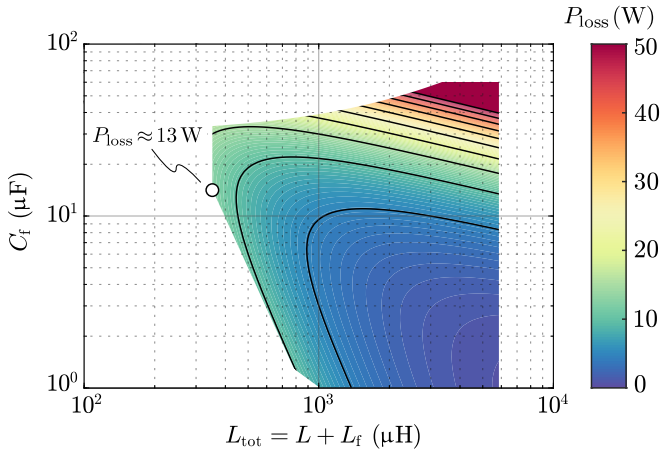


**Figure 11.** Resistive damping loss as function of $L_{tot}$ and $C_f$.