Rail-to-Rail Dynamic Voltage Comparator Scalable down to pW-Range Power and 0.15-V Supply

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***Abstract*— An ultra-low voltage, ultra-low power rail-to-rail dynamic voltage comparator solely based on digital standard cells is presented. Thanks to its digital nature, the comparator can be designed and integrated with fully-automated digital design flows and can operate at very low voltages down to deep sub-threshold. Measurements on an 180nm testchip show correct operation under rail-to-rail common-mode input at a supply voltage ranging from 0.6V down to 0.15V. The comparator delay (power) is lower than 442µs (10pW) at 0.15-V supply voltage. The input offset voltage is less than 30mV over the entire rail-to-rail common-mode input and supply range. The minimum supply voltage and power are the lowest reported to date, and make the circuit suitable for direct powering from mm-scale harvesters.**

***Index Terms*—Dynamic comparator, fully-synthesizable, ultra-low voltage, ultra-low power, sensor nodes, Internet of Things.**

I. INTRODUCTION

Relentless circuit innovation to enable operation over a wide range of supply voltages is necessary to meet the tight power and cost targets of sensor nodes for the Internet of Things (IoT) [1]. For this reason, circuit solutions based on digital standard cells have been explored to push the minimum supply voltage down to deep sub-threshold, and reduce the human design effort to drive cost down. Standard cell-based approaches are inherently more amenable for aggressive voltage scaling, automated design, design, and technology porting than their analog counterparts while enabling novel capabilities such as graceful quality degradation at over-scaled voltages [2]-[6].

Being a ubiquitous building block in sensor interfaces, fully-synthesizable dynamic voltage comparators (DVCs) have been widely explored [2], [7]-[10], in view of their ability to be automatically designed with the digital modules they drive [11], [12]. A popular fully-synthesizable DVC has been proposed for stochastic analog-to-digital converters [7]-[8]. Their power in the hundreds of nWs cannot be supported by low-cost systems being powered directly by an mm-scale harvester, and its narrow common-mode input range (CMR) restricts its usage to very specific applications. The latter limitations were removed in [9], which allows rail-to-rail input. Fully-synthesizable DVCs with reduced propagation delay were proposed in [2], [10], and enhanced with input stage redundancy in [11], at the cost of increased power that makes them unsuited for the above applications.

In this paper, a fully-synthesizable rail-to-rail dynamic voltage comparator (RRDVC [9]) is demonstrated on silicon and its key design tradeoffs are experimentally explored. Measurements show operation from near-threshold (600mV) down to deep sub-threshold (150mV) with power consumption down to the pW level and fJ-range power-delay product. Such properties make it well suited for integrated systems that are directly powered by harvesters, which have gained significant attention thanks to their low cost and small form factor [1].

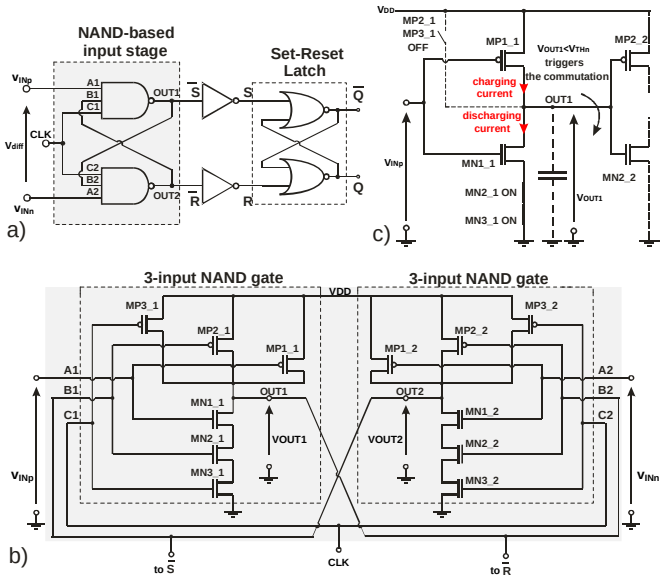

Fig. 1. Fully-synthesizable comparator with NAND3 input stage in [7]: a) gate-level and b) transistor-level view, c) equivalent circuit during output transition.

The paper is structured as follows. The CMR limitation of the DVC baseline in [7] is firstly analyzed in Section II. The improved DVC topology is then introduced in Section III to overcome its limitations. Section IV shows the measurement results and compares the performance with the state of the art. Concluding remarks are drawn in Section V.

II. PRIOR FULLY-SYNTHESIZABLE DYNAMIC VOLTAGE COMPARATORS AND LIMITATIONS

The DVC presented in this brief is inspired by the circuit originally proposed in [7], which is reported in Fig. 1a. The latter includes an input stage consisting of two NAND3 gates, which in turn drive a set-reset (SR) latch. The gate-level schematic of the NAND3-based input stage is shown in Fig. 1b. The inputs A1 and A2 of the NAND3 gates are tied to the gate terminals of transistors MN1_1, MP1_1, MN1_2 and MP1_2, and are connected to the non-inverting (v_{INp}) and inverting (v_{INn}) input. The inputs $B1$ and $B2$ drive the gate terminals of MN2_1, MP2_1 and MN2_2, MP2_2, and are tied to the outputs $OUT2$ and $OUT1$ of the NAND3 gates in a cross-coupled fashion. Finally, the inputs $C1$ and $C2$ are connected to the gate terminals of MN3_1, MP3_1 and MN3_2, MP3_2, and are connected to the sampling clock, as in Fig. 1b. The outputs $OUT1$ and $OUT2$ are also connected to the set (S) and reset (R) inputs of the SR latch via inverter gates to hold the comparator output when the sampling clock is low (i.e., hold state). In this case, $OUT1$ and $OUT2$ are precharged to the supply voltage V_{DD} and transistors MN2_1 and MN2_2 are on, due to the cross-coupled feedback connection.

The sampling phase starts at the rising clock transition, when transistors MP3_1 and MP3_2 are turned off, thus disabling the precharge of $OUT1$ and $OUT2$. At the same time, transistors MN3_1 and MN3_2 are turned on, thus enabling the pull-down networks of the two NAND gates. In particular, transistors MN2_1 and MN2_2 are still on immediately after the rising clock edge, since $OUT1$ and $OUT2$ are still at V_{DD}.

During the sampling phase and under a positive input differential voltage $v_{DM} = v_{INp} - v_{INn}$, $OUT1$ is pulled down faster than $OUT2$ by MN1_1, since the gate voltage of MN1_2 is lower than the gate voltage of MN1_1. As a consequence, $OUT1$ reaches V_{THn} before $OUT2$, where V_{THn} is the threshold voltage of NMOS transistors. The inherent positive feedback forces $OUT1$ to be latched low, and $OUT2$ to be latched high. Opposite considerations hold for negative differential input v_{DM}. In summary, the outputs of the SR latch Q and $\bar{Q}$ are set by the polarity of the input differential voltage at the rising clock edge as expected from a DVC, and is latched by the SR latch.

As a limitation of the DVC circuit in Fig. 1b, $OUT1$ ($OUT2$) is pulled down by transistor MN1_1 (MN1_2), which suffers from current contention with transistors MP1_1 (MP1_2) as they are both driven by the same analog input. The contention is negligible when the common-mode input is close to V_{DD}, since MP1_1 and MP1_2 are off and their current is insignificant compared to MN1_1 and MN1_2. Current contention between MP1_1 and MN1_1 (MP1_2 and MN1_2) inevitably increases at lower common-mode input voltages. Indeed, the drain current of MP1_1 and MP1_2 substantially increases at common-mode input voltages around $V_{DD}/2$ and below, and overwhelms the current of MN1_1 and MN1_2. Hence, the common-mode range is limited to voltages larger than $V_{DD}/2$ [7], whereas lower voltages incorrectly force $OUT1$ and $OUT2$ at V_{DD} regardless of the input (i.e., the comparator stops operating). Similarly, a dual issue occurs when the NAND3 gates in Fig. 1a are replaced by NOR3 gates as in Fig. 2, as this restricts the common-mode input range to $V_{DD}/2$ and below.

III. Rail-To-Rail Fully-Synthesizable Dynamic Voltage Comparator

The half-swing common-mode limitations of the fully-synthesizable DVCs in Figs. 1a and 2 are overcome by the proposed Rail-to-Rail DVC (RRDVC) in Fig. 3a. From this figure, the RRDVC combines the digital outputs of the NAND3- and NOR3-based DVCs in the same fashion as an NMOS and a PMOS differential pair are merged in "complementary differential pairs" for conventional rail-to-rail analog operational amplifiers [11].

To combine the outputs of the NAND3 and NOR3 DVCs, a special dual-input SR latch with two set inputs S1 and S2, and two reset inputs R1 and R2 are introduced. S1 and S2 (R1 and R2) are ORed to enable correct operation at any common-mode input from the ground to V_{DD}. Indeed, the correct operation of just one type of input stage (i.e., either the NAND3-based or the NOR3-based) is sufficient to drive the SR latch correctly, in view of the OR-based merger. In detail, at any given common-mode input voltage, the NAND3 (NOR3) gate in Fig. 3a is able to generate the correct output when common-mode input ranges from $V_{DD}/2$ to V_{DD} (ground to $V_{DD}/2$), whereas the NOR3 (NAND3) output is stuck at the pre-charged level. Accordingly,

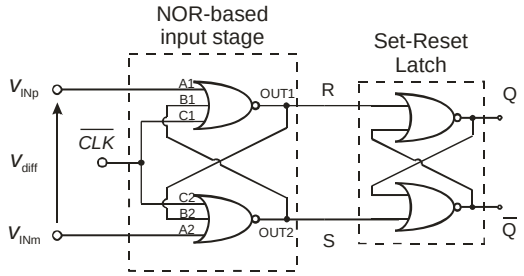

Fig. 2. Fully-synthesizable DVC with NOR-based input stage (NOR3-DVC), whose common-mode range goes from ground to $V_{DD}/2$ [9].

there is always at least one logic gate at the input stage (either NAND3 or NOR3) that operates correctly, and hence generate the correct outputs driving the dual-input SR latch at any common-mode input in Fig. 3a. At the same time, when the common-mode input is at $V_{DD}/2$ or above, the NOR3 gates fail and their outputs are stuck at the ground, and hence do not affect the correct DVC output since $S2$ and $R1$ are both low. Dually, when the common-mode input is at $V_{DD}/2$ or below, the NAND3 gates fail and their outputs are stuck at V_{DD}, leaving the correct DVC output unaffected since $S1$ and $R2$ are both low, due to the inverter gates I6-I7 in Fig. 3a.

When the common-mode input is around the mid-range, both the NOR3 and the NAND3 gates constructively contribute to the correct comparison decision. Due to simultaneous operation, power is expected to increase compared to the above cases with high or low common-mode range. This is due to the onset of the cross-conduction current in both NAND3 and NOR3 gates, due to current contention between MP1_1 and MN1_1, and between MP1_2 and MN1_2. Since the source-gate (gate-source) voltage of MP1_2 (MN1_2) is $V_{DD}/2 - V_{TH}$ at mid-range input, the cross conduction current problem is expectedly more pronounced at higher supply voltages and lower threshold voltages, and sets the supply voltage upper bound of the RRDVC at near-threshold voltages.

IV. Test Chip and Experimental Results

The proposed RRDVC was designed and fabricated in

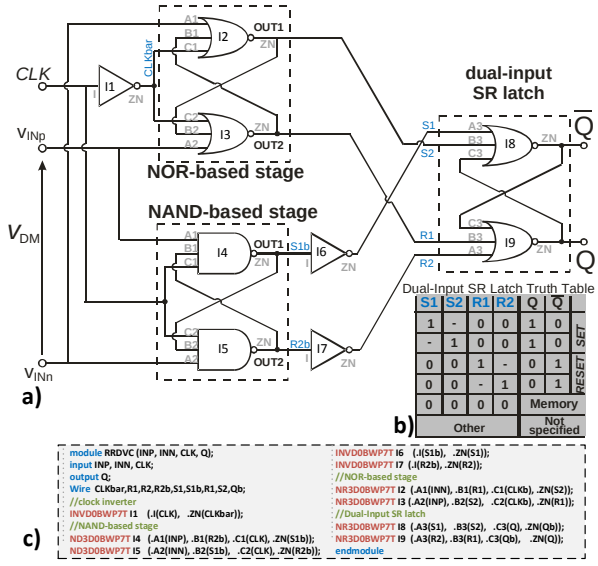

Fig. 3. Proposed fully-synthesizable RRDVC with complementary NAND/NOR input stage and dual-input SR latch: a) gate-level structure, b) truth table of the dual-input SR latch, c) structural Verilog code for synthesis.

180nm CMOS, starting from the structural Verilog description in Fig. 3c. Among the available power-speed trade-offs, minimum-sized standard cells were used to minimize power. Higher cell strengths reduce the propagation delay at the expense of higher power. The netlist was translated into the final layout via automated PnR with a commercial design tool with no pre- or post-layout optimization to preserve the original structure. This allows to integrate the RRDVC with the subsequent digital logic, e.g. SAR logic in ADCs. The die micrograph in Fig. 4 exhibits a very compact area of 900µm^2.

The choice of the strength of the input logic gates in Fig. 3 also affects the comparator offset, based on the Pelgrom's law offset dependence on the reciprocal of the square root of the cell strength [14]. In other words, input offset reductions come at the cost of a higher power and simultaneously reduce the propagation delay. The maximum size limitations imposed by the adopted standard cell library are easily removed by connecting more standard cells in parallel via structural Verilog description, while still suppressing any pre- or post-layout optimization during placement and routing.

Five RRDVC dice were experimentally characterized at three supply voltages covering the deep sub-threshold (V_{DD}=0.15V), the sub-threshold (V_{DD}=0.3V) and the near-threshold (V_{DD}=0.6V) region. The results are summarized in Subsection A and compared with the prior art in Subsection B.

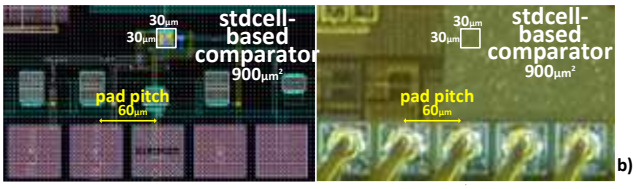

Fig. 4. Proposed fully-synthesizable comparator with complementary NAND/NOR input stage and dual-input SR latch: a) layout, b) die photo.

A. Measured Results

The clock-to-output propagation delay of the RRDVC was measured across the entire rail-to-rail input common-mode range for a differential input voltage v_{DM} of 10 mV. The measurement results are reported in Fig. 5 for a supply voltage of 0.15V (Fig. 5a), 0.3V (Fig. 5b), and 0.6V (Fig. 5c). From these figures, the propagation delay is expectedly maximum at v_{CM}=V_{DD}/2, due to the above discussed cross-conduction current at inputs with intermediate common-mode range. From Figs. 5a-c, the delay spread across the five dice is lower than its fluctuations determined by v_{CM} at 0.3V and 0.6V supply, whereas it is about 2X at 150mV.

The impact of the differential input voltage v_{DM} on the propagation delay is plotted versus the differential input v_{DM} in Figs. 6a-c for a supply voltage V_{DD} of 0.15V, 0.3V and 0.6V respectively, under v_{CM}=V_{DD}/2. The sensitivity of the propagation delay to the input differential voltage expectedly increases at lower supply voltages, due to the larger sensitivity of the current to the gate-source voltage in the sub-threshold and the deep sub-threshold region. Quantitatively, the maximum slope of the voltage-delay curve for die #1 is 25µs/V at V_{DD}=0.6V, 1.5ms/V at V_{DD}=0.3V, and reaches the highest value of 21.6ms/V at V_{DD}=0.15V.

Figs. 7a-c show the power consumption of the proposed RRDVC versus v_{CM} for a supply voltage of 0.15V, 0.3V and 0.6V respectively, and for a clock frequency of 10Hz and 10kHz. The maximum power consumption averaged on the five dice is respectively 6.2pW (27pW), 24pW (89pW) and 1.95nW

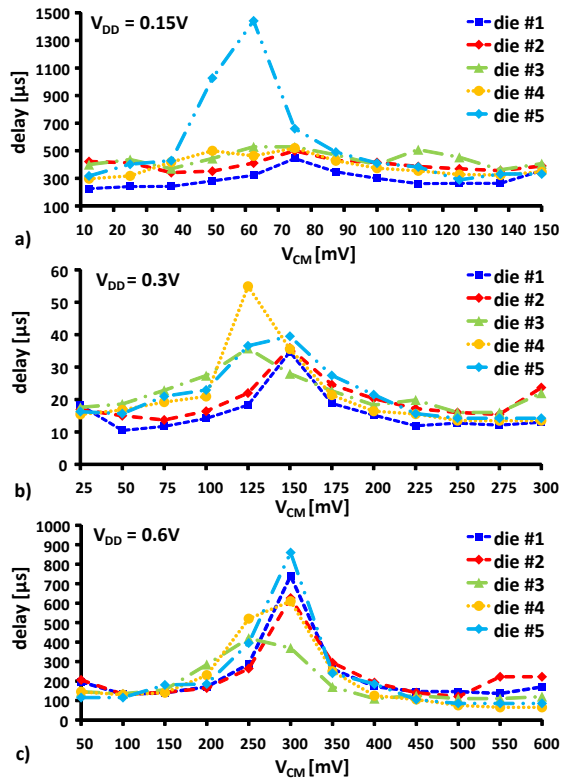

Fig. 5. Measured clock-to-output propagation delay of the proposed RRDVC vs. common-mode input voltage for five dice at differential input voltage v_{DM}=10mV and supply of a) V_{DD}=0.15V, b) V_{DD}=0.3V and c) V_{DD}=0.6V.

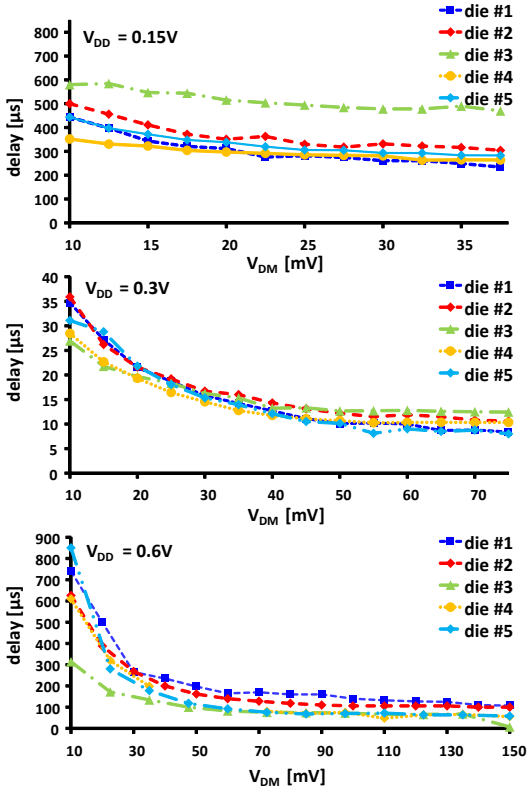

Fig. 6. Clock-to-output propagation delay versus differential input voltage v_{DM} for five dice of the proposed RRDVC at a) V_{DD}=0.15 V, b) V_{DD}=0.3 V and c) V_{DD}=0.6 V (v_{CM}=V_{DD}/2).

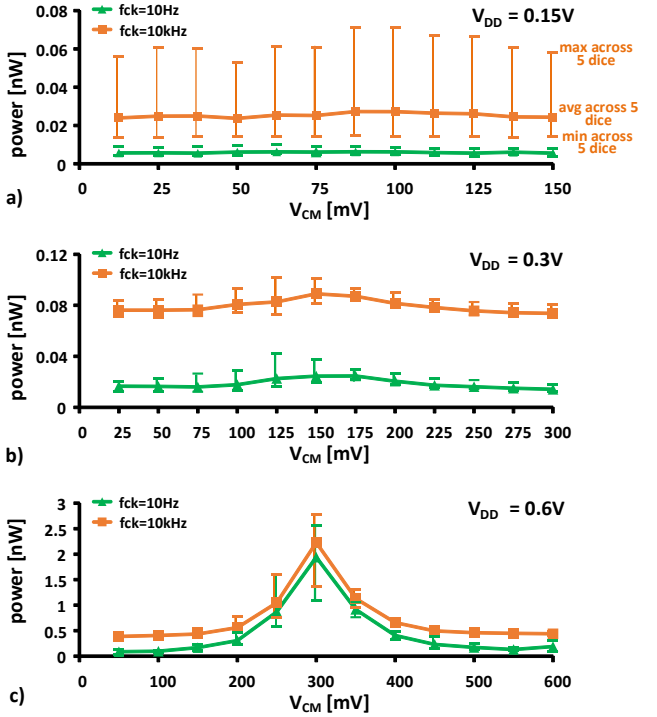

Fig. 7. Power of RRDVC vs. v_{CM} measured on five dice for a) V_{DD}=0.15V, b) V_{DD}=0.3V and c) V_{DD}=0.6V. Horizontal bars define min-max across five dice.

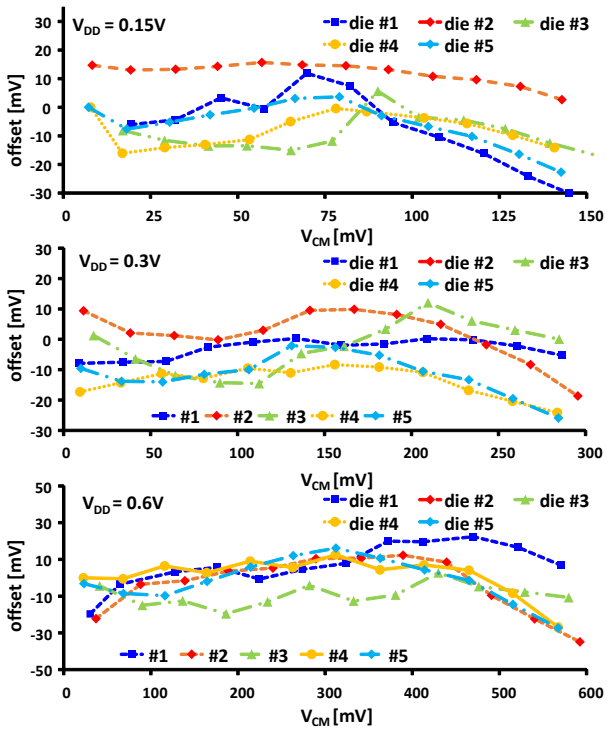

Fig. 8. Input offset voltage vs. v_{CM} for five dice of the proposed RRDVC at a) V_{DD}=0.15V, b) V_{DD}=0.3V and c) V_{DD}=0.6V.

(2.22nW) for a supply voltage equal to 0.15V, 0.3V, and 0.6V, at 10Hz (10kHz) clock frequency. From the above considerations, such maximum power takes place when the input common-mode range is around $V_{DD}/2$. The presence of such power peak and the underlying current contention are vastly mitigated at lower voltages. At 0.15V and 0.3V, the power consumption is indeed almost constant across the entire common-mode range from Figs. 7a-b, and is dominated by leakage. Instead, in Fig. 7c the dynamic and cross-conduction power dominates and explains the peak power when v_{CM}~$V_{DD}/2$. The power spread across the five dice is within 2X at v_{CM} at 0.3V and 0.6V supply, whereas it is about 5X at 150mV.

Finally, the input offset voltage is plotted versus the common-mode input voltage in Fig. 8. From this figure, the offset for die #1 is approximately constant across the entire common-mode range both at 0.3V and at 0.6V supply and is respectively -3mV and 7mV on average (between -8mV and 23mV in the worst case). Instead, it expectedly has a more significant dependence on the common-mode input at the very low supply voltage of 0.15V. In this case, the offset is always lower than 31mV in magnitude, and its mean value is -6.8mV. For the other dice, the offset is more consistent across the common-mode inputs at 0.15V, whereas it shows larger fluctuations at 0.3V and 0.6V supply. Measurements with temperature variations in the range from -25°C to 75°C shows that the worst-case offset increases by 22mV at V_{DD}=0.15V and less than 15mV for higher supply voltages. In the same temperature range, the power consumption ranges from sub-pW to sub-nW at V_{DD}= 0.15 V, and from sub-nW to nW for V_{DD}=0.6 V.

B. Performance Comparison

Table I compares the performance of the proposed RRDVC with prior fully-synthesizable and conventional analog dynamic voltage comparators. Within the first category, the former NAND-based solution [7] and the modified version in [10] are reported. Among the latter category, two recently proposed ultra-low analog solutions are considered [11], [12]. From Table I, the common-mode range of the proposed RRDVC is 1.25-1.5X wider than the previously proposed fully-synthesizable DVCs for the same supply voltage at 0.6V [7], [10], and uniquely covers the entire rail-to-rail swing. In particular, the achieved common-mode range is the widest among the fully-synthesizable solutions and is equivalent to or better than analog solutions [11], [12].

Compared to [7], [10]-[12], the proposed RRDVC operates at the lowest supply voltage $V_{DD,min}$=0.15V. Also, it exhibits the widest power supply voltage dynamic range $V_{DD,max}/V_{DD,min}$ equal to 4X, as compared to 2.86X in [10]. The consumption in

TABLE I. PERFORMANCE COMPARISON WITH THE STATE OF THE ART (BEST PERFORMANCE IN BOLD)

	This work			[10]*			[7]	[11]	[12]
design approach	fully-synthesizable			fully-synthesizable			fully-synthesizable	analog	analog
technology	180nm			45nm			40nm	130nm	180nm
area [μm^2]	900			59			**35**	N/A	N/A
normalized area $10^3 \cdot F^2$	27.7			29.1			**21.8**	N/A	N/A
V_{DD} [V]	0.6	0.3	**0.15**	1	0.6	0.35	0.6	1.2	1.8
input common-mode range (min-max [V])	**0-0.6**	**0-0.3**	**0-0.15**	0.1- 0.9	0.06-0.54	0.03-0.32	0.4 - 0.6	0.4 -1.2	0 - 1.8
max. delay [ns]	740	34,700	442,000	1	68	2,100	2	2	0.27
input offset voltage [mV]	23	8	31	5.78	5.81	4.73	40	7.8	**2.5**
power [nW]	1.95	0.024	**0.006**	6290	9.23	0.244	500	600,000	230,000
Power Delay Product (fJ)	1.9	1.0	3.5	6.3	0.63	**0.51**	1.0	1,200	62

* simulations only

the proposed RRDVC reaches 6-pW minimum power at 0.15V, which is the lowest reported to date for a rail-to-rail dynamic voltage comparator. Such power is 30.5-62,500X lower than previous synthesizable DVCs [7], [10]-[12]. This is more than seven orders of magnitude lower than analog DVCs [11]-[12], thanks to the suppression of any bias current. Compared to fully-synthesizable DVCs at its maximum 0.6-V power supply voltage, the proposed RRDVC power consumption is still 3.6X lower [10]. This makes the proposed RRDVC suitable for direct powering from millimeters-scale harvesters for low-cost and ultra-compact IoT sensor nodes [1].

The maximum clock-to-output propagation delay of the proposed RRDVC in 180nm is expectedly larger than other solutions at $V_{DD,min}$=0.15V, due to operation in deep sub-threshold. In particular, it is between three to six orders of magnitude higher than the analog DVC in [11] operating at 1.8V and 10.9-370X higher than fully-synthesizable RRDVC [10]-[7], due to their adoption of more advanced technologies at the same 0.6V supply voltage. Regarding the overall tradeoff between power and delay, the proposed RRDVC achieves the second-best power-delay product. In particular, the power-delay product in Table I is 2X worse than the best synthesizable DVC [10] for the same supply voltage of 0.6V and is 32.6-631X better than analog DVCs [11], [12]. This confirms a favorable power-delay tradeoff, regardless of the specific power achieved at a specific voltage.

The input offset voltage is comparable to other fully synthesized DVCs. In particular, it is 1.74X better than [7], 4X worse than [10] at the same 600mV supply, and 2.9X-9.2X worse than analog DVC in [11], [12]. The offset of the proposed RRDVC can be easily reduced by increasing the strength of the input standard cells as per Pelgrom's law, at the cost of increased power and area. In the specific design instance in this work, the input stage standard cells were sized minimum to favor power over offset. Finally, the above superiority in terms of power and voltage scalability is achieved at no area penalty. Indeed, from Table I the area normalized to F^2 (F = minimum feature size of the process) is comparable to the best fully-synthesizable DVCs.

V. Conclusion

A fully-synthesizable rail-to-rail dynamic voltage comparator in 180nm has been reported in this paper. Circuit operation has been experimentally demonstrated from 0.6V down to 0.15 V supply voltage. Its digital nature allows easy technology portability and voltage/power scalability. The measured power ranges from 2.6nW at 0.6V down to 8pW at 0.15 V. Both power and minimum operating voltage are the lowest reported to date for a rail-to-rail dynamic voltage comparator, to the best of the authors' knowledge. This makes the proposed comparator well suited to be employed in IoT nodes direct powered from energy harvesters (i.e., suppressing voltage regulation altogether) for threshold crossing event detection and in sub-kS/s A/D conversion.

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