Low-Complexity Reconfigurable DCT-V Architecture

# Low-Complexity Reconfigurable DCT-V Architecture

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***Abstract*—This brief presents a low-complexity, reconfigurable architecture for the Discrete Cosine Transform (DCT) of type V (DCT-V) of length 32. The proposed architecture can be reconfigured to compute five DCT-V of length 4 with negligible area overhead. As the DCT-V is one of the odd type transforms employed in the Adaptive Multiple Transform (AMT) scheme, the effect of fixed point implementation has been assessed in the Joint Exploration Model (JEM) developed by the JVET group for the Versatile-Video-Coding (VVC) forthcoming standard. Simulation results show that the proposed architecture is not only low-complexity and reconfigurable, but features also imperceptible quality loss. Moreover, when implemented in 90 nm CMOS technology it occupies only 90k eq. gates running at 187 MHz.**

***Index Terms*—Low-complexity, DCT, Video coding**

## I. Introduction

The Discrete Cosine Transform (DCT) [1] is one of the most popular transforms for image and video coding. Despite the DCT has been studied for several years, most of the works available in the literature concentrate on even type DCTs, mainly on the DCT of type II (DCT-II) [2], [3], [4] and its approximations [5], [6], [7], to be employed in several image and video standards, such as High-Efficiency-Video-Coding (HEVC) [8].

In the last years several researchers, e.g. [9], have shown that signals produced by intra and inter prediction schemes in video coding systems are better represented by a blend of trigonometric transforms rather than the DCT-II. In particular, an Adaptive Multiple Transform (AMT) scheme [10], derived from the Enhanced Multiple Transform in [11], has been recently proposed to encode the residual signal for both intra and inter coded blocks in the new Versatile-Video-Coding (VVC) forthcoming standard. Based on the coding mode, the encoder chooses for each block the best set of transforms from a certain pool. This pool contains odd type DCTs and odd type Discrete Sine Transforms (DSTs), namely DCT-V, DCT-VIII, DST-I and DST-VII [11]. Since each set is composed of two transform candidates, each of which is evaluated both for horizontal and vertical transforms, a total of five different transform candidates (DCT-II plus four multiple transform candidates of the AMT) have to be computed for each block. Moreover, the block length can be $N = 4, 8, 16, 32$, thus, as argued in [10], the computational complexity is very high. As a consequence, efficient computation of odd type DCTs is an important issue, which has been partially addressed in the literature. Indeed, while several fast algorithms have been proposed and implemented for the computation of even type DCTs and DSTs [12], only few works address the problem of finding low-complexity factorizations and implementations of odd type transforms (*i.e.* types V, VI, VII and VIII), e.g. [13]. In [14], the $2M+1$-point DCT-II matrix is decomposed into an $M+1$-point DCT-VI and an $M$-point DST-VII, by the means of the Discrete Fourier Transform (DFT) decomposition of Winograd. Recently, we showed in [15] that the DCT-V of length $N = 4, 8$ can be easily obtained from the $N = M + 1$ DCT-VI and implemented as low complexity architectures. However, such decompositions lead to irregular data flows; as a consequence the hardware reuse of the corresponding architectures is very limited.

Stemming from the general theory presented in [16], in this brief, we derive a new factorization of the DCT-V of length $N = 32$, which relies on five instances DCT-V of length $N = 4$. Such a factorization leads not only to an architecture with a reduced number of multiplications but also to a noteworthy hardware reuse. The proposed 1D-DCT architecture, which relies on butterfly and butterfly-like structures can compute either one DCT-V of length $N = 32$ or five DCT-V of length $N = 4$, indeed. The proposed factorization has been tested with a fixed point model in encoder of the Joint Exploration Model (JEM, version HM-16.6-JEM-7.2) developed by the JVET group for the Versatile-Video-Coding (VVC) forthcoming standard, showing negligible quality loss and the corresponding architecture has been implemented on a 90 nm standard cell technology featuring low complexity and power consumption.

## II. Factorization of the DCT-V of length $N = 32$

Let

$$\left[\mathbf{C}_N^{II}\right]_{k,l} = \cos\frac{\pi k(l+\frac{1}{2})}{N} \quad (1)$$

$$\left[\mathbf{C}_N^{III}\right]_{k,l} = \cos\frac{\pi l(k+\frac{1}{2})}{N} \quad (2)$$

$$\left[\mathbf{C}_N^{V}\right]_{k,l} = \cos\frac{2\pi kl}{2N-1} \quad (3)$$

$$\left[\mathbf{S}_N^{VII}\right]_{k,l} = \sin\frac{2\pi(k+\frac{1}{2})(l+1)}{2N+1} \quad (4)$$

with $k, l = [0, N-1]$ be the matrix representation of the DCT-II, DCT-III, DCT-V and DST-VII of length $N$. Moreover, let

$$\mathbf{A} \oplus \mathbf{B} = \begin{bmatrix} \mathbf{A} & \\ & \mathbf{B} \end{bmatrix} \quad \bigoplus_{i=1}^{n} \mathbf{A}_i = \begin{bmatrix} \mathbf{A}_1 & & & \\ & \mathbf{A}_2 & & \\ & & \ddots & \\ & & & \mathbf{A}_n \end{bmatrix} \quad (5)$$

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be the matrix direct sum operator and let $\otimes$ be the Kronecker (or tensor) product between two matrices. Any DCT of a signal $\mathbf{x} = \{x_0, x_1, \ldots, x_{N-1}\}$ of length $N$ can be written as $\mathbf{Y} = \mathbf{C}_N \cdot \mathbf{x}$, where $\mathbf{Y} = \{Y_0, Y_1, \ldots, Y_{N-1}\}$ is the transform result and $\mathbf{C}_N$ is the matrix representation of the DCT (either of even or odd type). From the theory presented in [16] the following factorization can be obtained:

$$\mathbf{C}_{32}^{V} = \mathbf{Q}_{10}^{32} \cdot \left[\mathbf{C}_{11}^{V} \oplus \mathbf{C}_{21}^{III}\left(\frac{2}{3}\right)\right] \cdot \mathbf{B}_{32}^{(C5)}, \tag{6}$$

where $\mathbf{Q}_{10}^{32}$ is a permutation matrix defined as

$$\mathbf{Q}_{m}^{3m+2} : i_1 + 3i_2 \mapsto \begin{cases} i_2, & \text{for } i_1 = 0, \\ 2i_2 + m + 1, & \text{for } i_1 = 1, \\ 2i_2 + m + 2, & \text{for } i_1 = 2 \end{cases} \tag{7}$$

with $i_2 = 0, \ldots, m$ and $i_1 + 3i_2 < 3m + 2$, and $\mathbf{B}_{32}^{(C5)}$ is the pre-addition matrix obtained from

$$\mathbf{B}_{3m+2}^{(C5)} = \left(\begin{array}{ccc|ccc} 1 & & & 1 & & \\ & \mathbf{I}_m & \mathbf{J}_m & & & \mathbf{I}_m \\ & & & -1/2 & & \\ & \mathbf{I}_{2m+1} & & & & -\mathbf{I}_m \\ & & & & & -\mathbf{J}_m \end{array}\right), \tag{8}$$

with $\mathbf{I}_m$ and $\mathbf{J}_m$ the m-order identity and anti-diagonal identity matrices and $m = 10$.

The term $\mathbf{C}_{21}^{III}\left(\frac{2}{3}\right)$ is a *skew* DCT-III of length $N = 21$. According with [16] it can be written as:

$$\mathbf{C}_{21}^{III}\left(\frac{2}{3}\right) = \mathbf{K}_{7}^{21} \cdot \left[\bigoplus_{0 \le i < 3} \mathbf{C}_{7}^{III}(r_i)\right] \cdot \mathbf{U}_{21} \cdot \mathbf{B}_{3,7}^{(C3)}, \tag{9}$$

where $r_0 = 2/9$, $r_1 = 4/9$, $r_2 = 8/9$,

$$\mathbf{U}_{21} = \mathbf{C}_{3}^{III}\left(\frac{2}{3}\right) \otimes \mathbf{I}_7 \tag{10}$$

and $\mathbf{C}_{3}^{III}\left(\frac{2}{3}\right)$ is the *skew* DCT-III of length $N = 3$, $\mathbf{K}_{7}^{21}$ and $\mathbf{B}_{3,7}^{(C3)}$ are a permutation and a pre-addition matrix, respectively defined as

$$\mathbf{K}_{7}^{21} = \left[\bigoplus_{i=1}^{3} (\mathbf{I}_3 \oplus \mathbf{J}_3)_i \oplus \mathbf{I}_3\right] \cdot \mathbf{L}_{7}^{21} \tag{11}$$

with

$$\mathbf{L}_{7}^{21} : i \mapsto \begin{cases} 7 \cdot i \bmod 20, & \text{for } 0 \le i < 20, \\ 20 & \text{otherwise} \end{cases} \tag{12}$$

and

$$\mathbf{B}_{3,7}^{(C3)} = \{\mathbf{I}_7 \oplus [\mathbf{I}_2 \otimes \mathrm{diag}_7(1, 2, \ldots, 2)]\} \cdot \mathbf{W}_{21} \tag{13}$$

where

$$\mathbf{W}_{21} = \begin{bmatrix} \mathbf{I}_7 & -\mathbf{Z}_7 & \mathbf{I}_7' \\ & \mathbf{I}_7 & -\mathbf{Z}_7 \\ & & \mathbf{I}_7 \end{bmatrix} \qquad \mathbf{Z}_7 = \begin{bmatrix} & & 0 \\ & & 0 \;\; 1 \\ & \iddots & \iddots \\ 0 & 1 & \end{bmatrix} \tag{14}$$

and $\mathbf{I}_7' = \mathrm{diag}_7(0, 1, \ldots, 1)$ with $\mathrm{diag}_n(a, b, \ldots, b)$ the diagonal matrix of size $n$, which elements are the ones listed inside the parenthesis. The factorization shown in (6) can be exploited to write:

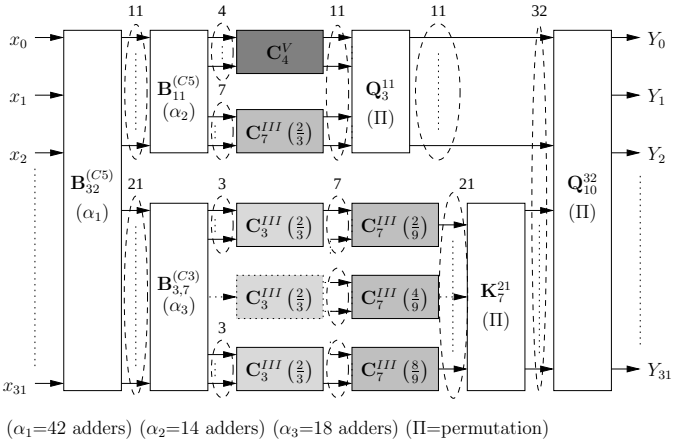



Figure 1. Architecture of the DCT-V $N = 32$.

$$\mathbf{C}_{11}^{V} = \mathbf{Q}_{3}^{11} \cdot \left[\mathbf{C}_{4}^{V} \oplus \mathbf{C}_{7}^{III}\left(\frac{2}{3}\right)\right] \cdot \mathbf{B}_{11}^{(C5)}, \tag{15}$$

where $\mathbf{Q}_{3}^{11}$ and $\mathbf{B}_{11}^{(C5)}$ are obtained as in (7) and (8) with $m = 3$. The *skew* DCTs which length is a prime number can be conveniently rewritten as $\mathbf{C}_{m}^{III}(r) = \mathbf{C}_{m}^{III} \cdot \mathbf{P}_{m}^{C3}(r)$, with

$$\mathbf{P}_{m}^{(C3)}(r) = \begin{bmatrix} 1 & 0 & \cdots & 0 \\ 0 & c_{1,r,m} & & s_{m-1,r,m} \\ \vdots & & \ddots \;\; \iddots & \\ \vdots & & \iddots \;\; \ddots & \\ 0 & s_{1,r,m} & & c_{m-1,r,m} \end{bmatrix}, \tag{16}$$

where $c_{l,r,m} = \cos\frac{(1/2-r)l\pi}{m}$, $s_{l,r,m} = \sin\frac{(1/2-r)l\pi}{m}$. As a consequence, $\mathbf{C}_{32}^{V}$ is now a function of $\mathbf{C}_{4}^{V}$, $\mathbf{C}_{7}^{III}$ and $\mathbf{C}_{3}^{III}$. Since $\mathbf{C}_{N}^{III} = \left(\mathbf{C}_{N}^{II}\right)^T$, with $(\cdot)^T$ being the transposition operator, the factorization proposed in [14] can be exploited to obtain:

$$\mathbf{C}_{7}^{III} = \mathbf{H}_7 \cdot \begin{bmatrix} \mathbf{J}_4 \cdot \mathbf{C}_{4}^{V} \cdot \mathbf{D}_4 & \\ & (\mathbf{S}_{3}^{VII})^T \end{bmatrix} \cdot \mathbf{G}_{7}^{T} \cdot \mathbf{D}_{7}', \tag{17}$$

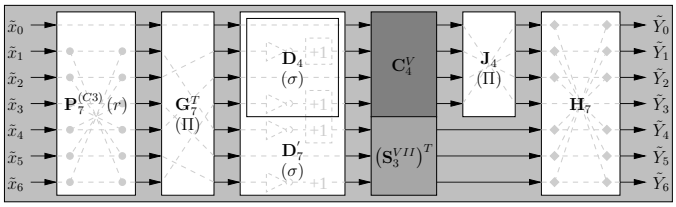
where

$$\mathbf{H}_7 = \begin{bmatrix} \mathbf{I}_3 & -\mathbf{J}_3 & \\ & 1 & \\ \mathbf{J}_3 & & \mathbf{I}_3 \end{bmatrix} \tag{18}$$

$\mathbf{D_4} = \mathrm{diag}_4(1, -1, 1 - 1)$, $\mathbf{S}_{3}^{VII}$ is the DST-VII of length $N = 3$,

$$\mathbf{G}_7 : i \mapsto \begin{cases} 2i, & i = 0, 1, 2, 3 \\ 2(i \bmod 4) + 1 & i = 4, 5, 6 \end{cases} \tag{19}$$

and $\mathbf{D}_{7}' = \mathrm{diag}_7(1, -1, 1, 1, 1, -1, 1)$. Thus, $\mathbf{C}_{32}^{V}$ is factorized in terms of five DCT-V with length $N = 4$, four DST-VII of length $N = 3$ and seven DCT-III of length $N = 3$, which can be implemented as in [15] and [17].




($\sigma$=sign alternation) (Π=permutation)

Figure 2. Architecture of the *skew* DCT-III $N = 7$.

## III. Proposed Architecture

Stemming from the factorization detailed in Section II, the architecture depicted in Fig. 1 has been obtained where several butterfly and butterfly-like structures are exploited. Let, for the sake of simplicity, $\hat{\mathbf{x}} = \{\hat{x}_0, \hat{x}_1, \ldots, \hat{x}_{N-1}\}$ and $\hat{\mathbf{Y}} = \{\hat{Y}_0, \hat{Y}_1, \ldots, \hat{Y}_{N-1}\}$ be the input and the output of each building block. As it can be inferred from (8), $\mathbf{B}_{32}^{(C5)}$ can be implemented by resorting to adders, which properly combine the inputs, e.g. the first and the second results are $\hat{Y}_0 = \hat{x}_0 + \hat{x}_{21}$ and $\hat{Y}_1 = \hat{x}_1 + \hat{x}_{20} + \hat{x}_{22}$. As a consequence, the total number of adders to implement $\mathbf{B}_{32}^{(C5)}$ is 42. Similarly, from (8) and (13) one can derive that $\mathbf{B}_{11}^{(C5)}$ and $\mathbf{B}_{3,7}^{(C3)}$ require 14 and 18 adders, respectively. Since permutations are fixed, they have been implemented by correctly wiring inputs to outputs, e.g. from (7) one can derive that the first and the second results of $\mathbf{Q}_3^{11}$ are $\hat{Y}_0 = \hat{x}_0$ and $\hat{Y}_1 = \hat{x}_3$. Similarly, from (11) and (7) it is possible to derive the connections required to build $\mathbf{K}_7^{21}$ and $\mathbf{Q}_{10}^{32}$.

The gray shaded blocks in Fig. 1, corresponding to DCT-V of length $N = 4$ and *skew* DCT-III of length $N = 7$ and $N = 3$, are depicted in Figs. 2, 3 and 4, respectively. In particular, Fig. 2 shows that the DCT-III of length $N = 7$, which inputs and outputs are $\tilde{\mathbf{x}} = \{\tilde{x}_0, \tilde{x}_1, \ldots, \tilde{x}_{N-1}\}$ and $\tilde{\mathbf{Y}} = \{\tilde{Y}_0, \tilde{Y}_1, \ldots, \tilde{Y}_{N-1}\}$, can be obtained as the cascade of some building blocks. The simplest ones are shown as white boxes where the inside gray shaded lines detail the implementation. On the other hand, blocks corresponding to trigonometric transforms are shown as gray shaded boxes and detailed in Figs. 3 and 5, respectively. As shown in Fig. 2, the $\mathbf{P}_7^{(C3)}(r)$ matrix, which is described by (16), requires 3 butterfly structures (gray shaded lines and dots) to compute $\hat{Y}_0 = \hat{x}_0$, $\hat{Y}_1 = c_{1,r,7} \cdot \hat{x}_1 + s_{6,r,7} \cdot \hat{x}_6$, $\ldots$, $\hat{Y}_6 = s_{1,r,7} \cdot \hat{x}_1 + c_{6,r,7} \cdot \hat{x}_6$. As a consequence, the implementation of $\mathbf{P}_7^{(C3)}(r)$ relies on 12 multipliers and 6 adders. Permutation blocks, namely $\mathbf{G}_7^T$ and $\mathbf{J}_4$ are hardwired. Sign alternation for $\mathbf{D}_4$ and $\mathbf{D}_7'$ require 4 adders to perform 2's complement operations, namely $\hat{Y}_1 = -\hat{x}_1$, $\hat{Y}_3 = -\hat{x}_3$, $\hat{Y}_4 = -\hat{x}_4$ and $\hat{Y}_6 = -\hat{x}_6$. $\mathbf{H}_7$ relies on 3 multiplierless butterfly structures (gray shaded lines and diamonds), implementing $\hat{Y}_0 = \hat{x}_0 - \hat{x}_6$, $\ldots$, $\hat{Y}_6 = \hat{x}_0 + \hat{x}_6$; thus, it requires 6 adders.

Finally, according with [15] and [17], the trigonometric transforms represented by $\mathbf{C}_4^V$, $\mathbf{C}_3^{III}(r)$ and $(\mathbf{S}_3^{VII})^T$ have been implemented as shown in Figs. 3, 4 and 5 by resorting to 4 multipliers and 13 adders, 6 multipliers and 6 adders, 4 multipliers and 10 adders, respectively. The value of the constants required by $\mathbf{C}_4^V$, $\mathbf{C}_3^{III}(r)$ and $(\mathbf{S}_3^{VII})^T$ are shown in Table I.

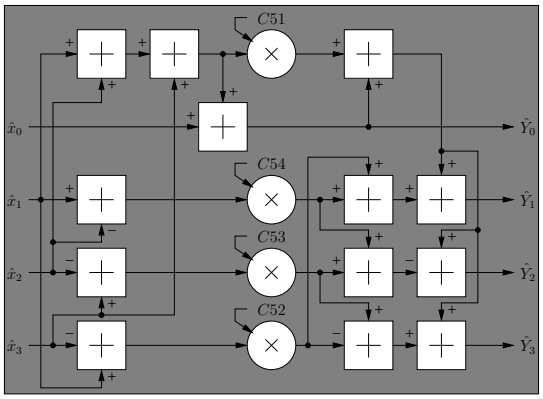



Figure 3. Architecture of the DCT-V $N = 4$, as in [15].

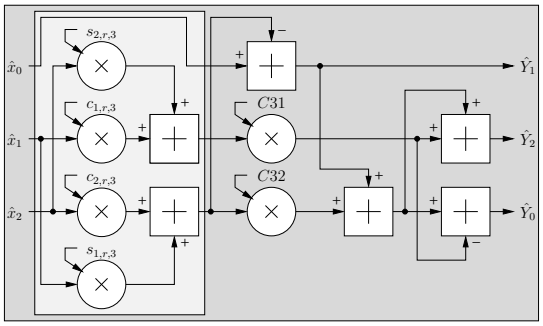



Figure 4. Architecture of the *skew* DCT-III $N = 3$.

Table I
Coefficients of the DCT-III with $N = 3$, DCT-V with $N = 4$ and DST-VII with $N = 4$.

| block | coefficient | value |
|---|---|---|
| $\mathbf{C}_3^{III}$ | $C31$ | $-\frac{\sqrt{3}}{2}$ |
| | $C32$ | 1.5 |
| $\mathbf{C}_4^V$ | $C51$ | $\frac{7}{6}$ |
| | $C52$ | $\frac{2\cos(u)-\cos(2u)-\cos(3u)}{3}$ |
| | $C53$ | $\frac{\cos(u)-2\cos(2u)+\cos(3u)}{3}$ |
| | $C54$ | $\frac{\cos(u)+\cos(2u)-2\cos(3u)}{3}$ |
| $(\mathbf{S}_3^{VII})^T$ | $S31$ | $\frac{\sin(u)+\sin(2u)-\sin(3u)}{3}$ |
| | $S32$ | $\frac{2\sin(u)-\sin(2u)+\sin(3u)}{3}$ |
| | $S33$ | $\frac{\sin(u)-2\sin(2u)-\sin(3u)}{3}$ |
| | $S34$ | $\frac{\sin(u)+\sin(2u)+2\sin(3u)}{3}$ |

The total number of multipliers and adders required to implement the proposed architecture is summarized in Table II and is equal to 126 and 285 respectively, which is significantly less than the number of multiplications and additions required by the $\mathbf{C}_{32}^V$ matrix product (i.e. 1024 multiplications and 992 additions).

## IV. Implementation Results

In order to properly size the proposed architecture, the corresponding factorization has been implemented in fixed point into the JEM, version HM-16.6-JEM-7.2 [18].. Input data are represented with 16 bits, the internal bit-width increases up to 32 bits to have enough precision where $\mathbf{C}_3^{III}(r)$ is cascaded with $\mathbf{C}_7^{III}(r)$ and the output data are scaled to be represented with 16 bits as well. Experiments showed that 8 fractional bits

Table II
NUMBER OF MULTIPLIERS AND ADDERS REQUIRED TO IMPLEMENT THE PROPOSED ARCHITECTURE FOR THE DCT-V OF LENGTH $N = 32$

| | $\mathbf{P}_7^{(C3)}(r)$ | $\mathbf{D}_7'$ | $\mathbf{D}_4$ | $\mathbf{C}_4^V$ | $(\mathbf{S}_3^{VII})^T$ | $\mathbf{H}_7$ | $\mathbf{C}_7^{III}(r)$ |
|---|---|---|---|---|---|---|---|
| MUL | 12 | 0 | 0 | 4 | 4 | 0 | 20 |
| ADD | 6 | 2 | 2 | 13 | 10 | 6 | 39 |

| | $\mathbf{B}_{32}^{(C5)}$ | $\mathbf{B}_{11}^{(C5)}$ | $\mathbf{B}_{3,7}^{(C3)}$ | $\mathbf{C}_4^V$ | $7 \times \mathbf{C}_3^{III}(r)$ | $4 \times \mathbf{C}_7^{III}(r)$ | $\mathbf{C}_{32}^V$ |
|---|---|---|---|---|---|---|---|
| MUL | 0 | 0 | 0 | 4 | 7×6 | 4×20 | 126 |
| ADD | 42 | 14 | 18 | 13 | 7×6 | 4×39 | 285 |

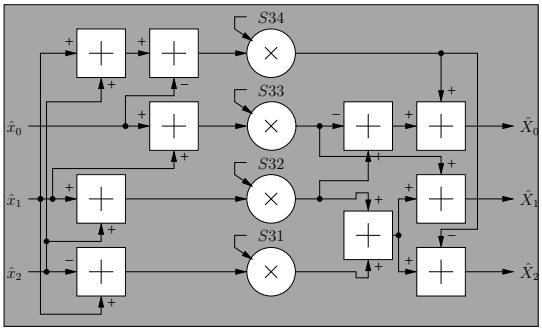



Figure 5. Architecture of the transpose DST-VII $N = 3$.

Table III
BJØNTEGAARD DELTA RATE LOSS.

| | mean [%] | std-var [%] | min [%] | max [%] |
|---|---|---|---|---|
| AI | 0.0398 | 0.0356 | 0.0139 | 0.1103 |
| RA | 0.0438 | 0.0404 | -0.0259 | 0.0874 |

can be used to correctly represent each constant coefficient for the multiplications. Indeed, as show in Table III the proposed solution achieves an average Bjøntegaard Delta rate loss [19] of about 0.04% in both all-intra (AI) and random-access (RA) configuration with the standard video sequences suggested in the common test conditions [20]. We also observed that the selection of the modified DCT-V with respect to the original one is always above 95% and 80% for $N = 4$ and $N = 32$ respectively.

Moreover, the proposed architecture for the computation of the DCT-V of length $N = 32$, contains five DCT-V of length $N = 4$. As a consequence, by adding few multiplexers the proposed architecture can be configured to compute one DCT-V of length $N = 32$ or five DCT-V of length $N = 4$, as shown in Fig. 6. This reconfigurable architecture has been implemented in VHDL with the TSMC 90 nm standard cell technology (typical) at 1.1V and $0^o$, by the means of Synopsys Design Compiler Graphical, reaching a maximum clock frequency of 222 MHz with an area of 0.32 mm$^2$ (about 113k eq. gate, NAND2X1) and a power consumption of 17.5 mW.

The proposed architecture cannot be directly compared with other DCT-V architectures, as, to the best of our knowledge, this is the first work addressing the implementation of an architecture for the DCT-V with $N = 32$. However, it can be compared with some flexible architectures able to compute the DCT-II of length $N = 32$ to quantify the complexity of the proposed solution. For this reason we also synthesized the proposed architecture for a target clock frequency of 187 MHz, as in [2], reaching an area occupation of 0.25 mm$^2$ (about 90k eq. gate, NAND2X1). Table IV compares the proposed low complexity and reconfigurable DCT-V architecture with some recent DCT-II architectures in terms of size support $N$, number of eq. gates, maximum/target clock frequency $f_{ck}$, power consumption and throughput (number of produced samples per cycle). It is worth noting that the different speed achieved by different architectures depends also on some architectural choices, such as the number of pipeline registers. As an example the solution referred to as [21] (1) is a pipeline architecture, whereas the proposed one contains registers only at the input and at the output. Moreover, the number of required multipliers can be different as well. As an example the architecture referred to as [21] (2) requires only 80 multipliers. As it can be observed, the proposed

Table IV
1D DCT ARCHITECTURES COMPARISON.

| Arch. | $N$ | eq. gates | $f_{ck}$ [MHz] | P [mW] | T [samples/cycle] |
|---|---|---|---|---|---|
| [2] | 4,8,16,32 | 131k(@90nm) | 187 | 23.17 | 32 |
| [3] | 4,8,16,32 | 88k(@90nm) | 256 | 16.20 | 32 |
| [22] | 4,8,16,32 | 97k(@45nm) | 50 | 24.20 | 32 |
| [23] | 4,8,16,32 | 163k(@90nm) | 250 | 15.30 | 32 |
| [21] (1) | 4,8,16,32 | 113k(@90nm) | 401 | 15.98 | 32 |
| [21] (2) | 4,8,16,32 | 88k(@90nm) | 187 | 32.09 | 32 |
| **Prop. (1)** | 4,32 | 113k(@90nm) | 222 | 17.50 | 20,32 |
| **Prop. (2)** | 4,32 | 90k(@90nm) | 187 | 13.10 | 20,32 |
| **Prop. (*)** | 4,8,16,32 | ≈158k(@90nm) | 187 | ≈23 | 20, 8, 16, 32 |

architecture supports only $N = 4$ and $N = 32$, whereas the other ones support all the DCT-II sizes specified in both the HEVC standard and in the VVC forthcoming standard, namely $N = 4, 8, 16, 32$. Indeed, the DCT-II of size $N$ can be factorized in terms of at least one DCT-II of size $N/2$ [12]. As a consequence, DCT-II architectures for $N = 32$ allow for a great hardware reuse to support $N = 4, 8, 16$. In order to take into account this aspect, we assume that the area and the power consumption required to implement an architecture for the DCT-V of size $N/2$ is roughly half the area and the power consumption required for size $N$. As a consequence, we can estimate that the total area and the total power consumption are roughly 1.75 times the area and the power consumption of the proposed architecture and that the critical path is located in the architecture that supports $N = 4, 32$. These estimation are summarized in the last line of table IV). Despite this comparison is not fair, as the proposed architecture and the compared ones implement different types of DCTs, they have similar complexities, clock frequencies, power consumption and throughput, thus showing the effectiveness of the proposed solution. Finally, the proposed 1D-DCT-V architecture can be used to implement either a folded or a fully parallel 2D-DCT-

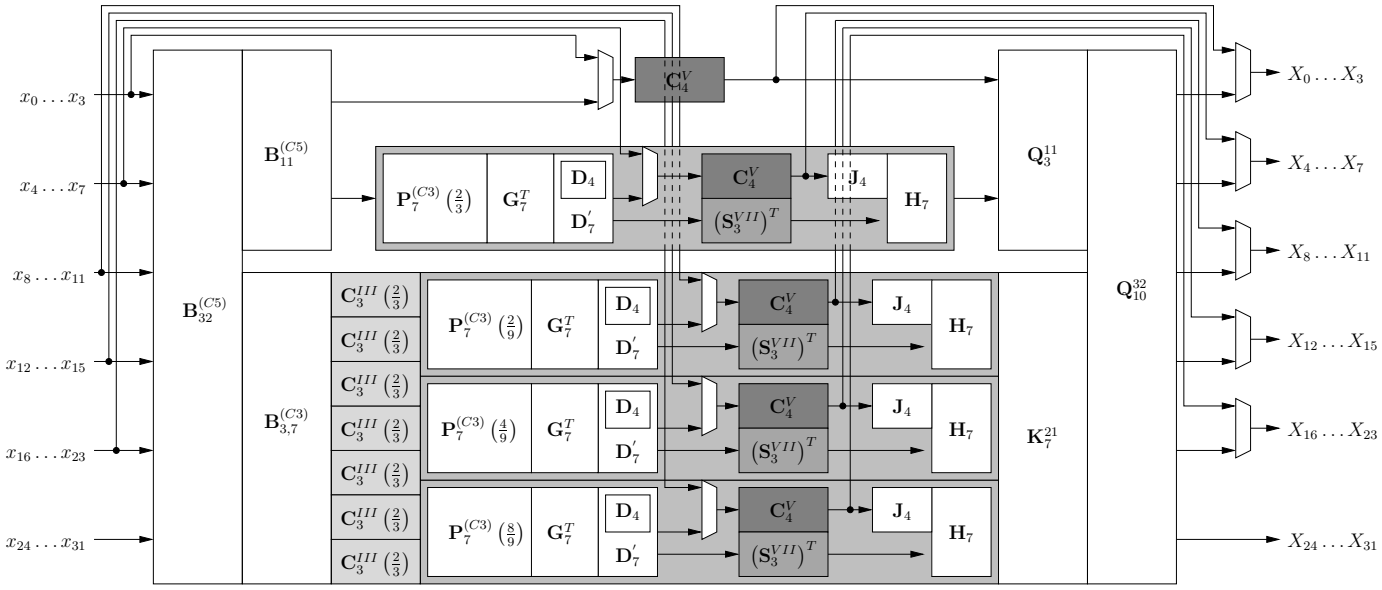



Figure 6. Architecture of the proposed reconfigurable DCT-V with $N = 4, 32$.

V architecture by resorting on the schemes which have already been proposed for the 2D-DCT-II in [2].

## V. Conclusions

In this brief, we presented a low-complexity architecture to compute the DCT-V of length $N = 32$, which involves only 126 multiplications. We have also shown that the proposed solution features near-optimal rate-distortion performance in all-intra and random-access configurations with an average Bjøntegaard Delta rate loss of about 0.04%, thus being well suited to implement the AMT scheme, which is part of the VVC forthcoming standard. We have used the proposed architecture to derive a flexible architecture, which can be reconfigured to compute five DCT-V of length $N = 4$. Implementation results show that the proposed architecture features complexity, speed and power consumption similar to the best architectures for the DCT-II available in the literature.

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