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Chaos-based High-EMC Spread-Spectrum Clock Generator

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Abstract — **This paper proposes a spread-spectrum clock generator which is meant to respect EMC norm compliance from standard regulations. This is obtained through a frequency modulation driven by a chaotic signal, i.e. through the injection of a chaos-based jitter, so to avoid strict periodicity in the clock and thus high peaks in its power spectral density. The circuit has been designed in $0.35\mu m$ technology; measurements from prototypes show EMC improvement of approximately 18dB with respect to the reference case.**

1 INTRODUCTION

The design of electromagnetic compatible (EMC) timing signals in integrated digital or mixed-signal circuits is of great practical concern. It is worth noticing that common solutions to increase system EMC, based on *a-posteriori* methodologies, such the adoption of filters, shielded cables and filtered connectors cannot be employed; hence, *design-time* solutions should be adopted [1], assuring that the implemented electronic equipment *generates* electromagnetic interference with power spectral density as flat as possible, so that its integral within any frequency range (and therefore in the bandwidth of any unintentional receiver) is as low as possible.

This point of view is perfectly coherent with FCC and CE regulations [2] that link compliance with the ability of fitting the interfering power spectrum within a prescribed *mask*. Regrettably, clock signals are most likely to fail such a compliance, due to their sharp edges and their periodic nature, which concentrate power at multiples of their frequency.

The key idea for reducing peak power density in clock signals is a frequency modulation, producing a clock signal with edges which are slightly *delayed* or *anticipated* to avoid perfect periodicity. Of course, it is assumed that the maximum frequency deviation is compatible with the devices depending on the clock for proper operation. It can be intuitively accepted that the efficiency of these methods critically depends on the statistical properties of the modulating signal. Signals produced by *chaotic systems* seem particularly appealing from this point of view, since they are typically aperiodic and broad-band.

Chaos-based frequency modulation [3, 4] has been shown to significantly reduce the EMI due to clock signals with respect to results achieved in classical literature [5, 6]. In those papers, emphasis is on continuous-valued chaotic modulation with large modulation indexes (*slow-modulation*) for which an analytical estimation of the spectrum profile can be provided.

More recently it has been introduced in [7] a *binary fast* chaotic modulation (section 2), which is meant to solve known problems connected with slow modulation, showing even *better* flattening properties as long as it is operated at proper modulation indexes, derived by means of numerical optimization.

In this paper we propose a Spread-Spectrum Clock Generator (SSCG) designed to implement a fast binary modulation. The SSCG structure is based on a PLL with few modifications to achieve a frequency modulator (section 3.2), which is designed to work with a mean frequency $f_0 = 100$ MHz. A random bit generator (section 3.1), whose purpose is to generate the driving signal is also implemented; it is designed to work up to 10 MHz and it can be shown that its realization can conveniently be derived by already existing circuit blocks.

The circuit has been manufactured with a 3.3V 0.35μm CMOS double-poly triple-metal process. Our implementation, as well as the achieved results and measurements (section 4), will be described in the following.

2 GENERATION OF SPREAD - SPECTRUM CLOCK SIGNALS

Let us consider clock signal $s(t)$ as the result of a frequency modulation:

$$s(t) = \operatorname{sgn}\left\{\cos\left[2\pi\left(f_0 t + \Delta f \int_{-\infty}^{t} \xi(\tau)d\tau\right)\right]\right\}$$

where f_0 indicates the carrier frequency, Δf the frequency deviation and $\xi(t)$ the driving PAM signal:

$$\xi(t) = \sum_{k=-\infty}^{+\infty} x_k g(t - kT) \qquad (1)$$

given that $g(t)$ is a unit pulse of duration T and that x_k are *random* values (being $\rho(x)$ their probability density function) constituting the modulating sequence, belonging to the interval $[-1, 1]$.

In [4] it has been proven that the contribution of each harmonic in the power spectrum can be analytically described by its corresponding low pass equivalent:

$$\Phi_{\tilde{S}\tilde{S}}(f) = E_x[\mathcal{K}_1(x,f)] + \mathrm{Re}\left\{\frac{E_x^2[\mathcal{K}_2(x,f)]}{1 - E_x[\mathcal{K}_3(x,f)]}\right\}$$

where:

$$\mathcal{K}_1(x,f) = \frac{1}{2}T\ \mathrm{sinc}^2(\pi T(f - \Delta f x))$$

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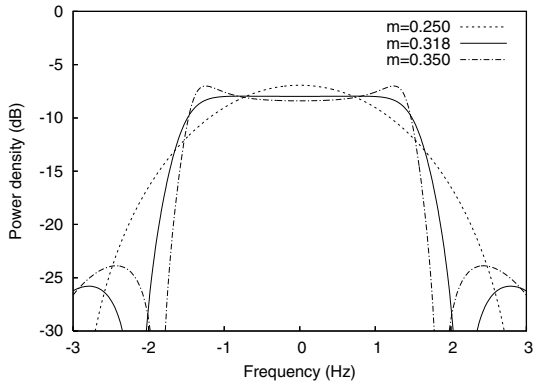

Figure 1: Binary Modulation: normalized ($\Delta f = 1$) low-pass equivalent for PSD for m around $m_{\rm opt}$

$$\mathcal{K}_2(x,f) = j\frac{e^{-j2\pi T(f-\Delta f x)}-1}{2\pi\sqrt{T}(f-\Delta f x)}$$
$$\mathcal{K}_3(x,f) = e^{-j2\pi T(f-\Delta f x)}.$$

where T is the pulse width in (1) and Δf is the frequency deviation for the considered harmonic, which is proportional to the harmonic number (and equal to the modulation Δf only for the fundamental tone). In the particular case of binary modulation, it is:

$$\rho(x) = \frac{1}{2}\delta(x+1) + \frac{1}{2}\delta(x-1) \quad (2)$$

while statistical indipendence of $\{x_k\}$ implies:

$$E_x[f(x)] = \int f(x)\rho(x)dx \quad (3)$$

Given the exact expression for $\Phi_{\tilde{s}\tilde{s}}(f)$ and substituting (2) and (3), by means of numerical optimization it has been found that peaks in the PSD are minimized for the value of the *modulation index* $m = \Delta f\ T = m_{\rm opt} \cong 0.318$. Lower values of m cause the PSD to increase around 0, while higher values increase it around $f = \pm\Delta f$ (Figure 1).

Each harmonic is described by a different modulation index (m is proportional to the harmonic number too), so this optimization can be achieved only on one single harmonic. Since the power content of the fundamental tone is much higher than all other harmonics, and so are the corresponding peaks, best results in overall peak reduction are achieved when the modulation index is optimized for the fundamental tone, i.e. $m = m_{\rm opt}$. Such a reduction is the best reduction with respect to all other known modulations [7].

Since it can be shown that a proper *quantization* of the symbols generated by a chaotic map gives a sequence of binary independent symbols [8, 9], it is worth noticing that such calculations and optimization are valid either when the modulating sequence $\{x_k\}$ is truly *random*, i.e. made of independent samples, or when it is *chaotic*, i.e. generated through a *chaotic map*.

3 CIRCUIT DESCRIPTION

The architecture of the proposed SSCG is based on a PLL driven by a binary random signal generated with a chaotic map. To perform a *frequency modulation* a standard PLL has been modified with the introduction of an analog adder at the VCO input (figure 2), as suggested in [10]. Actually, this scheme does not work exactly as a frequency modulator, due to the negative feedback of the PLL. However, if the driving signal is high-frequency it cannot pass through the feedback path due to its low-pass nature, and the LPF output voltage can be considered constant. In this case the PLL negative feedback sets the carrier frequency f_0 while the driving signal acts effectively as a modulating signal.

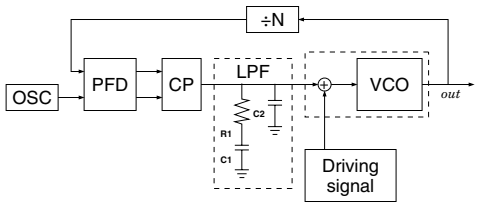

Figure 2: Block diagram of the PLL modified to achieve a frequency modulator.

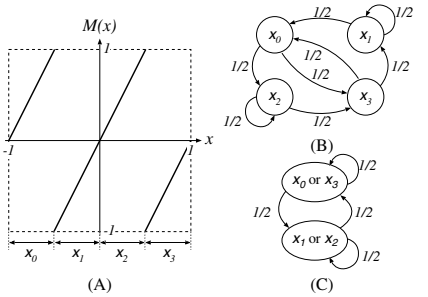

Figure 3: PWAM map found in ADC pipeline converters (A); Embedded Markov chain (B); and simplified chain (C).

3.1 Random bit generator

The driving signal comes from a random bit generator that relays on a simple chaotic map as entropy source. Chaotic maps [9] are 1D discrete-time au-

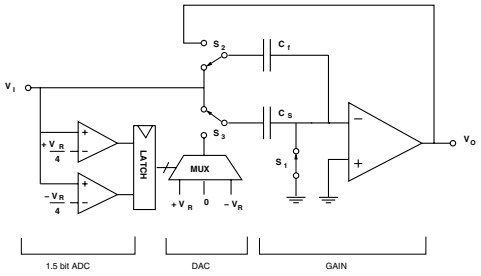

Figure 4: Switched capacitor 1.5bit A/D converter used as $M(x)$ block.

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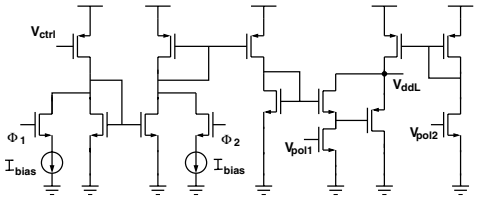

Figure 5: Modified input stage of the VCO

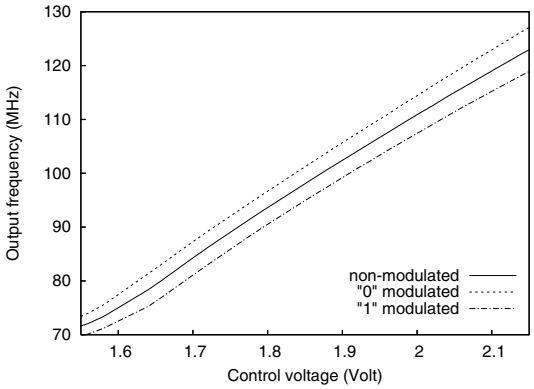

Figure 6: Voltage/Frequency characteristic of the VCO in non spread spectrum mode (solid line) and spread spectrum mode (dashed lines).

tonomous systems, whose evolution is described by:

$$x_{k+1} = M(x_k), \quad M : I \mapsto I \tag{4}$$

where M is a non-linear function that maps an interval I (usually $I = [-1, 1]$) into itself. These systems exhibit a strong dependence on the initial condition: two trajectories given by the same system with two very close initial conditions appear, after few steps, as completely uncorrelated. This property is fundamental since it guarantees unpredictability in true-implemented systems, where the system state x_k is known only with finite precision.

The map M used as chaotic source is depicted in figure 3-(A). This is a variant of the well-known *Bernoulli shift* and has very good robustness properties [11] against both noise perturbations and implementation errors, which make this map very suitable as true-implemented chaotic source. Also this map is a Piece-Wise Affine Markov (PWAM) map [9], i.e. it can be studied through its associated Markov chain. If we set the partition $\{X_0, X_1, X_2, X_3\} = \{[-1, -1/2[, [-1/2, 0[, [0, 1/2[, [1/2, 1]\}$ and consider only the interval where, at every time step, the map state x_k is, the dynamics of the system evolution is described by the Markov chain in figure 3-B. Furthermore, with a simple state aggregation (figure 3-C) we can get an easier Markov chain, which is suitable for the direct generation of independent and identically distributed (*iid*) – loosely speaking random – symbols.

The schematic of the block implementing the $M(x)$ function is the switched capacitor circuit shown in figure 4 which comes from 1.5bit/stage pipeline Analog-to-Digital converters [12]; while a single-ended configuration is shown for simplicity, the actual implementation is fully differential. The circuit operates on a two-phase clock. In the first phase, the input signal V_{in} is applied either to the 1.5 bit ADC and to the sampling capacitors C_s and C_f. In the second phase, C_f closes the negative feedback loop around the op-amp while C_s is switched to the output of the DAC (a simple three-input multiplexer), thus subtracting the output of the multiplexer from the output signal V_{out}. Setting $C_s = C_f$ the resulting input/output characteristic is the desired one, shown in figure 3-(A), as in [13]. Also from the 1.5 bit ADC can easily be obtained an output bit that follows the Markov chain in figure 3-C.

3.2 Frequency modulator

The digital output from the chaotic map is used as driving signal in the PLL as described above. However, due to the discrete nature of this signal, a full analog adder is not necessary, thus simplifying the circuit. The additive function is performed by the input stage of the VCO (figure 5), through the two pass-transistors driven by Φ_1 and Φ_2, along with the two current sources I_{bias}. This circuit is designed to work with $\Phi_1 = \overline{\Phi_2} = \Phi$, where Φ is the signal coming from the random bit generator; however its behavior is more evident considering these two signals separately. Supposing $\Phi_1 = \Phi_2 = 0$, the circuit acts as a linear voltage amplifier, where V_{ddL} is proportional to V_{ctrl}; the obtained VCO $f_{\text{out}}/V_{\text{ctrl}}$ characteristic is represented by the solid line in figure 6. When $\Phi_1 = 1$, the current I_{bias} is subtracted from the current mirror, thus shifting up the $f_{\text{out}}/V_{\text{ctrl}}$ characteristic. On the contrary, $\Phi_2 = 1$ adds I_{bias} to the current mirror and shifts down the characteristic. The two shifted characteristics are represented by dashed lines in figure 6. The distance between the curves is approximately constant in the range of interest and represents the frequency deviation Δf. Its value can be set with I_{bias}.

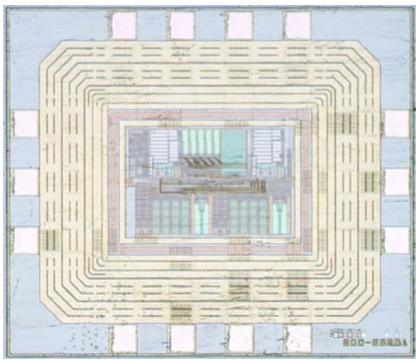

Figure 7: Microphotograph of the circuit.

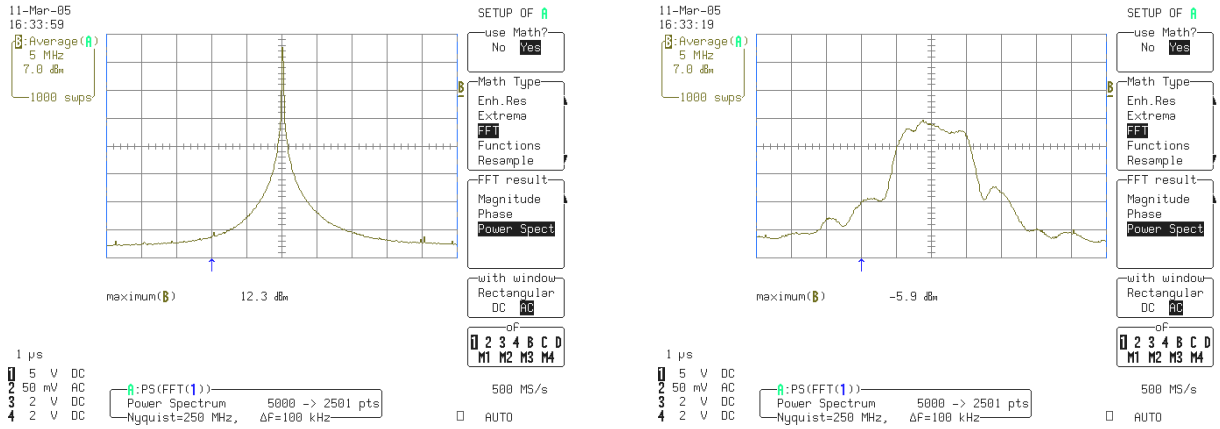

Figure 8: Measurements from prototype in non spread spectrum (A) and spread spectrum (B) mode.

Output frequency	100 MHz
Modulation type	Binary Chaotic
Modulation frequency	10 MHz
Frequency Deviation	3.18 MHz
Chip area	$1.38 \times 1.20\text{mm}^2$
Power consumption	20.5mW
Closed loop Bandwith	15 KHz $C_1 = 58\text{nF}, C_2 = 5.8\text{nF}$ $R_1 = 370\Omega$

Table 1: Performance summary

4 EXPERIMENTAL RESULTS

The proposed circuit has been designed with AMS 0.35μm double-poly triple-metal technology. Its microphotograph is shown in figure 7 while table 1 gives a performance summary of the proposed SSCG. The active area occupies $0.38\times0.65\text{mm}^2$ and the total area including pads is $1.38 \times 1.20\text{mm}^2$. The low-pass filter is left off-chip; its realization is shortly described in table 1. Figure 8 shows the measured spectrum of the 100 MHz output signal without any modulation (a) and modulated with the optimum index value $m = 0.318$ and Δf of about 3% (b). The observed peak reduction is about 18 dB.

5 CONCLUSION

In this brief, measurements from a prototype of a SSCG performing a fast binary modulation are presented. The prototype is fabricated in 0.35μm CMOS process and also includes a fast true-random bit generator implemented with a chaotic map. The measured spectrum shows that both peak amplitudes are attenuated as expected and the proposed architecture does achieve the spread spectrum function as expected.

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