Modulation Strategy Assessment for 3-Level Unidirectional Rectifiers in Electric Vehicle Ultra-Fast Charging Applications

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***Abstract*—This paper proposes a complete analysis and comparison of the most significant pulse-width modulation (PWM) strategies for unidirectional 3-level rectifiers. The basic operation of the converter is described and the stresses on the major passive components (i.e. DC-link capacitors, differential-mode inductors, common-mode chokes) are calculated, highlighting the general performance trade-off of each modulation strategy. This analysis is applied to a rectifier for electric vehicle (EV) ultra-fast charging connected to the European low-voltage grid (i.e. 50 Hz, 400 V line-to-line), adopting a 650 V DC-link. The best candidates concerning different performance metrics are identified and the most suitable strategy for EV battery charging is selected.**

***Index Terms*—pulse-width modulation (PWM), 3-level rectifiers, active front-end (AFE), power factor corrector (PFC), battery chargers, electric vehicles (EV), ultra-fast charging (UFC)**

I. Introduction

State of the art DC fast chargers are normally connected to the three-phase low-voltage grid, in order to leverage the low-voltage industrial power electronics expertise and availability. The structure of an off-board battery charger has no major differences with respect to an on-board EV charger and normally consists of two power converter stages [1], [2], schematically illustrated in Fig. 1. The first stage is a three-phase grid-connected AC/DC converter with unity power factor correction (PFC) capabilities, also referred to as active front-end (AFE). The role of this stage is to absorb the correct amount of power from the grid while ensuring a sinusoidal input current shaping (i.e. with low distortion and harmonics). The second stage is a high-frequency DC/DC converter, which must provide the battery-side current control and may or may not provide galvanic isolation. This work will only focus on the AC/DC conversion stage.

The main requirements for an EV ultra-fast battery charger can be identified in (1) high efficiency, (2) high power density, (3) wide input/output voltage range and (4) low battery-side current ripple, which may damage the battery itself. While requirements (3) and (4) are mainly dealt with by the DC/DC stage, (1) and (2) should also drive the AC/DC stage design.

The most simple and straightforward topology for active rectification is the 2-level inverter, which is naturally bidirectional. Nevertheless, this converter shows a strong performance trade-off between efficiency and power density, since lower converter volumes may be only achieved by increasing the operating switching frequency at the expense of higher switching losses, which decrease the conversion efficiency [3]. One way to push the performance envelop of the AC/DC stage is to adopt multi-level converter topologies, which may trade a higher complexity for better overall performance.

3-level unidirectional rectifiers show an excellent trade-off between efficiency, power-density and overall complexity [3]–[5]. The multi-level nature of these rectifiers allows, depending on the specific topology, to adopt semiconductor devices with half the voltage rating with respect to conventional 2-level inverters, strongly enhancing the switching frequency capability of the converter. Furthermore, the AFE input voltage formation is characterized by lower voltage steps, thus reducing the stress on the input magnetic devices (i.e. boost inductors, common-mode chokes). Overall, the enabled switching frequency increase and the multi-level output voltage waveform allow to decrease the size of the passive devices, thus improving power-density at constant efficiency or vice-versa. It is worth mentioning that the unidirectional nature of these rectifiers ensures minimum converter complexity, as the number of active devices is the same or lower with respect to 2-level inverters. For instance, due to the presence of only one 4-quadrant switch per converter leg, no dead-times have to be provided.

It is well known that the common-mode (zero-sequence) voltage injection represents a degree of freedom in the input voltage formation process, which gives origin to different pulse-width modulation (PWM) strategies [6], [7]. Although the common-mode component does not affect the local average of the output phase voltage, it has an impact on the passive component stresses, such as the differential-mode and common-mode current ripples, the DC-link voltage ripple and, in some cases, the converter switching losses. In particular, 3-level rectifiers may be affected by a low-frequency DC-link mid-point voltage oscillation (i.e. at three times the mains frequency) [6], [8], which strongly depends on the modulation strategy and can represent a notable issue in EV charging applications. For instance, the LLC resonant converter topology is often selected for the DC/DC stage [2], [9] and, in order to split the power and voltage ratings, sep-

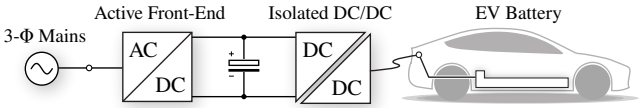


Fig. 1. Ultra-fast EV battery charger schematic overview.

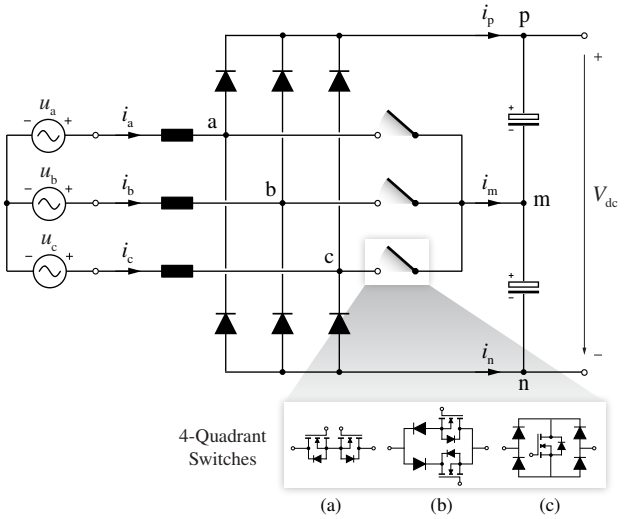


Fig. 2. 3-level rectifier schematic with highlight of the possible 4-quadrant switch implementations: T-type (a), NPC-type (b) and VIENNA-type (c).

arate units are usually connected to the upper and lower side of the AFE DC-link [10], thus being subject to the mid-point voltage ripple. Unfortunately, due to the extremely non-linear nature of resonant converters, low-frequency disturbance rejection may be hard to achieve outside the nominal operating conditions [11], thus allowing the voltage oscillation to get through and reach the battery-side.

According to the authors' best knowledge, only few comparisons between PWM strategies for 3-level rectifiers are found in literature [6], [12]. In particular, no comprehensive performance overview of 3-level rectifier PWM strategies is provided, especially applied to the specific requirements of EV ultra-fast battery chargers.

Therefore, the goal of this work is to provide a complete performance assessment of unidirectional 3-level rectifier modulation strategies, specifically targeted to EV battery charging. Since the rectifier is grid-connected, the modulation strategies can be compared in a narrow modulation index region (i.e. around the nominal grid voltage), thus simplifying the analysis.

This paper is organized as follows. In Section II, the basics of operation of unidirectional 3-level rectifiers are described. Section III introduces the most significant 3-level rectifier modulation strategies and provides their low-frequency common-mode injection expressions. In section IV, the PWM-induced passive component stresses are calculated and compared, highlighting the general performance trade-off of each modulation strategy. The stress comparison allows to select the most suited strategy for EV ultra-fast charging applications. Finally, section V summarizes and concludes this work.

II. Basics of Operation

A schematic overview of the general structure of a 3-level rectifier is illustrated in Fig. 2. The input phases are connected unidirectionally to the upper and lower DC-link rails through bridge diodes, while a 4-quadrant (i.e bipolar and bidirectional) switch connects them to the DC-link mid-point. The 4-quadrant switch may be realized in practice by connecting in anti-series and/or anti-parallel different devices, as highlighted in Fig. 2 (a), (b) and (c). Furthermore, switch implementations (b) and (c) may be integrated (or not) inside the diode bridge, trading higher (lower) conduction losses for lower (higher) switching losses, respectively, as the semiconductor devices must have a different blocking voltage capability in each case [4].

The AC terminal of each converter leg may be actively connected to the DC-link mid point m (switch in the ON state) or, depending on the current direction, passively connected to either the positive p or negative n DC-link rails (switch in the OFF state). Overall, the voltage applied by a single leg v_{xm} can assume three different values, which correspond to three separate states:

- P state: $v_{xm} = +V_{dc}/2$,
- M state: $v_{xm} = 0$,
- N state: $v_{xm} = -V_{dc}/2$.

Therefore, the instantaneous leg voltage can be expressed as

$$v_{xm} = (1 - s_x)\,\mathrm{sgn}(i_x)\,\frac{V_{dc}}{2} \quad x = a,\ b,\ c, \tag{1}$$

where s_x represents the switch signal (1 if ON, 0 if OFF). The zero-sequence (common-mode) voltage is obtained by averaging the three leg voltage contributions, as in

$$v_o = \frac{v_{am} + v_{bm} + v_{cm}}{3} = v_{o,LF} + v_{o,HF}. \tag{2}$$

Finally, the phase voltages are found by removing the common-mode component from the leg voltages, as

$$v_x = v_{xm} - v_o = v_{x,LF} + v_{x,HF} \quad x = a,\ b,\ c. \tag{3}$$

In equations (2) and (3) subscript LF indicates the low-frequency component of the waveform (i.e. mains frequency or multiples), while HF indicates the high-frequency one (i.e. switching frequency harmonics). Overall, the 3-level rectifier can be represented with the equivalent circuit illustrated in Fig. 3, where the AC filter topology considered in this work is also illustrated.

The LF phase voltage component is regulated to control the converter input currents i_a, i_b and i_c to the reference sinusoidal values. In particular, the phase current local average is driven by the difference between the mains voltage and the LF phase voltage applied by the rectifier, as

$$\frac{\mathrm{d}i_{x,LF}}{\mathrm{d}t} = \frac{u_x - v_{x,LF}}{L_{DM}} \quad x = a,\ b,\ c, \tag{4}$$

where L_{DM} is the differential-mode (boost) inductance of the AC filter. It should be noted that, assuming high switching

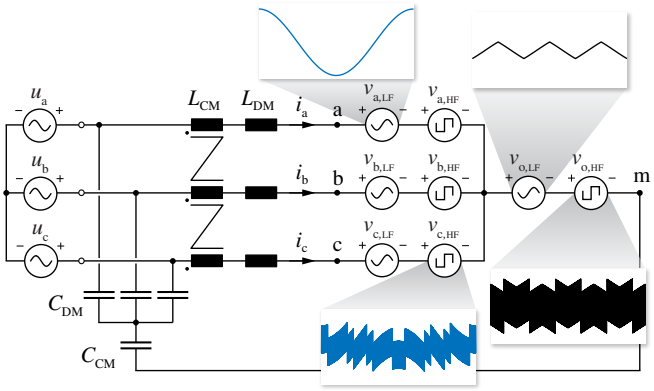


Fig. 3. 3-level rectifier equivalent circuit including the AC-side filter.

frequency and a consequent low L_{DM} value, the rectifier voltage is practically in phase with the mains voltage.

The LF common-mode component is injected for different reasons, first of which is the extension of the operational voltage range of the converter. This injection also affects the HF voltage components and, in some cases, the switching losses, representing the degree of freedom which differentiates the modulation strategies.

Finally, both the differential-mode and the common-mode HF components are responsible for the converter noise emissions and must be filtered according to grid or EMI standards [13]. These HF components define the stress on the differential-mode inductors (L_{DM}) and common-mode choke (L_{CM}) respectively, therefore they should be minimized.

III. Modulation Strategies

Pulse-width modulation (PWM) of three-level rectifiers may be implemented either with carrier-based (CB) or space-vector (SV) approaches. While SVPWM generates the output duty cycles by leveraging geometrical relationships inside the space vector hexagon, CBPWM is based on adding a suitable common-mode voltage component to the normalized phase voltage references. Although SVPWM strategies may be more straightforward to analyze and modify, they are characterized by higher levels of complexity and computational burden [7]. Therefore, a certain effort has been historically spent in converting SVPWM strategies in CBPWM, exploiting the relationship between redundant space vector allocation (SV approach) and common-mode injection level (CB approach) [6], [7], [12].

It is well known that the maximum rectifier peak input voltage V depends on the common-mode injection level. The maximum modulation index $M = V/(V_{\mathrm{dc}}/2)$ which preserves linearity in the voltage formation process varies between $M_{\max} = 1$ (no zero-sequence injection) and $M_{\max} = 2/\sqrt{3}$ (maximum zero-sequence injection), depending on the modulation strategy. This work considers a commonly adopted 650 V DC-link system connected to the European low-voltage grid (i.e. 50 Hz, 400 V line-to-line). In this specific situation, the modulation index is fixed in a narrow window of $M = 1.0 \pm 10\%$, which is achievable by all of the considered modulation strategies, except for sinusoidal PWM.

The 4-quadrant switch signals s_{a}, s_{b} and s_{c} are obtained by comparing the modulation references

$$m_{\mathrm{o}} + \begin{cases} m_{\mathrm{a}} = M\cos(\vartheta) \\ m_{\mathrm{b}} = M\cos(\vartheta + \frac{2\pi}{3}) \\ m_{\mathrm{c}} = M\cos(\vartheta + \frac{4\pi}{3}) \end{cases} \tag{5}$$

with two vertically shifted carriers, as illustrated in Fig. 4 (where m_{o} is the common-mode injection). The switch relative ON-times are found by

$$\tau_{\mathrm{x}} = 1 - \frac{2}{V_{\mathrm{dc}}}|v_{\mathrm{x,LF}} + v_{\mathrm{o,LF}}| = 1 - |m_{\mathrm{x}} + m_{\mathrm{o}}| \quad \mathrm{x} = \mathrm{a},\ \mathrm{b},\ \mathrm{c}. \tag{6}$$

For reasons of convenience, the m_{x} values are sorted:

$$\begin{cases} m_{\max} = \max\{m_{\mathrm{a}}, m_{\mathrm{b}}, m_{\mathrm{c}}\} \\ m_{\min} = \min\{m_{\mathrm{a}}, m_{\mathrm{b}}, m_{\mathrm{c}}\} \\ m_{\mathrm{mid}} = -(m_{\max} + m_{\min}) \end{cases} \tag{7}$$

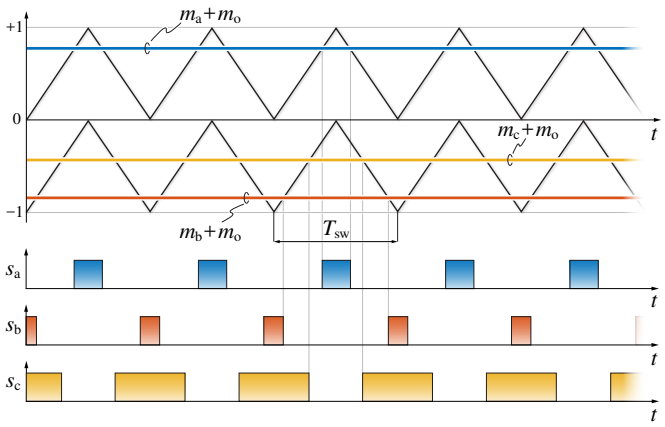


Fig. 4. Schematic overview of the 3-level rectifier modulator.

In this section, the most adopted modulation strategies for 3-level rectifiers are described and their common-mode injection expression is recalled. The local average values of leg-applied voltage, common-mode voltage and reference phase voltage are graphically illustrated in Fig. 5.

A. Sinusoidal PWM (SPWM)

The SPWM does not inject a LF common-mode component, thus resulting in the simplest modulation strategy:

$$m_{\mathrm{o}} = 0. \tag{8}$$

B. Third Harmonic Injection PWM (THIPWM)

The THIPWM injects a sinusoidal third harmonic with an amplitude of one-sixth of the fundamental reference:

$$m_{\mathrm{o}} = -\frac{1}{6}M\cos(3\vartheta). \tag{9}$$

C. Discontinuous PWM (DPWM)

Discontinuous modulation strategies, in essence, clamp the converter leg state either to P, N or M for a certain amount of the fundamental period, generating discontinuous switching. This property often allows to increase the converter switching frequency at constant overall loss. The most promising strategy for 3-level rectifiers is reported in [12]. This strategy takes into account the unidirectional nature of the rectifier, which does not allow most of the discontinuous modulation strategies adopted for bidirectional rectifiers. The common-mode injection expression is derived as in [14]:

$$m_{\mathrm{o}} = \begin{cases} -m_{\mathrm{mid}} & \text{if} \quad |m_{\max}| \geq |m_{\min}|,\ m_{\mathrm{shift}} \geq -m_{\mathrm{mid}} \\ m_{\mathrm{shift}} & \text{if} \quad |m_{\max}| \geq |m_{\min}|,\ m_{\mathrm{shift}} < -m_{\mathrm{mid}} \\ -m_{\mathrm{mid}} & \text{if} \quad |m_{\max}| < |m_{\min}|,\ m_{\mathrm{shift}} < -m_{\mathrm{mid}} \\ m_{\mathrm{shift}} & \text{if} \quad |m_{\max}| < |m_{\min}|,\ m_{\mathrm{shift}} \geq -m_{\mathrm{mid}} \end{cases} \tag{10}$$

where

$$m_{\mathrm{shift}} = \begin{cases} 1 - m_{\max} & \text{if} \quad |m_{\max}| \geq |m_{\min}| \\ -1 - m_{\min} & \text{if} \quad |m_{\max}| < |m_{\min}| \end{cases} \tag{11}$$

D. 2-Level Space Vector PWM (2LSVPWM)

The 2LSVPWM injects the same common-mode voltage as conventional 2-level inverters modulated with SVPWM:

$$m_{\mathrm{o}} = -\frac{1}{2}(m_{\max} + m_{\min}). \tag{12}$$

E. 3-Level Space Vector PWM (3LSVPWM)

The 3LSVPWM injects the same common-mode voltage as bidirectional 3-level inverters modulated with SVPWM:

$$m_{\mathrm{o}} = -\frac{1}{2}(m'_{\max} + m'_{\min}), \tag{13}$$

where

$$m'_{\mathrm{x}} = \begin{cases} m_{\mathrm{x}} + 1 & \text{if} \quad m_{\mathrm{x}} < 0 \\ m_{\mathrm{x}} - 1 & \text{if} \quad m_{\mathrm{x}} \geq 0 \end{cases} \tag{14}$$

$$\begin{cases} m'_{\max} = \max\{m'_{\mathrm{a}}, m'_{\mathrm{b}}, m'_{\mathrm{c}}\} \\ m'_{\min} = \min\{m'_{\mathrm{a}}, m'_{\mathrm{b}}, m'_{\mathrm{c}}\} \end{cases} \tag{15}$$

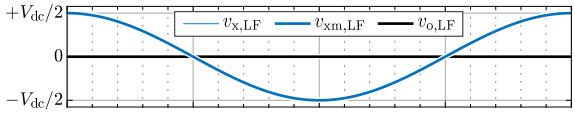
F. Zero Mid-Point Current PWM (ZMPCPWM)

The ZMPCPWM allows to have ideally zero mid-point current local average over the full fundamental period [6]:

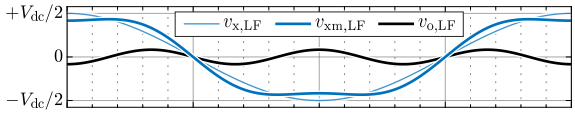
$$m_{\mathrm{o}} = m_{\mathrm{mid}}\left(\frac{m_{\mathrm{mid}}}{m_{\mathrm{max,abs}}} + 1\right) \approx -\frac{1}{4}M\cos(3\vartheta), \tag{16}$$

where

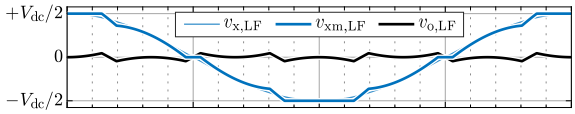
$$m_{\mathrm{max,abs}} = \begin{cases} m_{\mathrm{a}} & \text{if} \quad |m_{\mathrm{a}}| = \max\{|m_{\mathrm{a}}|, |m_{\mathrm{b}}|, |m_{\mathrm{c}}|\} \\ m_{\mathrm{b}} & \text{if} \quad |m_{\mathrm{b}}| = \max\{|m_{\mathrm{a}}|, |m_{\mathrm{b}}|, |m_{\mathrm{c}}|\} \\ m_{\mathrm{c}} & \text{if} \quad |m_{\mathrm{c}}| = \max\{|m_{\mathrm{a}}|, |m_{\mathrm{b}}|, |m_{\mathrm{c}}|\} \end{cases} \tag{17}$$



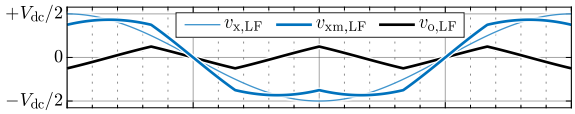
(a) Sinusoidal Modulation (SPWM)



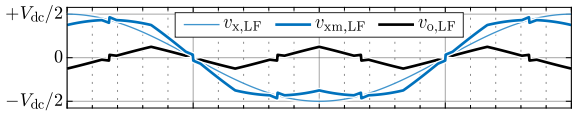
(b) Third Harmonic Injection Modulation (THIPWM)



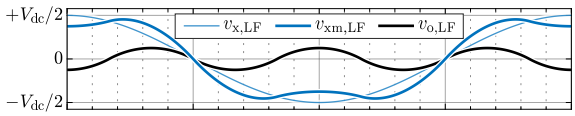
(c) Discontinuous Modulation (DPWM)



(d) 2-Level Space Vector Modulation (2LSVPWM)



(e) 3-Level Space Vector Modulation (3LSVPWM)



(f) Zero Mid Point Current Modulation (ZMPCPWM)

Fig. 5. Reference phase voltage $v_{\mathrm{x,LF}}$, leg-applied voltage $v_{\mathrm{xm,LF}}$ and common-mode voltage $v_{\mathrm{o,LF}}$ during a mains fundamental period.

IV. Component Stress

The component stress analysis in based on the following assumptions:

- resistive mains behaviour (current in phase with voltage);
- sinusoidal current shape;
- high carrier-to-fundamental frequency ratio;
- constant DC-link voltage;
- no discontinuous conduction mode operation.

In general, a carrier-to-fundamental frequency ratio $f_{\mathrm{sw}}/f > 200$ is sufficient to obtain normalized results which are independent on the specific application, i.e. on the power level. In the present case, this translates into $f_{\mathrm{sw}} > 10$ kHz. Moreover, the sinusoidal current shape hypothesis means that the DC-link capacitor RMS current calculation neglects the switching ripple in the phase currents.

The most relevant component stresses, which have a substantial impact on the converter design and operation, are the semiconductor losses, the high-frequency differential-mode and common-mode voltages applied to the input filter and the current and voltage stresses acting on the DC-link capacitor. While the conduction losses of the semiconductor devices are practically independent on the modulation strategy [6], the switching losses may differ if the modulation is of the continuous or discontinuous kind, since some devices may be switched less often in the latter case. The high-frequency voltage components $v_{\mathrm{x,HF}}$ and $v_{\mathrm{o,HF}}$ must be filtered by differential-mode inductors and common-mode chokes respectively, thus defining input filter size and losses (i.e. the AC filter topology of Fig. 3 is considered). Finally, the DC-link RMS current and voltage ripple define the size and rating of the DC-link capacitor.

In the following, only the passive component stresses are analysed and compared. Due to the reduced switching losses of the DPWM strategy, its switching frequency is increased by a factor equal to the inverse of the loss reduction. As shown in [12], this factor is approximately $\sqrt{3}M \approx \sqrt{3}$. Consequently, all modulation strategies are compared considering equal semiconductor losses.

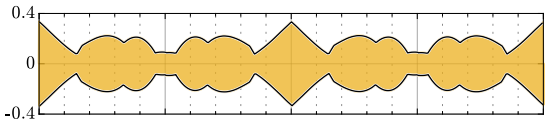
It is important to mention that analytical expressions of the average and RMS current stresses on all components can be derived, however they are characterized by high complexity and thus show little advantage with respect to the numerical approach adopted herein.

A. Differential-Mode Current Ripple

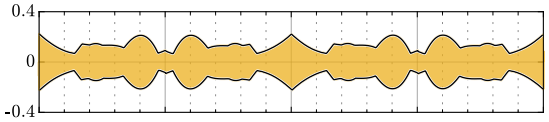
The HF differential-mode voltage $v_{\mathrm{x,HF}}$ generates a current ripple through the input inductors. The peak-to-peak and RMS values of this ripple are of particular interest when designing the differential-mode input filter. Since both values linearly depend on the switching frequency f_{sw}, DC-link voltage V_{dc} and inductance L values, the normalization constant

$$\Delta i_{\mathrm{n}} = \frac{V_{\mathrm{dc}}}{8 f_{\mathrm{sw}} L} \tag{18}$$

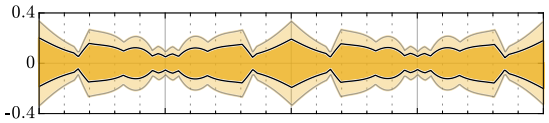
is defined. In this way, all results can be equally normalized, becoming independent on the specific ratings of the application. The normalized differential-mode current ripple resulting from each modulation strategy is shown in Fig. 6.



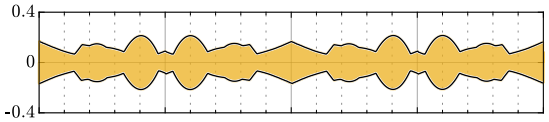
(a) Sinusoidal Modulation (SPWM)



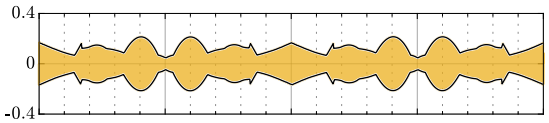
(b) Third Harmonic Injection Modulation (THIPWM)



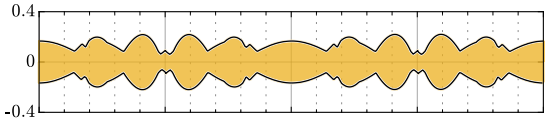
(c) Discontinuous Modulation (DPWM)



(d) 2-Level Space Vector Modulation (2LSVPWM)

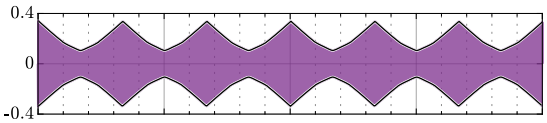


(e) 3-Level Space Vector Modulation (3LSVPWM)

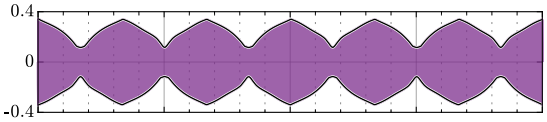


(f) Zero Mid Point Current Modulation (ZMPCPWM)

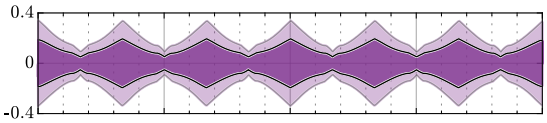
Fig. 6. Normalized differential-mode (DM) current ripple $\Delta i_{\mathrm{DM}}/\Delta i_{\mathrm{n}}$.



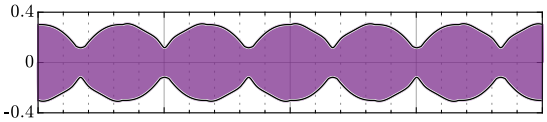
(a) Sinusoidal Modulation (SPWM)



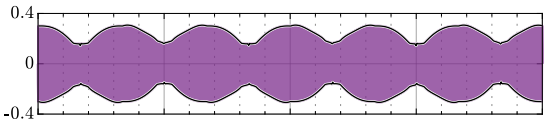
(b) Third Harmonic Injection Modulation (THIPWM)



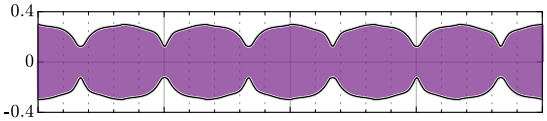
(c) Discontinuous Modulation (DPWM)



(d) 2-Level Space Vector Modulation (2LSVPWM)



(e) 3-Level Space Vector Modulation (3LSVPWM)



(f) Zero Mid Point Current Modulation (ZMPCPWM)

Fig. 7. Normalized common-mode (CM) current ripple $\Delta i_{\mathrm{CM}}/\Delta i_{\mathrm{n}}$.

B. Common-Mode Current Ripple

Similar considerations to the differential-mode can be done for the HF common-mode voltage $v_{\mathrm{o,HF}}$. The peak-to-peak and RMS current ripple values flowing through the common-mode chokes are of interest when designing the input common-mode filter. This ripple is also normalized by (18) and the results for the different modulation strategies are shown in Fig. 7.

C. Mid-Point Current

The mid-point current balancing is a common issue for all conventional multi-level converters [8]. In essence, depending on which is the state of the converter legs (i.e. P, N, M), a different current value flows into the DC-link mid-point. This current value has a natural zero average over one third of the fundamental period [6], however its local (i.e. switching-period related) average may be considerable, depending on the modulation strategy. A non-zero local average can generate a low-frequency (i.e. 150 Hz) mid-point voltage ripple of large amplitude, which may be considered unacceptable in the present application, due to the reasons mentioned in Section I. Furthermore, low-frequency current ripple must be addressed with large capacitance values, forcing the design choice to shift from film to electrolytic capacitors, with their well-documented reliability and lifetime limitations. The large required capacitance value would also not scale inversely with the switching frequency, setting a strict limit to the DC-link power density.

Being the voltage ripple linearly dependent on the phase current peak I, three times the fundamental frequency $3f$ and the capacitance C values, the following normalization factor is defined:

$$\Delta v_{\mathrm{n}} = \frac{I}{3fC}. \tag{19}$$

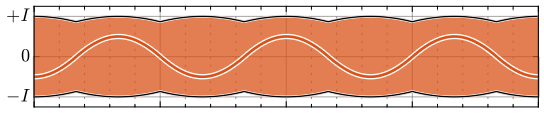
In this way, the DC-link mid-point peak-to-peak voltage ripple values ($\Delta v_{\mathrm{C,pp}}$) can be expressed in normalized form.

The mid-point current instantaneous and local average values are shown in Fig. 8. Although the local average of i_{m} depends on the modulation strategy, its RMS value does not [6]. Consequently, it is possible to derive that also the DC-link capacitor RMS current stress is independent on the adopted modulation strategy.

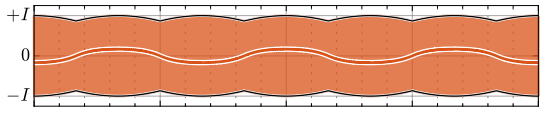
D. Comparison

The normalized component stress results for every modulation strategy are compared in Table I. It should be noted that the switching frequency of the DPWM strategy has been adjusted to yield the same switching losses of the other strategies. Moreover, it is observed that the only strategy achieving a zero LF voltage ripple is the ZMPCPWM.

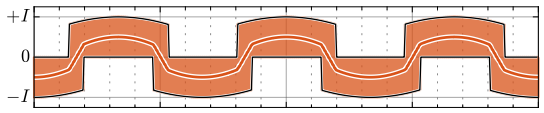
The present analysis highlights that there exists a fundamental trade-off between AC-side and DC-side performance, which must be accurately evaluated based on the application of the 3-level rectifier. In this case, being EV battery chargers sensitive to low-frequency DC-link voltage oscillations, the ZMPCPWM results the best strategy overall, providing



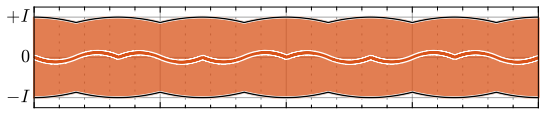
(a) Sinusoidal Modulation (SPWM)



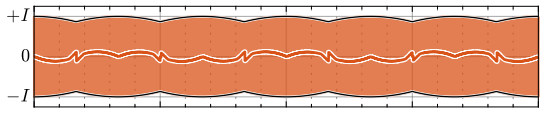
(b) Third Harmonic Injection Modulation (THIPWM)



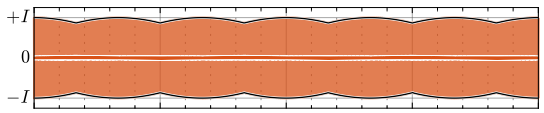
(c) Discontinuous Modulation (DPWM)



(d) 2-Level Space Vector Modulation (2LSVPWM)



(e) 3-Level Space Vector Modulation (3LSVPWM)



(f) Zero Mid Point Current Modulation (ZMPCPWM)

Fig. 8. Mid-point current i_{m} instantaneous value and local average.

zero low-frequency voltage ripple and adequate AC-side performance (i.e. similar or better than the other continuous modulation schemes). The DPWM strategy demonstrates the best AC-side performance by far, however it leads to the highest DC-side LF voltage oscillations. Therefore, this strategy should be selected in those applications where the input filter size minimization is of utmost importance.

V. Conclusion

This paper has presented a comparison between the most significant modulation strategies for unidirectional 3-phase 3-level rectifiers. In particular, the work has been focused on a rectifier for EV ultra-fast charging applications connected to the European low-voltage grid (i.e. 50 Hz, 400 V line-to-line) and adopting a 650 V DC-link.

The presented analysis has highlighted the general trade-off between AC-side and DC-side performance of each modulation strategy, defining the current and voltage numerical stresses on both the AC-side filter and the DC-side capacitors. The zero mid-point current (ZMPC) modulation strategy has been identified as the best candidate for EV fast-charging applications, due to its zero low-frequency DC-side voltage oscillation and satisfactory AC-side performance comparable to the other continuous modulation strategies. Furthermore, a possible candidate for alternative applications focused on minimizing the AC-side filter size has been identified in the discontinuous modulation (DPWM).

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TABLE I. Modulation strategy comparison based on the most significant component stresses: best results are underlined.

Modulation	$\boldsymbol{\Delta i}_{\mathbf{DM,pp}}/\Delta i_{\mathrm{n}}$	$\boldsymbol{\Delta i}_{\mathbf{DM,rms}}/\Delta i_{\mathrm{n}}$	$\boldsymbol{\Delta i}_{\mathbf{CM,pp}}/\Delta i_{\mathrm{n}}$	$\boldsymbol{\Delta i}_{\mathbf{CM,rms}}/\Delta i_{\mathrm{n}}$	$\boldsymbol{\Delta v}_{\mathbf{C,pp}}/\Delta v_{\mathrm{n}}$	$\boldsymbol{I}_{\mathbf{C,rms}}/I$
SPWM	0.666	0.106	0.676	0.154	0.082	0.356
THIPWM	0.444	0.077	0.682	0.176	0.030	0.356
DPWM*	0.385	0.068	0.389	0.083	0.097	0.356
2LSVPWM	0.428	0.075	0.610	0.175	0.019	0.356
3LSVPWM	0.428	0.074	0.608	0.176	0.019	0.356
ZMPCPWM	0.438	0.080	0.598	0.176	≈ 0	0.356

*evaluated at $\sqrt{3}M$ times the switching frequency with respect to the others.