Digital Multi-Loop Control of an LLC Resonant Converter for Electric Vehicle DC Fast Charging

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***Abstract*—This paper proposes a digital control strategy for LLC resonant converters, specifically intended for EV battery charging applications. Two cascaded control loops, i.e. an external battery voltage loop and an internal battery current loop, are designed and tuned according to analytically derived expressions. Particular attention is reserved to the output current control analysis, due to its extremely non-linear behaviour. The well known seventh-order LLC small-signal model, derived with the extended describing function (EDF) method, is simplified to an equivalent first-order model at the resonance frequency. In these conditions, which are proven to be the most underdamped, the current control loop is tuned taking into account the delays introduced by the digital control implementation. Moreover, the adoption of a look-up table (LUT) in the feed-forward path is proposed to counteract the system non-linearities, ensuring high dynamical performance over the full frequency operating range. Finally, the proposed control strategy and controller design procedure are verified both in simulation and experimentally on a 15 kW LLC converter prototype.**

***Index Terms*—digital control, LLC resonant converter, isolated DC/DC converters, electric vehicles (EV), battery charging**

I. Introduction

An electric vehicle (EV) DC fast battery charger generally consists of two power electronic converter stages [1], [2], schematically represented in Fig. 1. The first stage is a grid-connected front-end AC/DC converter with unity power factor correction (PFC) capabilities, also known as active front-end (AFE), and a high-frequency isolated DC/DC converter needed for galvanic isolation from the mains and battery current regulation.

The main requirements for EV charging applications include high efficiency, high power density, wide input/output voltage range and low battery-side current ripple.

In power electronics, high power density goes hand-in-hand with high switching frequencies, which may only be achieved by soft-switching operation when efficiency is a major concern. Conventional resonant converters (i.e. series-resonant and parallel-resonant) satisfy both efficiency and power density requirements, however they lack wide load/voltage regulation capabilities [3]. This limitation is overcome by the LLC resonant converter, which is characterized by [4]–[7]: (1) zero-voltage switching (ZVS) of the input bridge MOSFETs and (2) zero-current switching (ZCS) of the output bridge diodes, (3) wide voltage regulation capability with a relatively small switching frequency variation, (4) capacitive converter output, reducing the size of the output filter, and (5) limited EMI generation, due to the converter resonant operations (i.e. no hard switching). Elements (1) and (2) are responsible for the well documented high efficiency and high power density achievable by this converter topology.

Nevertheless, the LLC converter still poses some major challenges because of its complex multi-resonant nature. In particular, this converter is difficult to analyze and design due to its multiple operational modes [8]. Moreover, the inherent converter characteristics prevent to control it by switching frequency variation at light load and low output voltage, although this limitation may be overcome with burst-mode [9] or phase-shift/duty-cycle regulation [10]. Finally, the tight output current control required in battery charging applications can be extremely challenging, since the converter resonant nature causes drastic system transfer function variations when moving away from the resonance frequency [11], [12]. For instance, the input voltage ripple rejection (at multiples of the mains frequency depending on the PFC topology) requires high current loop bandwidth or proper feed-forward compensation strategies.

Most low-power LLC converters directly control the voltage across a resistive load, therefore the most widespread control solution is based on an analog closed-loop control of the output voltage, exploiting a voltage-controlled oscillator (VCO) to regulate the switching frequency [9]. However, battery chargers mostly operate in current-controlled mode, thus a closed-loop control of the output converter current must be designed. Moreover, due to the advent of modern powerful and low-cost digital signal processors (DSPs), industry is increasingly pushing for digital control implementations. The benefits of digital controllers are well known and mainly consist in high degree of reproducibility, strong noise immunity and great flexibility, together with the opportunity of implementing complex control strategies and look-up tables (LUTs) [13]. Nevertheless, the digital implementation is affected by some drawbacks, such as sampling and quantization effects, limited resolution is generating output signals, limited computational speed and zero-order hold (ZOH) effects. In particular, for variable-frequency resonant converter applications, the limited DSP clock resolution may cause limit-cycle oscillations during normal operation [14].

According to the authors' best knowledge, only few digital control implementations of the LLC resonant converter have been reported in literature and they all belong to recent years [11], [12], [14]–[18]. In particular, [15] is the only one applied to EV battery chargers, however a clear controller design procedure is not provided.

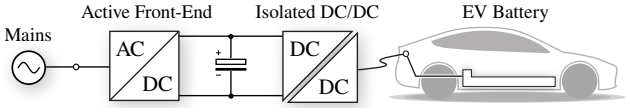

Fig. 1. Schematic overview of an EV off-board DC fast charger.

Therefore, the goal of the paper is to propose a digital multi-loop control strategy for an LLC resonant converter, specifically intended for battery charging applications. Since a wide input/output voltage range is required, the converter operating frequency can be far from resonance, nonetheless the current controller must still perform adequately. This wide closed-loop performance stability can be achieved by properly tuning the current controller and assisting it with an accurate LUT in the feed-forward path, ideally counteracting the system non-linear behaviour and contributing to the controller dynamic response away from the resonance.

This paper is structured as follows. In Section II, the complete small-signal model of the LLC converter is reported and a simplified dynamic relation between switching frequency and output converter current is derived at the resonance frequency. In Section III, the proposed LLC digital multi-loop control strategy is described and a straightforward tuning procedure for the current and voltage controllers, based on analytically derived expressions, is provided. The controller design procedure is validated in Section IV, where the dynamical performance predictions are compared to circuit simulations and experimental waveforms obtained on a 15 kW LLC converter prototype. Finally, Section V concludes this work with a brief summary of the main contributions.

II. LLC Small-Signal Model

The present analysis considers a full-bridge LLC resonant converter, schematically illustrated in Fig. 2. Nevertheless, all considerations maintain validity also for the half-bridge LLC topology, if the appropriate value of the applied input voltage square-wave is considered. The system is characterized by four state variables: the resonant inductor current i_r, the resonant capacitor voltage v_c, the transformer magnetizing current i_m and the output capacitor voltage v_o. The only system input variable is the switching frequency f_sw of the full-bridge, while the input voltage V_i and the battery equivalent resistance R_b and open-circuit voltage V_b can be considered as system parameters or disturbances.

The most widespread approach to derive an accurate small-signal model of the LLC resonant converter is the extended describing function (EDF) method [11], [12], [18]–[20], which is based on a sinusoidal first-harmonic approximation (FHA) of the converter state variables. This approach converts the non-linear contributions of the system equations (e.g. modulus and sign functions) into their first-harmonic components at the switching frequency. However, this process results in an increase of the system order, since each AC sinusoidal variable must be expressed by two independent sine and cosine components. The four original system state variables (i_r, v_c, i_m, v_o) thus become seven (i_rs, i_rc, v_cs, v_cc, i_ms, i_mc, v_o), where the subscripts s and c refer to the sine and cosine components respectively. A seventh-order system results [11]:

$$\begin{cases} \dfrac{\mathrm{d}i_\mathrm{rs}}{\mathrm{d}t} = -\omega_\mathrm{sw} i_\mathrm{rc} + \dfrac{1}{L_\mathrm{r}}\left(\dfrac{4}{\pi}V_\mathrm{i} - v_\mathrm{cs} - \dfrac{4}{\pi} n v_\mathrm{o} \dfrac{i_\mathrm{rs} - i_\mathrm{ms}}{i_\mathrm{p}}\right) \\ \dfrac{\mathrm{d}i_\mathrm{rc}}{\mathrm{d}t} = \omega_\mathrm{sw} i_\mathrm{rs} - \dfrac{1}{L_\mathrm{r}}\left(v_\mathrm{cc} + \dfrac{4}{\pi} n v_\mathrm{o} \dfrac{i_\mathrm{rc} - i_\mathrm{mc}}{i_\mathrm{p}}\right) \\ \dfrac{\mathrm{d}v_\mathrm{cs}}{\mathrm{d}t} = -\omega_\mathrm{sw} v_\mathrm{cc} + \dfrac{1}{C_\mathrm{r}} i_\mathrm{rs} \\ \dfrac{\mathrm{d}v_\mathrm{cc}}{\mathrm{d}t} = \omega_\mathrm{sw} v_\mathrm{cs} + \dfrac{1}{C_\mathrm{r}} i_\mathrm{rc} \\ \dfrac{\mathrm{d}i_\mathrm{ms}}{\mathrm{d}t} = -\omega_\mathrm{sw} i_\mathrm{mc} + \dfrac{1}{L_\mathrm{m}}\dfrac{4}{\pi} n v_\mathrm{o} \dfrac{i_\mathrm{rs} - i_\mathrm{ms}}{i_\mathrm{p}} \\ \dfrac{\mathrm{d}i_\mathrm{mc}}{\mathrm{d}t} = \omega_\mathrm{sw} i_\mathrm{ms} + \dfrac{1}{L_\mathrm{m}}\dfrac{4}{\pi} n v_\mathrm{o} \dfrac{i_\mathrm{rc} - i_\mathrm{mc}}{i_\mathrm{p}} \\ \dfrac{\mathrm{d}v_\mathrm{o}}{\mathrm{d}t} = \dfrac{1}{C_\mathrm{o}}\left(\dfrac{2}{\pi} n i_\mathrm{p} - \dfrac{v_\mathrm{o} - V_\mathrm{b}}{R_\mathrm{b}}\right) \end{cases} \tag{1}$$

where $\omega_\mathrm{sw} = 2\pi f_\mathrm{sw}$ and the auxiliary variable i_p is defined as

$$i_\mathrm{p} = \sqrt{(i_\mathrm{rs} - i_\mathrm{ms})^2 + (i_\mathrm{rc} - i_\mathrm{mc})^2}. \tag{2}$$

Since system (1) is non-linear, it can be represented in the form

$$\begin{cases} \dot{X}(t) = f(X(t), U(t)) \\ Y(t) = g(X(t), U(t)) \end{cases}, \tag{3}$$

where $X = [i_\mathrm{rs}, i_\mathrm{rc}, v_\mathrm{cs}, v_\mathrm{cc}, i_\mathrm{ms}, i_\mathrm{mc}, v_\mathrm{o}]^\mathrm{T}$ is the state vector, $U = \omega_\mathrm{sw}$ is the input vector and $Y = v_\mathrm{o}$ is the output vector. In order to proceed with a small-signal perturbation analysis, system (3) must be linearized around an equilibrium working point. The general steady-state solution $(\bar{X}, \bar{Y})$ of a non-linear system in response to a constant input $\bar{U}$ is found by solving numerically

$$\begin{cases} 0 = f(\bar{X}, \bar{U}) \\ \bar{Y} = g(\bar{X}, \bar{U}) \end{cases}. \tag{4}$$

Introducing a small perturbation in the input δU, the state and output perturbations δX and δY are obtained. Developing a first-order Taylor expansion of functions g and f, the linearized system

$$\begin{cases} \delta\dot{X} \approx A\,\delta X + B\,\delta U \\ \delta Y \approx C\,\delta X + D\,\delta U \end{cases} \tag{5}$$

is obtained, where $A = \frac{\partial f}{\partial X}\big|_{\bar{X},\bar{U}}$, $B = \frac{\partial f}{\partial U}\big|_{\bar{X},\bar{U}}$, $C = \frac{\partial g}{\partial X}\big|_{\bar{X},\bar{U}}$ and $D = \frac{\partial g}{\partial U}\big|_{\bar{X},\bar{U}}$ are the system Jacobian matrices and their expression is provided in [21]. The eigenvalues of matrix A represent the poles (p_i) of the seventh-order system linearized around an equilibrium point and thus determine the system dynamical response to a perturbation. A numerical analysis of the location of the system poles on the root locus allows to identify the most

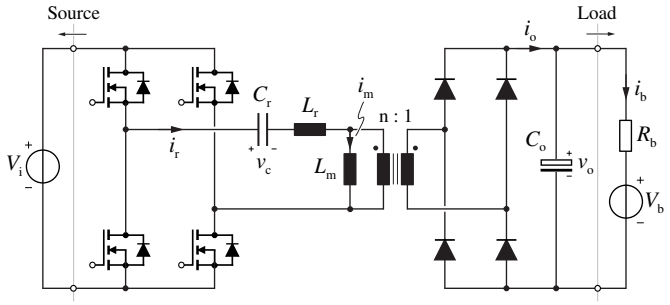

Fig. 2. Schematic of the considered system, composed of an ideal voltage source, a full-bridge LLC resonant converter and a battery equivalent load.

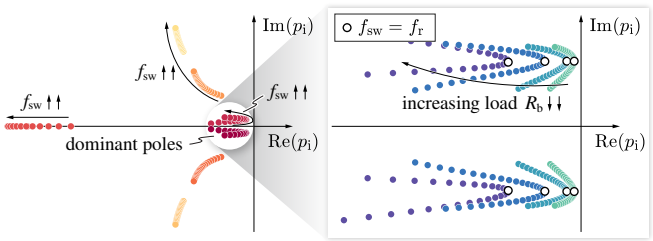

Fig. 3. Qualitative overview of the system poles p_i movement on the root locus as a function of the switching frequency $f_{sw} \in [0.75f_r, 1.25f_r]$ (a). Highlight of the dominant poles for different output load values (b).

critical (i.e. underdamped) situation. Fig. 3(a) qualitatively shows the movement of the system poles as a function of the switching frequency f_{sw}. The dominant poles, which define the dynamics of the system response, are identified and highlighted in Fig. 3(b), where the pole dependence on the converter load is illustrated. It is clearly observed that the most critical system operating condition is always found at the resonance frequency $f_r = 1/(2\pi\sqrt{L_r C_r})$, as previously reported in [12].

Since the closed-loop control must be stable in every operating condition, the worst-case design point for the system controllers coincides with the most underdamped plant transfer function. Therefore, a simplified small-signal model of the LLC converter, only valid for $f_{sw} = f_r$, is derived in the following.

The system equivalent circuit at the resonance frequency can be represented as in Fig. 4(a). Due to the negligible contribution of i_m, the input and output voltage square-waves are in phase and the resonant tank current is purely sinusoidal, as shown in Fig. 5. To isolate the resonant tank dynamical behavior from the rest of the system, a constant output voltage $v_o = V_o$ is considered in this analysis: this approximation is fairly valid in practice, as the output voltage loop dynamics are much slower than the current loop ones. The evolution of the current peak in the resonant tank is qualitatively illustrated in Fig. 5(b) and its expression can be derived as

$$\frac{\mathrm{d}\hat{i}_r}{\mathrm{d}t} = 4\frac{f_r}{Z_r}\left(V_i - nV_o\right), \tag{6}$$

where $Z_r = \sqrt{L_r/C_r}$ is the characteristic impedance of the resonant tank. The evolution of the average rectified secondary current $i_o = \frac{2}{\pi} n \hat{i}_r$ is obtained as

$$\frac{\mathrm{d}i_o}{\mathrm{d}t} = \frac{4}{\pi^2}\frac{n}{L_r}\left(V_i - nV_o\right), \tag{7}$$

from which L_{eq} is defined:

$$L_{eq} \overset{\text{def}}{=} \frac{\pi^2}{4} L_r. \tag{8}$$

The dynamics of the converter at the resonance frequency can be therefore represented by the DC equivalent circuit in Fig. 4(b), which highlights the integral nature of the plant.

To derive the system small-signal model, the effect of a switching frequency perturbation (i.e. system input) on the output current (i.e. system output) must be evaluated. It can be observed that a f_{sw} variation induces a stationary V_o variation, which can be quantified by leveraging the expression of the static FHA voltage gain [22]

$$M = \frac{nV_o}{V_i} = \frac{1}{\sqrt{\left(1 + \lambda - \lambda\frac{f_r^2}{f_{sw}^2}\right)^2 + Q^2\left(\frac{f_{sw}}{f_r} - \frac{f_r}{f_{sw}}\right)^2}} \tag{9}$$

where $\lambda = L_r/L_m$ and $Q = \frac{\pi^2}{8}\frac{Z_r}{n^2}\frac{i_o}{V_o}$, obtaining a load-independent expression [12]

$$\left.\frac{\partial V_o}{\partial f_{sw}}\right|_{f_{sw}=f_r} = -\frac{V_i}{n}\left.\frac{\partial M}{\partial f_{sw}}\right|_{f_{sw}=f_r} = \underbrace{-\frac{8}{\pi}\frac{V_i}{n}\frac{L_r}{L_m}\frac{1}{f_r}}_{k_f}. \tag{10}$$

It should be noted that k_f is negative, since an increase of the switching frequency leads to a lower steady-state output voltage. From a small-signal perspective, i.e. neglecting the constant voltage sources V_i and V_o, the static voltage gain variation induced by a f_{sw} perturbation appears as a dynamical forcing term on the equivalent inductor L_{eq}/n^2, as illustrated in Fig. 4(c). Therefore, the small-signal relation between i_o and f_{sw} is found as

$$\frac{\mathrm{d}i_o}{\mathrm{d}t} = \frac{n^2 k_f}{L_{eq}} f_{sw}. \tag{11}$$

Finally, if an effective dynamical decoupling between the output current and voltage loops is considered, the small-signal relation between v_o and i_o is derived from (1)

$$\frac{\mathrm{d}v_o}{\mathrm{d}t} = \frac{1}{C_o}\left(i_o - \underbrace{\frac{v_o - V_b}{R_b}}_{i_b}\right). \tag{12}$$

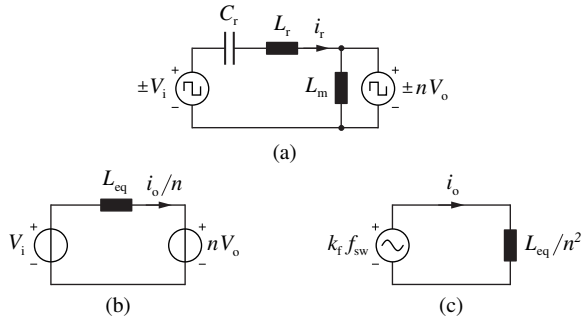

Fig. 4. LLC equivalent circuit models at resonance: (a) simplified AC circuit, (b) equivalent DC circuit and (c) small-signal equivalent circuit. The output voltage is considered constant, i.e. $v_o = V_o$, since the focus is on the faster output current i_o dynamics.

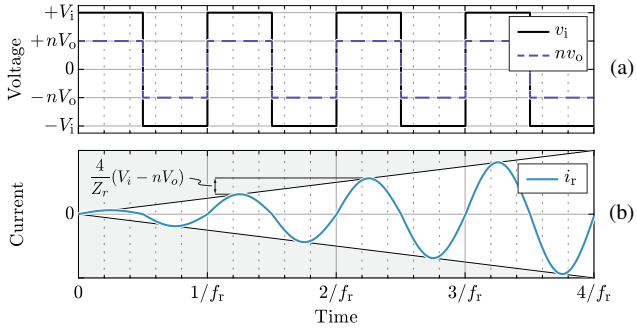

Fig. 5. Qualitative LLC waveforms at resonance, i.e. $f_{sw} = f_r$: (a) input and output voltage square-waves and (b) resonant tank current evolution.

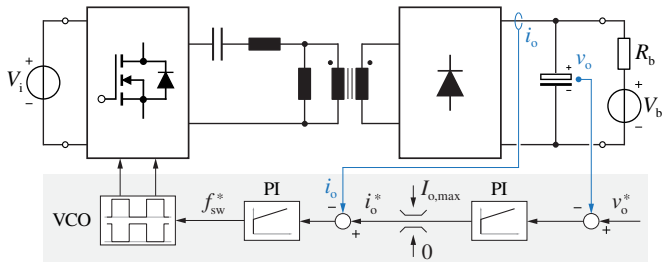

Fig. 6. Simplified schematic of the proposed multi-loop converter control, composed of the output voltage v_o loop and the output current i_o loop. The voltage controlled oscillator (VCO) is implemented by digital means.

III. Controller Design

A dual-loop control scheme, composed of an outer voltage control loop (v_o) and an inner current control loop (i_o), is implemented in digital form, as schematically illustrated in Fig. 6. The i_o control loop provides tight output current regulation by acting on the switching frequency of the input bridge. The v_o control loop only plays a role during start-up and constant-voltage battery charging (i.e. at the very end of the charging process). The voltage reference is set to the fully-charged maximum battery voltage value $V_{b,max}$, provided by the vehicle itself. During most of the time, the output of the voltage regulator is saturated to the maximum charging current value $I_{o,max}$, either limited by the vehicle battery management system (BMS) or by the converter current/power boundaries. Therefore, the voltage control dynamics are not of primary importance in the present application. Nevertheless, for reasons of completeness, a tuning procedure for both the current and the voltage controllers is provided in this section.

A. Output Current Control Loop

The proposed digital output current control scheme is illustrated in Fig. 7. The current is measured at the output of the diode bridge, i.e. as a rectified sine wave, and is averaged by means of a digital oversampling process. The control loop is composed of a proportional-integral (PI) regulator, a switching frequency feed-forward LUT, a minimum/maximum frequency saturation block, a delay deriving from the digital control implementation and the plant itself (i.e. frequency-to-current transfer function).

The digital sampling and update is performed at a constant frequency $f_s = 1/T_s$, i.e. the sampling or control frequency. To accurately tune the current control loop performance, the system delays introduced by the digital controller implementation must be taken into account, as each delay reduces the achievable control bandwidth and/or decreases the closed-loop stability margin [23], [24]. The current oversampling and averaging process is responsible for the first delay component, since it is approximately equivalent to a moving-average delay of $T_s/2$. The second component is directly related to the digital interrupt service routine (ISR), which introduces a one sampling period delay T_s between input and output signals. Finally, the third component is linked to the zero-order hold (ZOH) effect of one sampling period introduced by the digital update process of the output switching frequency. Even though the ZOH does not result in a pure delay, if the control bandwidth is sufficiently lower than the Nyquist frequency, it may be treated as such (i.e. a $T_s/2$ delay). Therefore, the total delay introduced by the digital control implementation is $T_d = 2\,T_s$, which may be approximated with a rational Padè transfer function

$$G_d(s) = e^{-s2T_s} \approx \frac{1 - sT_s}{1 + sT_s}. \tag{13}$$

The plant small-signal model (11), derived in Section II, links the switching frequency to the output current and results in the transfer function

$$G_{p,i}(s) = \frac{i_o(s)}{f_{sw}(s)} = \frac{n^2 k_f}{sL_{eq}}. \tag{14}$$

Since k_f depends on the input voltage V_i, its value is calculated in real time and the regulator output is divided by k_f to stabilize the system gain, as shown in Fig. 7.

Even though the integral nature of the plant would ensure a zero steady-state tracking error with a proportional regulator, transfer function (14) is only valid at the resonance. When the converter is operated either in buck or in boost modes, the plant transfer function loses its pole in zero and no longer behaves as a pure integrator. Therefore, a PI controller is here adopted to achieve zero steady-state error in every operating condition and better overall disturbance rejection capabilities. The controller transfer function is therefore

$$G_{c,i}(s) = k_{P,i} + \frac{k_{I,i}}{s}. \tag{15}$$

To unburden the integral part of the PI regulator and achieve more stable dynamical performance across the complete converter operating range, the steady-state switching frequency in the desired operating conditions is fed forward. Due to the extreme non-linear nature of the system, the steady-state f_{sw} value is extracted and stored in a LUT, as a function of the operating voltage gain M and quality factor Q. In particular, M and Q allow to normalize the converter operating conditions and uniquely identify a working point in the inductive region (i.e. the stable region) with only two parameters. Therefore, the LUT serves the purpose of unloading the PI controller from the major frequency steps, thus ensuring its small-signal operation: the linear regulator must only counteract the dynamical perturbations around equilibrium (proportional part) and the LUT steady state error (integral part).

The most simple albeit imprecise way to extract a $f_{sw}(M, Q)$ LUT is by numerically inverting the FHA gain expression (9). Better methods, ensuring increasing accu-

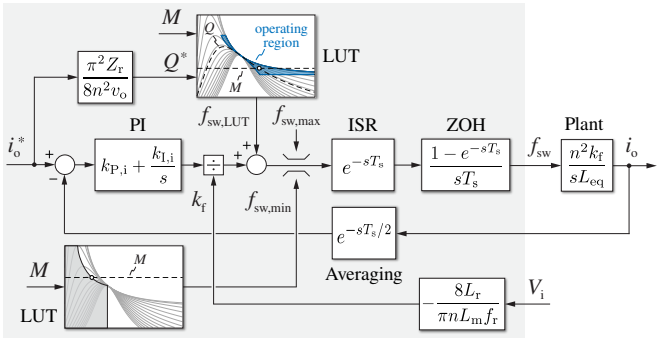

Fig. 7. Detailed schematic overview of the output current i_o closed-loop control. The digital controller is highlighted in grey.

racy at the expense of a higher realization effort, consist in solving a time-domain analysis (TDA) of the system operating modes [25], carrying out an extensive set of circuit simulations or characterizing the real converter prototype with experimental measurements. In this work, the results of the FHA and the TDA methods are compared. It is worth noting that the TDA method yields the exact same results as the extensive circuit simulations, however requiring far lower computational effort and time.

As illustrated in Fig. 7, a switching frequency saturation block must be present in the forward control path, to ensure that the converter operation remains inside the minimum and maximum frequency design boundaries. In particular, the minimum switching frequency limit is a function of the voltage gain M, as it represents the boundary between the stable (inductive) and unstable (capacitive) regions. Therefore, $f_{\mathrm{sw,min}}(M)$ is also extracted and stored in a LUT.

Since simplified rational transfer functions have been derived for every subsystem, the tuning of the PI regulator can be performed in the continuous time domain employing conventional techniques. In the present work, a phase-margin criteria is selected for demonstration purposes. For the reasons mentioned in Section II, the controller gains are tuned at the resonance frequency, to ensure control stability and sufficient damping across all operating points. The current control open-loop transfer function at $f_{\mathrm{sw}} = f_{\mathrm{r}}$ has the following form:

$$G_{\mathrm{ol,i}}(s) = G_{\mathrm{d}}(s)\, G_{\mathrm{p,i}}(s)\, G_{\mathrm{c,i}}(s). \tag{16}$$

The open-loop 0 dB cross-over frequency is derived by substituting equations (13), (14) and (15) into (16) and setting $|G_{\mathrm{ol,i}}(j\omega_{\mathrm{c,i}})| = 1$, obtaining

$$\omega_{\mathrm{c,i}} = \frac{1}{T_{\mathrm{s}}} \frac{\sqrt{\left[1+k_{\mathrm{z}}^2\right]\left[1+\tan^2\left(m_\varphi\right)\right]} - k_{\mathrm{z}} - \tan\left(m_\varphi\right)}{1 - k_{\mathrm{z}}\,\tan\left(m_\varphi\right)}$$

$$\overset{k_{\mathrm{z}} \ll 1}{\approx} \frac{1}{T_{\mathrm{s}}}\left[-\tan(m_\varphi) + \sqrt{1+\tan^2(m_\varphi)}\right], \tag{17}$$

where m_φ is the desired phase margin in radians, while k_{z} is the ratio between the PI zero $\omega_{\mathrm{z,i}} = k_{\mathrm{I,i}}/k_{\mathrm{P,i}}$ and the cross-over frequency $\omega_{\mathrm{c,i}}$. The PI parameters are directly obtained by:

$$\begin{cases} k_{\mathrm{P,i}} = \omega_{\mathrm{c,i}}\, \dfrac{L_{\mathrm{eq}}}{n^2} \dfrac{1}{\sqrt{1+k_{\mathrm{z}}^2}} \overset{k_{\mathrm{z}} \ll 1}{\approx} \omega_{\mathrm{c,i}}\, \dfrac{L_{\mathrm{eq}}}{n^2} \\ k_{\mathrm{I,i}} = \omega_{\mathrm{z,i}}\, k_{\mathrm{P,i}} \end{cases}. \tag{18}$$

In the following, $m_\varphi = 45^\circ$ and $k_{\mathrm{z}} = 1/10$ are considered, ensuring both fast reference step response and sufficient disturbance rejection capability. For the system at hand, i.e. with $f_{\mathrm{s}} = 20\,\mathrm{kHz}$, a $1.1\,\mathrm{kHz}$ cross-over frequency is obtained, which roughly corresponds to the bandwidth of the closed-loop control.

B. Output Voltage Control Loop

The complete output voltage control schematic is illustrated in Fig. 8. The plant transfer function is obtained

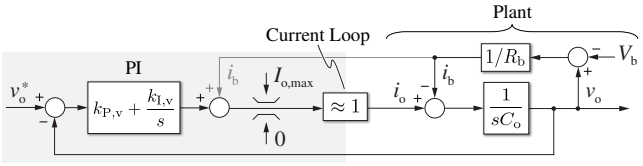

Fig. 8. Detailed schematic overview of the output voltage v_{o} closed-loop control. The digital controller is highlighted in grey.

from (12) considering the battery voltage V_{b} as a disturbance component:

$$G_{\mathrm{p,v}}(s) = \frac{v_{\mathrm{o}}(s)}{i_{\mathrm{o}}(s)} = \frac{R_{\mathrm{b}}}{1 + s\, R_{\mathrm{b}}\, C_{\mathrm{o}}}. \tag{19}$$

Since the measurement of the battery current i_{b} is normally available, its value can be fed forward. In this case, the compensated plant behaves as a pure integrator:

$$G_{\mathrm{p,v}}(s) \approx \frac{1}{sC_{\mathrm{o}}}. \tag{20}$$

Nevertheless, a PI regulator is selected to improve the controller dynamical performance and to ensure zero steady-state error when i_{b} is not known and cannot be fed forward:

$$G_{\mathrm{c,v}}(s) = k_{\mathrm{P,v}} + \frac{k_{\mathrm{I,v}}}{s}. \tag{21}$$

If the open-loop 0 dB cross-over frequency $\omega_{\mathrm{c,v}}$ is set sufficiently lower than the bandwidth of the current control loop (i.e. $\approx \omega_{\mathrm{c,i}}$), the dynamics of the two loops do not interfere with each other. Therefore, $\omega_{\mathrm{c,v}}$ is set to $\omega_{\mathrm{c,i}}/10$, resulting, in the present case, in a 110 Hz open-loop cross-over frequency. The controller parameters are derived as

$$\begin{cases} k_{\mathrm{P,v}} = \omega_{\mathrm{c,v}}\, C_{\mathrm{o}} \\ k_{\mathrm{I,v}} = \omega_{\mathrm{z,v}}\, k_{\mathrm{P,v}} \end{cases}, \tag{22}$$

where the PI zero $\omega_{\mathrm{z,v}} = k_{\mathrm{I,v}}/k_{\mathrm{P,v}}$ is set to $\omega_{\mathrm{c,v}}/5$ in order to improve the closed-loop disturbance rejection capabilities.

IV. Simulation and Experimental Results

The controller design procedure proposed in Section III is here applied to a 15 kW LLC converter for EV fast-charging applications, taking part in a modular and scalable structure presented in [26]. The specifications and the design operating region of the converter are reported in Table I. The control frequency f_{s} is set to 20 kHz, while the current oversampling and averaging process operates with 32 samples per period.

TABLE I. LLC converter specifications and operating region.

Parameter	Description	Value
n	transformer turn ratio	1
L_{r}	resonant inductance	8.7 µH
C_{r}	resonant capacitance	147.0 nF
L_{m}	magnetizing inductance	25.3 µH
C_{o}	output filter capacitance	220 µF
f_{r}	resonance frequency	140.6 kHz
Z_{r}	characteristic impedance	7.7 Ω
V_{i}	input voltage	325…400 V
V_{o}	output voltage	250…500 V
I_{o}	output current	37.5 A
P_{o}	output power	15 kW

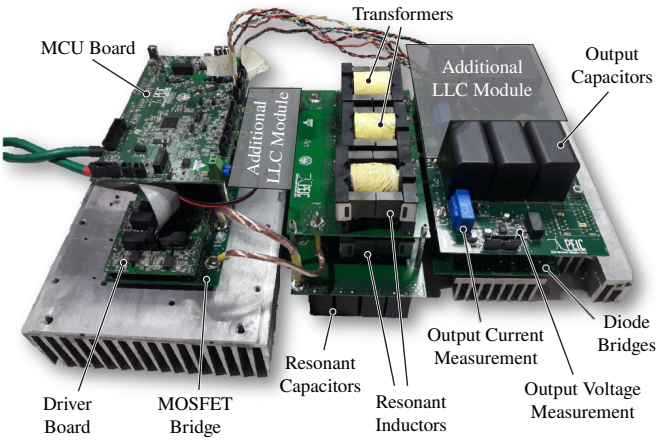

Fig. 9. Overview of the utilized 15 kW LLC converter prototype. Since the boards are designed for two paralleled 15 kW modules, the parts belonging to the second module are greyed out.

To validate the theoretical assumptions, the converter dynamical performance are tested both in simulation environment and by experimental means on the converter prototype illustrated in Fig. 9.

A. Simulation Verification

As previously mentioned, the $f_{\mathrm{sw}}(M,Q)$ LUT, required for the current control loop of Fig. 7, can be extracted in different ways. Fig. 10 compares the results obtained with FHA (a) and TDA (b): the derived $f_{\mathrm{sw,min}}(M)$ and $f_{\mathrm{sw,max}} = 250$ kHz boundaries are superimposed to graphically identify the feasible operating region. It can be observed that the FHA method yields a wider operating frequency range for the same (M,Q) values. Moreover, the behavior at low quality factors is extremely different between the two, as only the TDA method allows to correctly predict the operating frequency at light load. For instance, with the FHA method the steady-state switching frequency for $M=1$ is equal to f_{r} and is load independent, which is not the case for TDA. Since the TDA method is characterized by high accuracy and only requires a slight additional computation effort compared to FHA, it is the preferred choice for the LUT extraction when an experimental characterization of the converter is not available.

The converter small-signal behavior is verified in PLECS environment, where the proposed control strategy is implemented by means of a custom C-code script. To accurately simulate the discretized nature of digital systems, the control execution is triggered once every control period T_{s}, while the control outputs are updated at the following trigger instant.

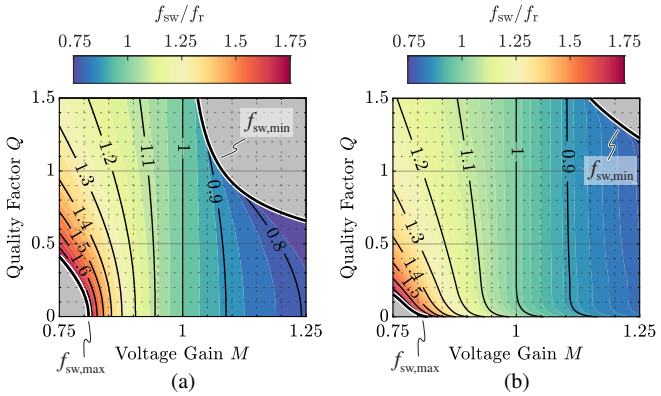

Fig. 10. Steady-state normalized switching frequency $f_{\mathrm{sw}}/f_{\mathrm{r}}$ as a function of M and Q, with minimum and maximum frequency limits superimposed. 101x101 LUT extracted with (a) FHA and (b) TDA.

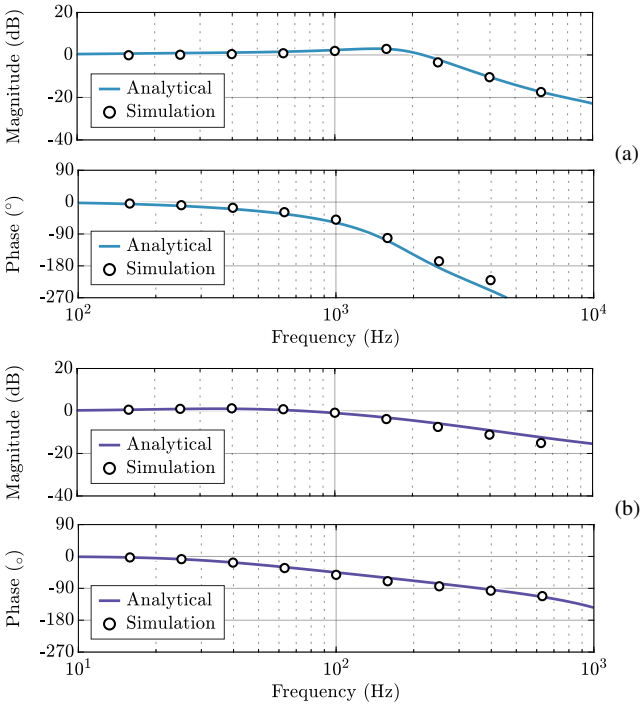

Fig. 11. Analytically derived and simulated closed-loop transfer functions of the i_{o} current control (a) and the v_{o} voltage control (b). Both transfer functions are extracted around the resonance working point, i.e. $V_{\mathrm{i}} = V_{\mathrm{o}}$ and $f_{\mathrm{sw}} = f_{\mathrm{r}}$, where the controllers have been tuned.

To verify the tuning of the i_{o} and v_{o} controllers, their closed-loop transfer functions are investigated at resonance, i.e. around $V_{\mathrm{i}} = V_{\mathrm{o}}$ $(M = 1)$ and $f_{\mathrm{sw}} = f_{\mathrm{r}}$. Several simulations are performed by setting sinusoidal references with different frequencies at the control input, measuring the system response and calculating its magnitude and phase by means of FFT post-processing in MATLAB environment. A DC offset is added to the i_{o} reference, in order to comply with the unidirectional nature of the LLC converter. The results of this analysis are illustrated in Fig. 11, where they are compared to the analytical expressions derived in Section III. It is observed that the analytical models show a high-level of accuracy over the full control frequency range, providing a first validation of the proposed controller design procedure.

B. Experimental Verification

The steady-state operation and the large-signal dynamical response of the output current controller are tested on the 15 kW LLC prototype illustrated in Fig. 9. The internal structure of this converter is unconventional, due to the adoption of coupled resonant inductors and two input-series/output-parallel connected transformers, as described in [26]. Nevertheless, from the control perspective, the prototype is equivalent to a conventional LLC converter with the parameters reported in Table I.

It is worth mentioning that the large-signal dynamical performance of the voltage loop are not verified experimentally, since the battery load (i.e. a voltage source with low internal impedance) does not comply with reference output voltage

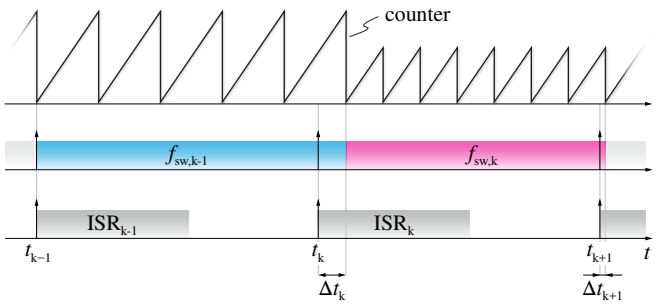

Fig. 12. Schematical overview of the implemented PWM update process. The switching frequency is updated in correspondence of the counter roll-over following the start of the ISR, in order to preserve the 50% duty-cycle constraint. A variable update delay Δt_k is introduced.

steps. In practice, during the converter start-up, the output voltage reference is ramped within a defined time period and the battery gets connected in parallel to C_o once v_o becomes higher than V_b, i.e. when the series protection diode, typically present in battery chargers, gets forward biased. Therefore, it is clear that the large-signal dynamical response of the closed-loop voltage controller is not of primary importance in this application.

The converter closed-loop control is implemented on a STM32G474VE microcontroller unit (MCU) from ST Microelectronics, with an ISR running at 20 kHz. The PWM signals are generated by a sawtooth counter realized with a high-resolution timer unit. The MCU clock frequency is 170 MHz and the timer unit internal clock can be sped up 16 times, yielding a PWM resolution of 368 ps. As highlighted in the timing diagram of Fig. 12, whenever f_{sw} is not an integer multiple of f_s, the PWM frequency is updated in correspondence of the counter roll-over following the start of the ISR. This solution ensures that the generated PWM signal maintains 50% duty-cycle when transitioning from a control period to the next one, i.e. making sure that no DC component is injected. However, a mismatch between the ISR and the switching frequency update is obtained, introducing an additional (variable) delay component in the control loop, depending on the converter switching frequency itself. Nevertheless, the effect of this delay can be neglected in a first approximation, as the minimum f_{sw}/f_s ratio considered herein is ≈ 6 (boost-mode). As a further note, the analog signals are acquired with the MCU internal 12-bit ADCs, but leveraging a 32-samples oversampling technique the measurement resolution can be increased up to 16-bit.

It is important to mention that, since the prototype is undergoing an early testing phase at the time of writing, the experimental waveforms are extracted with reduced current and voltage ratings with respect to Table I. Nevertheless, the control considerations and dynamical performance are not affected by the converter power level, thus remaining valid.

The steady-state output current waveforms with $i_o^* = 10$ A in different operating conditions are illustrated in Fig. 13. It is observed that the closed-loop current controller ensures zero steady-state error in all operating modes, including buck and boost (i.e. when the plant does not behave as a pure integrator), as a result of the integral part of the PI regulator.

Fig. 14 shows the closed-loop current control response to a current reference step from 5 A to 10 A in different operating conditions. The system dynamical behaviour at resonance is illustrated in Fig. 14(a), where the current reference i_o^* is also shown. The effect of the digital delay is highlighted, resulting in a blank time previous to the system response. Even though the battery current rise is superimposed to an oscillation deriving from the output filter capacitance resonating with the load parasitic inductance, the fast rise-time reflecting the designed control loop bandwidth (i.e. ≈ 2 kHz, see Fig. 11) is observed.

It is worth noting that the LUT plays a minor role at resonance, since the steady-state switching frequency is mostly independent on the load (see Fig. 10). However, this is not the case when operating in boost or buck modes. The role of the LUT becomes increasingly important when

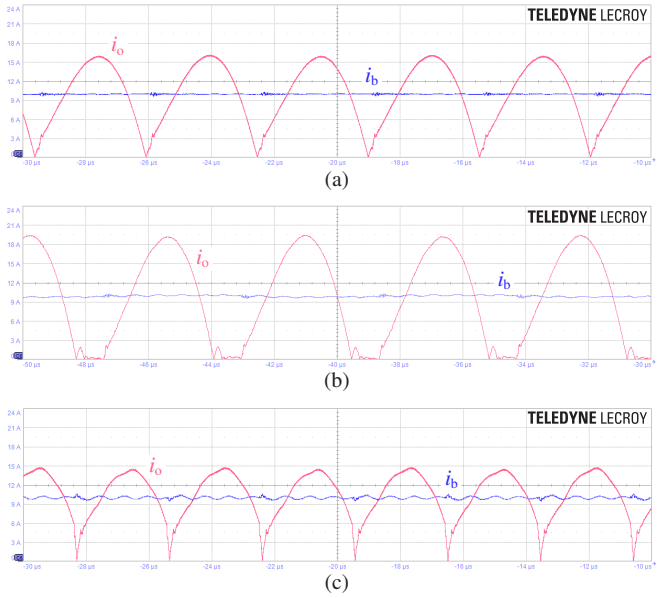

Fig. 13. Steady-state output current i_o and battery current i_b waveforms with $i_o^* = 10$ A and $V_i = 200$ V (X-axis 2 µs/div, Y-axis 3 A/div). Current i_o is obtained by taking the absolute value of the transformer secondary current. (a) resonance mode ($M = 1$, $f_{sw} = 141$ kHz), (b) boost mode ($M = 1.25$, $f_{sw} = 114$ kHz) and (c) buck mode ($M = 0.85$, $f_{sw} = 172$ kHz).

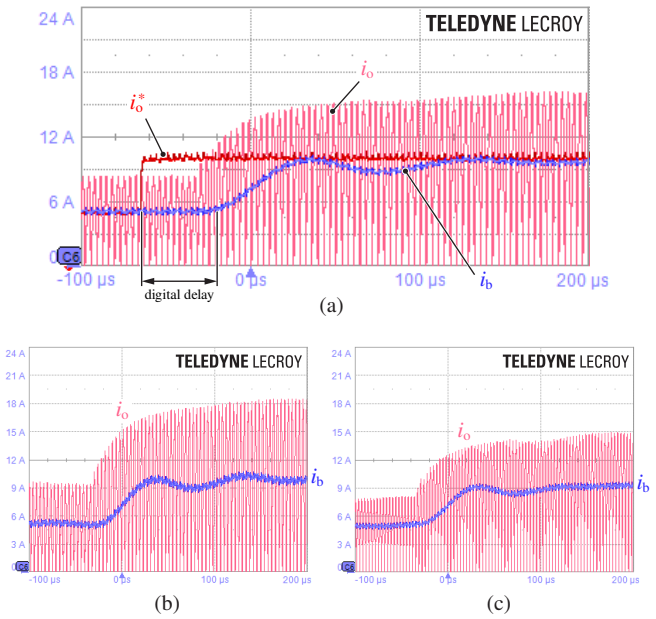

Fig. 14. Closed-loop current control response to a reference step i_o^* from 5 A to 10 A with $V_i = 200$ V (X-axis 100 µs/div, Y-axis 3 A/div). (a) resonance mode ($M = 1$, $f_{sw} = f_r$), (b) boost mode ($M = 1.1$, $f_{sw} < f_r$) and (c) buck mode ($M = 0.9$, $f_{sw} > f_r$). The 101x101 LUT of Fig. 10(b) is adopted.

moving away from resonance, as the system gain drops rapidly and the converter steady-state switching frequency becomes progressively dependent on the load. To verify the controller performance outside the resonance region, the system response in boost and buck modes is tested, as shown in Fig. 14(b) and (c), respectively. It is observed that, since the LUT directly provides the steady-state switching frequency value, the controller response remains practically constant, independently on the working point. Nevertheless, the LUT inaccuracy must be compensated by the integral part of the PI controller. For instance, this is particularly evident in Fig. 14(c), where the system rapidly jumps to $i_{\mathrm{b}} = 9$ A, but slowly progresses towards the 10 A reference (i.e. with a different time scale). Therefore, the LUT unloads the PI regulator from the major frequency steps, stabilizing and increasing the performance of the current controller.

It can be concluded that the proposed feed-forward LUT approach is essential for maintaining rapid and stable dynamic response in a wide voltage/current operating range, which is a major requirement for battery chargers.

V. Conclusion

In this work, a digital multi-loop control strategy for LLC converters, specifically targeted to EV battery charger applications, has been presented. The well-known LLC seventh-order non-linear system, derived according to the EDF method, has been simplified to an equivalent first-order model at the resonance frequency. Since the system gain is highest at resonance, both the output current and output voltage control loops have been tuned in this condition, by leveraging the derived first-order model. In particular, the delays introduced by the digital implementation of the control strategy have been taken into account in the current controller design, yielding an accurate and straightforward tuning methodology. Moreover, a feed-forward LUT providing the steady-state switching frequency has been added to the current control-loop, in order to stabilize the controller performance over the full converter gain/load operating range. Finally, the theoretical assumptions and the performance improvement deriving from the LUT have been verified by means of circuit simulations and experimental results on a 15 kW LLC converter prototype, highlighting the validity and the benefits of the proposed control strategy.

Acknowledgment

The authors would like to thank F. Mandrile, E. Vico and S. Borlo for their contributions in designing and testing the converter prototype.

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