Digital Multi-Loop Control of a 3-Level Rectifier for Electric Vehicle Ultra-Fast Battery Chargers

Digital Multi-Loop Control of a 3-Level Rectifier for Electric Vehicle Ultra-Fast Battery Chargers

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***Abstract*—This paper proposes a digital multi-loop control strategy for a 3-level unidirectional rectifier specifically targeted to electric vehicle (EV) ultra-fast charging applications. The basic operation of a 3-level rectifier is described and the state-space model of the complete system is explained, with particular focus on the mid-point current generation process. By means of an appropriate modeling of the delays and the discretization introduced by the digital control implementation, four controllers (i.e. dq-currents, DC-link voltage and mid-point voltage balancing loops) are analytically designed in the continuous time domain with conventional techniques. Ultimately, the proposed controller design procedure is tested on a 50 kW, 20 kHz T-type rectifier, both in simulation and hardware-in-the-loop (HIL) environments, verifying the dynamical performance of all control loops.**

***Index Terms*—digital control, 3-level rectifiers, active front-end (AFE), power factor corrector (PFC), electric vehicles (EV), ultra-fast charging (UFC), hardware-in-the-loop (HIL)**

I. Introduction

As of today, electric vehicle (EV) DC ultra-fast charging (UFC) is considered one of the key missing links to EV mainstream adoption [1]. The basic structure of a state-of-the-art UFC connected to the low-voltage grid consists of two main converter stages [2], schematically represented in Fig. 1. The first stage is a grid-connected AC/DC converter with unity power factor correction (PFC) capabilities, also referred to as active front-end (AFE). The role of the AFE is to absorb the desired amount of power from the mains, while ensuring low distortion and harmonics in the input current. The second stage is a high-frequency isolated DC/DC converter, which provides galvanic isolation from the mains and controls the EV charging process by regulating the battery current. This work focuses only on the AFE stage.

Nowadays, 2-level inverters represent the most widespread solution for general active rectification, due to their simplicity and their intrinsic bidirectional capabilities. However, because of the 2-level output voltage waveform and the high-voltage rating of the semiconductor devices, this topology shows a limited trade-off between efficiency and power-density [3], which may be considered insufficient for UFC applications. Since DC fast charging only requires that the power flows from the grid to the vehicle, unidirectional 3-level rectifiers may represent a better alternative. The multi-level nature of these rectifiers allows to increase the switching frequency (adopting semiconductor devices with a lower voltage rating) and number of output voltage levels at the same time, enabling a drastic grid-side filter size reduction and thus enlarging the efficiency-to-power density performance envelope [3], [4].

Apart from the converter performance, the main requirements for a 3-level rectifier for battery charging may be summarized in (1) providing sinusoidal input current shaping (i.e. low distortion and harmonics), (2) controlling the DC-link voltage according to the DC/DC converter optimal operating conditions, (3) minimizing third-harmonic voltage oscillations of the DC-link mid-point and (4) controlling the mid-point voltage deviation both in standard operating conditions and under unbalanced split loads [5]. All of these requirements must be ensured by a proper converter control with sufficient dynamical performance. In particular, point (1) must be tackled with both a high-bandwidth current control loop (to limit the low-frequency harmonics) and a suitable grid-side filter design (to attenuate the high-frequency harmonics) [6]. Requirements (2) and (4) are achieved by properly designing a DC-link voltage and a mid-point voltage balance loops, with high enough dynamics to ensure low voltage deviation under load or unbalance steps. Finally, point (3) is accomplished by an appropriate selection of the rectifier modulation strategy [7]–[9].

In recent years, due to the advent of powerful and low-cost digital signal processors (DSPs), the digital control implementation is becoming the de facto industry standard. The benefits of digital controllers are well known and mainly consist in excellent noise immunity, high degree of reproducibility and considerable flexibility, enabling the implementation of complex control strategies [10]. Nevertheless, the digital implementation is affected by limited computational capabilities and sampling, quantization and zero-order hold (ZOH) effects, which may have critical repercussions on the converter control.

Even though the small-signal modeling of unidirectional 3-level rectifiers has already been analyzed in literature [11], as of the authors' best knowledge a clear and exhaustive multi-loop control strategy and controller design procedure, taking into account the control delays and ZOH effects deriving from the digital implementation, has yet to be provided. This is especially true when considering the specific requirements of EV battery chargers, as in the present case.

Therefore, the goal of the paper is to provide a straightforward and effective controller design procedure for 3-phase 3-level unidirectional rectifiers intended for EV UFC ap-

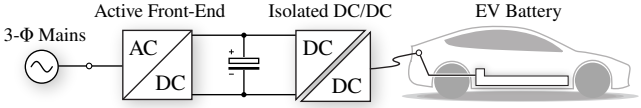


Fig. 1. Ultra-fast EV battery charger schematic overview.

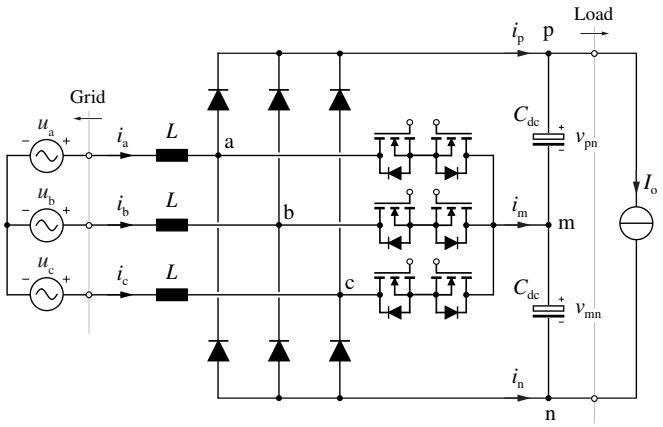


Fig. 2. Schematic of the considered system, composed of an ideal grid, a 3-phase 3-level unidirectional T-type rectifier and a current-source load.

plications. In particular, special attention is dedicated to the analysis and design of the DC-link capacitor voltage balancing control loop, since load unbalances may appear e.g. when the battery charger is built in a modular way, by connecting separate DC/DC units to the high-side and low-side DC-link capacitors [12].

This paper is structured as follows. In Section II the basic operation of 3-level rectifiers is described and the complete system state-space model is explained. In Section III the proposed multi-loop control structure is presented and all controllers are properly tuned according to derived analytical relations. In Section IV the dynamical performances of all control loops are tested both in simulation and hardware-in-the-loop (HIL) environments, validating the proposed controller design procedure. Finally, Section V summarizes and concludes this work.

II. System Model

The considered system is schematically illustrated in Fig. 2 and it is composed of a grid connected 3-level rectifier transferring power from the mains to a generic current-source load. A T-type unidirectional rectifier is selected for demonstration purposes, however the present analysis is valid for all three-level unidirectional converter topologies. It is worth noting that no inner grid impedance and no AC-side filter are considered for simplicity reasons, nevertheless these elements do not have a substantial impact on the general control considerations, particularly when the filter is properly damped [6].

The system state variables are the currents flowing through the inductors i_{abc} and the DC-link capacitor voltages v_{pm} and v_{mn}. Due to the three-wire nature of the system (i.e. no neutral conductor available), only two currents are independent, given

$$i_{\mathrm{a}} + i_{\mathrm{b}} + i_{\mathrm{c}} = 0. \tag{1}$$

Moreover, for reasons of convenience, the two voltage state variables are better expressed by

$$v_{\mathrm{dc}} = v_{\mathrm{pn}} + v_{\mathrm{mn}}, \tag{2}$$

$$v_{\mathrm{m}} = v_{\mathrm{pn}} - v_{\mathrm{mn}}, \tag{3}$$

where v_{dc} is the full DC-link voltage and v_{m} represents the mid-point voltage deviation from $v_{\mathrm{dc}}/2$.

Adopting a synchronous dq reference frame aligned with the grid voltage peak u, it is possible to express the system state-space equations in a compact form, as

$$\begin{cases} L\dfrac{\mathrm{d}i_{\mathrm{d}}}{\mathrm{d}t} = u - v_{\mathrm{d}} + \omega L i_{\mathrm{q}} \\ L\dfrac{\mathrm{d}i_{\mathrm{q}}}{\mathrm{d}t} = -v_{\mathrm{q}} - \omega L i_{\mathrm{d}} \\ \dfrac{C_{\mathrm{dc}}}{2}\dfrac{\mathrm{d}v_{\mathrm{dc}}}{\mathrm{d}t} = \dfrac{i_{\mathrm{p}} - i_{\mathrm{n}}}{2} - I_{\mathrm{o}} \\ C_{\mathrm{dc}}\dfrac{\mathrm{d}v_{\mathrm{m}}}{\mathrm{d}t} = -i_{\mathrm{m}} \end{cases} \tag{4}$$

where v_{d} and v_{q} are the phase voltages applied by the rectifier in the dq reference frame. These relations are schematically represented by the equivalent circuits in Fig. 3. In order to solve system (4), the DC-side currents i_{p}, i_{m} and i_{n} (with $i_{\mathrm{p}} + i_{\mathrm{m}} + i_{\mathrm{n}} = 0$) must be related to the state variables.

If balanced DC-link voltages are assumed, a first relation between AC-side and DC-side quantities is obtained as

$$P = v_{\mathrm{a}} i_{\mathrm{a}} + v_{\mathrm{b}} i_{\mathrm{b}} + v_{\mathrm{c}} i_{\mathrm{c}} = \\ = \frac{3}{2}(v_{\mathrm{d}} i_{\mathrm{d}} + v_{\mathrm{q}} i_{\mathrm{q}}) = \frac{1}{2} v_{\mathrm{dc}}(i_{\mathrm{p}} - i_{\mathrm{n}}). \tag{5}$$

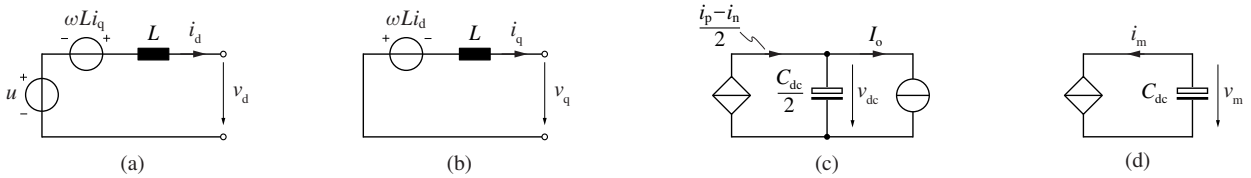
A second relation may be derived analysing of the mid-point current generation process. It is well documented in literature that this current is influenced by the zero-sequence (i.e. common-mode) voltage component v_{o} impressed at the AC-side [5]. This component does not affect the phase currents, however it modifies the distribution of the redundant switching states influencing the mid-point current local average value, expressed by

$$i_{\mathrm{m}} = \tau_{\mathrm{a}} i_{\mathrm{a}} + \tau_{\mathrm{b}} i_{\mathrm{b}} + \tau_{\mathrm{c}} i_{\mathrm{c}}, \tag{6}$$

where τ_{x} represents the relative ON-time of the mid-point switches:

$$\tau_{\mathrm{x}} = 1 - \frac{2}{v_{\mathrm{dc}}}|v_{\mathrm{x}} + v_{\mathrm{o}}| \qquad \mathrm{x} = \mathrm{a},\ \mathrm{b},\ \mathrm{c}. \tag{7}$$

By substituting (7) in (6) and integrating over one-third of the fundamental period T (i.e. the DC-side current periodicity), the expression of the mid-point current periodical average is



(a) (b) (c) (d)

Fig. 3. Equivalent circuits representing the system state-space equations: (a) d-axis current, (b) q-axis current, (c) DC-link voltage and (d) mid-point voltage.

obtained as

$$I_{\mathrm{m}} = \frac{3}{T}\int_{0}^{T/3} i_{\mathrm{m}}\,\mathrm{d}t = \frac{3}{T}\int_{0}^{T/3}\sum_{\mathrm{x=a,\,b,\,c}}\left(i_{\mathrm{x}} - \frac{2}{V_{\mathrm{dc}}}|v_{\mathrm{x}}+v_{\mathrm{o}}|i_{\mathrm{x}}\right)\mathrm{d}t. \quad (8)$$

Since unidirectional rectifiers can only apply leg voltage values with the same sign as the phase current, e.g. $v_{\mathrm{am}} = 0$ when the mid-point switch is ON and $v_{\mathrm{am}} = \mathrm{sign}(i_{\mathrm{a}})\,v_{\mathrm{dc}}/2$ when the switch is OFF, the following relation is valid:

$$|v_{\mathrm{xm}}|\,i_{\mathrm{x}} = |v_{\mathrm{x}}+v_{\mathrm{o}}|\,i_{\mathrm{x}} = (v_{\mathrm{x}}+v_{\mathrm{o}})\,|i_{\mathrm{x}}| \quad \mathrm{x=a,\,b,\,c}. \quad (9)$$

Subdiving the zero-sequence voltage into a third-harmonic component $v_{\mathrm{o},3}$ related to the selected modulation strategy and an additional component δv_{o} for control purposes, by substituting (9) in (8), the following expression is obtained:

$$I_{\mathrm{m}} = -\frac{6}{V_{\mathrm{dc}}T}\int_{0}^{T/3}\sum_{\mathrm{x=a,\,b,\,c}}(v_{\mathrm{x}}+v_{\mathrm{o},3}+\delta v_{\mathrm{o}})\,|i_{\mathrm{x}}|\,\mathrm{d}t = -\frac{6}{V_{\mathrm{dc}}T}\int_{0}^{T/3}\delta v_{\mathrm{o}}\left(|i_{\mathrm{a}}|+|i_{\mathrm{b}}|+|i_{\mathrm{c}}|\right)\mathrm{d}t. \quad (10)$$

Equation (10) may estimate the average mid-point current generated by adding a constant δv_{o} contribution to all phase voltage references. However, since the instantaneous zero-sequence voltage v_{o} is dynamically limited along the fundamental period, the δv_{o} effectively applied at the output is a function of time. This time-dependent limit is expressed by

$$\begin{cases} v_{\mathrm{o,max}} = \min\left[\dfrac{V_{\mathrm{dc}}}{4}\left(\mathrm{sign}(i_{\mathrm{x}})+1\right) - v_{\mathrm{x}}\right] \\ v_{\mathrm{o,min}} = \max\left[\dfrac{V_{\mathrm{dc}}}{4}\left(\mathrm{sign}(i_{\mathrm{x}})-1\right) - v_{\mathrm{x}}\right] \end{cases} \quad \mathrm{x=a,\,b,\,c}. \quad (11)$$

The zero-sequence voltage injection limits are illustrated in Fig. 4, where an increase in the DC-link voltage value is shown to widen the feasible injection region. Due to these restrictions and considering unity power factor, the shape of the applied δv_{o} depends on the modulation index and the adopted modulation strategy. Nevertheless, since the mid-point voltage control loop must be designed in the worst-case

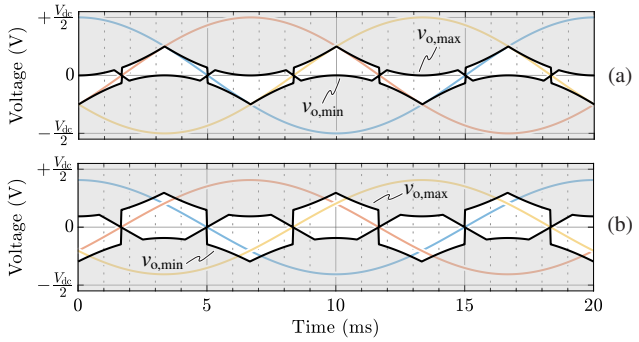


Fig. 4. Zero-sequence voltage limits for $V_{\mathrm{dc}} = 650$ V (a) and $V_{\mathrm{dc}} = 800$ V (b), considering a mains voltage of 400 V line-to-line (i.e. European grid).

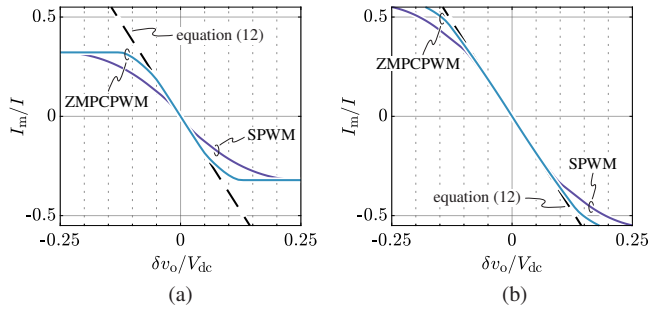


Fig. 5. Mid-point current periodical average for $V_{\mathrm{dc}} = 650$ V (a) and $V_{\mathrm{dc}} = 800$ V (b). Results obtained with sinusoidal modulation (SPWM) and zero mid-point current modulation (ZMPCPWM) are compared to expression (12).

condition (i.e. for maximum open-loop gain), the maximum mid-point current value is of practical interest. Therefore, neglecting the zero-sequence voltage limits, (10) can be solved, obtaining

$$I_{\mathrm{m}} \approx -\frac{12}{\pi}\frac{i_{\mathrm{d}}}{v_{\mathrm{dc}}}\delta v_{\mathrm{o}}, \quad (12)$$

which is an algebraic expression and represents the last relation to practically solve system (4).

It is worth mentioning that equation (12) maintains validity for sufficiently low values of injected δv_{o}. This validity is broadened if a zero-sequence third-harmonic component $v_{3,\mathrm{o}}$ is added to the reference signals. A comparison between the average mid-point current obtained with sinusoidal modulation (SPWM), zero mid-point current modulation (ZMPCPWM) and expression (12) is reported in Fig. 5. ZMPCPWM is adopted in this work, because of the benefits reported in [9].

III. Controller Design

This work considers a 50 kW T-type rectifier switching at 20 kHz, connected to the European low-voltage grid (i.e. 50 Hz, 400 V line-to-line). The converter DC-link voltage can be varied between 650 V and 800 V, in order to narrow the voltage regulation range of the following DC/DC conversion stage. The main parameter values are $L = 150\,\mu$H and $C_{\mathrm{dc}} = 4080\,\mu$F.

A multi-loop control scheme is implemented in digital form, including the DC-link voltage loop, the mid-point voltage balancing loop and the phase current loops in the dq frame, as illustrated in Fig. 6. A standard voltage-oriented control is adopted, synchronizing the d-axis of the rotating dq frame with the peak of the phase voltages measured at the point of common coupling (PCC): the synchronization process is obtained by means of a PLL [13].

A. Phase Current Control Loops

The current control is implemented in the dq frame to achieve zero steady-state reference tracking error and high disturbance rejection capabilities. All three phase currents i_{a}, i_{b} and i_{c} are measured for redundancy reasons, as only two of them are independent, enabling better measurement offset and gain compensations. The d-axis current reference i_{d}^{*} is provided by the outer DC-link voltage control loop, while the q-axis current reference i_{q}^{*} is set to 0 to ensure unity power factor operation.

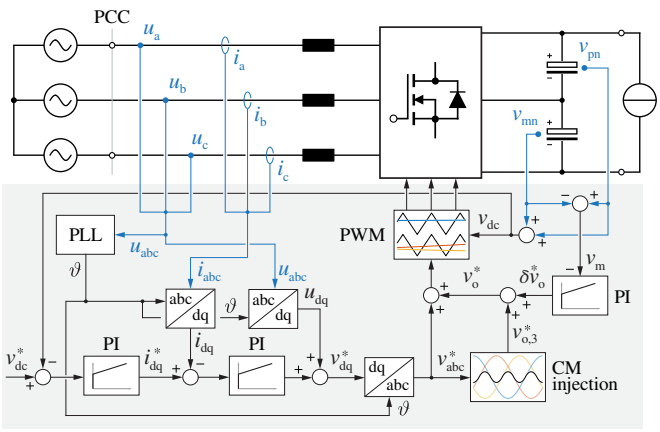


Fig. 6. Simplified schematic of the converter control, including the DC-link voltage loop, the mid-point voltage loop and the dq current loops.

The digital sampling and update is performed once per switching period (i.e. at 20 kHz), however the current feedback values are obtained with an oversampling and averaging process, in order to improve the measurement reliability and thus the control performance around the current zero-crossings, i.e. when discontinuous conduction mode is encountered.

To correctly design the current regulators, the system delays introduced by the digital controller implementation must be taken into account, since each delay reduces the achievable control bandwidth and/or decreases the closed-loop stability margin [14]. The first delay component is generated by the current oversampling and averaging process, which results in a moving-average delay of $T_\mathrm{s}/2$ (where T_s is the sampling period). The second component is directly related to the digital processing, which introduces a one sampling period delay T_s between the measured quantities and the control signal output. Finally, the third component is linked to the PWM modulator, which yields a ZOH effect of one sampling period. Even though the ZOH transfer function is not a pure delay, if the control bandwidth is sufficiently lower than the Nyquist frequency, it may be treated as such (i.e. a $T_\mathrm{s}/2$ delay). Overall, a total delay of $2T_\mathrm{s}$ results in

$$G_\mathrm{d}(s) = e^{-s2T_\mathrm{s}} \approx \frac{1 - sT_\mathrm{s}}{1 + sT_\mathrm{s}}, \tag{13}$$

where a first-order Padè approximation has been adopted to rationalize the exponential transfer function.

By disregarding the disturbance components, the plant transfer functions of the dq currents are derived from (4):

$$G_\mathrm{p,i}(s) = \frac{i_\mathrm{d}(s)}{v_\mathrm{d}(s)} = \frac{i_\mathrm{q}(s)}{v_\mathrm{q}(s)} = \frac{1}{sL}. \tag{14}$$

Even though the integral nature of the plant would ensure a zero steady-state tracking error with a proportional regulator, a proportional-integral (PI) controller is here adopted to achieve better disturbance rejection capabilities, particularly needed to counteract the current distortion around the current zero crossings. The controller transfer function is therefore

$$G_\mathrm{c,i}(s) = k_\mathrm{P,i} + \frac{k_\mathrm{I,i}}{s}. \tag{15}$$

To unburden the integral part of the PI regulator and achieve better dynamical performance, the phase voltages and the current cross-coupling terms are fed forward. The complete current closed-loop control schematic is illustrated in Fig. 7.

Since simplified rational transfer functions have been derived for every subsystem block, a straightforward open-loop transfer function expression is obtained. Therefore, the PI regulators may be tuned employing conventional techniques in the continuous time domain. In the present work, a phase-margin criteria is adopted. If the zero of the PI regulator $\omega_\mathrm{z,i}$ is located sufficiently below the cross-over frequency $\omega_\mathrm{c,i}$, the following relation holds:

$$\omega_\mathrm{c,i} \approx \frac{1}{T_\mathrm{s}}\left[-\tan(m_\varphi) + \sqrt{1 + \tan^2(m_\varphi)}\right], \tag{16}$$

where m_φ is the desired open-loop phase margin. Therefore:

$$\begin{cases} k_\mathrm{P,i} = \omega_\mathrm{c,i}\, L \\ k_\mathrm{I,i} = \omega_\mathrm{z,i}\, k_\mathrm{P,i} \end{cases} \tag{17}$$

If a 60° phase margin is considered, an open-loop cross-over frequency of 850 Hz is obtained, which roughly corresponds to the closed-loop control bandwidth. The PI zero is positioned at one-fifth of this frequency, to improve the disturbance rejection capabilities of the control loop meanwhile ensuring minimum impact on the phase margin.

B. DC-Link Voltage Control Loop

In this battery charger, the AFE DC-link voltage must be controlled according to an optimal reference level provided by the subsequent DC/DC stage. This control loop acts on the d current reference, adjusting the active power absorbed from the mains, in order to balance the load power and regulate the DC-link voltage. Assuming the load current as a disturbance component and $i_\mathrm{q} = i_\mathrm{q}^* = 0$ for unity power factor operation, the plant transfer function is derived from (4) and (5):

$$G_\mathrm{p,v}(s) = \frac{v_\mathrm{dc}(s)}{i_\mathrm{d}(s)} = \frac{3}{2}\frac{v_\mathrm{d}}{v_\mathrm{dc}}\frac{2}{sC_\mathrm{dc}}. \tag{18}$$

Since $G_\mathrm{p,v}$ depends on v_dc, the transfer function is non-linear. Nevertheless, this non-linearity is compensated by control means, multiplying the regulator output with the measured DC-link voltage.

A PI regulator is selected to improve the load disturbance rejection capabilities of the controller, since the load current is generally not known and cannot be fed forward. If the cross-over frequency of the voltage control loop $\omega_\mathrm{c,v}$ is set sufficiently lower than the bandwidth of the current control loop $\omega_\mathrm{c,i}$, the dynamics of the outer and inner loops do not interfere with each other. Therefore, $\omega_\mathrm{c,v}$ is set to $\omega_\mathrm{c,i}/10$,

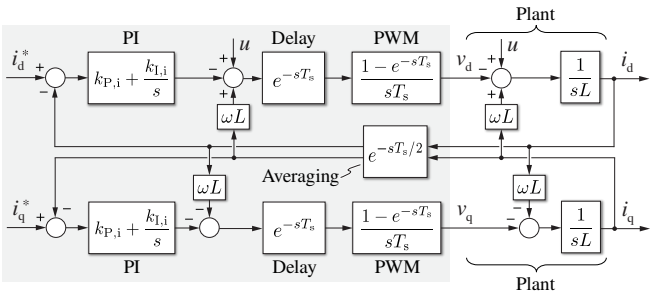


Fig. 7. Complete schematic overview of the i_d and i_q current control loops.

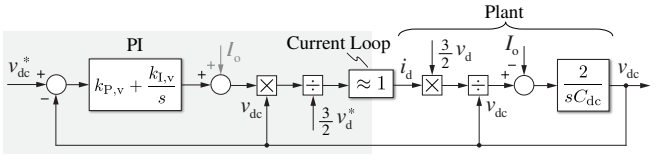


Fig. 8. Complete schematic overview of the v_{dc} voltage control loop.

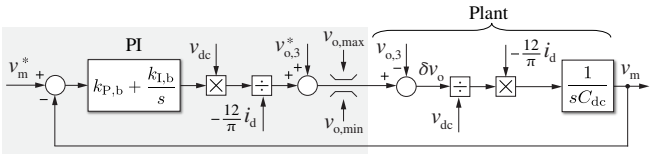


Fig. 9. Complete schematic overview of the v_m voltage control loop.

resulting in a 85 Hz open-loop cross-over frequency. The regulator parameters are derived as

$$\begin{cases} k_{P,v} = \omega_{c,v}\, C_{dc}/2 \\ k_{I,v} = \omega_{z,v}\, k_{P,v} \end{cases} \tag{19}$$

where the PI zero is set to $\omega_{z,v} = \omega_{c,v}/2$. The complete DC-link voltage control schematic is illustrated in Fig. 8.

C. DC-Link Mid-Point Voltage Balancing Loop

Since a voltage unbalance between the split DC-link capacitors may appear in normal operating conditions (e.g. due to device and control non-idealities) or in unbalanced load conditions (e.g. if separate DC/DC units are connected to the upper and lower DC-link halves as in [12]) a voltage balancing loop is required in 3-level inverters/rectifiers. The DC-link mid-point voltage control is achieved by acting on the common-mode voltage injection level, which modifies the mid-point current periodical average, as explained in Section II. As the zero-sequence voltage has no effects on the AC-side currents or on the power transfer, in a first approximation the mid-point voltage loop does not interfere with the other control loops. The plant transfer function is thus derived from (4) and (12):

$$G_{p,b}(s) = \frac{v_m(s)}{\delta v_o(s)} = -\frac{12}{\pi}\frac{i_d}{v_{dc}}\frac{1}{sC_{dc}} \tag{20}$$

Since $G_{p,b}$ depends on other state variables, these are actively compensated in the forward loop to maintain stable controller dynamics for all operating conditions.

As the mid-point voltage is generally characterized by a 150 Hz ripple component with an amplitude dependent on the modulation strategy [9], the balancing loop cross-over frequency $\omega_{c,b}$ is set one decade lower (i.e. 15 Hz). To achieve improved dynamical performance, a PI controller is adopted and its zero is set to $\omega_{z,b} = \omega_{c,b}/2$:

$$\begin{cases} k_{P,b} = \omega_{c,b}\, C_{dc} \\ k_{I,b} = \omega_{z,b}\, k_{P,b} \end{cases} \tag{21}$$

The complete mid-point voltage balancing schematic is illustrated in Fig. 9.

IV. Simulation and Experimental Results

A system simulation is set up in PLECS environment, adopting a custom C-code script for the control strategy implementation. To accurately simulate the discretized nature of digital systems, the control execution is triggered once every sampling period T_s (i.e. $f_s = 20$ kHz), while the control outputs are made available at the next trigger instant. As a further note, the current oversampling and averaging process operates with 32 samples per period.

To verify the small-signal behavior of the designed control loops, all closed-loop transfer functions are obtained by simulation. The results are illustrated in Fig. 10, where they are compared with the corresponding analytical transfer functions derived from Section III. An excellent match between simulated and analytically-derived expressions is observed for all control loops, providing a first validation of the proposed controller design procedure.

To test the system stationary operation and its large-signal dynamical response, a HIL environment is set up, consisting of a PLECS RT Box, simulating the AFE system of Fig. 2 in real-time (3 µs update time), and a customized STM32G474VE microcontroller unit (MCU) board, which implements the multi-loop control at 20 kHz and provides the switching signals to the emulated converter.

The measured HIL phase and mid-point current waveforms with $i_d^* = 100$ A are reported in Fig. 11(a). The impact of the integral part of the PI controller is demonstrated by observing the currents generated with a purely proportional regulator in

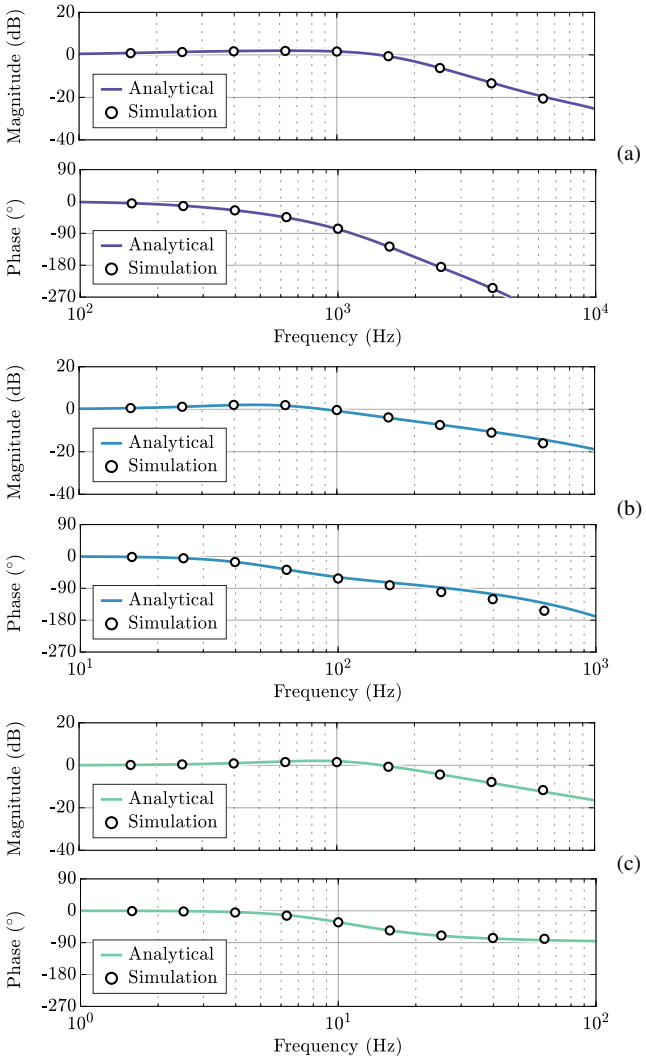


Fig. 10. Analytically derived and simulated closed-loop transfer functions of the i_{dq} current control loop (a), the v_{dc} voltage control loop (b) and the v_m voltage control loop (c).

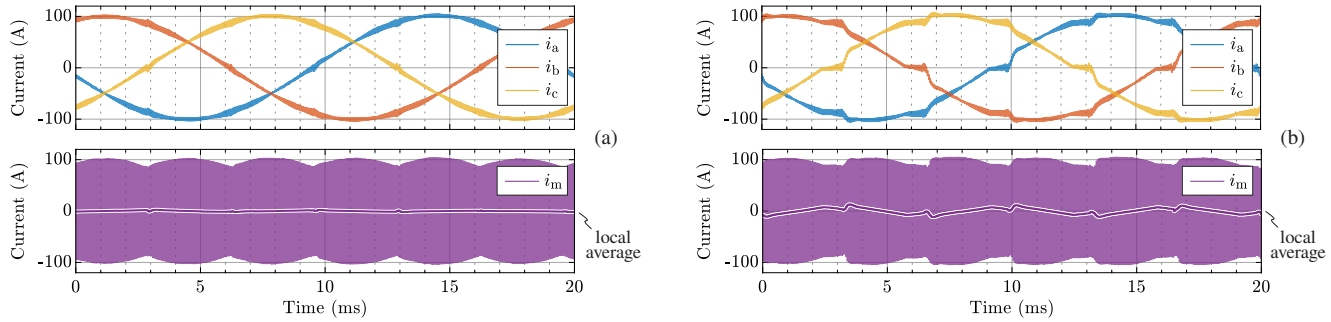


Fig. 11. HIL phase and mid-point current waveforms in stationary operating conditions ($I = 100\,\mathrm{A}$), with a PI regulator (a) and with a P regulator (b).

Fig. 11(b). In this case, a high distortion around the current zero crossings is present, since the low-frequency gain of the current control loop is insufficient. Moreover, the mid-point i_m current shows an effective zero local average (i.e. due to ZMPCPWM) only when the PI is adopted.

Fig. 12(a) shows the i_d control loop response to a reference step from $50\,\mathrm{A}$ to $100\,\mathrm{A}$, resulting in a rise-time of $0.3\,\mathrm{ms}$ and a $\approx 35\,\%$ overshoot. It is worth noting that i_d is discretized in time, since it is calculated once per control period (i.e. $50\,\mu\mathrm{s}$), and it is measured at the output of one of the MCU 12 bit digital-to-analog converters (DAC), hence it is rescaled. A substantial noise is visible, due to the small voltage scale of the DAC output (0 - $3.3\,\mathrm{V}$).

The main dynamical requirement of the DC-link voltage control loop is to minimize the voltage drop following a load step. The closed-loop response to a load step from $50\,\%$ to $100\,\%$ of the rated load is reported in Fig. 12(b). A maximum voltage drop of $\approx 25\,\mathrm{V}$ is observed, mostly counteracted by the integral part of the controller.

Ultimately, the dynamical performance of the mid-point voltage balancing control loop is illustrated in Fig. 12(c), where the loop response to a voltage unbalance of $50\,\mathrm{V}$ is shown, resulting in a rise-time of $18\,\mathrm{ms}$ and a $20\,\%$ overshoot.

Due to the close correspondence between analytical and HIL waveforms, the multi-loop control strategy and controller design procedure can be considered successfully verified.

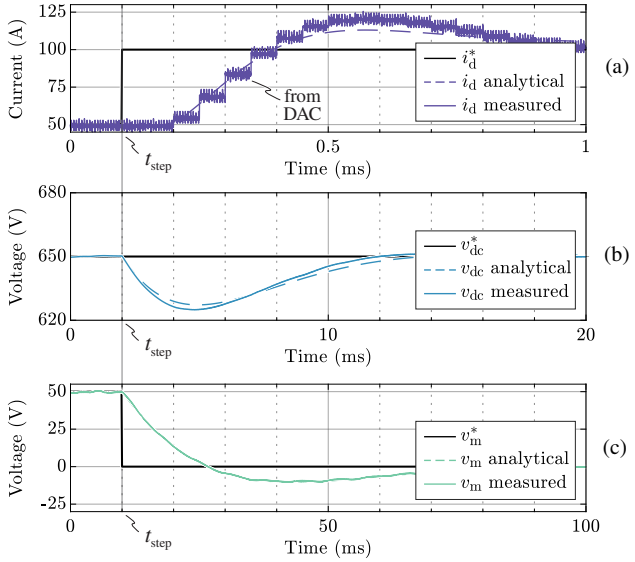


Fig. 12. HIL measured d-axis current response to a reference step (a), DC-link voltage response to an output load step (b) and mid-point voltage response to a reference step (c). t_step indicates the step time instant.

V. Conclusion

This work has presented a digital multi-loop control strategy for a 3-level unidirecitonal rectifier targeting EV UFC applications. The system state-space model has been derived and exploited to analytically design and tune the loop controllers (i.e. i_d, i_q, v_dc and v_m). The dynamical performances of each loop have been verified by means of simulation and HIL implementation, including the analysis of the closed-loop small-signal transfer function in the frequency domain and the large-signal step-response in the time domain.

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