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Re-thinking Analog Integrated Circuits in Digital Terms: A New Design Concept for the IoT Era

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***Abstract*—A steady trend towards the design of mostly-digital and digital-friendly analog circuits, suitable to integration in mainstream nanoscale CMOS by a highly automated design flow, has been observed in the last years to address the requirements of the emerging Internet of Things (IoT) applications. In this context, this tutorial brief presents an overview of concepts and design methodologies that emerged in the last decade, aimed to the implementation of analog circuits like Operational Transconductance Amplifiers, Voltage References and Data Converters by digital circuits. The current design challenges and application scenarios as well as the future perspectives and opportunities in the field of digital-based analog processing are finally discussed.**

***Index Terms*—Digital-based analog processing, Analog and Mixed Signal Circuits, Dyadic Digital Pulse Modulation (DDPM), Digital-to-Analog Converter (DAC), Virtual Voltage Reference, Digital Operational Transconductance Amplifier (DIGOTA), Relaxation DAC (ReDAC).**

I. Introduction

THE Internet of Things (IoT) is the vision of the world in which integrated circuits (ICs) are embedded in everyday life objects for gathering, processing, and exchanging useful information. The design of cubic-centimeter down to cubic-millimeter-scale [1], energy autonomous, pervasive sensor nodes envisioned in the IoT paradigm [2], however, raises stringent constraints on IC area (sub mm^2), average power budget (from the low microWatt down to nanoWatt scale for nodes operated by tiny batteries or energy harvesters) and cost.

The IoT requirements are particularly difficult to be met for analog interfaces, which do not take advantage of CMOS geometrical scaling [3–5] and face specific design challenges due to the poor analog features of nanoscale transistors (as the feature size is shrunk from 0.5 μm to 22nm node, the transistor intrinsic gain drops from 180 to 6 V/V, while the transistor f_T increases by 25X, from 16 GHz to 400 GHz) [4] and to the reduced signal swing at sub-1V power supply voltage.

These drawbacks entirely offset the potential benefits of scaling in terms of reduced parasitics and negatively impact on area, performance, energy efficiency, and especially on design effort of analog cells in advanced technology nodes. In view of that, there has been almost no net power advantage [3] and no area reduction in analog cells like Operational Transconductance Amplifiers (OTAs) or bandgap references when moving from older to more recent technologies [5].

Last, but not least, analog ICs are characterized by a limited reconfigurability and portability across technology nodes compared to digital ICs, and require a significant time and effort in design, transistor-level optimization, simulation, full-custom layout, physical verification and prototyping [4], [6].

In view of these limitations, there has been a strong research interest towards the implementation of traditionally analog blocks by digital friendly and digital intensive replacements in the last years, which can be also observed in the number of CAS Transactions papers on related topics reported in Fig.1, which are more than doubled in the last decade.

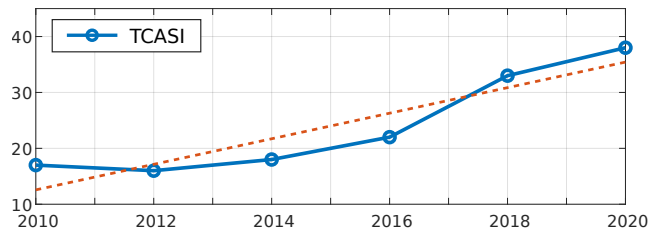

Fig. 1. Digital intensive analog/RF building block published in TCASI transactions over the last 10 years.

Following this trend, fully digital phase-locked loops (PLLs) [7–9], synthesizable A/D converters (ADCs) based on successive approximation registers (SARs) [10–12] and on domino-logic [13], stochastic flash ADCs [14], [15] and VCO-Based ADCs [16–23] have been proposed, extensively investigated and are increasingly employed in applications. Highly digital D/A converters (DACs) [24–28], voltage comparators [29–31], oscillators [32], low-dropout regulators (LDOs) [33–38], buck converters[39], [40], filters [41], [42], voltage references, [43–45], temperature sensors [46] and OTAs [47–52] have also been proposed. This trend can be noticed not only at block-level, but also at system-level, considering that mostly-digital RF transmitters [53–57], receivers [7], [58], [59], and biomedical front-ends [60], [61] have also been introduced.

While most of the above solutions address the challenges of analog interfaces by more "digital friendly" analog cells based on traditional design concepts [62], the possibility to implement analog functions with true digital circuits, which fully take advantage of scaling and of the benefits of a digital design flow, is also emerging as a promising alternative and will be specifically covered in this tutorial brief.

After a general background on information representation and processing in Section II, the implementation of the functions of OTAs, voltage references, and DACs will be covered in section III revealing that digital-based analog building blocks can take advantage of CMOS scaling with minimal design effort. Finally, the current design challenges in digital-based analog processing, new perspectives and application scenarios are discussed in Section IV, and some concluding remarks are drawn in Section V.

II. Information representation and design flow

Despite the intrinsically analog and smooth perception of our surrounding environment, stated with Leibniz's words

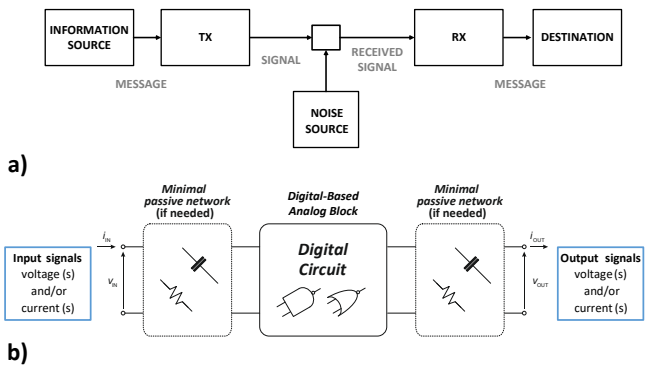

Fig. 2. a) Block diagram of a communication channel [64]. b) Block diagram of digital-based analog block.

as *"Natura non facit saltus"* (*"Nature does not jump"*), the achievements of science and technology in the last two centuries have extensively shown that, at an in-depth analysis, what appears to be continuous proves to be discrete in a variety of forms: matter is indeed composed by atoms, and all fundamental physical quantities from electric charge to electromagnetic field and angular momentum are also quantized.

Not only the inanimate world proves to be discrete, but also in animals and in humans information is processed and transmitted as discrete pulses, as discovered and modeled by Hodgkin and Huxley [63]. Then, we may conclude that our everyday life analog feeling is based on an underlying discrete structure.

Moreover, as shown by C.E.Shannon in his groundbreaking work [64], *information* is discrete in itself. In a channel with bandwidth B and background noise power N (Fig. 2a), which could be regarded, in wide sense, as a model of any information transmission and processing equipment, under a fixed signal power budget S, the maximum amount of information that can be reliably transferred in the unit time (expressed in bit/s) is finite and upper-bounded by the capacity $C = B\log_2(1 + S/N)$ of the channel [64], no matter if analog signals, whose value at each time instant is a real number and - as such - is expected to carry in theory an infinite amount of information, or digital signals are adopted.

In practice, the amount of information that can be transferred over the channel by analog means proves to be much less than the theoretical limit C, whereas, by digital encoding, the Shannon limit can be almost achieved [65]. The full awareness and understanding of this result and its application in information and communication systems have paved the way to the "digital revolution", which has been so profoundly impacting our lives and technology [66], [67].

Shannon's results, however, do not apply just to computers and communication networks. Actually, they also suit any kind of information, including information processed in sensors, actuators, interfaces, and analog circuits like OTAs and voltage references. This consideration suggests that even these circuits could take advantage of a better awareness of the discrete nature of information, and that digital circuits can possibly perform their functions.

Looking at Fig. 1, indeed, it is reasonable to state that a "digital revolution" in analog blocks is now happening, and it can be clearly observed in two common threads, which can be noticed in recent publications.

The first, is the effort in moving information processing from the amplitude to the time domain [20], [21], [68–71], which has an intrinsic advantage in nanoscale CMOS where timing resolution, as opposed to amplitude resolution, is steadily increasing in more advanced nodes, due to the smaller delays of digital gates (the fan-out-of-4 (FO4) delay of an inverter has decreased by from 140ps (0.5μm) to 6ps (22nm node), i.e. by 23X [4]).

The second, is the effort aimed to extend digital automated design techniques to analog and RF systems. Although promising semi-automatic analog design techniques like procedure-based layout generation and optimization-based layout synthesis have been proposed in the last years [72], the synthesis-friendly analog circuits that use the existing digital flow tools for designing seem to be the most attractive ones.

These two threads, indeed, are closely related to each other - since analog circuits based on time-domain information processing are inherently more suitable to automated synthesis, and the functional/logical decomposition and abstraction required for automated design naturally lead to time-domain, algorithmic processing - and both converge towards the implementation of the functions of analog circuits by *true digital circuits*, as illustrated in Fig.2b, i.e. circuits in which information is internally processed in the form of two-level digital signals (i.e. *without* using digital gates as analog amplifying stages, as in [73]), possibly preceded and/or followed by minimal, non-critical, passive networks, that can grasp relevant information from any finite-amplitude, band-limited input signals (voltages and/or currents), and can generate the desired band-limited output voltages/currents at a pre-fixed degree of accuracy.

III. Digital-Based Analog Building Blocks

In this section, the possibility to translate into digital the functions of fundamental analog building blocks like OTAs, voltage references and data converters following the paradigm in Fig.2b, which has been recently explored, will be reviewed with reference to four digital-based analog circuit topologies presented in the last years.

A. Digital-Based analog differential circuit

In [50], the possibility to translate into digital the operation of an MOS differential pair has been explored. In a traditional MOS differential pair [74], as shown in Fig. 3a, the Common-Mode (CM) signal is tracked by node V_S, and is subtracted from the external inputs in the gate-source voltages of the input devices, so that the control voltages of the input devices are CM-voltage independent and their drain currents are proportional to the differential mode input v_d [75]. In [50] it has been shown that a similar behavior can be obtained by using two digital buffers to sense the analog input signal (Differential-Mode (DM) *Amplifer* in Fig. 3b), and operating two three-state buffers according to their digital outputs OUT = (OUT+, OUT−), which can take four values: 11, 00, 10, 01. Fig. 3c shows explicitly the relationship between each

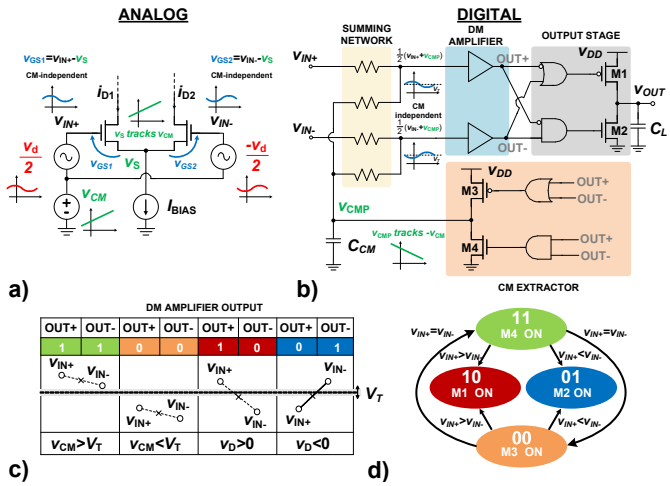

Fig. 3. a) Analog NMOS differential pair b) DIGOTA schematic proposed in [50] and its integrated version in [48], [49]. (c) Relationship between each state (OUT+,OUT−) and the voltage level of the inputs (v_{IN+},v_{IN-}). (d) DIGOTA state transition diagram.

state and the voltage level of both inputs (v_{IN+},v_{IN-}) referred to the buffer trip point (V_T).

Whenever OUT is 10, in fact, it can be concluded that $v_d > 0$ and similarly, OUT = 01 implies that $v_d < 0$ and the three-state output stage can be driven accordingly so that to charge or discharge the output capacitor. On the other hand, for OUT = 00 or OUT = 11, no information of the differential input can be obtained, but it can be concluded that the CM input is below or above the trip point of the buffers and this can be exploited to generate a compensation signal, to be added to the external inputs so that bring their CM component close to the buffer trip point, at which they are sensitive to the differential input.

This is indeed similar to what happens in the differential pair of Fig.3a in which V_S tracks the CM signal and removes it from the input signal through the *summing network* [50]. This digital CM cancellation generates an internal self-oscillation within the DIGOTA where all the logic gates works digitally decreasing considerably the total power consumption (no DC bias). Fig.3d reveals the state transition diagram of the DIGOTA in the function of the inputs, where the transition moments occur obeying the V_T-crossing events dictated by its intrinsic self-oscillation (no external clock is needed).

A proof-of-concept DIGOTA was first implemented by off-the-shelf components in [50] and simulations results for an integrated version of the same architecture were presented in [48], [49]. However, issues such as mismatch and intrinsic -6dB loss from the summing network limit the circuit robustness under Process-Voltage-Temperature (PVT) conditions requiring then static or dynamic calibration [76].

Recently, such issues have been substantially mitigated by replacing the passive summing network by Muller-C elements [47] revealing state of the art energy efficiency figures of merit $FOM_S = GBW \cdot C_L/\text{Power}$ and $FOM_L = SR \cdot C_L/\text{Power}$ for ultra low voltage applications. Even more interestingly, unlike in traditional OTAs, both FOM_S and FOM_L have been shown to increase in finer technology nodes [47], [48], as expected in view of the digital nature of the circuit.

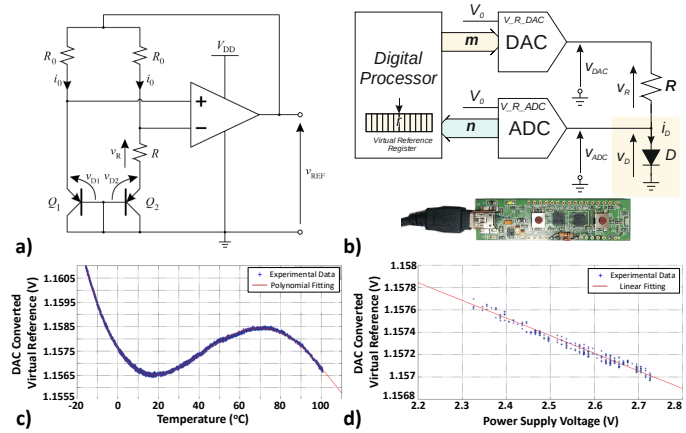

Fig. 4. a) Kuijk's Bandgap voltage reference. b) Microcontroller-based proof of concept prototype c) V_{REF} vs. temperature d) V_{REF} vs. V_{DD} [43].

B. Virtual Voltage Reference Concept

Reference voltages and currents which are insensitive to PVT variations are essential building blocks in ICs and are often generated by bandgap references, like Kujik's circuit in Fig. 4a [77], taking advantage of the complementary-to-absolute-temperature (CTAT) thermal drift of a forward voltage v_D of a silicon *pn* junction biased at a constant current density and of the proportional-to-absolute-temperature (PTAT) drift of the voltage difference $\Delta v_D = v_{D1} - v_{D2}$ of two *pn* junctions biased at different current densities, so that to get a first-order temperature independent reference voltage

$$v_{REF} = v_D + \chi \Delta v_D \tag{1}$$

for an appropriate value of χ (equal to the ratio R_0/R_1 in the Kujik circuit in Fig. 4a).

Aiming to translate the above operation into digital, the virtual voltage reference concept has been introduced in [43], [78]. A virtual voltage reference is defined in a microprocessor (μP)-based system including a DAC and an ADC, both referenced to a possibly inaccurate and PVT dependent pseudo-reference V_0, as shown Fig.4b. In this system, a virtual voltage reference is defined as the binary number r, which depends in general on PVT, that, if converted by the DAC referenced to the pseudo-reference V_0, gives an output voltage V_{REF} which is PVT-independent within 1 LSB of the DAC resolution.

To get r, the behavior of a bandgap circuit can be translated into an algorithm to be run by the μP fed by the ADC acquisitions of a physical voltage. With reference to the digital platform in Fig.4b, in order to get a temperature independent V_{REF}, a diode, used as physical standard, is biased through a resistor R by the output voltage of the DAC. By converting two different values $m^{(1)}$ and $m^{(2)}$ into analog by the DAC, indeed, the diode is biased at two different current densities and its forward voltages are acquired and converted into the binary numbers $n^{(1)}$ and $n^{(2)}$ by the ADC referenced to V_0, so that, neglecting quantization error, $n^{(i)} = v_D^{(i)} 2^N / V_0$ where $i \in \{1, 2\}$ and N is the DAC resolution.

As in Kuijk circuit and in other bandgap references (including MOSFET-only references [79]) an appropriate weight $\chi^\star$,

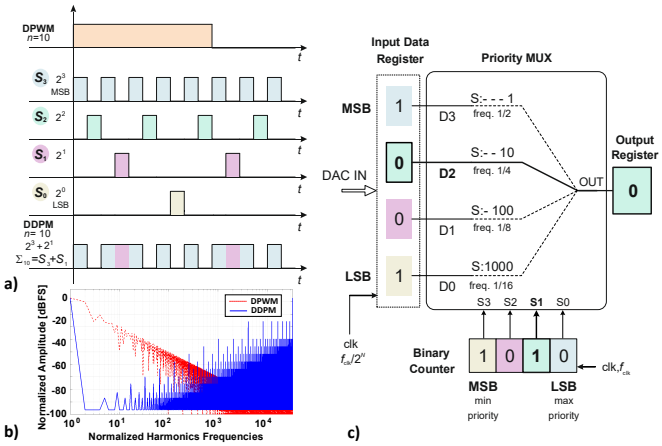

Fig. 5. a) DDPM and DPPM waveforms for $N = 4$ and $n = 10$ [24] b) DPWM vs. DDPM spectrum for a input word ($n = 29365$) and resolution ($N = 16$ bits) [76] c) Priority multiplexer hardware [24].

can be found to balance the CTAT behavior of $v_{\mathrm{D}}^{(1)}$ and PTAT behavior of $v_{\mathrm{D}}^{(2)}$-$v_{\mathrm{D}}^{(1)}$ so that the voltage

$$v_{\mathrm{REF}} = v_{\mathrm{D}}^{(1)} + \frac{\chi^{\star}}{\log h}\left(v_{\mathrm{D}}^{(1)} - v_{\mathrm{D}}^{(2)}\right) \tag{2}$$

where $h = \frac{m^{(1)}-n^{(1)}}{m^{(2)}-n^{(2)}}$, is first-order temperature independent. In a virtual voltage reference, however, v_{REF} is not obtained by summing physical voltages, but its definition in (2) is exploited to evaluate the virtual voltage reference r.

By expressing $v_{\mathrm{D}}^{(1)}$ and $v_{\mathrm{D}}^{(2}$ in (2) in terms of the ADC acquisitions $n^{(1)}$ and $n^{(2)}$, in fact, one gets that (2) can be expressed as

$$v_{\mathrm{REF}} = \left[n^{(1)} + \chi\frac{\log h^{\star}}{\log h}\left(n^{(1)} - n^{(2)}\right)\right]\frac{V_0}{2^N} = \frac{V_0}{2^N}r \tag{3}$$

where the quantity in the square brackets, which can be calculated algorithmically inside the digital processor, can be immediately identified as the virtual voltage reference and can be possibly converted into analog by the DAC in Fig.4b. An effective temperature coefficient $TC_{\mathrm{eff}} = 18\mathrm{ppm}/^{o}\mathrm{C}$, Fig. 4c, and line sensitivity $LS = 0.15\%/V$, Fig. 4d, have been achieved by this approach in a microcontroller-based proof of concept prototype.

Since processing is moved to the digital domain in a virtual reference circuit, this approach is well suited to implement complex, high order temperature-compensation strategies, which would not be suitable to an analog implementation, and it has been adopted indeed in a precision virtual voltage reference which achieves a measured $TC_{\mathrm{eff}} = 5\,\mathrm{ppm}/^{o}\mathrm{C}$ [78]. Two years after, a circuit based on a similar approach has been implemented on silicon [44] achieving a $TC_{\mathrm{eff}} = 18\,\mathrm{ppm}/^{o}\mathrm{C}$ which is fully in line with the results obtained by the microcontroller based prototype.

C. Highly Digital DAC

Bitstream D/A conversion is a key enabling concept for digital-based analog processing, since it can be directly adopted in digital-based analog blocks in Fig.2b to implement analog outputs and also analog inputs, when used in a feedback configuration with a gate-based comparator [11].

In this framework, Digital Pulse-Width Modulation (DPWM) [80], [81] and single-bit sigma-delta ($\Sigma\Delta$) [82], [83] are well known bitstream D/A conversion techniques: single-bit $\Sigma\Delta$ is suitable to achieve high resolution thanks to noise shaping, but it is not well suited to DC conversion, it requires rather complex digital hardware and careful design is needed to avoid stability issues and idle tones. Digital PWM, by contrast, requires very simple digital HW and does not suffer of stability issues, but it poses stringent requirements on the output filter, since most of the spurious spectral content of DPWM signals is close to the baseband. In view of these limitations, two new D/A conversion techniques, the Dyadic Digital Pulse Modulation (DDPM) and Relaxation Digital to Analog Converter (ReDAC) have been recently proposed to address the demand for ultra low-cost and energy efficient D/A conversion in digital-based analog interfaces for the IoT.

1) Dyadic Digital Pulse Modulation: The DDPM modulation proposed in [24] associates to a digital input code n on N bits, expressed in terms of its binary representation $B_n[N-1:0] = (b_{N-1}, b_{N-2}, \ldots, , b_1, b_0)$ as $n = \sum_{i=0}^{N-1} b_i 2^i$, the periodic bitstream

$$\Sigma_n(t) = \sum_{i=0}^{N-1} b_i S_i(t) \tag{4}$$

obtained by superposition of orthogonal dyadic basis signals (ODBSs) $S_i(t)$ ($i = 0, \ldots, N-1$) shown in Fig.5a for N=4, which are non-overlapping, periodically repeated digital streams of 2^N clock cycles, organized so that S_{N-1} is high (i.e. at V_{DD}) every other clock cycle (i.e., in 2^{N-1} cycles per period), S_{N-2} is high every other cycle in which S_{N-1} is low (i.e., in 2^{N-2} cycles), S_{N-3} is high every other cycle in which both S_{N-1} and S_{N-2} are low (i.e., in 2^{N-3} cycles per period) and so on, till S_0, which is high just in one cycle per period, as shown in Fig.5a. Being ODBSs S_i non-overlapping and high in 2^i clock cycles per period, DDPM streams Σ_n defined in (4) are high for exactly n clock cycles per period and their time average is therefore $n/2^N V_{\mathrm{DD}}$, as observed in the same Fig.5a, where the construction of a DDPM stream by superposition of ODBSs is illustrated for $n = 10$.

In practice, DDPM streams can be generated by a priority multiplexer [24], i.e. a tiny digital hardware as in DPWM, but they show much more favorable spectral features compared to DPWM as shown in Fig.5b. This is due to the fact that ODBS related to the $i-th$ MSB are by construction periodic with a frequency 2^{N-i} times higher than the fundamental. Other than in baseband D/A and A/D conversion [11], [24], [27], the favorable spectral properties of DDPM have also been exploited in band-pass D/A conversion [54] and in digitally controlled switching mode power converters [84] to avoid the onset of limit cycle oscillations.

2) Relaxation DAC: A Relaxation DAC [85], whose principle schematic is shown in Fig.6a exploits the time response of a first-order RC network driven by the bitstream corresponding to the digital input code (LSB-first) by a shift register operated at clock cycle T, to perform D/A conversion. After the conversion of the MSB of the input code is completed, the

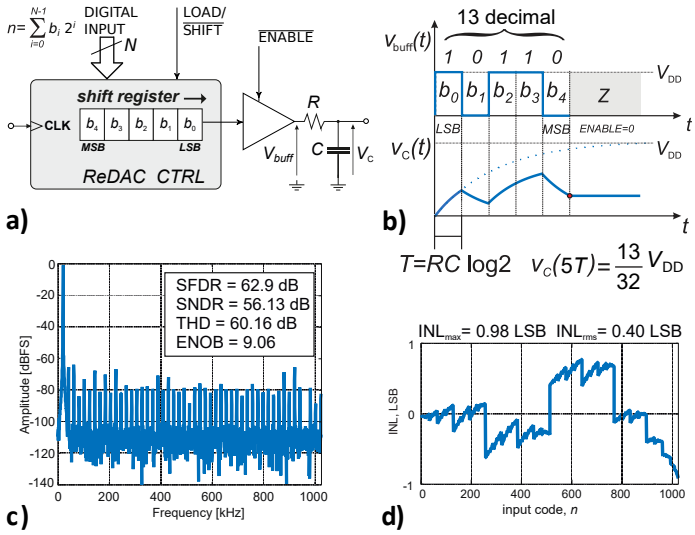

Fig. 6. a) ReDAC converter [85] b) ReDAC conversion waveforms example [85] c) Self-calibrated ReDAC dynamic performance at 20kHz, 90% swing [26]. d) Self-calibrated ReDAC INL

voltage across the capacitor of the *RC* network, which is in general expressed by first-order linear transient analysis as:

$$v_C(NT) = V_{DD}\left(1 - e^{-\frac{T}{\tau}}\right) \cdot \sum_{i=0}^{N-1} b_i e^{-\frac{(N-i-1)T}{\tau}} \tag{5}$$

becomes just

$$v_C(NT) = \frac{V_{DD}}{2^N} \sum_{i=0}^{N-1} b_i 2^i \tag{6}$$

provided that the relation $T = \tau \log 2$ between the clock period T and time constant $\tau = RC$ is satisfied. Fig. 6b shows the ReDAC conversion waveform example for $N = 5$ and $n = 13$.

The condition $T = \tau \log 2$, can be imposed by tuning the clock period so that to enforce the equality of the ReDAC output voltages corresponding to $2^{N-1} - 1$ and 2^{N-1} inputs at a conveniently high resolution, since the maximum INL error always appears between these two codes and it is found to be proportional to the relative timing error ($\mathrm{INL_{max}} \simeq 2^{N-1} \log 2 \cdot \frac{\Delta T}{T}$, where $\Delta T = T - \tau \log 2$). A 2MS/s, 10bit ReDAC featuring digital background self-calibration achieves less than 1LSB of $\mathrm{INL_{max}}$ and $\mathrm{DNL_{max}}$ and 9.06 ENOB (Fig. 6c,d) [85].

With respect to switched-capacitor DACs, a ReDAC is matching-insensitive and its operation relies on a single parameter to be calibrated. As a consequence the ReDAC capacitance can be chosen close to the thermal noise limit, thus enabling ultra-low energy per conversion of 0.73pJ/conv at 2MS/s, as demonstrated in post-layout simulations [86] performed in 40nm CMOS technology of a 10bit ReDAC occupying an area of $910\mu m^2$. These features make the ReDAC concept very well suited to IoT applications.

IV. Challenges and future opportunities

The feasibility of all-digital and mostly digital implementations of analog interfaces has been conceptually proven and demonstrated on silicon over the last decade, revealing significant advantages in terms of area and power compared to more traditional approaches, as show in Fig. 7 for ADC [24], DAC [27], OTA [47], voltage reference [43] and oscillator [32]. Such solutions are now mature enough to address the requirements of a number of applications in the IoT field, and have been already adopted in fact in systems like frequency synthesizers [8], [9], biomedical signal acquisition front-ends [60], [87] and smart sensors [46], [88–90], achieving relevant performance. Their potential in applications, however, is far from being fully exploited and it could be expected that, in a foreseeable future, general-purpose, fully synthesizable and re-configurable digital architectures with direct sensing and actuator driving features can be developed to target an increasing number of applications.

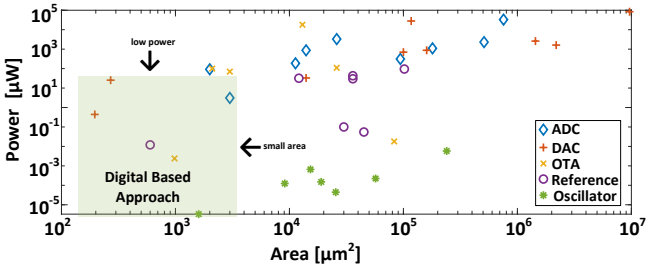

Fig. 7. Power vs Area for for ADCs [24], DACs [27], OTAs [47], voltage reference [43] and oscillators [32].

At the same time, it should be observed in most of the cases the performance of digital-based implementations of analog interfaces is not yet competitive with the best traditional analog implementations in the state of the art (e.g., digital-based OTAs show lower DC gain and common-mode rejection, standalone DDPM DAC and ReDAC bandwidth and effective resolution should be enhanced, just rather elementary virtual references have been demonstrated so far). This is reasonable considering that most of such techniques have been proposed only in the last ten years and are still in their childhood, whereas traditional analog ones have been constantly refined and improved over the last 60 years. By the way, considerations on the discrete nature of information lead to conclude that there is no fundamental limit in digital-based analog processing compared to traditional analog approaches.

Since digital-based analog circuits process the signal in time-domain and time resolution improves as technology scale, any improvement in digital technology makes it reasonable to expect that the performance gap with traditional analog implementations can be rapidly filled in the next few years.

V. Conclusion

The current trend in CMOS digital-based analog circuit design over the last decade and its foundations have been reviewed in this tutorial brief, with a special emphasis on the implementation of analog functions by fully digital circuits. Under this perspective, digital-based OTAs, virtual voltage references and bitstream DDPM and Relaxation DACs proposed in the last years, have been reviewed, highlighting their suitability to emerging IoT applications. The current challenges of digital-based analog processing and their potential application scenarios have been finally considered and future perspectives have been discussed.

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