POLITECNICO DI TORINO
Repository ISTITUZIONALE

A New Single Event Transient Hardened Floating Gate Configurable Logic Circuit

Original
A New Single Event Transient Hardened Floating Gate Configurable Logic Circuit / Azimi, Sarah; DE SIO, Corrado; Yang, Weitao; Sterpone, Luca. - ELETTRONICO. - (2020), pp. 311-314. (Intervento presentato al convegno 18th IEEE International NEWCAS tenutosi a Montreal, Canada nel June 16-19, 2020) [10.1109/NEWCAS49341.2020.9159844].

Availability:
This version is available at: 11583/2838599 since: 2020-07-07T10:10:47Z

Publisher:
IEEE International NEWCAS

Published
DOI:10.1109/NEWCAS49341.2020.9159844

Terms of use:

This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

Publisher copyright
IEEE postprint/Author's Accepted Manuscript

©2020 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collecting works, for resale or lists, or reuse of any copyrighted component of this work in other works.

(Article begins on next page)

12 October 2024

A New Single Event Transient Hardened Floating Gate Configurable Logic Circuit

Sarah Azimi, Corrado De Sio, Weitao Yang and Luca Sterpone

Dipartimento di Automatica e Informatica
Politecnico di Torino
Torino, Italy

***Abstract*— Radiation-induced soft errors have become a significant reliability challenge in modern CMOS logic. The main concern for safety-critical applications such aerospace is due to Single Event Transient (SET) effects. SETs are exacerbated by the technology scaling of modern technologies especially when they are adopted in harsh environments. This paper evaluates the SET sensitivity of state-of-the-art floating gate configurable logic circuit and proposes a novel methodology for filtering a SET pulse generated inside the logic cells by increasing the charge sharing effect on the sensitive node of a cell due to remapping of its configurable switches. Experimental results, performed with radiation particle simulation on several benchmark circuits implemented in a 130nm floating-gate device demonstrate an improvement in filtering SET effects of more than 24% on the average with negligible delay degradation.**

***Keywords*—Configurable Logic, Transient effects, Logic Element, Charge Sharing.**

I. Introduction

As technology scales, the closeness of transistors along with the reduction of transistor currents and nodal capacitances leads to an increase of vulnerability of circuits to soft errors [1]. Single Event Transient (SET) has been known as one of the most critical soft errors. When a charged particle hits the target device, it may cause a voltage glitch that can propagate, like a normal signal, reaching a memory element, e.g. Flip-Flop. Depending on the arrival time, duration, and amplitude of the SET pulse, it may be sample and corrupts the data stored in the memory cells [2].

The collected charge at a node struck by an ion determines the pulse characteristics, such as the width and amplitude. Moreover, a strong pulse width dependency on the incident particle Linear Energy Transfer (LET) has been observed. The mechanisms affecting the SET pulse width include classical drift, diffusion, and parasitic amplification at the struck node [3]. Additionally, it impacts the enhanced parasitic effects in scaled technologies, such as the removal of charge by substrate contacts and the collection effects of neighboring transistors. [4]. In particular, for Floating-gate (e.g., Flash-based) circuits oriented to programmable technologies, the proximity of device nodes results in charge collection in multiple logic switches when a single heavy ion strikes a node. This phenomenon results in different transient pulses related to the LET absorbed by the switch junction.

Several studies have been dedicated to analyzing the effect of charge sharing in recent technologies[4][5][6]. In [6], the authors performed a heavy-ion board-beam experiment on a 130 nm CMOS technology together with 3-D TCAD mixed-mode modeling in 90 nm and 130 nm bulk CMOS which identifies a mechanism for quenching propagated SET pulse due to simultaneous charge collection.

This work has been dedicated to evaluating the effect of radiation-induced SET pulses on a 130 nm configurable logic of Flash-based FPGA and proposing a new SET filtering solution based on charge sharing effect. Furthermore, the exploitation of charge sharing effect for the mitigation of SETs proposed in this paper is not constrained to the specific vendor architecture and can be applied to any circuit configurable through switches based on floating-gate.

The paper has been organized as follows: Section II describes the background regarding the configurable tile known as VersaTile used in Flash-based FPGAs. Section III describes the charge sharing effect on the SET pulse traversing the circuit. Section IV elaborates on the developed workflow for analyzing the sensitivity of an implemented circuit regarding SET considering different switches configuration for the configurable cell. Section V explains the conclusions and future works.

II. Background

The configurable logic circuit consists of gates and routing resources both programmable by turning ON/OFF switches implemented by Floating Gate (FG) transistors. In detail, the FG switch circuit is a set of two NMOS transistors represented in Figure 1. The two transistors share the floating gate, which contains the configuration information of a memory cell.

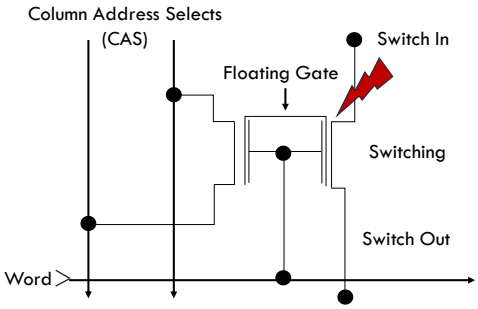

Fig. 1. The Floating-Gate (FG) based Configuration circuitry.

Typically, the whole Configurable Logic Circuit is used to implement N-inputs logic function, a Flip-Flop with clear or reset, and a latch with clear and reset [8]. The routing resources

inside the Configurable Logic Circuit have a different level of hierarchy: ultra-fast local resources, efficient long-line resources, high-speed, and very-long line resources [3]. Considering this resource scenario, a radiation particle can hit both routing and switching resources, in case a particle hits a switch-based transistor in the OFF state, it will provoke a transient SET in the switch configuration, creating a transient pulse or bit-flip in the Configurable Logic Circuit which will be propagated to the subsequent circuit resources depending on its configuration. For each configuration of the Configurable Logic Circuit, the number of FG switches and transistors in the input-to-output path is different. This work has been dedicated to evaluating the sensitivity of the Configurable Logic Circuit resources versus Single Event Transient with respect to the number of used FG switches in the configuration and proposing a new switches configuration of the cell, increasing the charge sharing effect in a sensitive node in order to decrease the sensitivity against SET pulses.

III. The Proposed Mitigation Mechanism

The main goal of the proposed methodology is the generation of an equivalent switches configuration for the Configurable Logic Circuit capable to increase the charge sharing characteristics of each circuit node while keeping the same functionality, which eventually results in reduced sensitivity to SETs. Firstly, it is necessary to consider that Floating-gate based Configurable Logic Circuits are used in various Field Programmable Gate Arrays (FPGAs) devices. As a case study, we focus on the scheme of ProASIC3, a Flash-based FPGA fabricated by Microsemi. However, the concept behind and the methodology can be applied to any configurable switch-based tile.

The ProASIC3 core consists of VersaTile logic cores and routing structures. Each Versatile is programmed by 30 floating-based switches. Different switches configurations of the VersaTile connect the combinational and digital logic gates of the design. In particular, many different switches configurations can configure the VersaTile to the same logic function. In order to have a robust design against radiation-induced SET pulses, we propose a new configuration of the switches of VersaTile cells to maximize the charge sharing effect of each node.

In Figure 2, an example of the configuration of the VersaTile for generating a two-inputs *OR* is illustrated. In this configuration, 16 switches have been used to implement the *OR* logic function, while the rest of the switches do not have any direct effect on the gate truth table. Thus, they can be configured as *1* or *0* without changing the function of the cell. We exploit this feature to increase the charge sharing effect on each logic gate circuit node of the VersaTile. Therefore, the states of the *no-matter* switches have been redefined to maximize the capacitive charge effect of the sensitive locations with the scope of filter any SET pulse traversing the VersaTile cell. In detail, Figure 2 shows the switches that are mandatorily programmed surrounded by a *yellow square*. Differently, the *no-matter* switches, highlighted with a *blue circle,* can have either 0 or 1 configurations without changing the functionality of the logic cell.

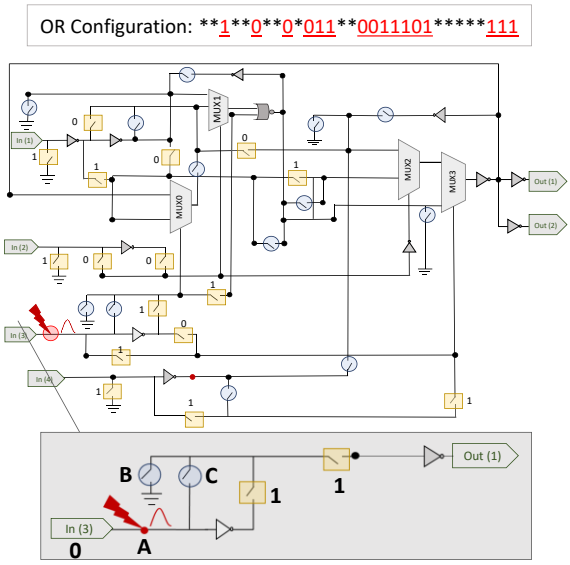

Fig. 2. A Microsemi VersaTile configuring a 2-input OR logic gate.

However, configuring them as 0 or 1 can change the charge of the node by sharing it between several transistors, reducing the amplitude and duration of the SET pulse generated by radiation particles.

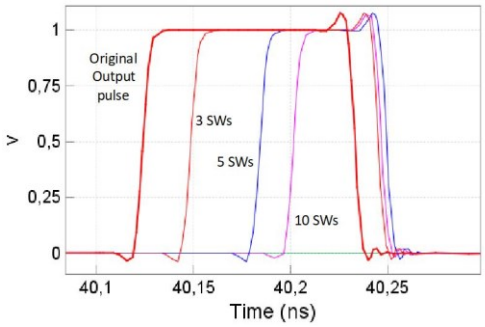

Fig. 3. The output pulse obtained for an OR gate after the introduction of a 250ps transient effect into the input of the VersaTile using the configuration of extra-switches.

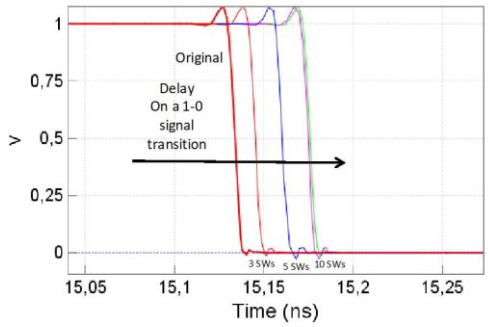

Fig. 4. View of the delay for a 1-to-0 transition of a signal for original configuration and in the case of 3, 5, or 10 extra switches.

Figure 3 represents the output of the VersaTile while a SET pulse with the duration of 250ps is introduced in the input of the VersaTile using the SPICE environment. As can be seen, by increasing the number of programmed switches, the duration of the pulse decreases, leading to the shrinking of the pulse in terms of duration. However, as it is expected, increasing the number of programmed switches increases the delay, as it is represented in Figure 4.

IV. The Radiation Effects Experimental Workflow

In order to evaluate the sensitivity of the circuits implemented on 130nm Floating-gate configurable logic, the workflow represented in Figure 5 is proposed. Firstly, we developed an electrical model of the VersaTile which has been used to generate the GDS-II layout. The generated layout together with the radiation profile is provided to the Geant4 Monte Carlo simulation to perform a radiation analysis and obtain the deposited energy and consequently, the predicted SET pulse durations, represented as *SET Database*. This database is used to perform an electrical analysis of the behavior of a pulse traversing through the VersaTile, evaluating the broadening or filtering effect of the pulse knowing as Propagation Induced Pulse Broadening (PIPB) effect [2] for different switching configurations.

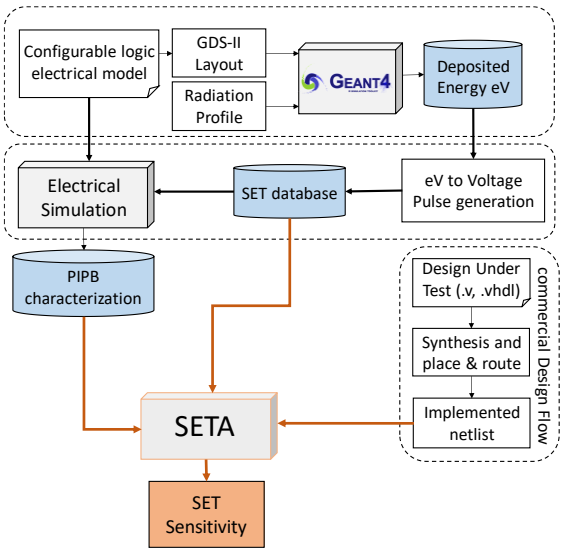

Fig. 5. An Overview of the developed workflow for analyzing the sensitivity of the circuit implemented using 130nm configurable logic.

As a result, the PIPB characterization of the configurable tile for different configuration of the switches are defined. The PIPB characterization is provided to the SETA [9] to perform a SET analysis of different circuits implemented using the 130nm technology model of the Configurable Logic Circuit and reporting the SET sensitivity of the implemented circuits with respect to different switching configuration of the Tiles.

A. Radiation Monte-Carlo Analysis

In order to effectively evaluate the resiliency of the proposed solution, we performed a radiation particle Monte Carlo simulation using the Geant4 toolkit. Gean4 can mimic the transportation and interaction of particles in the device taking into account the material, geometry, and thickness of layers of the physical structure of the device and calculate the deposited energy is each layer [9]. Figure 6 represents the fabric of a Geant4 simulation on 130nm device. We used the Heavy Ion profile related to the UCL facility to perform the radiation analysis [11]. We chose 4 different Heavy Ions with the initial energy reported by UCL to perform the radiation analysis by Geat4. Figure 7 represents the radiation analysis result in terms of the energy deposited in each layer of the device for the chosen ions.

According to the deposited charge for different ions, it is expected to observe SET pulses with a duration between 250 ps to 400 ps in the technology under the study. More details about the prediction of the SET pulse duration with respect to the deposited energy is reported in [12].

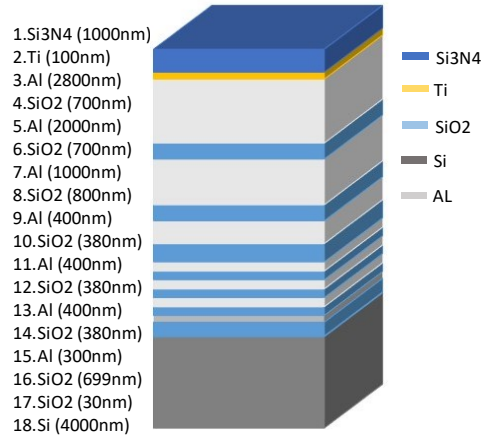

Fig. 6. A z-section of the Circuit Layout used by the Geant4 radiation analysis Simulation Module

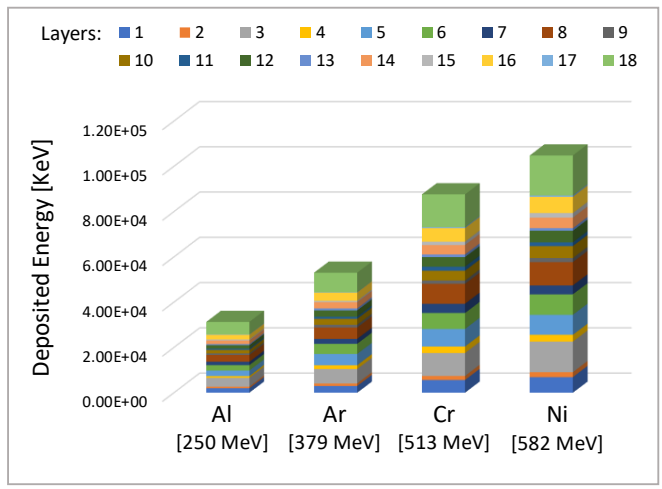

Fig. 7. Deposited Energy in each layer for different Ions analyzed by Geant4

B. VersaTile Model and PIPB Characterization

In order to automatize the model and apply it to different VersaTile configurations, we designed the SPICE model of the ProASIC3 VersaTile. We used the FreePDK physical library tuned at 130nm and adopting the electrical Predictive Technology Model (PTM) of 130nm BISM4 model for bulk CMOS. The model has been designed adopting *Wired-Or* logic node in correspondence of the junctions of the scheme provided by Microsemi and illustrated in Figure 2. The routing segments have been obtained after the place and route process using our internal GDS-oriented Place and Route algorithm. The obtained wire segments length may vary between 200nm and 350nm compared to the original lengths.

We achieved the PIPB effect characterization performing an exhaustive analysis of all possible configuration of floating gate switches for four logic functions such as AND, OR, NOR, and NOT. The obtained characterization is shown in Table I, where

we report the PIPB coefficient versus the number of extra switches configured for the SET pulses less than 400ps as they have identified by the radiation analysis. In detail, we report the original PIPB coefficient and the coefficients obtained with 3, 5, and 10 extra switches configured as *closed*. Please note that a PIPB effect greater than 1 means that the input transient pulse is broadened on the output of the cell. Furthermore, we provided the maximum delay of the new configured cell that for our model accounts to around 51ps for all the different configurations related to 10 extra switches used. The PIPB characterization has been provided to the next stage in order to evaluate the behavior of the circuits implemented on 130nm technology.

TABLE I. PIPB CHARACTERIZATION AND MAXIMUM DELAY

Circuits	Number of Extra Switches / PIPB Coefficients				Maximum Delay [ps]
	Original	3	5	10	
AND	1.18	1.02	0.86	0.79	51.20
OR	1.21	1.01	0.87	0.81	52.18
NOR	1.19	1.02	0.84	0.79	51.22
INV	1.08	0.89	0.70	0.64	48.60

C. SET Sensitivity Analysis

In order to analyze the SET sensitivity of the circuit, we used a SET Analyzer tool (SETA) previously developed. SETA evaluates the propagation of SET pulse considering the PIPB effect. The tool starts with the hardware description of the design (HDL), elaborating the Physical Design Description, extracting the combinational logics, Flip-Flops, and I/O pins. SETA inserts SET pulses reported in the *SET database* in all the inputs and outputs of the combinational logic of the implemented circuit, propagating the pulse until the storage element. During this propagation, SETA takes into account the PIPB characterization previously identified to calculate the duration of the pulse reaching to the storage element of the implemented circuits. Eventually, it reports the static error rate in terms of the number of the FFs which are facing broadened SET pulses with respect to the inserted source SETs. More details about the SETA tool is provided in [9].

TABLE II. CHARACTERIZATION OF THE SELECTED CIRCUITS

Circuits	Logic Type				
	AND	OR	NOR	INVD	FF
B09	8	15	26	33	20
B10	17	39	33	57	24
B11	38	62	143	196	39
B12	86	125	279	382	123
B13	19	40	13	59	50
B14	986	1465	1188	2825	1038

In order to validate the proposed method, we selected circuits with different complexity from the ITC99 benchmark collection [12]. The selected circuits have been implemented on ProASIC3 A3P3000L PQ208 Flash-based, 130 nm technology. Table II reports the characteristic of the implemented benchmark circuit with respect to the number of VersaTile which have been configured as *AND*, *OR*, *NOR,* and *NOT* gates.

TABLE III. ERROR RATE REPORT FOR DIFFERENT FLOATING SWITCH CONFIGURATION FOR ORIGINAL AND MITIGATED

Circuits	B09	B10	B11	B12	B13	B14
Original Error Rate [%]	38.85	38.12	38.46	38.61	36.47	37.71
Mitigated Error Rate [%]	14.43	14.75	14.24	14.81	13.02	13.86

Firstly, we use SETA to evaluate the sensitivity of the implemented circuits with respect to the PIPB characterization for the original configuration of VersaTile and report the static error rate in Table III. Secondly, the SET analysis has been performed for the same circuits but using the PIPB characteristics for mitigated configuration.

V. CONCLUSION AND FUTURE WORK

In this paper, we proposed a method for analyzing the sensitivity Floating Gate Configurable Logic Circuit versus radiation-induced SET pulse and proposing a new switching configuration of VersaTile which is increasing the charge sharing effect in the tiles. A 130nm circuit electrical model of the Configurable Logic Circuit has been developed to perform a PIPB characterization for different switching configurations. Applying the PIPB characterization to analyze the SET sensitivity of real circuits implemented on 130nm technology shows reduction of the effects for 24% on the average.

REFERENCES

[1] A. Dixit, A. Wood, “The impact of new technology on soft error rates”, IEEE International Reliability Physics Symposium, 2011, pp. 5B.4.1-5B.4.7.

[2] V. Ferlet-Cavrois, L. W. Massengill and P. Gouker, "Single Event Transients in Digital CMOS—A Review," in *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp.1767-1790, 2013.

[3] F. Kastensmidt, P. Rech, “FPGAs and Parallel Architectures for Aerospace Applications”, Springer, ISBN 9783319143514, 2016.

[4] Duan Xueyan, Wang Liyun, and Lai Jinmei. “Effect of charge sharing on the single event transient response of CMOS logic gates,” Journal of Semiconductors, vol.32, no.9, Sep. 2011.

[5] Zhang Zhun, He Wei, Luo Sheng, Jianmin Cao and Qingyang Wu, "Research on the influence of charge sharing for SEE locations based on 65nm CMOS technology," 2015 IEEE International Conference on Communication Problem-Solving (ICCP), Guilin, 2015, pp. 257-260.

[6] L. Sterpone, S. Azimi, “Radiation-induced SET on Flash-based FPGAs: analysis and filtering methods”, in 30th International Conference on Architecture of Computing Systems (ARCS), pp. 1-8, April 2017.

[7] J. R. Ahlbin, L. W. Massengill, B. L. Bhuva, B. Narasimham, M. J. Gadlage, “Single Event Transient pulse quenching in advanced CMOS logic circuits”, IEEE Tran. Nuc. Scien., 2009, pp. 3050- 3056.

[8] ProAsic3 Flash Family FPGAs Datasheet.

[9] S. Azimi, B. Du, L. Sterpone, D.M. Codinachs, R. Grimoldi, L. Cattaneo, “A new CAD tool for Single Event Transient Analysis and mitigation on Flash-based FPGAs”,in Integration, vol. 67, pp. 73-81, ISSN 0167-9260, 2019.

[10] S . Agostinelli et al., “Geant4 – a simulation toolkit,“ Nucl. Instr. Meth. A, vol 506, pp.250-303, 2003.

[11] A. O. Akhmetov et al., "IC SEE Comparative Studies at UCL and JINR Heavy Ion Accelerators," 2016 IEEE Radiation Effects Data Workshop (REDW), Portland, OR, USA, 2016, pp. 1-4.

[12] S. Azimi, B. Du, L. Sterpone, “On the prediction of radiation-induced SETs in Flash-based FPGAs,” in Microelectronic Reliability, vol. 64, pp. 230-234, Jul. 2016.

[13] F. Corno, M. S. Reorda, G. Squillero, “RT- level ITC99 benchmarks and first ATPG results”, IEEE Des. Test Comput. 17(3), pp 44-53, Sep. 2000.