Silicon photo-multiplier (SiPM) is a new generation of solid-state photon sensors, invented by Russian scientists during the 1990s, which working principle is based on the operation of photo-diode arrays in Geiger mode. Similarly to the conventional Photon-Multiplier Tube (PMT), a SiPM features a high gain in the same range, high Photon Detect Efficiency (PDE) and excellent time response. On top of that, SiPMs provide important advantages such as low operating voltage, compactness and insensitivity to magnetic fields. Initial drawbacks in terms of high cross-talk, dark count and generally high correlated noise, has been significantly reduced with constant improvements in manufacturing technology. As a consequence, SiPMs became an attractive choice for an increased number of applications in nuclear medicine, high energy and astroparticle physics experiments, automotive (LIDAR) and homeland security.

ASICs (Application Specified Integrated Circuits) have been used in radiation sensor readout for more than 40 years, providing specific solutions in terms of signal amplification, shaping, and digitization. The development of custom integrated electronics for the readout of highly segmented SiPM matrices allowed for the construction of compact photoelectronic modules for detectors implementing aggressive spatial resolution and channel density.

This thesis exploits the development of innovative CMOS integrated electronics for SiPM readout. The versatility of the architecture of the ASICs herein described should allow for the use of these electronics in system-grade detectors for medical imaging, particle and nuclear physics, using both room temperature inorganic (crystal) scintillators or the fast scintillation of compton scattering in novel noble-liquid based PET detectors operating at cryogenic temperatures.

This manuscript provides detailed description, analytical depiction and silicon characterisation results of the front-end CMOS circuitry to readout SiPM sensors at liquid nitrogen temperature and room temperature. In order to study and verify the functionalities of the basic circuit modules for a chip-level integration. Then, a 32-pixel mixed-signal ASIC for the readout of SiPM matrices at cryogenic temperature is developed. This chip arranges its channels in 4 × 8 arrays, expected to readout large area SiPMs. The readout channel consists of high bandwidth and low input-impedance pre-amplifier, leading edge discriminators, lowpower TDCs and logic control and data transmission blocks, providing the time based SiPM readout up tp 1 cm^2 and maximum event rate of 5 MHz per channel, with the power consumption less than 10 mW per channel and time bin 50ps (25ps). A 64-channel mixed-signal ASIC for highly capacitive silicon detectors is also described.